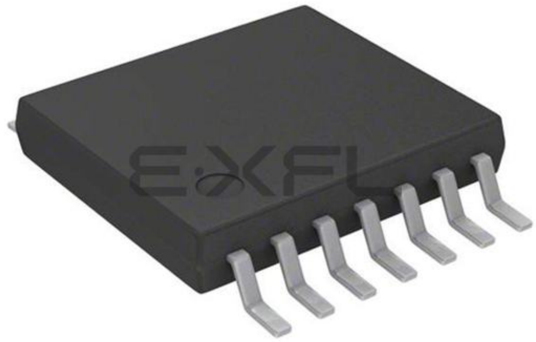

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	11
Program Memory Size	7KB (4K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	14-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	14-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f1824-i-st

PIC12(L)F1822/1840/PIC16(L)F182x/1847 Family Types

Device	Data Sheet Index	Program Memory Flash (words)	Data EEPROM (bytes)	Data SRAM (bytes)	I/O's(2)	10-bit ADC (ch)	CapSense (ch)	Comparators	Timers (8/16-bit)	EUSART	MSSP (I^2C™/SPI)	ECCP (Full-Bridge) ECCP (Half-Bridge) CCP	SR Latch	Debug(1)	XLP
PIC12(L)F1822	(1)	2K	256	128	6	4	4	1	2/1	1	1	0/1/0	Y	I/H	Y
PIC12(L)F1840	(2)	4K	256	256	6	4	4	1	2/1	1	1	0/1/0	Y	I/H	Y
PIC16(L)F1823	(1)	2K	256	128	12	8	8	2	2/1	1	1	1/0/0	Y	I/H	Y
PIC16(L)F1824	(3)	4K	256	256	12	8	8	2	4/1	1	1	1/1/2	Y	I/H	Y
PIC16(L)F1825	(4)	8K	256	1024	12	8	8	2	4/1	1	1	1/1/2	Y	I/H	Y
PIC16(L)F1826	(5)	2K	256	256	16	12	12	2	2/1	1	1	1/0/0	Y	I/H	Y
PIC16(L)F1827	(5)	4K	256	384	16	12	12	2	4/1	1	2	1/1/2	Y	I/H	Y
PIC16(L)F1828	(3)	4K	256	256	18	12	12	2	4/1	1	1	1/1/2	Y	I/H	Y
PIC16(L)F1829	(4)	8K	256	1024	18	12	12	2	4/1	1	2	1/1/2	Y	I/H	Y
PIC16(L)F1847	(6)	8K	256	1024	16	12	12	2	4/1	1	2	1/1/2	Y	I/H	Y

Note 1: I - Debugging, Integrated on Chip; H - Debugging, available using Debug Header.
2: One pin is input-only.

Data Sheet Index: (Unshaded devices are described in this document.)

1: DS41413 PIC12(L)F1822/PIC16(L)F1823 Data Sheet, 8/14-Pin Flash Microcontrollers.
2: DS41441 PIC12(L)F1840 Data Sheet, 8-Pin Flash Microcontrollers.
3: DS41419 PIC16(L)F1824/1828 Data Sheet, 28/40/44-Pin Flash Microcontrollers.
4: DS41440 PIC16(L)F1825/1829 Data Sheet, 14/20-Pin Flash Microcontrollers.
5: DS41391 PIC16(L)F1826/1827 Data Sheet, 18/20/28-Pin Flash Microcontrollers.
6: DS41453 PIC16(L)F1847 Data Sheet, 18/20/28-Pin Flash Microcontrollers.

Note: For other small form-factor package availability and marking information, please visit www.microchip.com/packaging or contact your local sales office.

TABLE 1-3: PIC16(L)F1828 PINOUT DESCRIPTION

Name	Function	Input Type	Output Type	Description
RA0/AN0/CPS0/C1IN+/VREF-/DACOUT/ICSPDAT/ICDDAT	RA0	TTL	CMOS	General purpose I/O.
	AN0	AN	—	A/D Channel 0 input.
	CPS0	AN	—	Capacitive sensing input 0.
	C1IN+	AN	—	Comparator C1 positive input.
	VREF-	AN	—	A/D and DAC Negative Voltage Reference input.
	DACOUT	—	AN	Digital-to-Analog Converter output.
	ICSPDAT	ST	CMOS	ICSP™ Data I/O.
	ICDDAT	ST	CMOS	In-Circuit Data I/O.
RA1/AN1/CPS1/C12IN0-/VREF+/SRI/ICSPCLK/ICDCLK	RA1	TTL	CMOS	General purpose I/O.
	AN1	AN	—	A/D Channel 1 input.
	CPS1	AN	—	Capacitive sensing input 1.
	C12IN0-	AN	—	Comparator C1 or C2 negative input.
	VREF+	AN	—	A/D and DAC Positive Voltage Reference input.
	SRI	ST	—	SR latch input.
	ICSPCLK	ST	—	Serial Programming Clock.
	ICDCLK	ST	—	In-Circuit Debug Clock.
RA2/AN2/CPS2/T0CKI/INT/C1OUT/SRQ/CCP3/FLT0	RA2	ST	CMOS	General purpose I/O.
	AN2	AN	—	A/D Channel 2 input.
	CPS2	AN	—	Capacitive sensing input 2.
	T0CKI	ST	—	Timer0 clock input.
	INT	ST	—	External interrupt.
	C1OUT	—	CMOS	Comparator C1 output.
	SRQ	—	CMOS	SR latch non-inverting output.
	CCP3	ST	CMOS	Capture/Compare/PWM3.
	FLT0	ST	—	ECCP Auto-Shutdown Fault input.
RA3/T1G(1)/VPP/$\overline{\text{MCLR}}$	RA3	TTL	—	General purpose input.
	T1G	ST	—	Timer1 Gate input.
	VPP	HV	—	Programming voltage.
	$\overline{\text{MCLR}}$	ST	—	Master Clear with internal pull-up.
RA4/AN3/CPS3/OSC2/CLKOUT/T1OSO/CLKR/P2B(1)/T1G(1,2)	RA4	TTL	CMOS	General purpose I/O.
	AN3	AN	—	A/D Channel 3 input.
	CPS3	AN	—	Capacitive sensing input 3.
	OSC2	—	CMOS	Comparator C2 output.
	CLKOUT	—	CMOS	FOSC/4 output.
	T1OSO	XTAL	XTAL	Timer1 oscillator connection.
	CLKR	—	CMOS	Clock Reference output.
	P2B	—	CMOS	PWM output.
	T1G	ST	—	Timer1 Gate input.

Legend: AN = Analog input or output; CMOS = CMOS compatible input or output; OD = Open Drain; TTL = TTL compatible input; ST = Schmitt Trigger input with CMOS levels; I^2C™ = Schmitt Trigger input with I^2C levels; HV = High Voltage; XTAL = Crystal

Note 1: Pin functions can be moved using the APFCONO and APFCON1 registers (Register 12-1 and Register 12-2).
2: Default function location.

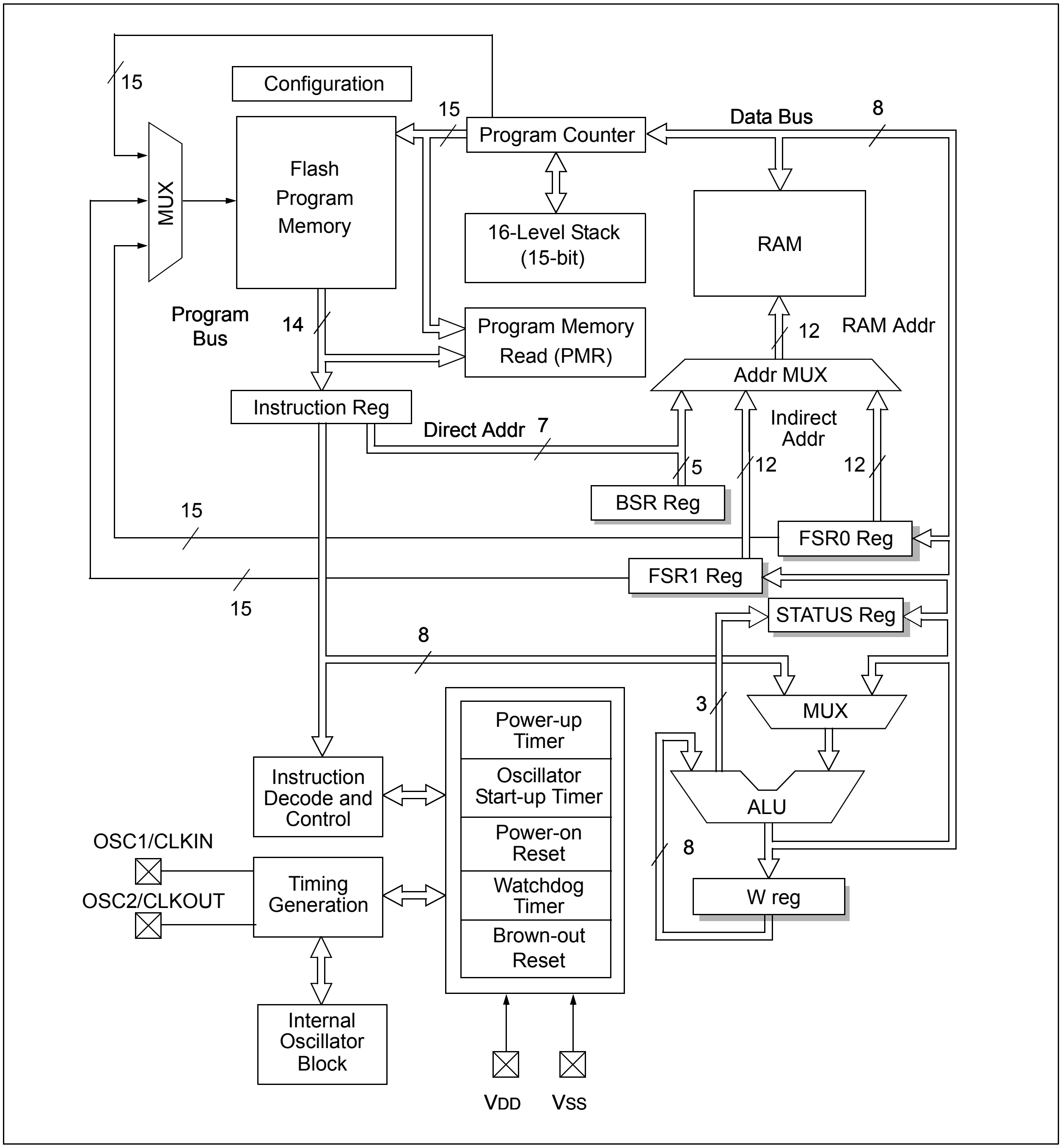
TABLE 1-3: PIC16(L)F1828 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RA5/CLKIN/OSC1/T1OSI/ T1CKI/P2A(1)/CCP2(1)	RA5	TTL	CMOS	General purpose I/O.
	CLKIN	CMOS	—	External clock input (EC mode).
	OSC1	XTAL	—	Crystal/Resonator (LP, XT, HS modes).
	T1OSI	XTAL	XTAL	Timer1 oscillator connection.
	T1CKI	ST	—	Timer1 clock input.
	P2A	—	CMOS	PWM output.
	CCP2	ST	CMOS	Capture/Compare/PWM2.
RB4/AN10/CPS10/SDA1/SDI1	RB4	TTL	CMOS	General purpose I/O.
	AN10	AN	—	A/D Channel 10 input.
	CPS10	AN	—	Capacitive sensing input 10.
	SDA1	I^2C	OD	I^2C data input/output.
	SDI1	CMOS	—	SPI data input.
RB5/AN11/CPS11/RX(1,2)/DT(1,2)	RB5	TTL	CMOS	General purpose I/O.
	AN11	AN	—	A/D Channel 11 input.
	CPS11	AN	—	Capacitive sensing input 11.
	RX	ST	—	USART asynchronous input.
	DT	ST	CMOS	USART synchronous data.
RB6/SCL1/SCK1	RB6	TTL	CMOS	General purpose I/O.
	SCL1	I^2C	OD	I^2C™ clock 1.
	SCK1	ST	CMOS	SPI clock 1.
RB7/TX(1,2)/CK(1,2)	RB7	TTL	CMOS	General purpose I/O.
	TX	—	CMOS	USART asynchronous transmit.
	CK	ST	CMOS	USART synchronous clock.
RC0/AN4/CPS4/C2IN+/P1D(1)	RC0	TTL	CMOS	General purpose I/O.
	AN4	AN	—	A/D Channel 4 input.
	CPS4	AN	—	Capacitive sensing input 4.
	C2IN+	AN	—	Comparator C2 positive input.
	P1D	—	CMOS	PWM output.
RC1/AN5/CPS5/C12IN1-/P1C(1)	RC1	TTL	CMOS	General purpose I/O.
	AN5	AN	—	A/D Channel 5 input.
	CPS5	AN	—	Capture/Compare/PWM4.
	C12IN1-	AN	—	Comparator C1 or C2 negative input.
	P1C	—	CMOS	PWM output.
RC2/AN6/CPS6/C12IN2-/ P1D(1,2)/P2B(1,2)/MDCIN1	RC2	TTL	CMOS	General purpose I/O.
	AN6	AN	—	A/D Channel 6 input.
	CPS6	AN	—	Capacitive sensing input 6.
	C12IN2-	AN	—	Comparator C1 or C2 negative input.
	P1D	—	CMOS	PWM output.
	P2B	—	CMOS	PWM output.
	MDCIN1	ST	—	Modulator Carrier Input 1.

Legend: AN = Analog input or output; CMOS = CMOS compatible input or output; OD = Open Drain; TTL = TTL compatible input; ST = Schmitt Trigger input with CMOS levels; I^2C™ = Schmitt Trigger input with I^2C levels; HV = High Voltage; XTAL = Crystal

Note 1: Pin functions can be moved using the APFCONO and APFCON1 registers (Register 12-1 and Register 12-2).
2: Default function location.

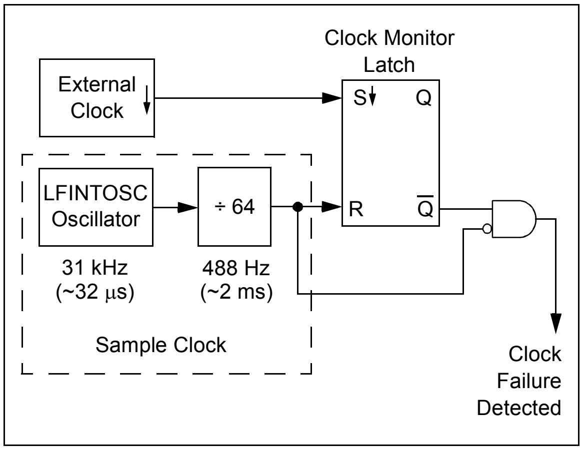
FIGURE 2-1: CORE BLOCK DIAGRAM



5.5 Fail-Safe Clock Monitor

The Fail-Safe Clock Monitor (FSCM) allows the device to continue operating should the external oscillator fail. The FSCM can detect oscillator failure any time after the Oscillator Start-up Timer (OST) has expired. The FSCM is enabled by setting the FCMEN bit in the Configuration Word 1. The FSCM is applicable to all external Oscillator modes (LP, XT, HS, EC, Timer1 Oscillator and RC).

FIGURE 5-9: FSCM BLOCK DIAGRAM



5.5.1 FAIL-SAFE DETECTION

The FSCM module detects a failed oscillator by comparing the external oscillator to the FSCM sample clock. The sample clock is generated by dividing the LFINTOSC by 64. See Figure 5-9. Inside the fail detector block is a latch. The external clock sets the latch on each falling edge of the external clock. The sample clock clears the latch on each rising edge of the sample clock. A failure is detected when an entire half-cycle of the sample clock elapses before the external clock goes low.

5.5.2 FAIL-SAFE OPERATION

When the external clock fails, the FSCM switches the device clock to an internal clock source and sets the bit flag OSFIF of the PIR2 register. Setting this flag will generate an interrupt if the OSFIE bit of the PIE2 register is also set. The device firmware can then take steps to mitigate the problems that may arise from a failed clock. The system clock will continue to be sourced from the internal clock source until the device firmware successfully restarts the external oscillator and switches back to external operation.

The internal clock source chosen by the FSCM is determined by the IRCF<3:0> bits of the OSCCON register. This allows the internal oscillator to be configured before a failure occurs.

5.5.3 FAIL-SAFE CONDITION CLEARING

The Fail-Safe condition is cleared after a Reset, executing a SLEEP instruction or changing the SCS bits of the OSCCON register. When the SCS bits are changed, the OST is restarted. While the OST is running, the device continues to operate from the INTOSC selected in OSCCON. When the OST times out, the Fail-Safe condition is cleared after successfully switching to the external clock source. The OSFIF bit should be cleared prior to switching to the external clock source. If the Fail-Safe condition still exists, the OSFIF flag will again become set by hardware.

5.5.4 RESET OR WAKE-UP FROM SLEEP

The FSCM is designed to detect an oscillator failure after the Oscillator Start-up Timer (OST) has expired. The OST is used after waking up from Sleep and after any type of Reset. The OST is not used with the EC or RC Clock modes so that the FSCM will be active as soon as the Reset or wake-up has completed. When the FSCM is enabled, the Two-Speed Start-up is also enabled. Therefore, the device will always be executing code while the OST is operating.

Note: Due to the wide range of oscillator start-up times, the Fail-Safe circuit is not active during oscillator start-up (i.e., after exiting Reset or Sleep). After an appropriate amount of time, the user should check the Status bits in the OSCSTAT register to verify the oscillator start-up and that the system clock switchover has successfully completed.

11.0 DATA EEPROM AND FLASH PROGRAM MEMORY CONTROL

The data EEPROM and Flash program memory are readable and writable during normal operation (full V_{DD} range). These memories are not directly mapped in the register file space. Instead, they are indirectly addressed through the Special Function Registers (SFRs). There are six SFRs used to access these memories:

- EECON1
- EECON2
- EEDATL
- EEDATH
- EEADRL
- EEADRH

When interfacing the data memory block, EEDATL holds the 8-bit data for read/write, and EEADRL holds the address of the EEDATL location being accessed. These devices have 256 bytes of data EEPROM with an address range from 0h to 0FFh.

When accessing the program memory block, the EEDATH:EEDATL register pair forms a 2-byte word that holds the 14-bit data for read/write, and the EEADRL and EEADRH registers form a 2-byte word that holds the 15-bit address of the program memory location being read.

The EEPROM data memory allows byte read and write. An EEPROM byte write automatically erases the location and writes the new data (erase before write).

The write time is controlled by an on-chip timer. The write/erase voltages are generated by an on-chip charge pump rated to operate over the voltage range of the device for byte or word operations.

Depending on the setting of the Flash Program Memory Self Write Enable bits WRT<1:0> of the Configuration Word 2, the device may or may not be able to write certain blocks of the program memory. However, reads from the program memory are always allowed.

When the device is code-protected, the device programmer can no longer access data or program memory. When code-protected, the CPU may continue to read and write the data EEPROM memory and Flash program memory.

11.1 EEADRL and EEADRH Registers

The EEADRH:EEADRL register pair can address up to a maximum of 256 bytes of data EEPROM or up to a maximum of 32K words of program memory.

When selecting a program address value, the MSB of the address is written to the EEADRH register and the LSB is written to the EEADRL register. When selecting a EEPROM address value, only the LSB of the address is written to the EEADRL register.

11.1.1 EECON1 AND EECON2 REGISTERS

EECON1 is the control register for EE memory accesses.

Control bit EEPGD determines if the access will be a program or data memory access. When clear, any subsequent operations will operate on the EEPROM memory. When set, any subsequent operations will operate on the program memory. On Reset, EEPROM is selected by default.

Control bits RD and WR initiate read and write, respectively. These bits cannot be cleared, only set, in software. They are cleared in hardware at completion of the read or write operation. The inability to clear the WR bit in software prevents the accidental, premature termination of a write operation.

The WREN bit, when set, will allow a write operation to occur. On power-up, the WREN bit is clear. The WRERR bit is set when a write operation is interrupted by a Reset during normal operation. In these situations, following Reset, the user can check the WRERR bit and execute the appropriate error handling routine.

Interrupt flag bit EEIF of the PIR2 register is set when the write is complete. It must be cleared in the software.

Reading EECON2 will read all '0's. The EECON2 register is used exclusively in the data EEPROM write sequence. To enable writes, a specific pattern must be written to EECON2.

REGISTER 11-6: EECON2: EEPROM CONTROL 2 REGISTER

W-0/0	W-0/0	W-0/0	W-0/0	W-0/0	W-0/0	W-0/0	W-0/0
EEPROM Control Register 2							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
S = Bit can only be set	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **Data EEPROM Unlock Pattern bits**

To unlock writes, a 55h must be written first, followed by an AAh, before setting the WR bit of the EECON1 register. The value written to this register is used to unlock the writes. There are specific timing requirements on these writes. Refer to **Section 11.2.2 “Writing to the Data EEPROM Memory”** for more information.

TABLE 11-3: SUMMARY OF REGISTERS ASSOCIATED WITH DATA EEPROM

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
EECON1	EEPGD	CFGS	LWLO	FREE	WRERR	WREN	WR	RD	114
EECON2	EEPROM Control Register 2 (not a physical register)								115*
EEADRL	EEADRL<7:0>								113
EEADRH	—(1)	EEADRH<6:0							113
EEDATL	EEDATL<7:0>								113
EEDATH	—	—	EEDATH<5:0>						113
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	89
PIE2	OSFIE	C2IE	C1IE	EEIE	BCL1IE	—	—	CCP2IE	91
PIR2	OSFIF	C2IF	C1IF	EEIF	BCL1IF	—	—	CCP2IF	94

Legend: — = unimplemented location, read as ‘0’. Shaded cells are not used by data EEPROM module.
* Page provides register information.
Note 1: Unimplemented, read as ‘1’.

TABLE 12-1: SUMMARY OF REGISTERS ASSOCIATED WITH PORTA

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ANSELA	—	—	—	ANSA4	—	ANSA2	ANSA1	ANSA0	122
APFCON0(1)	RXDTSEL	SDOSEL	SSSEL	—	T1GSEL	TXCKSEL	—	—	117
APFCON1	—	—	—	—	P1DSEL	P1CSEL	P2BSEL	CCP2SEL	118
INLVLA	—	—	INLVLA5	INLVLA4	INLVLA3	INLVLA2	INLVLA1	INLVLA0	123
LATA	—	—	LATA5	LATA4	—	LATA2	LATA1	LATA0	122
OPTION_REG	$\overline{\text{WPUEN}}$	INTEDG	TMR0CS	TMR0SE	PSA	PS<2:0>			176
PORTA	—	—	RA5	RA4	RA3	RA2	RA1	RA0	121
TRISA	—	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	121
WPUA	—	—	WPUA5	WPUA4	WPUA3	WPUA2	WPUA1	WPUA0	123

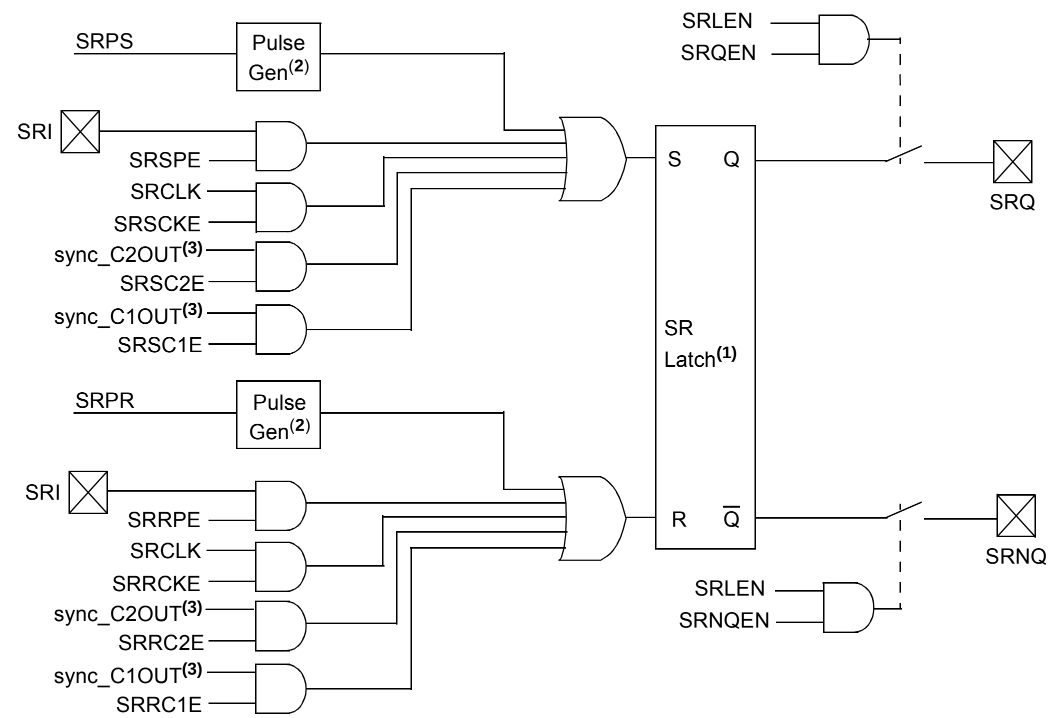
Legend: x = unknown, u = unchanged, – = unimplemented locations, read as '0'. Shaded cells are not used by PORTA.
Note 1: Unshaded cells apply to PIC16(L)F1824 only.

TABLE 12-2: SUMMARY OF CONFIGURATION WORD WITH PORTA

Name	Bits	Bit -/7	Bit -/6	Bit 13/5	Bit 12/4	Bit 11/3	Bit 10/2	Bit 9/1	Bit 8/0	Register on Page
CONFIG1	13:8	—	—	FCMEN	IESO	$\overline{\text{CLKOUTEN}}$	BOREN<1:0>		$\overline{\text{CPD}}$	48
	7:0	$\overline{\text{CP}}$	MCLRE	$\overline{\text{PWRTE}}$	WDTE<1:0>		FOSC<2:0>			

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by PORTA.

FIGURE 18-1: SR LATCH SIMPLIFIED BLOCK DIAGRAM



Note 1: If R = 1 and S = 1 simultaneously, Q = 0, $\overline{Q}$ = 1

2: Pulse generator causes a 1 Q-state pulse width.

3: Name denotes the connection point at the comparator output.

REGISTER 18-2: SRCON1: SR LATCH CONTROL 1 REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
SRSPE	SRSCKE	SRSC2E	SRSC1E	SRRPE	SRRCKE	SRRC2E	SRRC1E
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7 **SRSPE:** SR Latch Peripheral Set Enable bit
1 = SR latch is set when the SRI pin is high
0 = SRI pin has no effect on the set input of the SR latch

bit 6 **SRSCKE:** SR Latch Set Clock Enable bit
1 = Set input of SR latch is pulsed with SRCLK
0 = SRCLK has no effect on the set input of the SR latch

bit 5 **SRSC2E:** SR Latch C2 Set Enable bit
1 = SR latch is set when the C2 Comparator output is high
0 = C2 Comparator output has no effect on the set input of the SR latch

bit 4 **SRSC1E:** SR Latch C1 Set Enable bit
1 = SR latch is set when the C1 Comparator output is high
0 = C1 Comparator output has no effect on the set input of the SR latch

bit 3 **SRRPE:** SR Latch Peripheral Reset Enable bit
1 = SR latch is reset when the SRI pin is high
0 = SRI pin has no effect on the reset input of the SR latch

bit 2 **SRRCKE:** SR Latch Reset Clock Enable bit
1 = Reset input of SR latch is pulsed with SRCLK
0 = SRCLK has no effect on the reset input of the SR latch

bit 1 **SRRC2E:** SR Latch C2 Reset Enable bit
1 = SR latch is reset when the C2 Comparator output is high
0 = C2 Comparator output has no effect on the reset input of the SR latch

bit 0 **SRRC1E:** SR Latch C1 Reset Enable bit
1 = SR latch is reset when the C1 Comparator output is high
0 = C1 Comparator output has no effect on the reset input of the SR latch

24.3.7 OPERATION IN SLEEP MODE

In Sleep mode, the TMRx register will not increment and the state of the module will not change. If the CCPx pin is driving a value, it will continue to drive that value. When the device wakes up, TMRx will continue from its previous state.

24.3.8 CHANGES IN SYSTEM CLOCK FREQUENCY

The PWM frequency is derived from the system clock frequency. Any changes in the system clock frequency will result in changes to the PWM frequency. See **Section 5.0 "Oscillator Module (With Fail-Safe Clock Monitor)"** for additional details.

24.3.9 EFFECTS OF RESET

Any Reset will force all ports to Input mode and the CCP registers to their Reset states.

24.3.10 ALTERNATE PIN LOCATIONS

This module incorporates I/O pins that can be moved to other locations with the use of the alternate pin function registers, APFCON0 and APFCON1. To determine which pins can be moved and what their default locations are upon a Reset, see **Section 12.1 "Alternate Pin Function"** for more information.

TABLE 24-8: SUMMARY OF REGISTERS ASSOCIATED WITH STANDARD PWM

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
APFCON1	—	—	—	—	P1DSEL	P1CSEL	P2BSEL	CCP2SEL	118
CCPxCON	PxM<1:0>(1)		DCxB<1:0>		CCPxM<3:0>				225
CCPTMRS0	C4TSEL<1:0>		C3TSEL<1:0>		C2TSEL<1:0>		C1TSEL<1:0>		226
INLVLA	—	—	INLVLA5	INLVLA4	INLVLA3	INLVLA2	INLVLA1	INLVLA0	123
INLVLC	INLVLC7(2)	INLVLC6(2)	INLVLC5	INLVLC4	INLVLC3	INLVLC2	INLVLC1	INLVLC0	134
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	89
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	90
PIE2	OSFIE	C2IE	C1IE	EEIE	BCLIE	—	—	CCP2IE	91
PIE3	—	—	CCP4IE	CCP3IE	TMR6IE	—	TMR4IE	—	92
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	93
PIR2	OSFIF	C2IF	C1IF	EEIF	BCLIF	—	—	CCP2IF	94
PIR3	—	—	CCP4IF	CCP3IF	TMR6IF	—	TMR4IF	—	95
PRx	Timer2/4/6 Period Register								189*
TxCON	—	TxOUTPS<3:0>				TMRxON	TxCKPS<:0>1		191
TMRx	Timer2/4/6 Module Register								189*
TRISA	—	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	121
TRISC	TRISC7(2)	TRISC6(2)	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	132

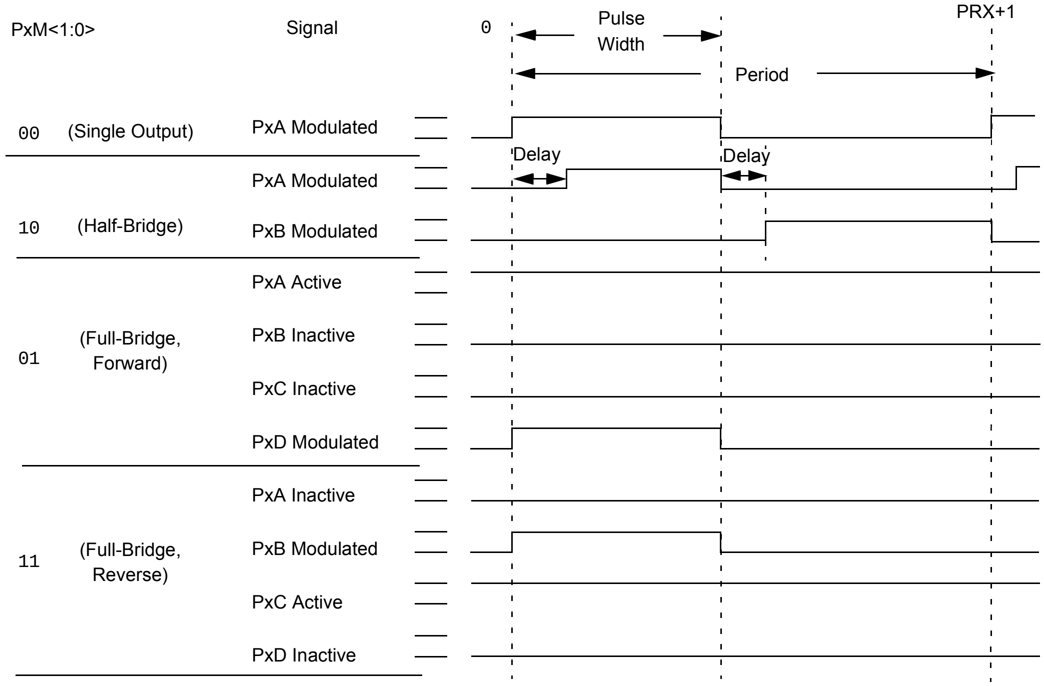
Legend: — = unimplemented location, read as '0'. Shaded cells are not used by the PWM.
* Page provides register information.
Note 1: Applies to ECCP modules only.
2: PIC16(L)F1828 only.

TABLE 24-9: EXAMPLE PIN ASSIGNMENTS FOR VARIOUS PWM ENHANCED MODES

ECCP Mode	PxM<1:0>	CCPx/PxA	PxB	PxC	PxD
Single	00	Yes(1)	Yes(1)	Yes(1)	Yes(1)
Half-Bridge	10	Yes	Yes	No	No
Full-Bridge, Forward	01	Yes	Yes	Yes	Yes
Full-Bridge, Reverse	11	Yes	Yes	Yes	Yes

Note 1: PWM Steering enables outputs in Single mode.

FIGURE 24-6: EXAMPLE PWM (ENHANCED MODE) OUTPUT RELATIONSHIPS (ACTIVE-HIGH STATE)



Relationships:

- Period = 4 * TOSC * (PRx + 1) * (TMRx Prescale Value)
- Pulse Width = TOSC * (CCPRxL<7:0>:CCPxCON<5:4>) * (TMRx Prescale Value)
- Delay = 4 * TOSC * (PWMxCON<6:0>)

25.2.6 SPI OPERATION IN SLEEP MODE

In SPI Master mode, module clocks may be operating at a different speed than when in Full Power mode; in the case of the Sleep mode, all clocks are halted.

Special care must be taken by the user when the MSSP1 clock is much faster than the system clock.

In Slave mode, when MSSP1 interrupts are enabled, after the master completes sending data, an MSSP1 interrupt will wake the controller from Sleep.

If an exit from Sleep mode is not desired, MSSP1 interrupts should be disabled.

In SPI Master mode, when the Sleep mode is selected, all module clocks are halted and the transmission/reception will remain in that state until the device wakes. After the device returns to Run mode, the module will resume transmitting and receiving data.

In SPI Slave mode, the SPI Transmit/Receive Shift register operates asynchronously to the device. This allows the device to be placed in Sleep mode and data to be shifted into the SPI Transmit/Receive Shift register. When all eight bits have been received, the MSSP1 interrupt flag bit will be set and if enabled, will wake the device.

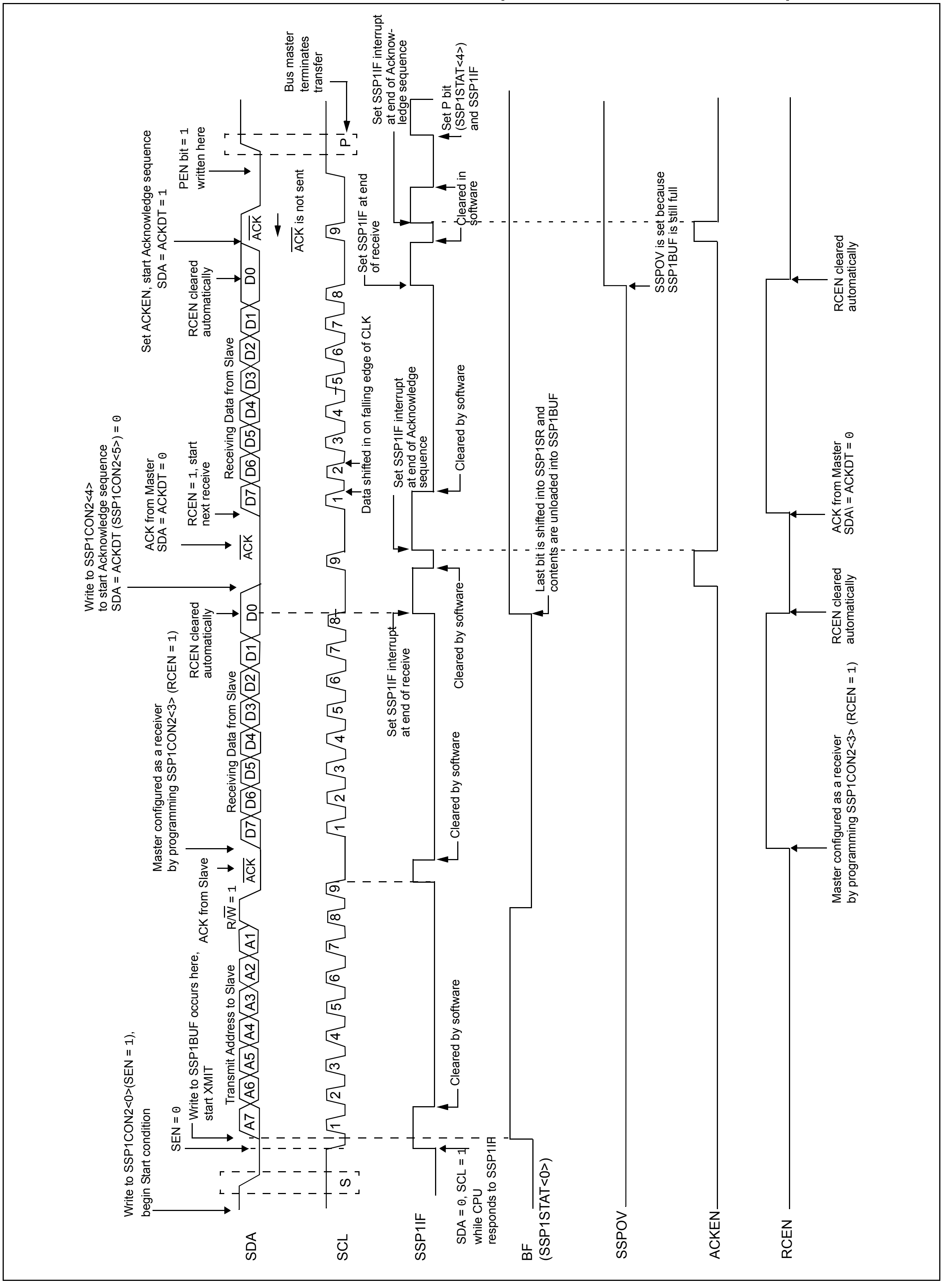
TABLE 25-1: SUMMARY OF REGISTERS ASSOCIATED WITH SPI OPERATION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ANSELA	—	—	—	ANSA4	—	ANSA2	ANSA1	ANSA0	122
ANSELB(1)	—	—	ANSB5	ANSB4	—	—	—	—	128
ANSELC	ANSC7(1)	ANSC6(1)	—	—	ANSC3	ANSC2	ANSC1	ANSC0	128
APFCON0	RXDTSEL	SDOSEL(2)	SSSEL(2)	—	T1GSEL	TXCKSEL	—	—	117
INLVLA(3)	—	—	INLVLA5	INLVLA4	INLVLA3	INLVLA2	INLVLA1	INLVLA0	123
INLVLA(4)	—	—	INLVLA5	INLVLA4	INLVLA3	INLVLA2	INLVLA1	INLVLA0	123
INLVLB(1)	INLVLB7	INLVLB6	INLVLB5	INLVLB4	—	—	—	—	128
INLVLC(3)	INLVLC7(1)	INLVLC6(1)	INLVLC5	INLVLC4	INLVLC3	INLVLC2	INLVLC1	INLVLC0	134
INLVLC(4)	INLVLC7(1)	INLVLC6(1)	INLVLC5	INLVLC4	INLVLC3	INLVLC2	INLVLC1	INLVLC0	134
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	89
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	90
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	93
SSP1BUF	Synchronous Serial Port Receive Buffer/Transmit Register								234*
SSP1CON1	WCOL	SSPOV	SSPEN	CKP	SSPM<3:0>				281
SSP1CON3	ACKTIM	PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN	283
SSP1STAT	SMP	CKE	$D/\overline{A}$	P	S	$R/\overline{W}$	UA	BF	280
TRISA(3)	—	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	121
TRISA(4)	—	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	121
TRISB(1)	TRISB7	TRISB6	TRISB5	TRISB4	—	—	—	—	127
TRISC(3)	TRISC7(1)	TRISC6(1)	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	127
TRISC(4)	TRISC7(1)	TRISC6(1)	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	127

Legend: — = Unimplemented location, read as ‘0’. Shaded cells are not used by the MSSP1 in SPI mode.
* Page provides register information.

Note 1: PIC16(L)F1828 only.
2: PIC16(L)F1824 only.
3: Unshaded cells apply to PIC16(L)F1828 only.
4: Unshaded cells apply to PIC16(L)F1824 only.

FIGURE 25-29: I²C MASTER MODE WAVEFORM (RECEPTION, 7-BIT ADDRESS)



25.6.13.3 Bus Collision During a Stop Condition

Bus collision occurs during a Stop condition if:

a) After the SDA pin has been deasserted and allowed to float high, SDA is sampled low after the BRG has timed out.
b) After the SCL pin is deasserted, SCL is sampled low before SDA goes high.

The Stop condition begins with SDA asserted low. When SDA is sampled low, the SCL pin is allowed to float. When the pin is sampled high (clock arbitration), the Baud Rate Generator is loaded with SSP1ADD and counts down to 0. After the BRG times out, SDA is sampled. If SDA is sampled low, a bus collision has occurred. This is due to another master attempting to drive a data '0' (Figure 25-38). If the SCL pin is sampled low before SDA is allowed to float high, a bus collision occurs. This is another case of another master attempting to drive a data '0' (Figure 25-39).

FIGURE 25-38: BUS COLLISION DURING A STOP CONDITION (CASE 1)

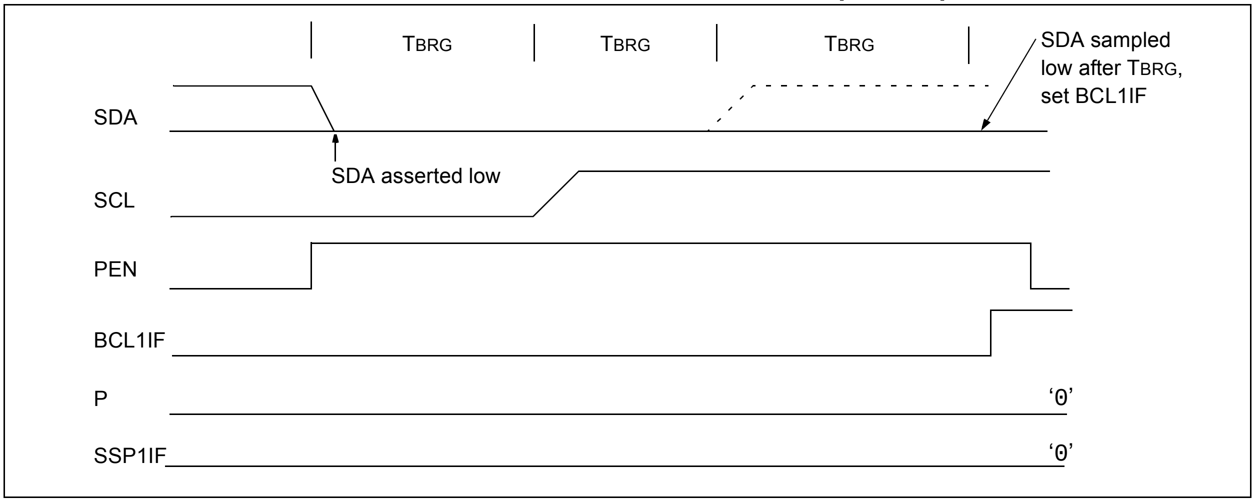
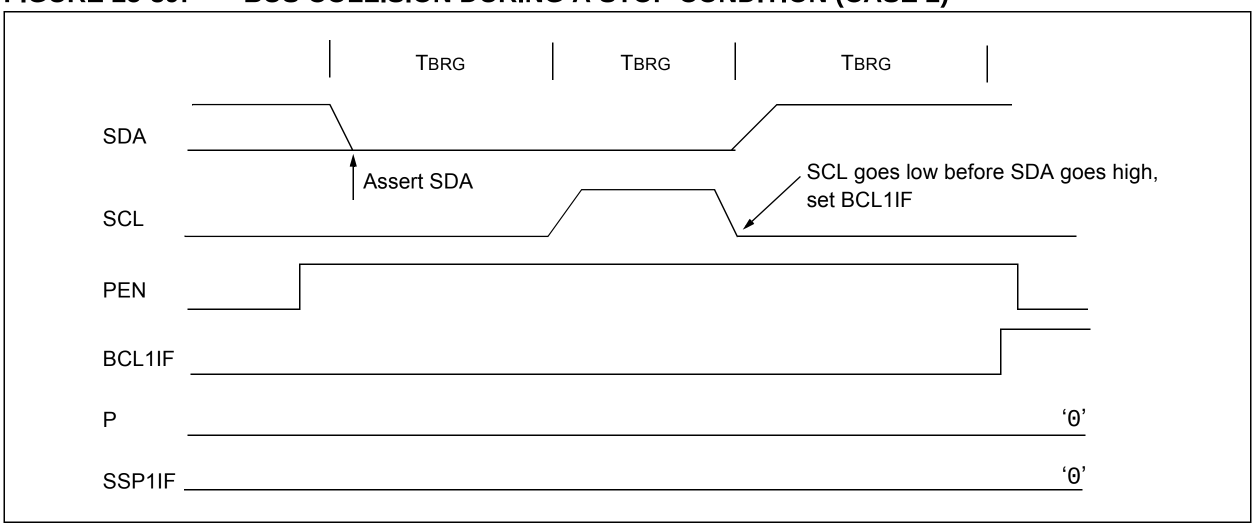


FIGURE 25-39: BUS COLLISION DURING A STOP CONDITION (CASE 2)



REGISTER 27-2: CPSCON1: CAPACITIVE SENSING CONTROL REGISTER 1

U-0	U-0	U-0	U-0	R/W-0/0(1)	R/W-0/0	R/W-0/0	R/W-0/0
—	—	—	—	CPSCH<3:0>			
bit 7							bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-4 **Unimplemented:** Read as ‘0’

bit 3-0 **CPSCH<3:0>:** Capacitive Sensing Channel Select bits

If CPSON = 0:

These bits are ignored. No channel is selected.

If CPSON = 1:

- 0000 = channel 0, (CPS0)
- 0001 = channel 1, (CPS1)
- 0010 = channel 2, (CPS2)
- 0011 = channel 3, (CPS3)
- 0100 = channel 4, (CPS4)
- 0101 = channel 5, (CPS5)
- 0110 = channel 6, (CPS6)
- 0111 = channel 7, (CPS7)
- 1000 = channel 8, (CPS8)(1)
- 1001 = channel 9, (CPS9)(1)
- 1010 = channel 10, (CPS10)(1)
- 1011 = channel 11, (CPS11)(1)
- 1100 = Reserved. Do not use.
- •
- •
- •
- 1111 = Reserved. Do not use.

Note 1: These channels are only implemented on the PIC16(L)F1828.

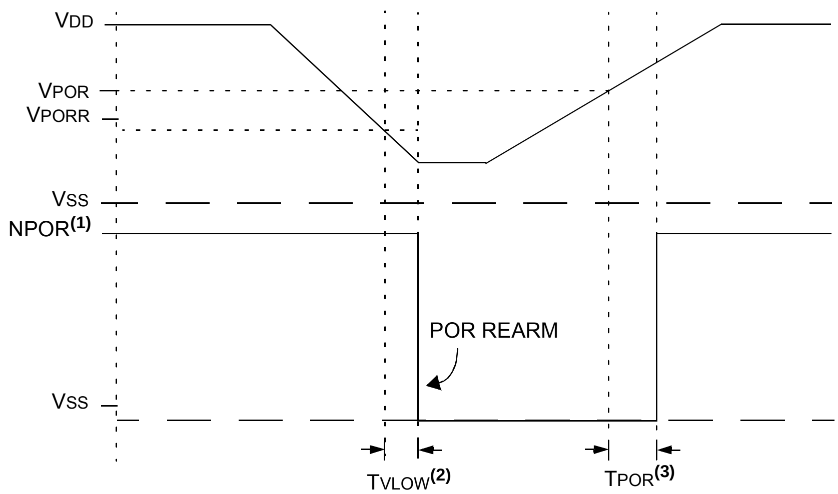
TABLE 27-3: SUMMARY OF REGISTERS ASSOCIATED WITH CAPACITIVE SENSING

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ANSELA	—	—	—	ANSA4	—	ANSA2	ANSA1	ANSA0	122
ANSELC	ANSC7	ANSC6	—	—	ANSC3	ANSC2	ANSC1	ANSC0	133
CPSCON0	CPSON	CPSRM	—	—	CPSRNG<1:0>		CPSOUT	T0XCS	319
CPSCON1	—	—	—	—	CPSCH<3:0>				320
INLVLA	—	—	INLVLA5	INLVLA4	INLVLA3	INLVLA2	INLVLA1	INLVLA0	123
INLVLB(1)	INLVLB7	INLVLB6	INLVLB5	INLVLB4	—	—	—	—	128
INLVLC	INLVLC7(1)	INLVLC6(1)	INLVLC5	INLVLC4	INLVLC3	INLVLC2	INLVLC1	INLVLC0	134
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	89
OPTION_REG	$\overline{\text{WPUEN}}$	INTEDG	TMR0CS	TMR0SE	PSA	PS2	PS1	PS0	176
T1CON	TMR1CS1	TMR1CS0	T1CKPS1	T1CKPS0	T1OSCEN	$\overline{\text{T1SYNC}}$	—	TMR1ON	186
TRISA	—	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	121
TRISB(1)	TRISB7	TRISB6	TRISB5	TRISB4	—	—	—	—	127
TRISC	TRISC7(1)	TRISC6(1)	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	132

Legend: — = Unimplemented locations, read as ‘0’. Shaded cells are not used by the capacitive sensing module.

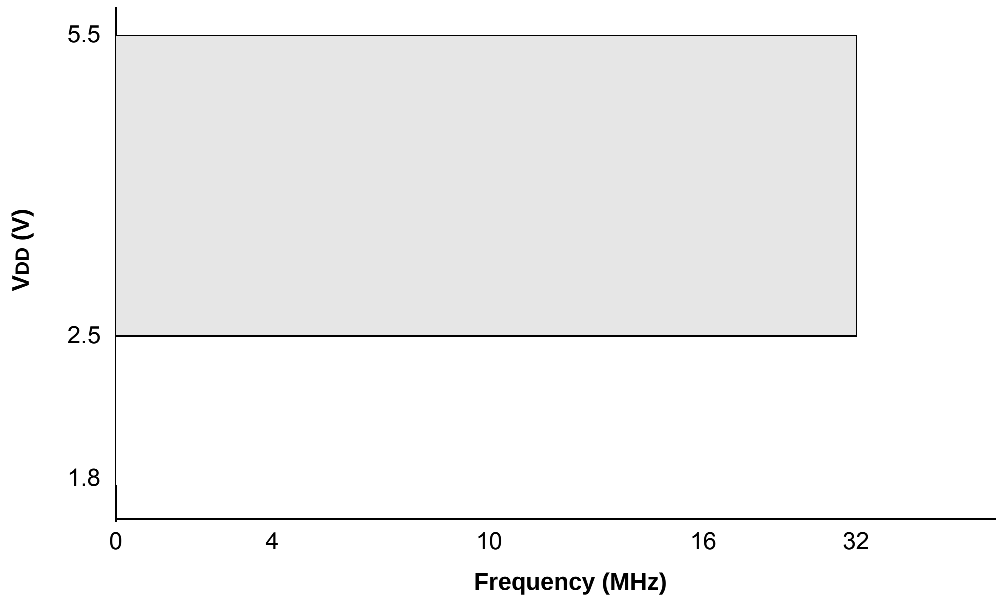
Note 1: PIC16(L)F1828 only.

FIGURE 30-4: POR AND POR REARM WITH SLOW RISING VDD



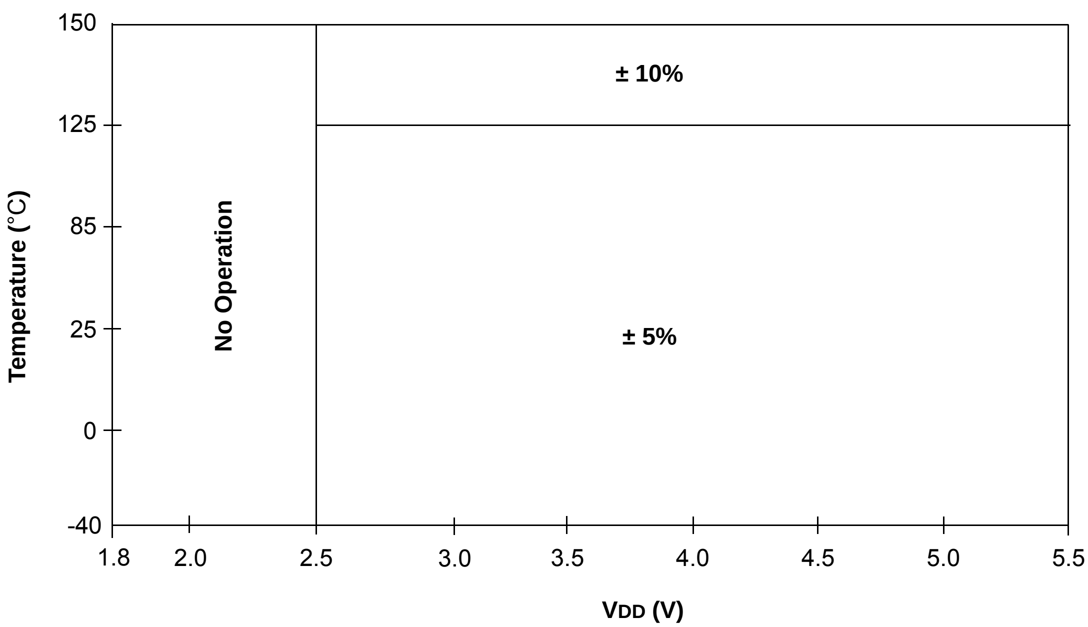
Note 1: When NPOR is low, the device is held in Reset.
2: TPOR 1 μs typical.
3: TVLOW 2.7 μs typical.

FIGURE 30-23: PIC16F1824/8 VOLTAGE FREQUENCY GRAPH, -40°C $\leq$ TA $\leq$ +150°C



Note 1: The shaded region indicates the permissible combinations of voltage and frequency.
2: Refer to Table 30-1 for each Oscillator mode's supported frequencies.

FIGURE 30-24: HFINTOSC FREQUENCY ACCURACY OVER DEVICE VDD AND TEMPERATURE



32.11 Demonstration/Development Boards, Evaluation Kits, and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

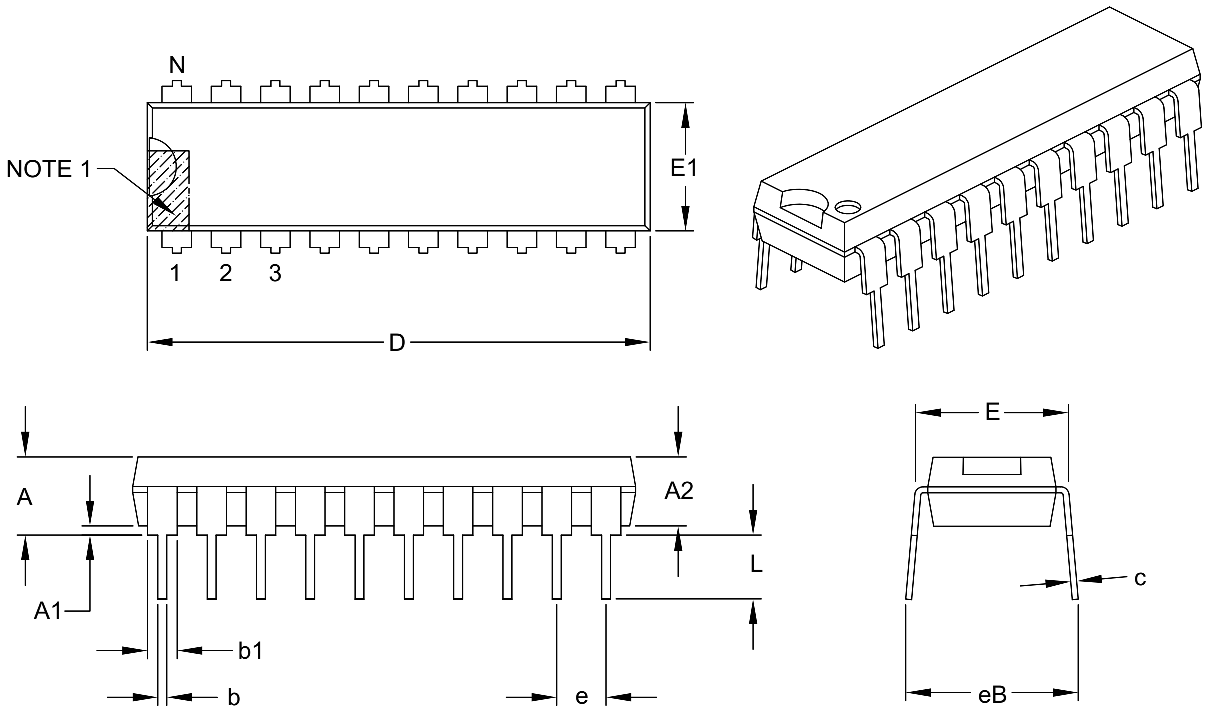
32.12 Third-Party Development Tools

Microchip also offers a great collection of tools from third-party vendors. These tools are carefully selected to offer good value and unique functionality.

- Device Programmers and Gang Programmers from companies, such as SoftLog and CCS
- Software Tools from companies, such as Gimpel and Trace Systems
- Protocol Analyzers from companies, such as Saleae and Total Phase
- Demonstration Boards from companies, such as MikroElektronika, Digilent® and Olimex
- Embedded Ethernet Solutions from companies, such as EZ Web Lynx, WIZnet and IPLogika®

20-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



		Units	INCHES		
		Dimension Limits	MIN	NOM	MAX
Number of Pins		N		20	
Pitch		e		.100 BSC	
Top to Seating Plane		A	–	–	.210
Molded Package Thickness		A2	.115	.130	.195
Base to Seating Plane		A1	.015	–	–
Shoulder to Shoulder Width		E	.300	.310	.325
Molded Package Width		E1	.240	.250	.280
Overall Length		D	.980	1.030	1.060
Tip to Seating Plane		L	.115	.130	.150
Lead Thickness		c	.008	.010	.015
Upper Lead Width		b1	.045	.060	.070
Lower Lead Width		b	.014	.018	.022
Overall Row Spacing §		eB	–	–	.430

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-019B