Microchip Technology - PIC16F1828-I/SO Datasheet





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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	17
Program Memory Size	7KB (4K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f1828-i-so

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

5.2.2.7 Internal Oscillator Clock Switch Timing

When switching between the HFINTOSC, MFINTOSC and the LFINTOSC, the new oscillator may already be shut down to save power (see Figure 5-7). If this is the case, there is a delay after the IRCF<3:0> bits of the OSCCON register are modified before the frequency selection takes place. The OSCSTAT register will reflect the current active status of the HFINTOSC, MFINTOSC and LFINTOSC oscillators. The sequence of a frequency selection is as follows:

- 1. IRCF<3:0> bits of the OSCCON register are modified.
- 2. If the new clock is shut down, a clock start-up delay is started.
- 3. Clock switch circuitry waits for a falling edge of the current clock.
- 4. The current clock is held low and the clock switch circuitry waits for a rising edge in the new clock.
- 5. The new clock is now active.
- 6. The OSCSTAT register is updated as required.
- 7. Clock switch is complete.

See Figure 5-7 for more details.

If the internal oscillator speed is switched between two clocks of the same source, there is no start-up delay before the new frequency is selected. Clock switching time delays are shown in Table 5-1.

Start-up delay specifications are located in the oscillator tables of **Section 30.0** "**Electrical Specifications**".

U-0	U-0	R/W-x/x	R/W-x/x	R-x/x	R/W-x/x	R/W-x/x	R/W-x/x	
		RA5	RA4	RA3	RA2	RA1	RA0	
bit 7							bit 0	
Legend:								
R = Readable bit W = Writable bit		bit	U = Unimplemented bit, read as '0'					
u = Bit is uncha	anged	x = Bit is unkr	nown	-n/n = Value a	at POR and BO	R/Value at all o	ther Resets	
'1' = Bit is set '0' = Bit is cleared		ared						
bit 7-6 Unimplemented: Read as '0								
bit 5-0 RA<5:0>: PORTA I/O Value bits ⁽¹⁾								

REGISTER 12-3: PORTA: PORTA REGISTER

1 = Port pin is > VIH 0 = Port pin is < VIL

REGISTER 12-4: TRISA: PORTA TRI-STATE REGISTER

U-0	U-0	R/W-1/1	R/W-1/1	R-1/1	R/W-1/1	R/W-1/1	R/W-1/1
—	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-6	Unimplemented: Read as '0
bit 5-4	TRISA<5:4>: PORTA Tri-State Control bit 1 = PORTA pin configured as an input (tri-stated) 0 = PORTA pin configured as an output
bit 3	TRISA3: RA3 Port Tri-State Control bit This bit is always '1' as RA3 is an input only
bit 2-0	TRISA<2:0>: PORTA Tri-State Control bit 1 = PORTA pin configured as an input (tri-stated) 0 = PORTA pin configured as an output

Note 1: Writes to PORTA are actually written to corresponding LATA register. Reads from PORTA register is return of actual I/O pin values.

12.3.3 PORTB FUNCTIONS AND OUTPUT PRIORITIES

Each PORTB pin is multiplexed with other functions. The pins, their combined functions and their output priorities are briefly described here. For additional information, refer to the appropriate section in this data sheet.

When multiple outputs are enabled, the actual pin control goes to the peripheral with the lowest number in the following lists.

Analog input and some digital input functions are not included in the list below. These input functions can remain active when the pin is configured as an output. Certain digital input functions override other port functions and are included in the priority list.

RB4 SDA (MSSP) RB5 RX/DT (EUSART) RB6 SCL/SCK (MSSP) RB7 TX/CK (EUSART)

14.0 FIXED VOLTAGE REFERENCE (FVR)

The Fixed Voltage Reference (FVR), is a stable voltage reference, independent of VDD, with 1.024V, 2.048V or 4.096V selectable output levels. The output of the FVR can be configured to supply a reference voltage to the following:

- · ADC input channel
- · ADC positive reference
- · Comparator positive input
- Digital-to-Analog Converter (DAC)

The FVR can be enabled by setting the FVREN bit of the FVRCON register.

14.1 Independent Gain Amplifiers

The output of the FVR supplied to the ADC, Comparators, and DAC is routed through two independent programmable gain amplifiers. Each amplifier can be configured to amplify the reference voltage by 1x, 2x or 4x, to produce the three possible voltage levels.

The ADFVR<1:0> bits of the FVRCON register are used to enable and configure the gain amplifier settings for the reference supplied to the ADC module. Reference **Section 16.0 "Analog-to-Digital Converter (ADC) Module**" for additional information.

The CDAFVR<1:0> bits of the FVRCON register are used to enable and configure the gain amplifier settings for the reference supplied to the DAC and comparator module. Reference Section 17.0 "Digital-to-Analog Converter (DAC) Module" and Section 19.0 "Comparator Module" for additional information.

14.2 FVR Stabilization Period

When the Fixed Voltage Reference module is enabled, it requires time for the reference and amplifier circuits to stabilize. Once the circuits stabilize and are ready for use, the FVRRDY bit of the FVRCON register will be set. See **Section 30.0** "**Electrical Specifications**" for the minimum delay requirement.

FIGURE 14-1: VOLTAGE REFERENCE BLOCK DIAGRAM



25.2.4 SPI SLAVE MODE

In Slave mode, the data is transmitted and received as external clock pulses appear on SCK. When the last bit is latched, the SSP1IF interrupt flag bit is set.

Before enabling the module in SPI Slave mode, the clock line must match the proper Idle state. The clock line can be observed by reading the SCK pin. The Idle state is determined by the CKP bit of the SSP1CON1 register.

While in Slave mode, the external clock is supplied by the external clock source on the SCK pin. This external clock must meet the minimum high and low times as specified in the electrical specifications.

While in Sleep mode, the slave can transmit/receive data. The shift register is clocked from the SCK pin input and when a byte is received, the device will generate an interrupt. If enabled, the device will wake-up from Sleep.

25.2.4.1 Daisy-Chain Configuration

The SPI bus can sometimes be connected in a daisy-chain configuration. The first slave output is connected to the second slave input, the second slave output is connected to the third slave input, and so on. The final slave output is connected to the master input. Each slave sends out, during a second group of clock pulses, an exact copy of what was received during the first group of clock pulses. The whole chain acts as one large communication shift register. The daisy-chain feature only requires a single Slave Select line from the master device.

Figure 25-7 shows the block diagram of a typical Daisy-Chain connection when operating in SPI Mode.

In a daisy-chain configuration, only the most recent byte on the bus is required by the slave. Setting the BOEN bit of the SSP1CON3 register will enable writes to the SSP1BUF register, even if the previous byte has not been read. This allows the software to ignore data that may not apply to it.

25.2.5 SLAVE SELECT SYNCHRONIZATION

The Slave Select can also be used to synchronize communication. The Slave Select line is held high until the master device is ready to communicate. When the Slave Select line is pulled low, the slave knows that a new transmission is starting.

If the slave fails to receive the communication properly, it will be reset at the end of the transmission, when the Slave Select line returns to a high state. The slave is then ready to receive a new transmission when the Slave Select line is pulled low again. If the Slave Select line is not used, there is a risk that the slave will eventually become out of sync with the master. If the slave misses a bit, it will always be one bit off in future transmissions. Use of the Slave Select line allows the slave and master to align themselves at the beginning of each transmission.

The \overline{SS} pin allows a Synchronous Slave mode. The SPI must be in Slave mode with \overline{SS} pin control enabled (SSP1CON1<3:0> = 0100).

When the \overline{SS} pin is low, transmission and reception are enabled and the SDO pin is driven.

When the \overline{SS} pin goes high, the SDO pin is no longer driven, even if in the middle of a transmitted byte and becomes a floating output. External pull-up/pull-down resistors may be desirable depending on the application.

Note 1:	When the SPI is in Slave mode with \overline{SS} pin control enabled (SSP1CON1<3:0> = 0100), the SPI module will reset if the \overline{SS} pin is set to VDD.
2:	When the SPI is used in Slave mode with CKE set; the user must enable \overline{SS} pin control.
3:	While operated in SPI Slave mode the SMP bit of the SSP1STAT register must remain clear.

When the SPI module resets, the bit counter is forced to '0'. This can be done by either forcing the \overline{SS} pin to a high level or clearing the SSP1EN bit.

25.5.2 SLAVE RECEPTION

When the R/\overline{W} bit of a matching received address byte is clear, the R/\overline{W} bit of the SSP1STAT register is cleared. The received address is loaded into the SSP1BUF register and acknowledged.

When the overflow condition exists for a received address, then not Acknowledge is given. An overflow condition is defined as either bit BF bit of the SSP1STAT register is set, or bit SSPOV bit of the SSP1CON1 register is set. The BOEN bit of the SSP1CON3 register modifies this operation. For more information see Register 25-4.

An MSSP1 interrupt is generated for each transferred data byte. Flag bit, SSP1IF, must be cleared by software.

When the SEN bit of the SSP1CON2 register is set, SCL will be held low (clock stretch) following each received byte. The clock must be released by setting the CKP bit of the SSP1CON1 register, except sometimes in 10-bit mode. See **Section 25.2.3 "SPI Master Mode"** for more detail.

25.5.2.1 7-bit Addressing Reception

This section describes a standard sequence of events for the MSSP1 module configured as an I^2C Slave in 7-bit Addressing mode. Figure 25-14 and Figure 25-15 are used as a visual reference for this description.

This is a step by step process of what typically must be done to accomplish I²C communication.

- 1. Start bit detected.
- 2. S bit of SSP1STAT is set; SSP1IF is set if interrupt on Start detect is enabled.
- 3. Matching address with R/\overline{W} bit clear is received.
- 4. The slave pulls SDA low sending an ACK to the master, and sets SSP1IF bit.
- 5. Software clears the SSP1IF bit.
- 6. Software reads received address from SSP1BUF clearing the BF flag.
- 7. If SEN = 1; Slave software sets CKP bit to release the SCL line.
- 8. The master clocks out a data byte.
- 9. Slave drives SDA low sending an ACK to the master, and sets SSP1IF bit.
- 10. Software clears SSP1IF.
- 11. Software reads the received byte from SSP1BUF clearing BF.
- 12. Steps 8-12 are repeated for all received bytes from the Master.
- 13. Master sends Stop condition, setting P bit of SSP1STAT, and the bus goes idle.

25.5.2.2 7-bit Reception with AHEN and DHEN

Slave device reception with AHEN and DHEN set operate the same as without these options with extra interrupts and clock stretching added after the 8th falling edge of SCL. These additional interrupts allow the slave software to decide whether it wants to ACK the receive address or data byte, rather than the hardware. This functionality adds support for PMBus[™] that was not present on previous versions of this module.

This list describes the steps that need to be taken by slave software to use these options for I^2C communication. Figure 25-16 displays a module using both address and data holding. Figure 25-17 includes the operation with the SEN bit of the SSP1CON2 register set.

- 1. S bit of SSP1STAT is set; SSP1IF is set if interrupt on Start detect is enabled.
- Matching address with R/W bit clear is clocked in. SSP1IF is set and CKP cleared after the 8th falling edge of SCL.
- 3. Slave clears the SSP1IF.
- Slave can look at the ACKTIM bit of the SSP1CON3 register to <u>determine</u> if the SSP1IF was after or before the ACK.
- 5. Slave reads the address value from SSP1BUF, clearing the BF flag.
- 6. Slave sets ACK value clocked out to the master by setting ACKDT.
- 7. Slave releases the clock by setting CKP.
- 8. SSP1IF is set after an ACK, not after a NACK.
- 9. If SEN = 1 the slave hardware will stretch the clock after the ACK.

10. Slave clears SSP1IF.

Note: SSP1IF is still set after the 9th falling edge of SCL even if there is no clock stretching and BF has been cleared. Only if NACK is sent to Master is SSP1IF not set

- 11. SSP1IF set and CKP cleared after 8th falling edge of SCL for a received data byte.
- 12. Slave looks at ACKTIM bit of SSP1CON3 to determine the source of the interrupt.
- 13. Slave reads the received data from SSP1BUF clearing BF.
- 14. Steps 7-14 are the same for each received data byte.
- 15. Communication is ended by either the slave sending an ACK = 1, or the master sending a Stop condition. If a Stop is sent and Interrupt on Stop Detect is disabled, the slave will only know by polling the P bit of the SSPSTAT register.

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25.5.8 GENERAL CALL ADDRESS SUPPORT

The addressing procedure for the I^2C bus is such that the first byte after the Start condition usually determines which device will be the slave addressed by the master device. The exception is the general call address which can address all devices. When this address is used, all devices should, in theory, respond with an acknowledge.

The general call address is a reserved address in the I^2C protocol, defined as address 0x00. When the GCEN bit of the SSP1CON2 register is set, the slave module will automatically ACK the reception of this address regardless of the value stored in SSP1ADD. After the slave clocks in an address of all zeros with the R/W bit clear, an interrupt is generated and slave software can read SSP1BUF and respond. Figure 25-24 shows a general call reception sequence.

In 10-bit Address mode, the UA bit will not be set on the reception of the general call address. The slave will prepare to receive the second byte as data, just as it would in 7-bit mode.

If the AHEN bit of the SSP1CON3 register is set, just as with any other address reception, the slave hardware will stretch the clock after the eighth falling edge of SCL. The slave must then set its ACKDT value and release the clock with communication progressing as it would normally.





25.5.9 SSP1 MASK REGISTER

An SSP1 Mask (SSP1MSK) register (Register 25-5) is available in I²C Slave mode as a mask for the value held in the SSP1SR register during an address comparison operation. A zero ('0') bit in the SSP1MSK register has the effect of making the corresponding bit of the received address a "don't care."

This register is reset to all '1's upon any Reset condition and, therefore, has no effect on standard SSP1 operation until written with a mask value.

The SSP1 Mask register is active during:

- 7-bit Address mode: address compare of A<7:1>.
- 10-bit Address mode: address compare of A<7:0> only. The SSP1 mask has no effect during the reception of the first (high) byte of the address.



REGISTER 25-1: SSP1STAT: SSP1 STATUS REGISTER

R/W-0/0	R/W-0/0	R-0/0	R-0/0	R-0/0	R-0/0	R-0/0	R-0/0		
SMP	CKE		P	9	R M	114	RF		
hit 7	UNE	DIA	Г	3	17/17	UA	bit 0		
							bit 0		
Legend:									
R = Readable bi	t	W = Writable bit	ł	U = Unimplem	ented bit read as	ʻ0'			
$\mu = \text{Bit is unchar}$, naed	x = Bit is unknown	wn	-n/n = Value a	POR and BOR/	alue at all other R	Pasats		
'1' = Bit is cot	igeu	x = Dit is unknown -i/ii = value at POK and BOK/value at all other Resets							
T - Dit is set			eu				J		
hit 7	SMP SPI Data	Input Sample bit							
Sit /	SPI Master mode:								
	1 = Input data s	sampled at end o	f data output tir	ne					
	0 = Input data s	sampled at middle	e of data outpu	t time					
	SPI Slave mode SMP must be c	<u>e:</u> leared when SPI	is used in Slav	e mode					
	In I ² C Master o	r Slave mode:							
	 1 = Slew rate of 0 = Slew rate of 	control disabled for control enabled for for the state of the state	or standard spe or high speed n	ed mode (100 k node (400 kHz)	(Hz and 1 MHz)				
bit 6	CKE: SPI Clock	k Edge Select bit	(SPI mode onl	y)					
	In SPI Master of	or Slave mode:							
	1 = Transmit or	ccurs on transition	n from active to	Idle clock state					
	0 = Transmit of		i irom idie to a	clive clock state					
	1 = Enable inpu	ut logic so that thi	resholds are co	mpliant with SM	Ibus specification				
	0 = Disable SM	lbus specific inpu	ts		·				
bit 5	D/A: Data/Addr	ess bit (I ² C mode	e only)						
	1 = Indicates th	at the last byte re	eceived or trans	smitted was data	a				
	0 = Indicates th	hat the last byte re	eceived or trans	smitted was add	ress				
bit 4	P: Stop bit	This bit is shown							
	(I ⁻ C mode only.	. This bit is cleare	ed when the ME	SP1 module is	disabled, SSP1EN	is cleared.)			
	0 = Stop bit was	s not detected las	st		on Reset)				
bit 3	S: Start bit								
	(I ² C mode only	. This bit is cleare	d when the MS	SP1 module is	disabled, SSP1EN	l is cleared.)			
	1 = Indicates th	at a Start bit has	been detected	last (this bit is '	o' on Reset)				
1. i. o	0 = Start bit wa	s not detected las	st (1 ² 0	2					
bit 2	R/W: Read/Wri	te bit information R/M bit information	(I-C mode only	/) ho last addross i	match. This hit is a	nly valid from the	addross match		
	to the next Star	t bit, Stop bit, or r	not ACK bit.			any valid norm the	address match		
	In I ² C Slave mo	ode:							
	$\perp = \text{Read}$ 0 = Write								
	In I ² C Master m	node:							
	1 = Transmit is	s in progress							
	0 = Transmit is	s not in progress							
L 14 A		IS DIT WITH SEIN, F	20 martin anti-	JEN OF ACKEN	will indicate if the i	VISSP1 is in late r	node.		
DIT	UA: Update Ad 1 = Indicates th	dress bit (10-bit i	-C mode only)	address in the	SSP1ADD register				
	0 = Address do	es not need to be	e updated		Sol WEB register				
bit 0	BF: Buffer Full	Status bit							
	Receive (SPI a	nd I ² C modes):							
	1 = Receive co	mplete, SSP1BU	F is full						
	$\cup = \kappa e c e i v e no$	n complete, SSP	IDUF IS EMPTY						
	1 = Data transm	nit in progress (d	oes not include	the ACK and S	top bits), SSP1BU	F is full			
	0 = Data transr	nit complete (doe	s not include th	ne ACK and Stop	bits), SSP1BUF	is empty			

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RETFIE	Return from Interrupt						
Syntax:	[label] RETFIE						
Operands:	None						
Operation:	$TOS \rightarrow PC, \\ 1 \rightarrow GIE$						
Status Affected:	None						
Description:	Return from Interrupt. Stack is POPed and Top-of-Stack (TOS) is loaded in the PC. Interrupts are enabled by setting Global Interrupt Enable bit, GIE (INTCON<7>). This is a 2-cycle instruction.						
Words:	1						
Cycles:	2						
Example:	RETFIE						
	After Interrupt PC = TOS GIE = 1						

RETURN	Return from Subroutine					
Syntax:	[label] RETURN					
Operands:	None					
Operation:	$TOS \rightarrow PC$					
Status Affected:	None					
Description:	Return from subroutine. The stack is POPed and the top of the stack (TOS) is loaded into the program counter. This is a 2-cycle instruction.					

RETLW	Return with literal in W		Pototo Loft f through Corry			
Syntax:	[<i>label</i>] RETLW k	RLF				
Operands:	$0 \le k \le 255$	Syntax:	[<i>label</i>] RLF f,d			
Operation:	$k \rightarrow (W);$ TOS \rightarrow PC	Operands:	$0 \le f \le 127$ $d \in [0,1]$			
Status Affected	None	Operation:	See description below			
	The W register is loaded with the 8-bit	Status Affected:	С			
Description.	literal 'k'. The program counter is loaded from the top of the stack (the return address). This is a 2-cycle instruction.	Description:	The contents of register 'f' are rotated one bit to the left through the Carry flag. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is			
Words:	1		stored back in register T.			
Cycles:	2					
Example:	CALL TABLE;W contains table	Words:	1			
	;offset value . :W now has table value	Cycles:	1			
TABLE	•	Example:	RLF REG1,0			
	• ADDWF PC ;W = offset RETLW k1 ;Begin table RETLW k2 ; • • RETLW kn ; End of table		Before Instruction REG1 = 1110 0110 C = 0 After Instruction REG1 = 1110 0110 W = 1100 1100 C = 1			
	Before Instruction W = 0x07 After Instruction W = value of k8					

30.3 DC Characteristics: PIC16(L)F1824/8-I/E (Power-Down)

PIC16LF1824/8		$\begin{array}{llllllllllllllllllllllllllllllllllll$					nerwise stated) 'C for industrial 5°C for extended	
PIC16F1824/8		Standard Operating Condi Operating temperature			itions (unless otherwise stated) -40°C \leq TA \leq +85°C for industrial -40°C \leq TA \leq +125°C for extended			
Param	Param Device Characteristics Min		Tunt	Max.	Max.	Unite		Conditions
No.		WIIII.	וקעי	+85°C	+125°C	Units	Vdd	Note
Power-down Base Current (IPD) ⁽²⁾								
D022			0.02	1.0	2.4	μA	1.8	WDT, BOR, FVR, and T1OSC
		—	0.03	1.5	3.0	μA	3.0	disabled, all Peripherals Inactive
D022			18	37	44	μA	1.8	WDT, BOR, FVR, and T1OSC
		_	20	42	48	μA	3.0	disabled, all Peripherals Inactive
		—	22	45	65	μA	5.0	
D023			0.2	2.0	3.0	μA	1.8	LPWDT Current (Note 1)
			0.5	2.0	4.0	μA	3.0	
D023			18	38	44	μA	1.8	LPWDT Current (Note 1)
		_	21	43	48	μA	3.0	4
		—	22	46	65	μA	5.0	
D023A			12	22	25	μA	1.8	FVR current
			13	24	27	μA	3.0	
D023A			33	62	65	μA	1.8	FVR current
			40	72	75	μA	3.0	_
			68	115	120	μA	5.0	
D024			7.0	14	16	μA	3.0	BOR Current (Note 1)
D024			24	47	50	μA	3.0	BOR Current (Note 1)
		—	29	55	70	μA	5.0	
D025			0.65	3.5	4.0	μA	1.8	T1OSC Current (Note 1)
		—	2.3	4.0	4.5	μA	3.0	
D025			19	39	45	μA	1.8	T1OSC Current (Note 1)
			21	43	59	μA	3.0	4
		-	23	55	75	μA	5.0	
D026			0.03	1.5	3.0	μA	1.8	A/D Current (Note 1, 3),
		-	0.04	2.0	3.5	μA	3.0	
D026			18	38	45	μA	1.8	A/D Current (Note 1, 3),
		_	20	43	49	μA	3.0	no conversion in progress
		—	22	46	65	μA	5.0	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The peripheral current is the sum of the base IDD or IPD and the additional current consumed when this peripheral is enabled. The peripheral △ current can be determined by subtracting the base IDD or IPD current from this limit. Max values should be used when calculating total current consumption.

2: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD.

3: A/D oscillator source is FRC.

30.7 Timing Parameter Symbology

The timing parameter symbols have been created with one of the following formats:

- 1. TppS2ppS
- 2. TppS

T			
F	Frequency	т	Time
Lowerc	case letters (pp) and their meanings:		
рр			
сс	CCP1	osc	OSC1
ck	CLKOUT	rd	RD
CS	CS	rw	RD or WR
di	SDIx	sc	SCKx
do	SDO	ss	SS
dt	Data in	tO	TOCKI
io	I/O PORT	t1	T1CKI
mc	MCLR	wr	WR
Upperc	case letters and their meanings:	·	
S			
F	Fall	Р	Period
Н	High	R	Rise
I	Invalid (High-impedance)	V	Valid
L	Low	Z	High-impedance

FIGURE 30-5: LOAD CONDITIONS



TABLE 30-12: USART SYNCHRONOUS TRANSMISSION REQUIREMENTS

Standard Operating Conditions (unless otherwise stated)Operating Temperature $-40^{\circ}C \le TA \le +125^{\circ}C$								
Param. No.	Symbol	Characteristic		Min.	Max.	Units	Conditions	
US120	TCKH2DTV	SYNC XMIT (Master and Slave) Clock high to data-out valid	3.0-5.5V	—	80	ns		
			1.8-5.5V	_	100	ns		
US121	TCKRF	Clock out rise time and fall time (Master mode)	3.0-5.5V	—	45	ns		
			1.8-5.5V	—	50	ns		
US122	TDTRF	Data-out rise time and fall time	3.0-5.5V		45	ns		
			1.8-5.5V		50	ns		

FIGURE 30-15: USART SYNCHRONOUS RECEIVE (MASTER/SLAVE) TIMING



TABLE 30-13: USART SYNCHRONOUS RECEIVE REQUIREMENTS

Standard Operating Conditions (unless otherwise stated)Operating Temperature $-40^{\circ}C \le TA \le +125^{\circ}C$							
Param. No.	Symbol	Characteristic	Min.	Max.	Units	Conditions	
US125	TDTV2CKL	SYNC RCV (Master and Slave) Data-hold before $CK \downarrow$ (DT hold time)	10		ns		
US126	TCKL2DTL	Data-hold after CK \downarrow (DT hold time)	15		ns		

PIC16(L)F1824/8









32.2 MPLAB XC Compilers

The MPLAB XC Compilers are complete ANSI C compilers for all of Microchip's 8, 16, and 32-bit MCU and DSC devices. These compilers provide powerful integration capabilities, superior code optimization and ease of use. MPLAB XC Compilers run on Windows, Linux or MAC OS X.

For easy source level debugging, the compilers provide debug information that is optimized to the MPLAB X IDE.

The free MPLAB XC Compiler editions support all devices and commands, with no time or memory restrictions, and offer sufficient code optimization for most applications.

MPLAB XC Compilers include an assembler, linker and utilities. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. MPLAB XC Compiler uses the assembler to produce its object file. Notable features of the assembler include:

- · Support for the entire device instruction set
- · Support for fixed-point and floating-point data
- Command-line interface
- · Rich directive set
- · Flexible macro language
- MPLAB X IDE compatibility

32.3 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for PIC10/12/16/18 MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel[®] standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code, and COFF files for debugging.

The MPASM Assembler features include:

- Integration into MPLAB X IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multipurpose source files
- Directives that allow complete control over the assembly process

32.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

32.5 MPLAB Assembler, Linker and Librarian for Various Device Families

MPLAB Assembler produces relocatable machine code from symbolic assembly language for PIC24, PIC32 and dsPIC DSC devices. MPLAB XC Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- · Support for the entire device instruction set
- · Support for fixed-point and floating-point data
- Command-line interface
- Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility









33.3 Package Marking Information (Continued)

20-Lead SSOP (5.30 mm)





20-Lead QFN (4x4x0.9 mm) 20-Lead UQFN (4x4x0.5mm)



Example



20-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	MILLIMETERS				
Dimension	MIN	NOM	MAX		
Contact Pitch	E	0.65 BSC			
Contact Pad Spacing	С		7.20		
Contact Pad Width (X20)	X1			0.45	
Contact Pad Length (X20)	Y1			1.75	
Distance Between Pads	G	0.20			

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2072A