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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	11
Program Memory Size	7KB (4K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	14-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	14-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf1824t-i-st

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4.0 DEVICE CONFIGURATION

Device Configuration consists of Configuration Word 1 and Configuration Word 2, Code Protection and Device ID.

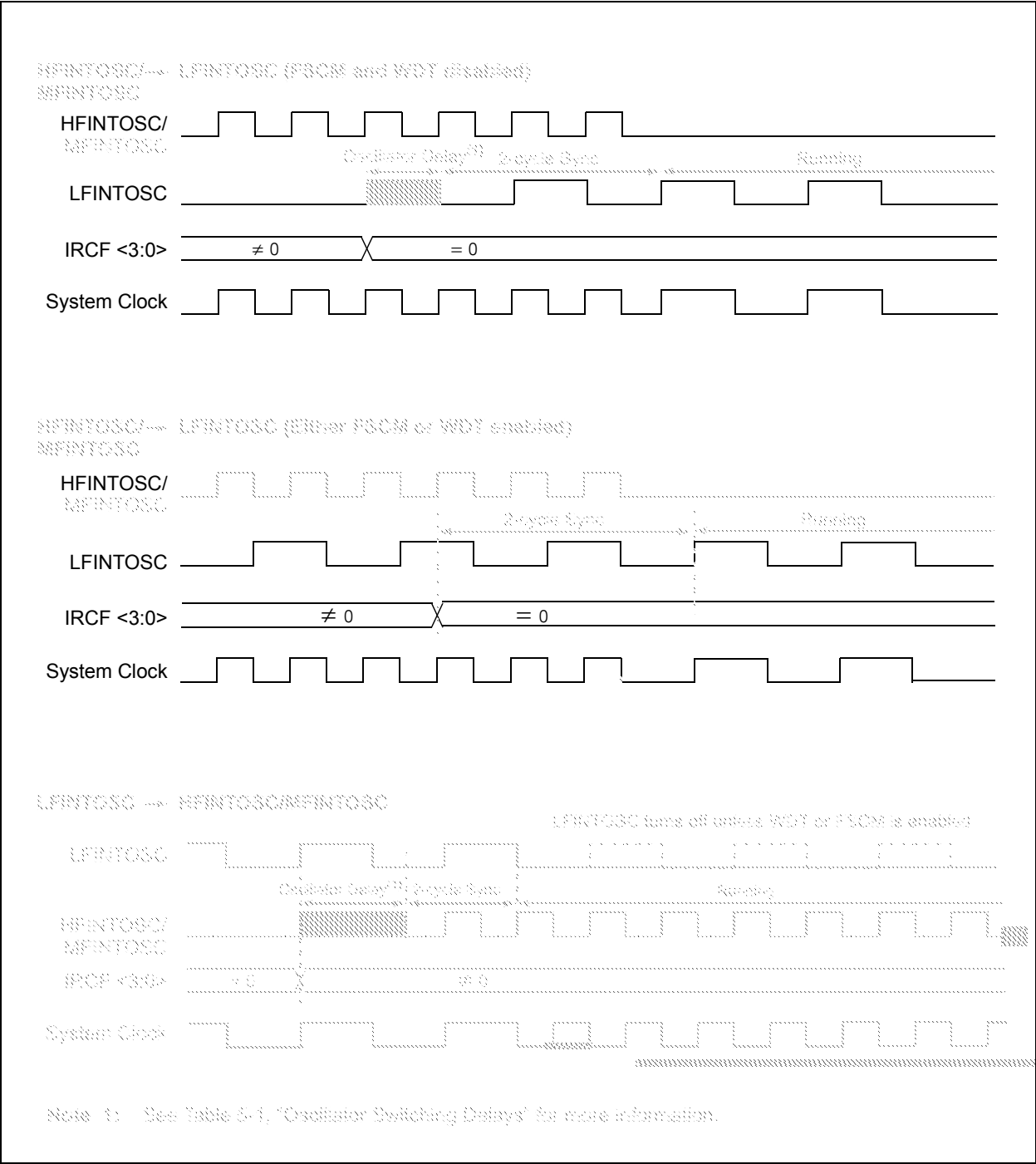
4.1 Configuration Words

There are several Configuration Word bits that allow different oscillator and memory protection options. These are implemented as Configuration Word 1 at 8007h and Configuration Word 2 at 8008h.

<p>Note: The <code>DEBUG</code> bit in Configuration Word is managed automatically by device development tools including debuggers and programmers. For normal device operation, this bit should be maintained as a '1'.</p>

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FIGURE 5-7: INTERNAL OSCILLATOR SWITCH TIMING



9.0 POWER-DOWN MODE (SLEEP)

The Power-Down mode is entered by executing a `SLEEP` instruction.

Upon entering Sleep mode, the following conditions exist:

1. WDT will be cleared but keeps running, if enabled for operation during Sleep.
2. \overline{PD} bit of the STATUS register is cleared.
3. \overline{TO} bit of the STATUS register is set.
4. CPU clock is disabled.
5. 31 kHz LFINTOSC is unaffected and peripherals that operate from it may continue operation in Sleep.
6. Timer1 oscillator is unaffected and peripherals that operate from it may continue operation in Sleep.
7. ADC is unaffected, if the dedicated FRC clock is selected.
8. Capacitive Sensing oscillator is unaffected.
9. I/O ports maintain the status they had before `SLEEP` was executed (driving high, low or high-impedance).
10. Resets other than WDT are not affected by Sleep mode.

Refer to individual chapters for more details on peripheral operation during Sleep.

To minimize current consumption, the following conditions should be considered:

- I/O pins should not be floating
- External circuitry sinking current from I/O pins
- Internal circuitry sourcing current from I/O pins
- Current draw from pins with internal weak pull-ups
- Modules using 31 kHz LFINTOSC
- Modules using Timer1 oscillator

I/O pins that are high-impedance inputs should be pulled to VDD or VSS externally to avoid switching currents caused by floating inputs.

Examples of internal circuitry that might be sourcing current include modules such as the DAC and FVR modules. See **Section 17.0 “Digital-to-Analog Converter (DAC) Module”** and **Section 14.0 “Fixed Voltage Reference (FVR)”** for more information on these modules.

9.1 Wake-up from Sleep

The device can wake-up from Sleep through one of the following events:

1. External Reset input on \overline{MCLR} pin, if enabled
2. BOR Reset, if enabled
3. POR Reset
4. Watchdog Timer, if enabled
5. Any external interrupt
6. Interrupts by peripherals capable of running during Sleep (see individual peripheral for more information)

The first three events will cause a device Reset. The last three events are considered a continuation of program execution. To determine whether a device Reset or wake-up event occurred, refer to **Section 7.10 “Determining the Cause of a Reset”**.

When the `SLEEP` instruction is being executed, the next instruction (`PC + 1`) is prefetched. For the device to wake-up through an interrupt event, the corresponding interrupt enable bit must be enabled. Wake-up will occur regardless of the state of the GIE bit. If the GIE bit is disabled, the device continues execution at the instruction after the `SLEEP` instruction. If the GIE bit is enabled, the device executes the instruction after the `SLEEP` instruction, the device will call the Interrupt Service Routine. In cases where the execution of the instruction following `SLEEP` is not desirable, the user should have a `NOP` after the `SLEEP` instruction.

The WDT is cleared when the device wakes up from Sleep, regardless of the source of wake-up.

9.1.1 WAKE-UP USING INTERRUPTS

When global interrupts are disabled (GIE cleared) and any interrupt source has both its interrupt enable bit and interrupt flag bit set, one of the following will occur:

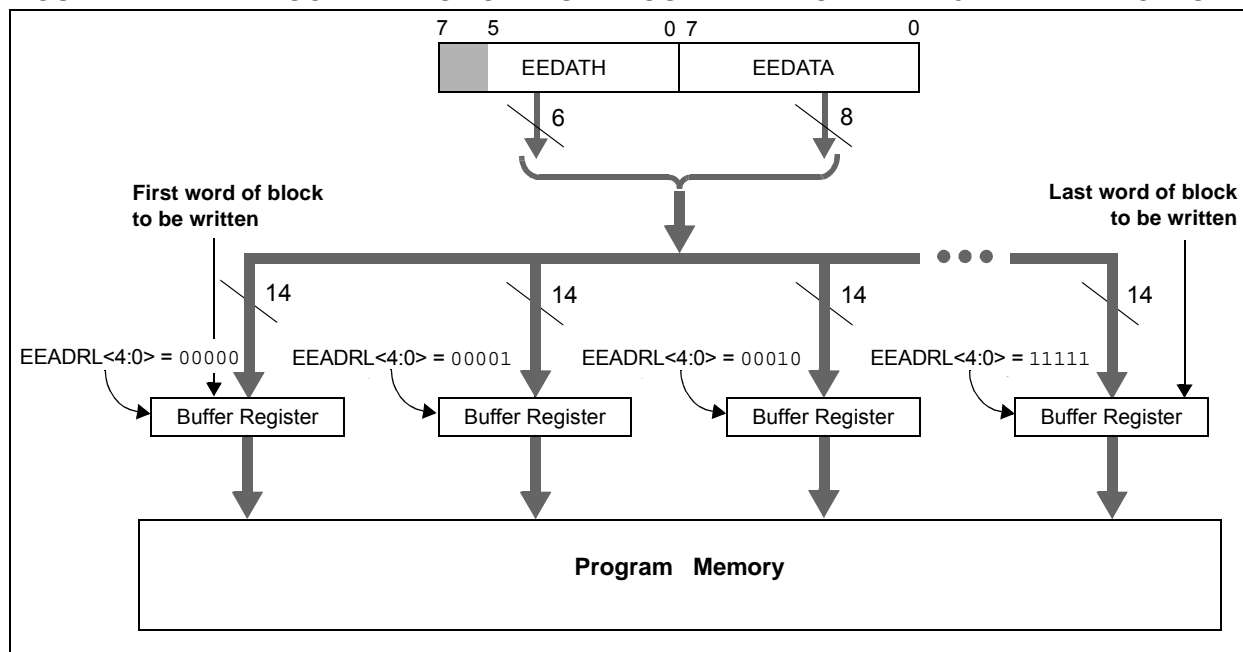
- If the interrupt occurs **before** the execution of a `SLEEP` instruction
 - `SLEEP` instruction will execute as a `NOP`
 - WDT and WDT prescaler will not be cleared
 - \overline{TO} bit of the STATUS register will not be set
 - \overline{PD} bit of the STATUS register will not be cleared
- If the interrupt occurs **during or after** the execution of a `SLEEP` instruction
 - `SLEEP` instruction will be completely executed
 - Device will immediately wake-up from Sleep
 - WDT and WDT prescaler will be cleared
 - \overline{TO} bit of the STATUS register will be set
 - \overline{PD} bit of the STATUS register will be cleared

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After the “BSF `EECON1, WR`” instruction, the processor requires two cycles to set up the write operation. The user must place two `NOP` instructions after the `WR` bit is set. The processor will halt internal operations for the typical 2ms, only during the cycle in which the write takes place (i.e., the last word of the block write). This is not Sleep mode, as the clocks and peripherals will

continue to run. The processor does not stall when `LWLO = 1`, loading the write latches. After the write cycle, the processor will resume operation with the third instruction after the `EECON1` write instruction.

FIGURE 11-2: BLOCK WRITES TO FLASH PROGRAM MEMORY WITH 32 WRITE LATCHES



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11.6 Write Verify

Depending on the application, good programming practice may dictate that the value written to the data EEPROM or program memory should be verified (see Example 11-6) to the desired value to be written. Example 11-6 shows how to verify a write to EEPROM.

EXAMPLE 11-6: EEPROM WRITE VERIFY

```
BANKSEL EEDATL      ;  
MOVF    EEDATL, W    ;EEDATL not changed  
                      ;from previous write  
BSF      EECON1, RD   ;YES, Read the  
                      ;value written  
XORWF    EEDATL, W    ;  
BTFSS    STATUS, Z    ;Is data the same  
GOTO     WRITE_ERR    ;No, handle error  
:        ;Yes, continue
```

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REGISTER 12-5: LATA: PORTA DATA LATCH REGISTER

U-0	U-0	R/W-x/u	R/W-x/u	U-0	R/W-x/u	R/W-x/u	R/W-x/u
—	—	LATA5	LATA4	—	LATA2	LATA1	LATA0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

bit 7-6 **Unimplemented:** Read as '0'

bit 5-4 **LATA<5:4>**: RA<5:4> Output Latch Value bits⁽¹⁾

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **LATA<2:0>**: RA<2:0> Output Latch Value bits⁽¹⁾

Note 1: Writes to PORTA are actually written to corresponding LATA register. Reads from PORTA register is return of actual I/O pin values.

REGISTER 12-6: ANSELA: PORTA ANALOG SELECT REGISTER

U-0	U-0	U-0	R/W-1/1	U-0	R/W-1/1	R/W-1/1	R/W-1/1
—	—	—	ANSA4	—	ANSA2	ANSA1	ANSA0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

bit 7-5 **Unimplemented:** Read as '0'

bit 4 **ANSA4**: Analog Select between Analog or Digital Function on pins RA4, respectively

0 = Digital I/O. Pin is assigned to port or digital special function.

1 = Analog input. Pin is assigned as analog input⁽¹⁾. Digital input buffer disabled.

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **ANSA<2:0>**: Analog Select between Analog or Digital Function on pins RA<2:0>, respectively

0 = Digital I/O. Pin is assigned to port or digital special function.

1 = Analog input. Pin is assigned as analog input⁽¹⁾. Digital input buffer disabled.

Note 1: When setting a pin to an analog input, the corresponding TRIS bit must be set to Input mode in order to allow external control of the voltage on the pin.

PIC16(L)F1824/8

REGISTER 12-20: INLVLC: PORTC INPUT LEVEL CONTROL REGISTER

U-0 ⁽³⁾ R/W-1/1 ⁽²⁾	U-0 ⁽³⁾ R/W-1/1 ⁽²⁾	R/W-0/0 ⁽³⁾ R/W-1/1 ⁽²⁾	R/W-0/0 ⁽³⁾ R/W-1/1 ⁽²⁾	R/W-0/0 ⁽³⁾ R/W-1/1 ⁽²⁾	R/W-0/0 ⁽³⁾ R/W-1/1 ⁽²⁾	R/W-0/0 ⁽³⁾ R/W-1/1 ⁽²⁾	R/W-0/0 ⁽³⁾ R/W-1/1 ⁽²⁾
INLVLC7 ⁽¹⁾	INLVLC6 ⁽¹⁾	INLVLC5	INLVLC4	INLVLC3	INLVLC2	INLVLC1	INLVLC0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
u = Bit is unchanged x = Bit is unknown -n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set '0' = Bit is cleared

bit 7-0 **INLVLC<7:0>**: PORTC Input Level Select bits⁽¹⁾
For RC<7:0> pins, respectively
1 = ST input used for PORT reads and Interrupt-on-Change
0 = TTL input used for PORT reads and Interrupt-on-Change

- Note 1:** INLVLC<7:6> available on PIC16(L)F1828 only. Otherwise, they are unimplemented and read as '0'.
2: PIC16(L)F1828 only, Reset default value.
3: PIC16(L)F1824 only, Reset default value.

TABLE 12-4: SUMMARY OF REGISTERS ASSOCIATED WITH PORTC

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ANSEL	ANSC7 ⁽¹⁾	ANSC6 ⁽¹⁾	—	—	ANSC3	ANSC2	ANSC1	ANSC0	133
INLVLC	INLVLC7 ⁽¹⁾	INLVLC6 ⁽¹⁾	INLVLC5	INLVLC4	INLVLC3	INLVLC2	INLVLC1	INLVLC0	134
LATC	LATC7 ⁽¹⁾	LATC6 ⁽¹⁾	LATC5	LATC4	LATC3	LATC2	LATC1	LATC0	132
PORTC	RC7 ⁽¹⁾	RC6 ⁽¹⁾	RC5	RC4	RC3	RC2	RC1	RC0	132
TRISC	TRISC7 ⁽¹⁾	TRISC6 ⁽¹⁾	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	132
WPUC	WPUC7 ⁽¹⁾	WPUC6 ⁽¹⁾	WPUC5	WPUC4	WPUC3	WPUC2	WPUC1	WPUC0	133

Legend: x = unknown, u = unchanged, - = unimplemented locations, read as '0'. Shaded cells are not used by PORTC.

Note 1: PIC16(L)F1828 only.

PIC16(L)F1824/8

16.2.6 A/D CONVERSION PROCEDURE

This is an example procedure for using the ADC to perform an Analog-to-Digital conversion:

1. Configure Port:
 - Disable pin output driver (Refer to the TRIS register)
 - Configure pin as analog (Refer to the ANSEL register)
2. Configure the ADC module:
 - Select ADC conversion clock
 - Configure voltage reference
 - Select ADC input channel
 - Turn on ADC module
3. Configure ADC interrupt (optional):
 - Clear ADC interrupt flag
 - Enable ADC interrupt
 - Enable peripheral interrupt
 - Enable global interrupt⁽¹⁾
4. Wait the required acquisition time⁽²⁾.
5. Start conversion by setting the GO/DONE bit.
6. Wait for ADC conversion to complete by one of the following:
 - Polling the GO/DONE bit
 - Waiting for the ADC interrupt (interrupts enabled)
7. Read ADC Result.
8. Clear the ADC interrupt flag (required if interrupt is enabled).

Note 1: The global interrupt can be disabled if the user is attempting to wake-up from Sleep and resume in-line code execution.

2: Refer to **Section 16.3 “A/D Acquisition Requirements”**.

EXAMPLE 16-1: A/D CONVERSION

```
;This code block configures the ADC
;for polling, Vdd and Vss references, Frc
;clock and AN0 input.
;
;Conversion start & polling for completion
; are included.
;
BANKSEL    ADCON1        ;
MOVLW      B'11110000'   ;Right justify, Frc
                                ;clock
MOVWF      ADCON1        ;Vdd and Vss Vref
BANKSEL    TRISA         ;
BSF         TRISA,0       ;Set RA0 to input
BANKSEL    ANSEL         ;
BSF         ANSEL,0       ;Set RA0 to analog
BANKSEL    ADCON0        ;
MOVLW      B'00000001'   ;Select channel AN0
MOVWF      ADCON0        ;Turn ADC On
CALL       SampleTime    ;Acquisition delay
BSF         ADCON0,ADGO   ;Start conversion
BTFSF      ADCON0,ADGO   ;Is conversion done?
GOTO       $-1           ;No, test again
BANKSEL    ADRESH        ;
MOVF       ADRESH,W      ;Read upper 2 bits
MOVWF      RESULTHI      ;store in GPR space
BANKSEL    ADRESL        ;
MOVF       ADRESL,W      ;Read lower 8 bits
MOVWF      RESULTLO      ;Store in GPR space
```

24.4.2 FULL-BRIDGE MODE

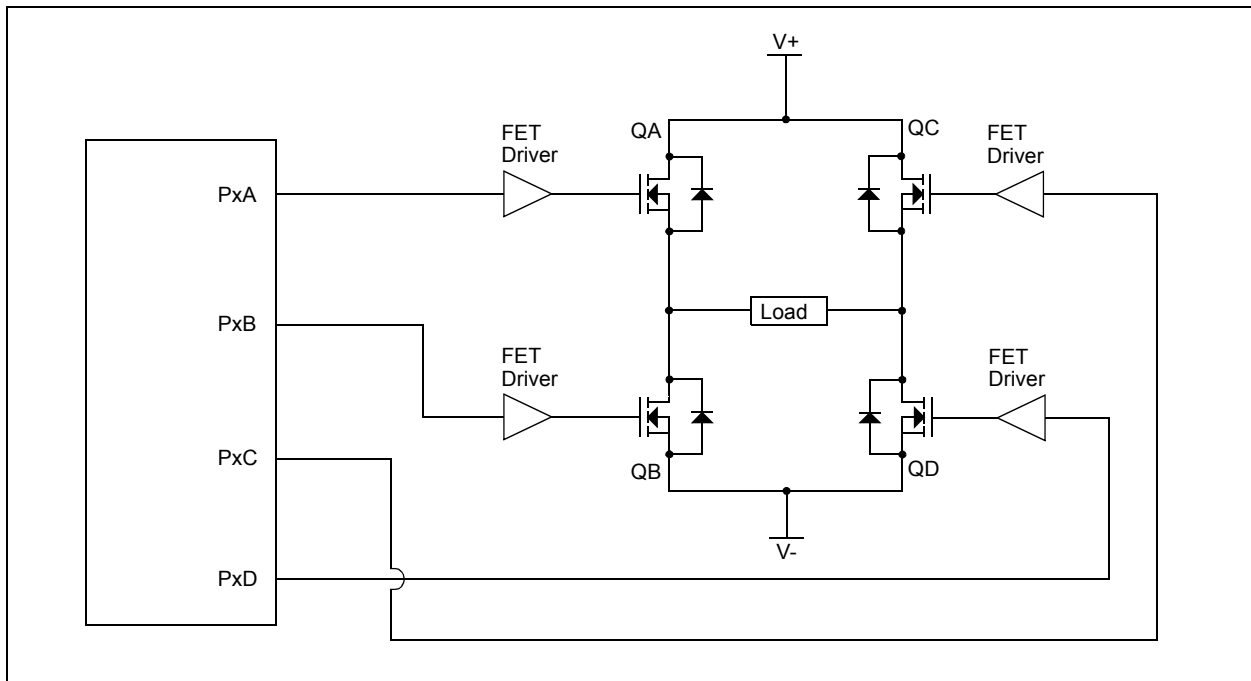
In Full-Bridge mode, all four pins are used as outputs. An example of Full-Bridge application is shown in Figure 24-10.

In the Forward mode, pin CCPx/PxA is driven to its active state, pin PxD is modulated, while PxB and PxC will be driven to their inactive state as shown in Figure 24-11.

In the Reverse mode, PxC is driven to its active state, pin PxB is modulated, while PxA and PxD will be driven to their inactive state as shown Figure 24-11.

PxA, PxB, PxC and PxD outputs are multiplexed with the PORT data latches. The associated TRIS bits must be cleared to configure the PxA, PxB, PxC and PxD pins as outputs.

FIGURE 24-10: EXAMPLE OF FULL-BRIDGE APPLICATION



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24.4.6 PWM STEERING MODE

In Single Output mode, PWM steering allows any of the PWM pins to be the modulated signal. Additionally, the same PWM signal can be simultaneously available on multiple pins.

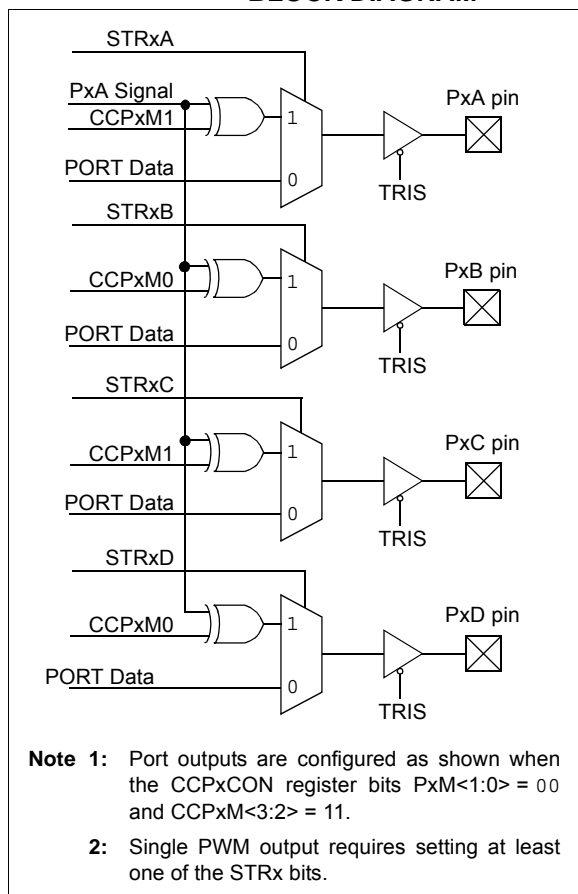
Once the Single Output mode is selected ($CCPxM<3:2> = 11$ and $PxM<1:0> = 00$ of the $CCPxCON$ register), the user firmware can bring out the same PWM signal to one, two, three or four output pins by setting the appropriate $STRx<D:A>$ bits of the $PSTRxCON$ register, as shown in Table 24-9.

Note: The associated TRIS bits must be set to output ('0') to enable the pin output driver in order to see the PWM signal on the pin.

While the PWM Steering mode is active, $CCPxM<1:0>$ bits of the $CCPxCON$ register select the PWM output polarity for the $Px<D:A>$ pins.

The PWM auto-shutdown operation also applies to PWM Steering mode as described in **Section 24.4.3 “Enhanced PWM Auto-shutdown mode”**. An auto-shutdown event will only affect pins that have PWM outputs enabled.

FIGURE 24-18: SIMPLIFIED STEERING BLOCK DIAGRAM



PIC16(L)F1824/8

FIGURE 25-14: I²C SLAVE, 7-BIT ADDRESS, RECEPTION (SEN = 0, AHEN = 0, DHEN = 0)

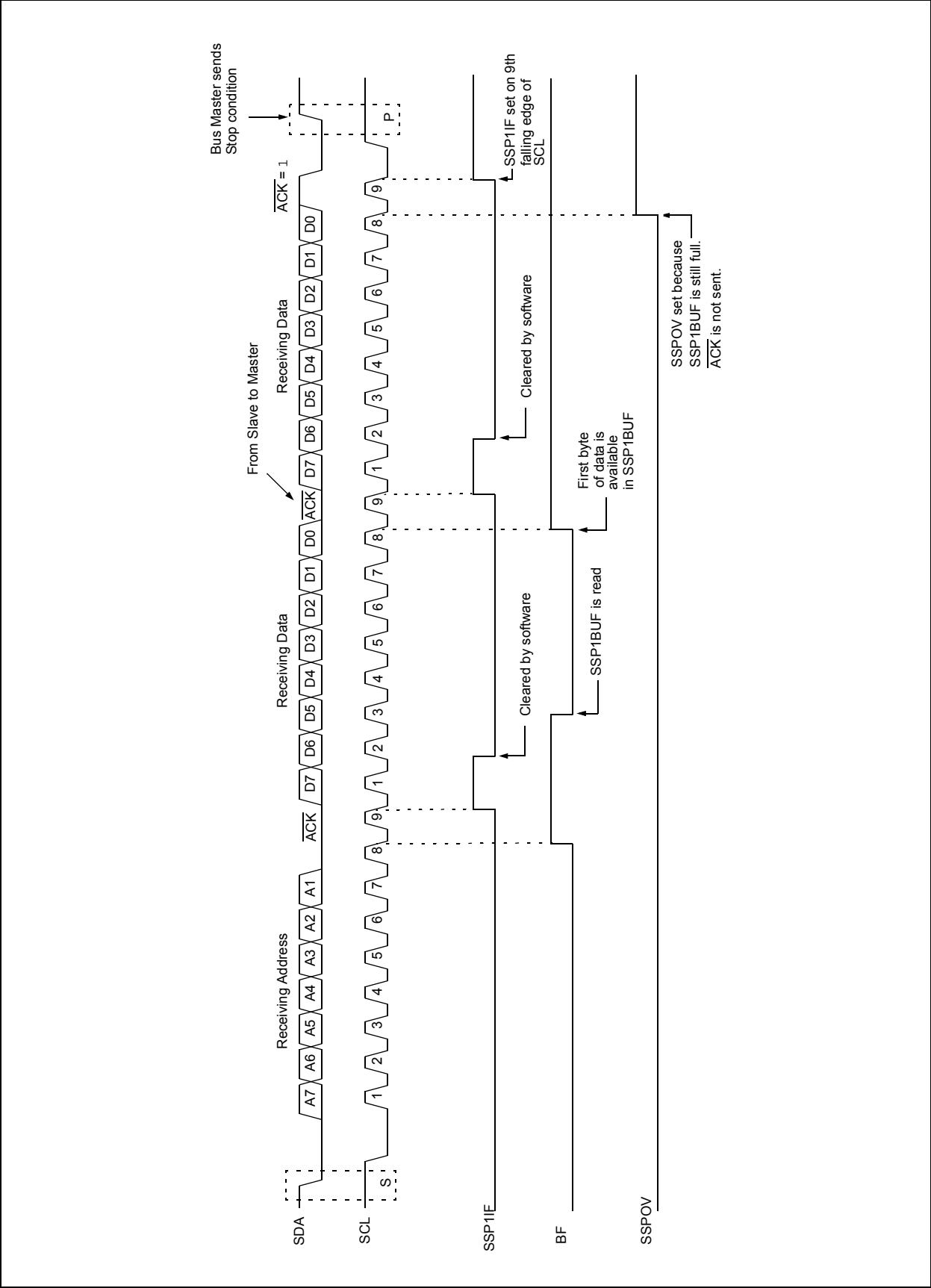


FIGURE 25-18: I²C SLAVE, 7-BIT ADDRESS, TRANSMISSION (AHEN = 0)

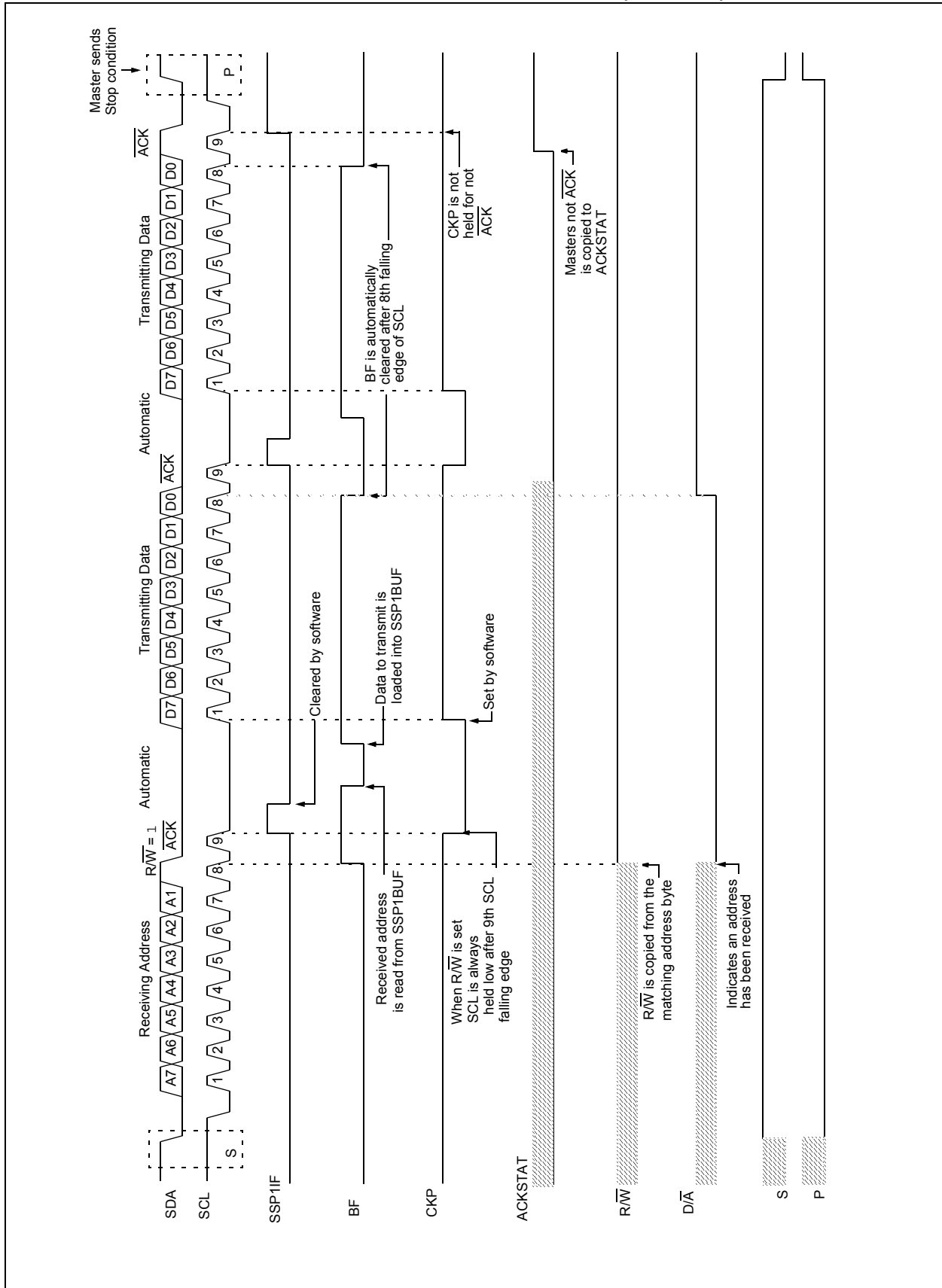
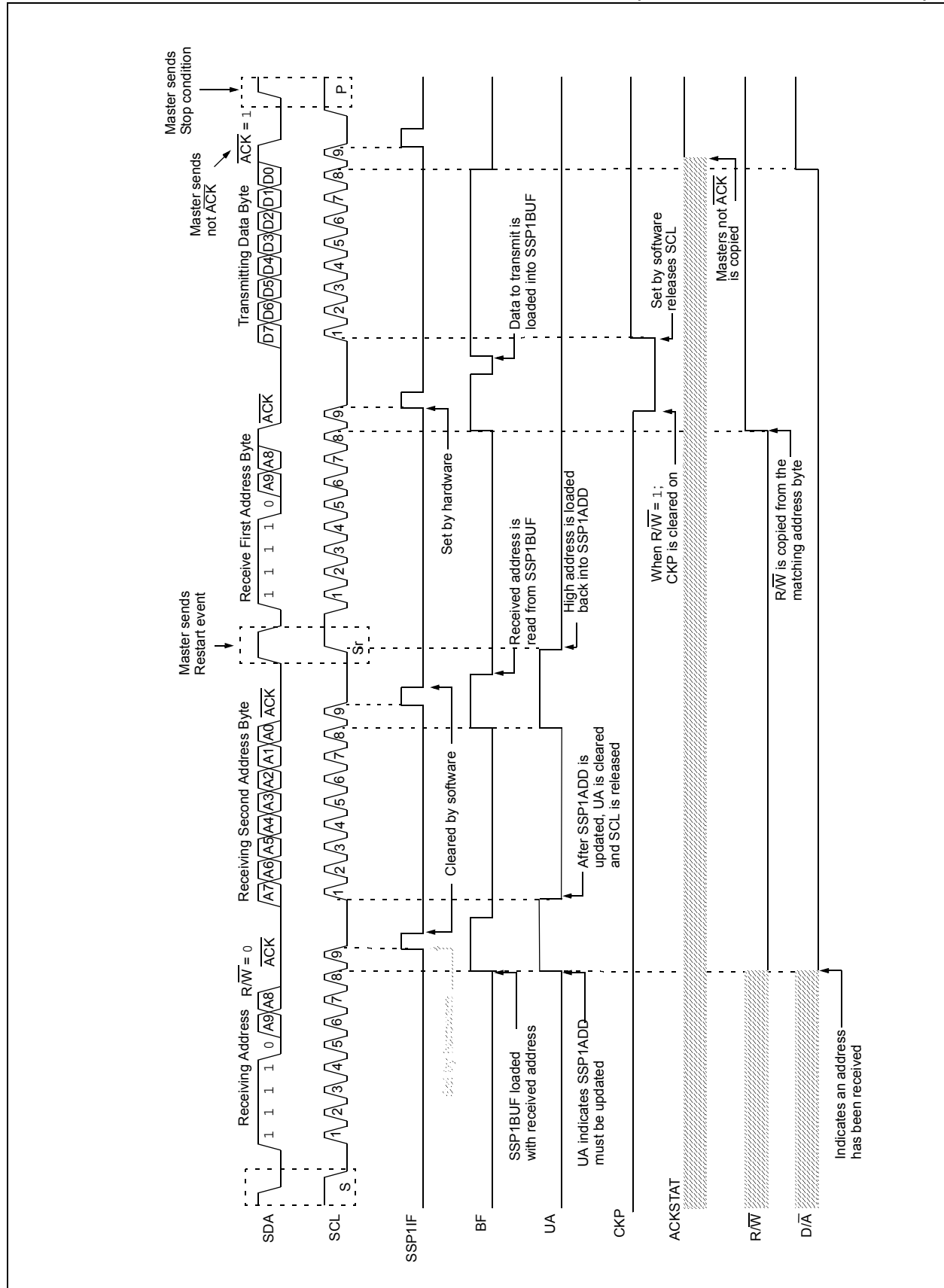


FIGURE 25-22: I²C SLAVE, 10-BIT ADDRESS, TRANSMISSION (SEN = 0, AHEN = 0, DHEN = 0)



PIC16(L)F1824/8

25.7 Baud Rate Generator

The MSSP1 module has a Baud Rate Generator available for clock generation in both I²C and SPI Master modes. The Baud Rate Generator (BRG) reload value is placed in the SSP1ADD register (Register 25-6). When a write occurs to SSP1BUF, the Baud Rate Generator will automatically begin counting down.

Once the given operation is complete, the internal clock will automatically stop counting and the clock pin will remain in its last state.

An internal signal “Reload” in Figure 25-40 triggers the value from SSP1ADD to be loaded into the BRG counter. This occurs twice for each oscillation of the

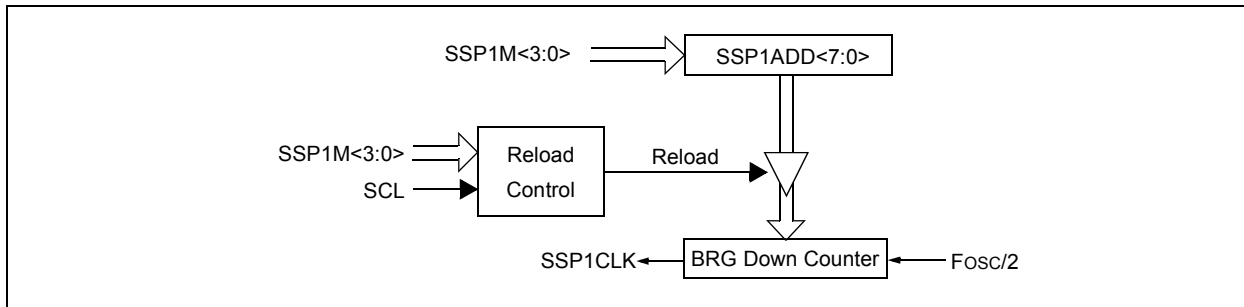
module clock line. The logic dictating when the reload signal is asserted depends on the mode the MSSP1 is being operated in.

Table 25-4 demonstrates clock rates based on instruction cycles and the BRG value loaded into SSP1ADD.

EQUATION 25-1:

$$F_{CLOCK} = \frac{F_{OSC}}{(SSP_{xADD} + 1)(4)}$$

FIGURE 25-40: BAUD RATE GENERATOR BLOCK DIAGRAM



Note: Values of 0x00, 0x01 and 0x02 are not valid for SSP1ADD when used as a Baud Rate Generator for I²C. This is an implementation limitation.

TABLE 25-4: MSSP1 CLOCK RATE W/BRG

Fosc	Fcy	BRG Value	FCLOCK (2 Rollovers of BRG)
32 MHz	8 MHz	13h	400 kHz
32 MHz	8 MHz	19h	308 kHz
32 MHz	8 MHz	4Fh	100 kHz
16 MHz	4 MHz	09h	400 kHz
16 MHz	4 MHz	0Ch	308 kHz
16 MHz	4 MHz	27h	100 kHz
4 MHz	1 MHz	09h	100 kHz

Note: Refer to the I/O port electrical and timing specifications in Table 30-4 and Figure 30-7 to ensure the system is designed to support the I/O requirements.

PIC16(L)F1824/8

TABLE 26-3: BAUD RATE FORMULAS

Configuration Bits			BRG/EUSART Mode	Baud Rate Formula
SYNC	BRG16	BRGH		
0	0	0	8-bit/Asynchronous	$F_{osc}/[64 (n+1)]$
0	0	1	8-bit/Asynchronous	$F_{osc}/[16 (n+1)]$
0	1	0	16-bit/Asynchronous	
0	1	1	16-bit/Asynchronous	$F_{osc}/[4 (n+1)]$
1	0	x	8-bit/Synchronous	
1	1	x	16-bit/Synchronous	

Legend: x = Don't care, n = value of SPBRGH, SPBRGL register pair

TABLE 26-4: SUMMARY OF REGISTERS ASSOCIATED WITH THE BAUD RATE GENERATOR

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
BAUDCON	ABDOVF	RCIDL	—	SCKP	BRG16	—	WUE	ABDEN	296
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	295
SPBRGL	BRG7	BRG6	BRG5	BRG4	BRG3	BRG2	BRG1	BRG0	297*
SPBRGH	BRG15	BRG14	BRG13	BRG12	BRG11	BRG10	BRG9	BRG8	297*
TXSTA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	294

Legend: — = unimplemented location, read as '0'. Shaded cells are not used for the Baud Rate Generator.

* Page provides register information.

PIC16(L)F1824/8

FIGURE 30-18: SPI SLAVE MODE TIMING (CKE = 0)

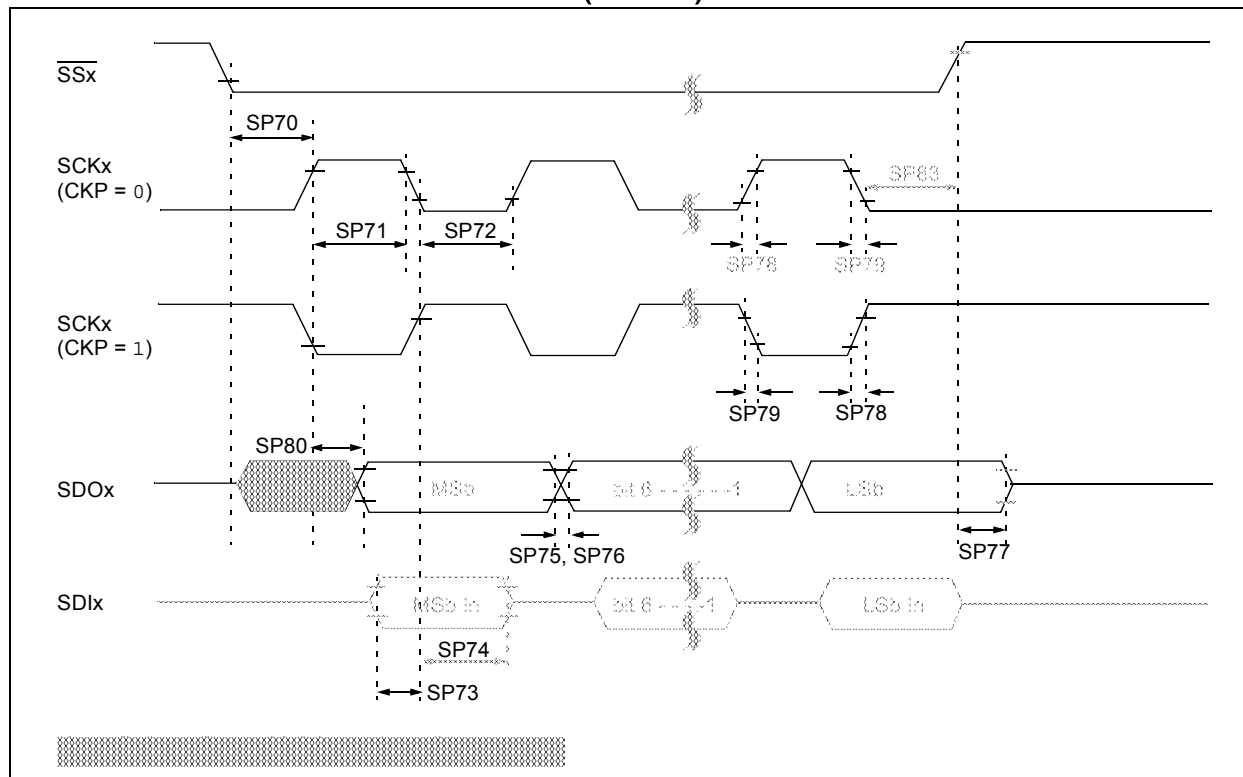
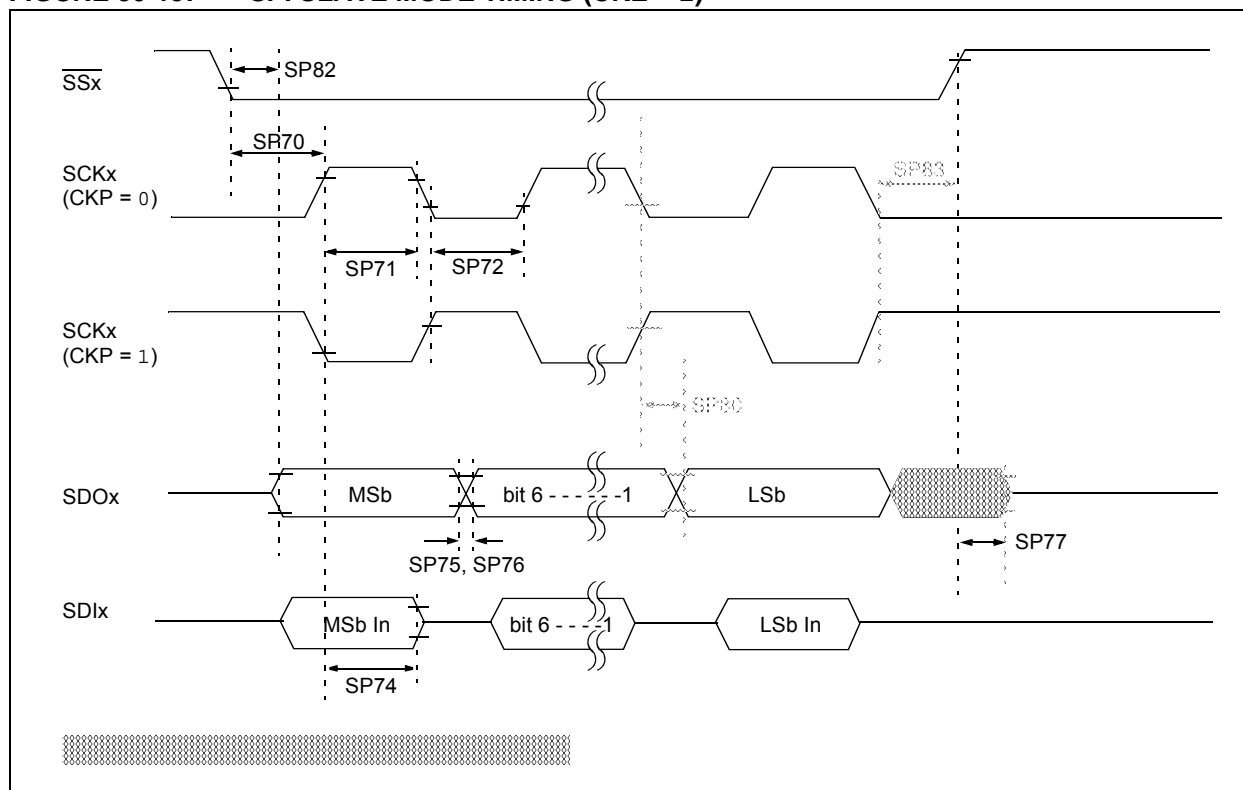


FIGURE 30-19: SPI SLAVE MODE TIMING (CKE = 1)



31.0 DC AND AC CHARACTERISTICS GRAPHS AND CHARTS

The graphs and tables provided in this section are for **design guidance** and are **not tested**.

In some graphs or tables, the data presented are **outside specified operating range** (i.e., outside specified V_{DD} range). This is for **information only** and devices are ensured to operate properly only within the specified range.

<p>Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.</p>
--

“Typical” represents the mean of the distribution at 25°C. “MAXIMUM”, “Max.”, “MINIMUM” or “Min.” represents (mean + 3σ) or (mean - 3σ) respectively, where σ is a standard deviation, over each temperature range.

FIGURE 31-7: I_{DD} TYPICAL, EC OSCILLATOR, MEDIUM-POWER MODE, PIC16LF1824/8 ONLY

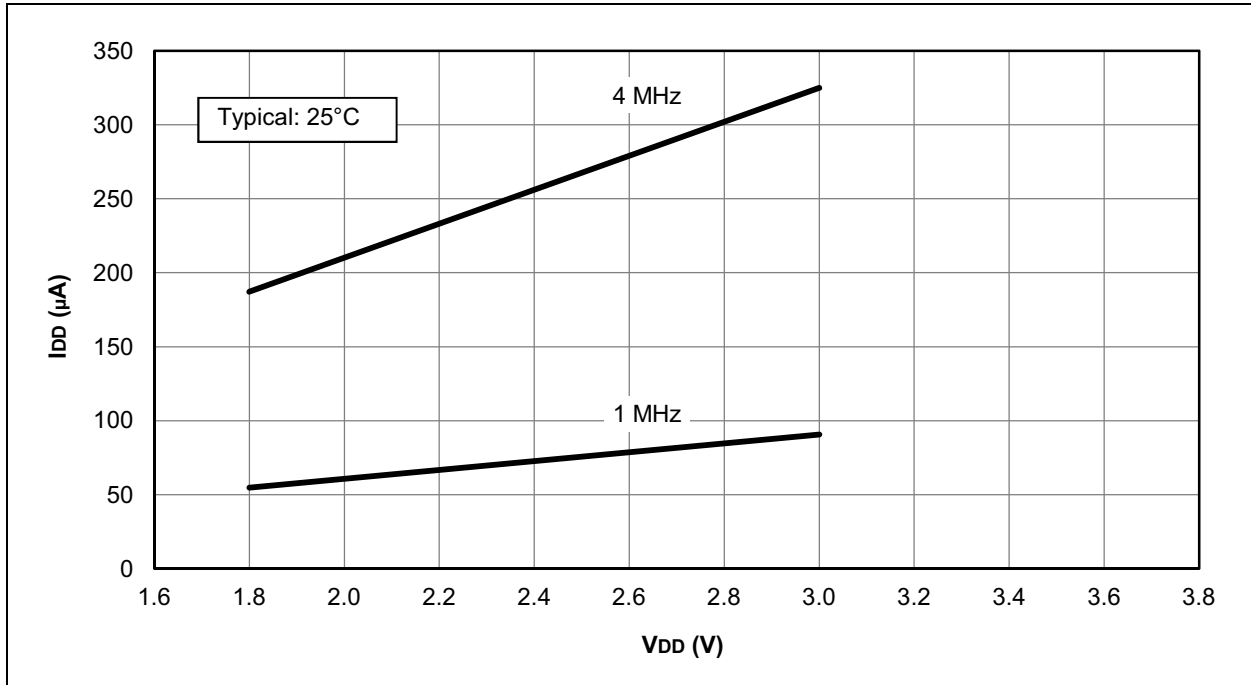
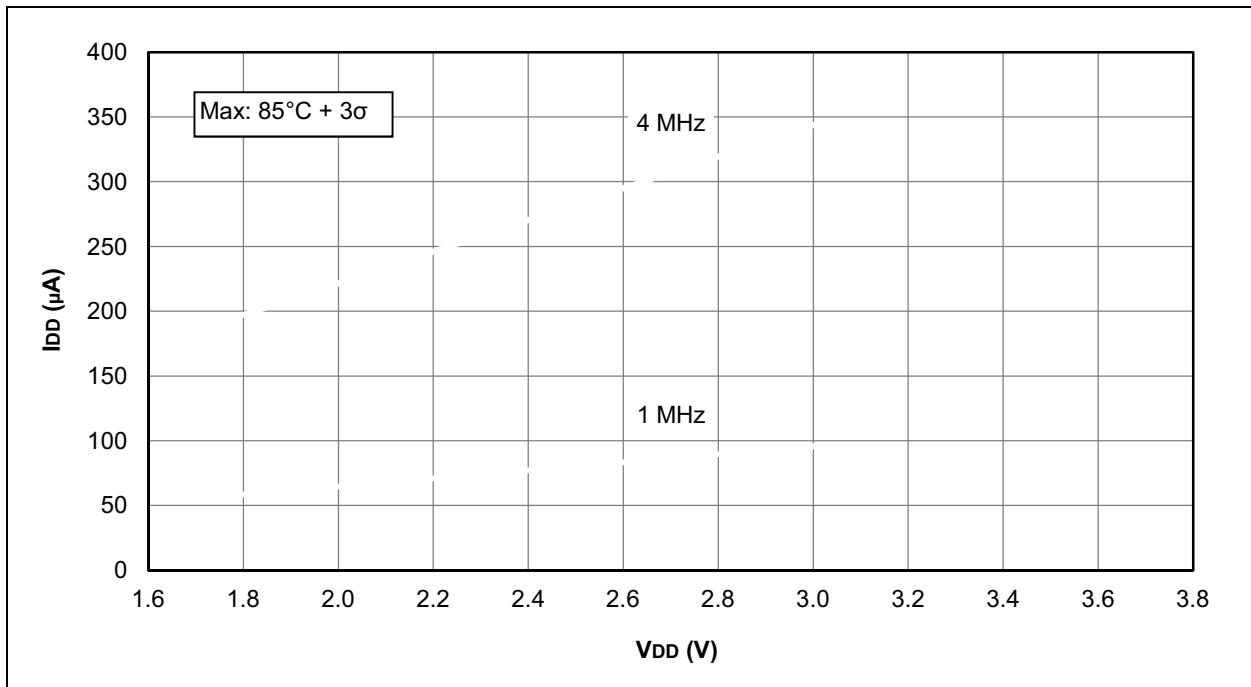


FIGURE 31-8: I_{DD} MAXIMUM, EC OSCILLATOR, MEDIUM-POWER MODE, PIC16LF1824/8 ONLY



PIC16(L)F1824/8

FIGURE 31-45: V_{OH} vs. I_{OH} OVER TEMPERATURE ($V_{DD} = 1.8V$)

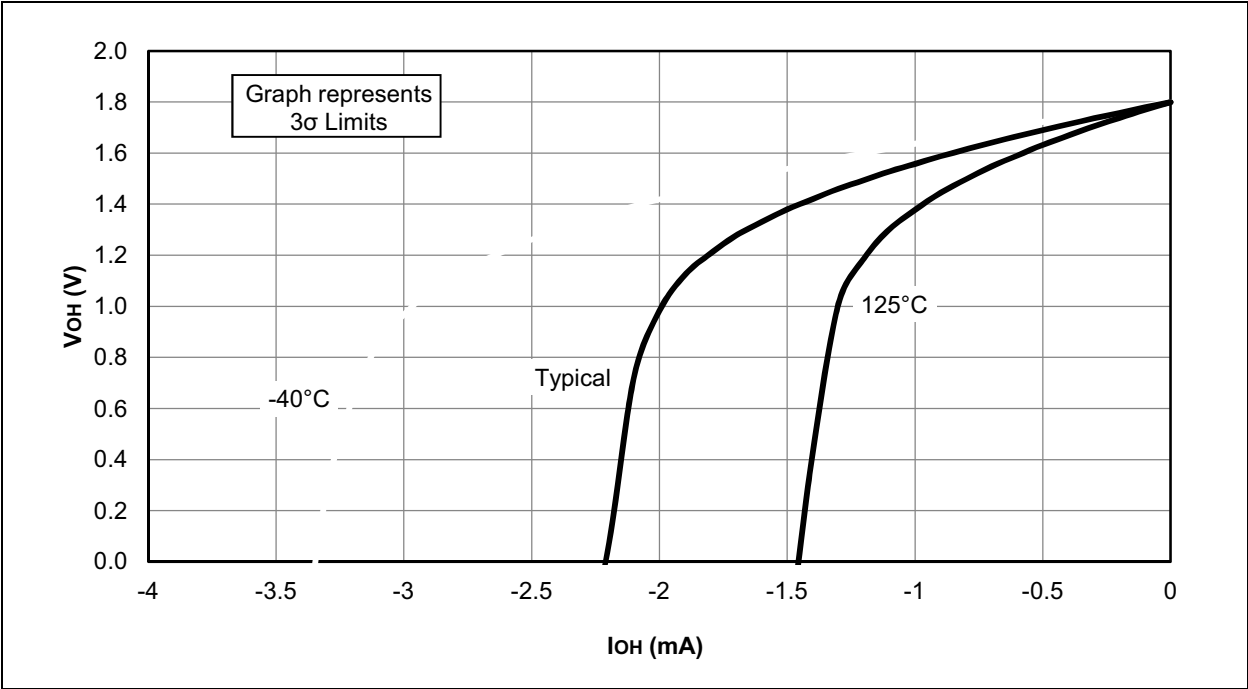


FIGURE 31-46: V_{OL} vs. I_{OL} OVER TEMPERATURE ($V_{DD} = 1.8V$)

