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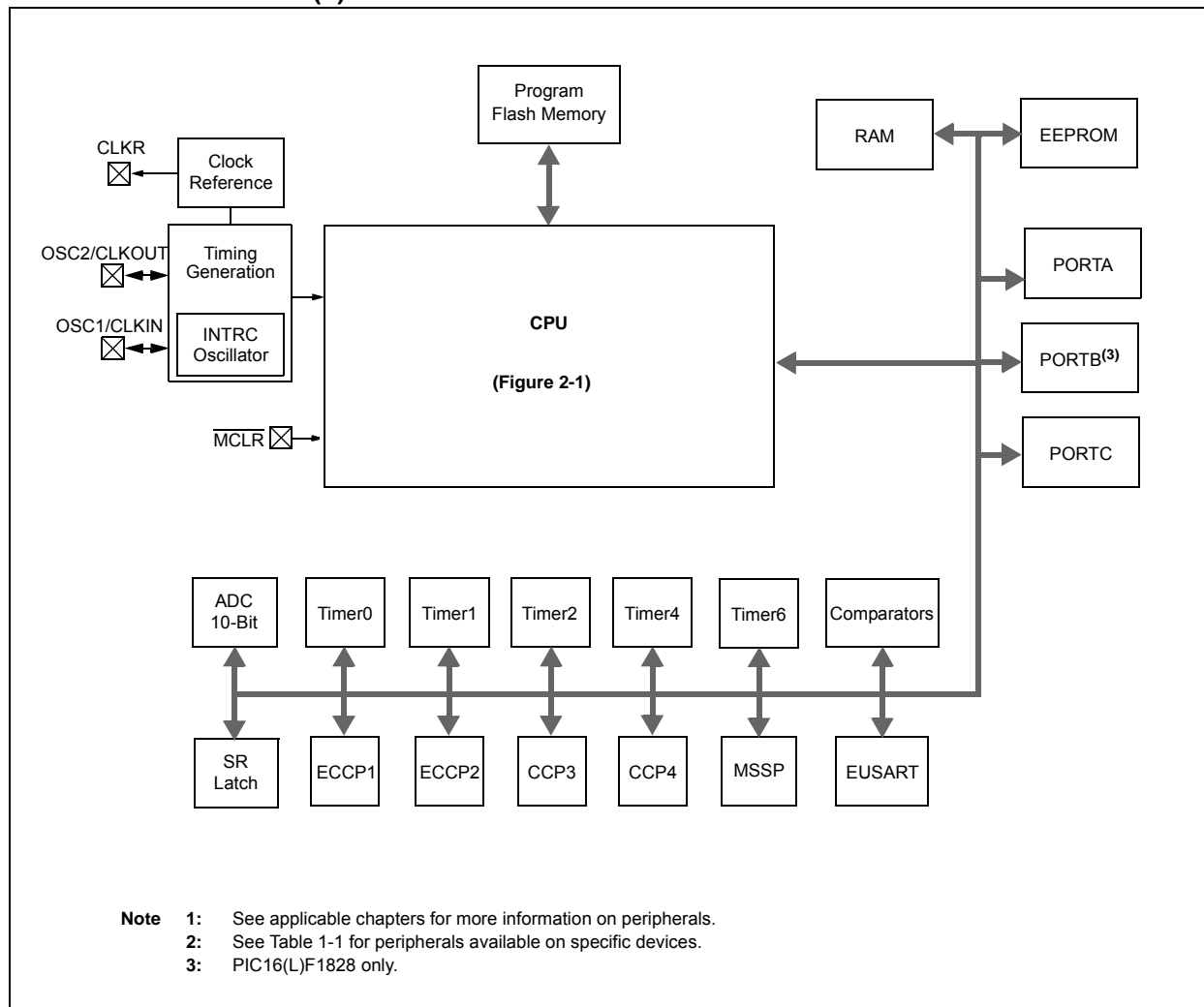
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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	17
Program Memory Size	7KB (4K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-VQFN Exposed Pad
Supplier Device Package	20-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf1828-i-ml

PIC16(L)F1824/8

FIGURE 1-1: PIC16(L)F1824/8 BLOCK DIAGRAM



3.2.2 SPECIAL FUNCTION REGISTER

The Special Function Registers are registers used by the application to control the desired operation of peripheral functions in the device. The Special Function Registers occupy the 20 bytes after the core registers of every data memory bank (addresses x0Ch/x8Ch through x1Fh/x9Fh). The registers associated with the operation of the peripherals are described in the appropriate peripheral chapter of this data sheet.

3.2.3 GENERAL PURPOSE RAM

There are up to 80 bytes of GPR in each data memory bank. The Special Function Registers occupy the 20 bytes after the core registers of every data memory bank (addresses x0Ch/x8Ch through x1Fh/x9Fh).

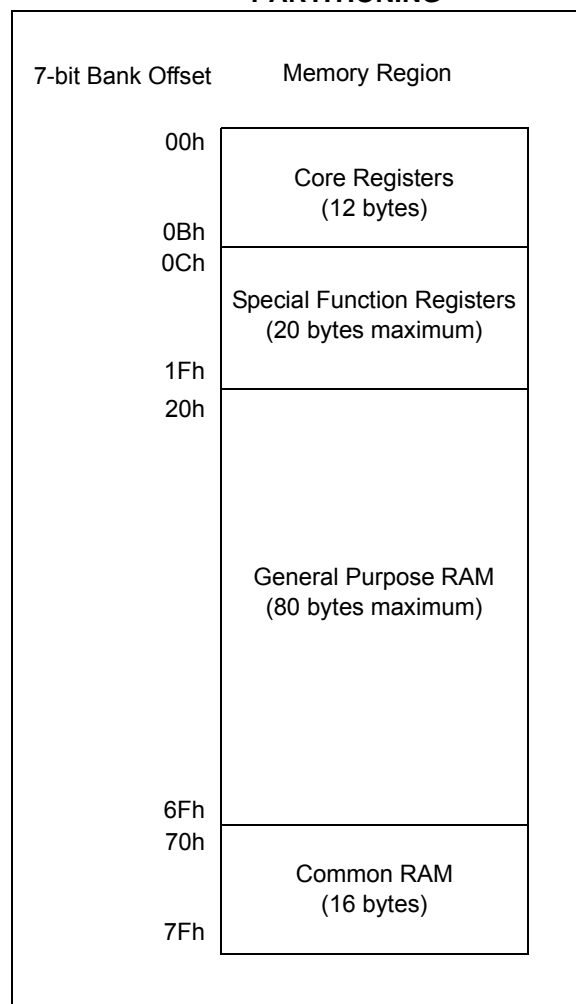
3.2.3.1 Linear Access to GPR

The general purpose RAM can be accessed in a non-banked method via the FSRs. This can simplify access to large memory structures. See **Section 3.5.2 “Linear Data Memory”** for more information.

3.2.4 COMMON RAM

There are 16 bytes of common RAM accessible from all banks.

FIGURE 3-2: BANKED MEMORY PARTITIONING



3.2.5 DEVICE MEMORY MAPS

The memory maps for the device family are as shown in Table 3-3.

TABLE 3-3: MEMORY MAP TABLES

Device	Banks	Table No.
PIC16(L)F1824	0-7	Table 3-4
PIC16(L)F1828	8-15	Table 3-5
	16-23	Table 3-6
	24-31	Table 3-7
	31	Table 3-8

PIC16(L)F1824/8

TABLE 3-9: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets		
Bank 5													
280h ⁽¹⁾	INDF0	Addressing this location uses contents of FSR0H/FSR0L to address data memory (not a physical register)								xxxx xxxx	xxxx xxxx		
281h ⁽¹⁾	INDF1	Addressing this location uses contents of FSR1H/FSR1L to address data memory (not a physical register)								xxxx xxxx	xxxx xxxx		
282h ⁽¹⁾	PCL	Program Counter (PC) Least Significant Byte								0000 0000	0000 0000		
283h ⁽¹⁾	STATUS	—	—	—	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C	---1 1000	---q quuu		
284h ⁽¹⁾	FSR0L	Indirect Data Memory Address 0 Low Pointer								0000 0000	uuuu uuuu		
285h ⁽¹⁾	FSR0H	Indirect Data Memory Address 0 High Pointer								0000 0000	0000 0000		
286h ⁽¹⁾	FSR1L	Indirect Data Memory Address 1 Low Pointer								0000 0000	uuuu uuuu		
287h ⁽¹⁾	FSR1H	Indirect Data Memory Address 1 High Pointer								0000 0000	0000 0000		
288h ⁽¹⁾	BSR	—	—	—	BSR<4:0>					---0 0000	---0 0000		
289h ⁽¹⁾	WREG	Working Register								0000 0000	uuuu uuuu		
28Ah ⁽¹⁾	PCLATH	—	Write Buffer for the upper 7 bits of the Program Counter								-000 0000	-000 0000	
28Bh ⁽¹⁾	INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCF	0000 000x	0000 000u		
28Ch	—	Unimplemented								—	—		
28Dh	—	Unimplemented								—	—		
28Eh	—	Unimplemented								—	—		
28Fh	—	Unimplemented								—	—		
290h	—	Unimplemented								—	—		
291h	CCPR1L	Capture/Compare/PWM Register 1 (LSB)								xxxx xxxx	uuuu uuuu		
292h	CCPR1H	Capture/Compare/PWM Register 1 (MSB)								xxxx xxxx	uuuu uuuu		
293h	CCP1CON	P1M<1:0>		DC1B<1:0>		CCP1M<3:0>				0000 0000	0000 0000		
294h	PWM1CON	P1RSEN	P1DC<6:0>									0000 0000	0000 0000
295h	CCP1AS	CCP1ASE	CCP1AS<2:0>			PSS1AC<1:0>		PSS1BD<1:0>		0000 0000	0000 0000		
296h	PSTR1CON	—	—	—	STR1SYNC	STR1D	STR1C	STR1B	STR1A	---0 0001	---0 0001		
297h	—	Unimplemented								—	—		
298h	CCPR2L	Capture/Compare/PWM Register 2 (LSB)								xxxx xxxx	uuuu uuuu		
299h	CCPR2H	Capture/Compare/PWM Register 2 (MSB)								xxxx xxxx	uuuu uuuu		
29Ah	CCP2CON	P2M<1:0>		DC2B<1:0>		CCP2M<3:0>				0000 0000	0000 0000		
29Bh	PWM2CON	P2RSEN	P2DC<6:0>									0000 0000	0000 0000
29Ch	CCP2AS	CCP2ASE	CCP2AS<2:0>			PSS2AC<1:0>		PSS2BD<1:0>		0000 0000	0000 0000		
29Dh	PSTR2CON	—	—	—	STR2SYNC	STR2D	STR2C	STR2B	STR2A	---0 0001	---0 0001		
29Eh	CCPTMRS0	C4TSEL<1:0>		C3TSEL<1:0>		C2TSEL<1:0>		C1TSEL<1:0>		0000 0000	0000 0000		
29Fh	—	Unimplemented								—	—		

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, r = reserved.
Shaded locations are unimplemented, read as '0'.

- Note**
- 1: These registers can be addressed from any bank.
 - 2: PIC16(L)F1828 only.
 - 3: PIC16(L)F1824 only.
 - 4: Unimplemented, read as '1'.

PIC16(L)F1824/8

5.4 Two-Speed Clock Start-up Mode

Two-Speed Start-up mode provides additional power savings by minimizing the latency between external oscillator start-up and code execution. In applications that make heavy use of the Sleep mode, Two-Speed Start-up will remove the external oscillator start-up time from the time spent awake and can reduce the overall power consumption of the device. This mode allows the application to wake-up from Sleep, perform a few instructions using the INTOSC internal oscillator block as the clock source and go back to Sleep without waiting for the external oscillator to become stable.

Two-Speed Start-up provides benefits when the oscillator module is configured for LP, XT, or HS modes. The Oscillator Start-up Timer (OST) is enabled for these modes and must count 1024 oscillations before the oscillator can be used as the system clock source.

If the oscillator module is configured for any mode other than LP, XT or HS mode, then Two-Speed Start-up is disabled. This is because the external clock oscillator does not require any stabilization time after POR or an exit from Sleep.

If the OST count reaches 1024 before the device enters Sleep mode, the OSTS bit of the OSCSTAT register is set and program execution switches to the external oscillator. However, the system may never operate from the external oscillator if the time spent awake is very short.

Note: Executing a `SLEEP` instruction will abort the oscillator start-up time and will cause the OSTS bit of the OSCSTAT register to remain clear.

5.4.1 TWO-SPEED START-UP MODE CONFIGURATION

Two-Speed Start-up mode is configured by the following settings:

- IESO (of the Configuration Word 1) = 1; Internal/External Switchover bit (Two-Speed Start-up mode enabled).
- SCS (of the OSCCON register) = 00.
- FOSC<2:0> bits in the Configuration Word 1 configured for LP, XT or HS mode.

Two-Speed Start-up mode is entered after:

- Power-on Reset (POR) and, if enabled, after Power-up Timer (PWRT) has expired, or
- Wake-up from Sleep.

Note: When FSCM is enabled, Two-Speed Start-up will automatically be enabled.

TABLE 5-1: OSCILLATOR SWITCHING DELAYS

Switch From	Switch To	Frequency	Oscillator Delay
Sleep/POR	LFINTOSC ⁽¹⁾ MFINTOSC ⁽¹⁾ HFINTOSC ⁽¹⁾	31 kHz 31.25 kHz-500 kHz 31.25 kHz-16 MHz	Oscillator Warm-up Delay (TWARM)
Sleep/POR	EC, RC ⁽¹⁾	DC – 32 MHz	2 cycles
LFINTOSC	EC, RC ⁽¹⁾	DC – 32 MHz	1 cycle of each
Sleep/POR	Timer1 Oscillator LP, XT, HS ⁽¹⁾	32 kHz-20 MHz	1024 Clock Cycles (OST)
Any clock source	MFINTOSC ⁽¹⁾ HFINTOSC ⁽¹⁾	31.25 kHz-500 kHz 31.25 kHz-16 MHz	2 μ s (approx.)
Any clock source	LFINTOSC ⁽¹⁾	31 kHz	1 cycle of each
Any clock source	Timer1 Oscillator	32 kHz	1024 Clock Cycles (OST)
PLL inactive	PLL active	16-32 MHz	2 ms (approx.)

Note 1: PLL inactive.

REGISTER 10-1: WDTCON: WATCHDOG TIMER CONTROL REGISTER

U-0	U-0	R/W-0/0	R/W-1/1	R/W-0/0	R/W-1/1	R/W-1/1	R/W-0/0
—	—	WDTPS4	WDTPS3	WDTPS2	WDTPS1	WDTPS0	SWDTEN
bit 7							bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-m/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-6 **Unimplemented:** Read as '0'

bit 5-1 **WDTPS<4:0>:** Watchdog Timer Period Select bits

Bit Value = Prescale Rate

00000	= 1:32 (Interval 1 ms typ)
00001	= 1:64 (Interval 2 ms typ)
00010	= 1:128 (Interval 4 ms typ)
00011	= 1:256 (Interval 8 ms typ)
00100	= 1:512 (Interval 16 ms typ)
00101	= 1:1024 (Interval 32 ms typ)
00110	= 1:2048 (Interval 64 ms typ)
00111	= 1:4096 (Interval 128 ms typ)
01000	= 1:8192 (Interval 256 ms typ)
01001	= 1:16384 (Interval 512 ms typ)
01010	= 1:32768 (Interval 1s typ)
01011	= 1:65536 (Interval 2s typ) (Reset value)
01100	= 1:131072 (2^{17}) (Interval 4s typ)
01101	= 1:262144 (2^{18}) (Interval 8s typ)
01110	= 1:524288 (2^{19}) (Interval 16s typ)
01111	= 1:1048576 (2^{20}) (Interval 32s typ)
10000	= 1:2097152 (2^{21}) (Interval 64s typ)
10001	= 1:4194304 (2^{22}) (Interval 128s typ)
10010	= 1:8388608 (2^{23}) (Interval 256s typ)

10011 = Reserved. Results in minimum interval (1:32)

•
•
•

11111 = Reserved. Results in minimum interval (1:32)

bit 0 **SWDTEN:** Software Enable/Disable for Watchdog Timer bit

If WDTE<1:0> = 00:

This bit is ignored.

If WDTE<1:0> = 01:

1 = WDT is turned on

0 = WDT is turned off

If WDTE<1:0> = 1x:

This bit is ignored.

TABLE 12-3: SUMMARY OF REGISTERS ASSOCIATED WITH PORTB⁽¹⁾

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ANSELB	—	—	ANSB5	ANSB4	—	—	—	—	128
INLVLB	INLVLB7	INLVLB6	INLVLB5	INLVLB4	—	—	—	—	128
LATB	LATB7	LATB6	LATB5	LATB4	—	—	—	—	127
PORTB	RB7	RB6	RB5	RB4	—	—	—	—	127
TRISB	TRISB7	TRISB6	TRISB5	TRISB4	—	—	—	—	127
WPUB	WPUB7	WPUB6	WPUB5	WPUB4	—	—	—	—	128

Legend: x = unknown, u = unchanged, - = unimplemented locations, read as '0'. Shaded cells are not used by PORTB.

Note 1: PIC16(L)F1828 only.

PIC16(L)F1824/8

REGISTER 12-20: INLVLC: PORTC INPUT LEVEL CONTROL REGISTER

U-0 ⁽³⁾ R/W-1/1 ⁽²⁾	U-0 ⁽³⁾ R/W-1/1 ⁽²⁾	R/W-0/0 ⁽³⁾ R/W-1/1 ⁽²⁾	R/W-0/0 ⁽³⁾ R/W-1/1 ⁽²⁾	R/W-0/0 ⁽³⁾ R/W-1/1 ⁽²⁾	R/W-0/0 ⁽³⁾ R/W-1/1 ⁽²⁾	R/W-0/0 ⁽³⁾ R/W-1/1 ⁽²⁾	R/W-0/0 ⁽³⁾ R/W-1/1 ⁽²⁾
INLVLC7 ⁽¹⁾	INLVLC6 ⁽¹⁾	INLVLC5	INLVLC4	INLVLC3	INLVLC2	INLVLC1	INLVLC0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
u = Bit is unchanged x = Bit is unknown -n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set '0' = Bit is cleared

bit 7-0 **INLVLC<7:0>**: PORTC Input Level Select bits⁽¹⁾
For RC<7:0> pins, respectively
1 = ST input used for PORT reads and Interrupt-on-Change
0 = TTL input used for PORT reads and Interrupt-on-Change

- Note 1:** INLVLC<7:6> available on PIC16(L)F1828 only. Otherwise, they are unimplemented and read as '0'.
2: PIC16(L)F1828 only, Reset default value.
3: PIC16(L)F1824 only, Reset default value.

TABLE 12-4: SUMMARY OF REGISTERS ASSOCIATED WITH PORTC

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ANSEL	ANSC7 ⁽¹⁾	ANSC6 ⁽¹⁾	—	—	ANSC3	ANSC2	ANSC1	ANSC0	133
INLVLC	INLVLC7 ⁽¹⁾	INLVLC6 ⁽¹⁾	INLVLC5	INLVLC4	INLVLC3	INLVLC2	INLVLC1	INLVLC0	134
LATC	LATC7 ⁽¹⁾	LATC6 ⁽¹⁾	LATC5	LATC4	LATC3	LATC2	LATC1	LATC0	132
PORTC	RC7 ⁽¹⁾	RC6 ⁽¹⁾	RC5	RC4	RC3	RC2	RC1	RC0	132
TRISC	TRISC7 ⁽¹⁾	TRISC6 ⁽¹⁾	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	132
WPUC	WPUC7 ⁽¹⁾	WPUC6 ⁽¹⁾	WPUC5	WPUC4	WPUC3	WPUC2	WPUC1	WPUC0	133

Legend: x = unknown, u = unchanged, - = unimplemented locations, read as '0'. Shaded cells are not used by PORTC.

Note 1: PIC16(L)F1828 only.

16.2.7 ADC REGISTER DEFINITIONS

The following registers are used to control the operation of the ADC.

REGISTER 16-1: ADCON0: A/D CONTROL REGISTER 0

U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	CHS<4:0>					GO/DONE	ADON
bit 7							bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **Unimplemented:** Read as '0'

bit 6-2 **CHS<4:0>:** Analog Channel Select bits

00000 = AN0
 00001 = AN1
 00010 = AN2
 00011 = AN3
 00100 = AN4
 00101 = AN5
 00110 = AN6
 00111 = AN7
 01000 = AN8⁽³⁾
 01001 = AN9⁽³⁾
 01010 = AN10⁽³⁾
 01011 = AN11⁽³⁾
 01100 = Reserved. No channel connected
 .
 .
 .
 11100 = Reserved. No channel connected
 11101 = Temperature Indicator
 11110 = DAC_output⁽¹⁾
 11111 = FVR (Fixed Voltage Reference) Buffer 1 Output⁽²⁾

bit 1 **GO/DONE:** A/D Conversion Status bit

1 = A/D conversion cycle in progress. Setting this bit starts an A/D conversion cycle.
 This bit is automatically cleared by hardware when the A/D conversion has completed.
 0 = A/D conversion completed/not in progress

bit 0 **ADON:** ADC Enable bit

1 = ADC is enabled
 0 = ADC is disabled and consumes no operating current

Note 1: See **Section 17.0 “Digital-to-Analog Converter (DAC) Module”** for more information.

2: See **Section 14.0 “Fixed Voltage Reference (FVR)”** for more information.

3: PIC16(L)F1828 only.

TABLE 18-1: SRCLK FREQUENCY TABLE

SRCLK	Divider	Fosc = 32 MHz	Fosc = 20 MHz	Fosc = 16 MHz	Fosc = 4 MHz	Fosc = 1 MHz
111	512	62.5 kHz	39.0 kHz	31.3 kHz	7.81 kHz	1.95 kHz
110	256	125 kHz	78.1 kHz	62.5 kHz	15.6 kHz	3.90 kHz
101	128	250 kHz	156 kHz	125 kHz	31.25 kHz	7.81 kHz
100	64	500 kHz	313 kHz	250 kHz	62.5 kHz	15.6 kHz
011	32	1 MHz	625 kHz	500 kHz	125 kHz	31.3 kHz
010	16	2 MHz	1.25 MHz	1 MHz	250 kHz	62.5 kHz
001	8	4 MHz	2.5 MHz	2 MHz	500 kHz	125 kHz
000	4	8 MHz	5 MHz	4 MHz	1 MHz	250 kHz

REGISTER 18-1: SRCON0: SR LATCH CONTROL 0 REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/S-0/0	R/S-0/0
SRLEN	SRCLK<2:0>			SRQEN	SRNQEN	SRPS	SRPR
bit 7							bit 0

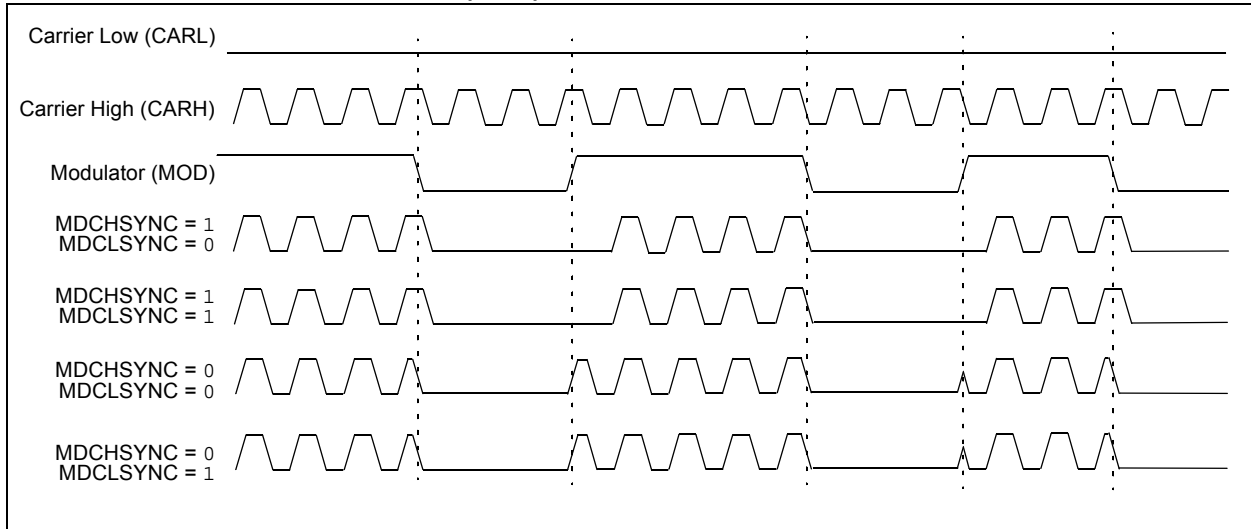
Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	S = Bit is set only

- bit 7 **SRLEN:** SR Latch Enable bit
1 = SR latch is enabled
0 = SR latch is disabled
- bit 6-4 **SRCLK<2:0>:** SR Latch Clock Divider bits
000 = Generates a 1 Fosc wide pulse every 4th Fosc cycle clock
001 = Generates a 1 Fosc wide pulse every 8th Fosc cycle clock
010 = Generates a 1 Fosc wide pulse every 16th Fosc cycle clock
011 = Generates a 1 Fosc wide pulse every 32nd Fosc cycle clock
100 = Generates a 1 Fosc wide pulse every 64th Fosc cycle clock
101 = Generates a 1 Fosc wide pulse every 128th Fosc cycle clock
110 = Generates a 1 Fosc wide pulse every 256th Fosc cycle clock
111 = Generates a 1 Fosc wide pulse every 512th Fosc cycle clock
- bit 3 **SRQEN:** SR Latch Q Output Enable bit
If SRLEN = 1:
1 = Q is present on the SRQ pin
0 = External Q output is disabled
If SRLEN = 0:
SR latch is disabled
- bit 2 **SRNQEN:** SR Latch \overline{Q} Output Enable bit
If SRLEN = 1:
1 = \overline{Q} is present on the SRnQ pin
0 = External \overline{Q} output is disabled
If SRLEN = 0:
SR latch is disabled
- bit 1 **SRPS:** Pulse Set Input of the SR Latch bit⁽¹⁾
1 = Pulse set input for 1 Q-clock period
0 = No effect on set input.
- bit 0 **SRPR:** Pulse Reset Input of the SR Latch bit⁽¹⁾
1 = Pulse reset input for 1 Q-clock period
0 = No effect on reset input.

Note 1: Set only, always reads back '0'.

FIGURE 23-2: ON OFF KEYING (OOK) SYNCHRONIZATION



EXAMPLE 23-1: NO SYNCHRONIZATION (MDSHSYNC = 0, MDCLSYNC = 0)

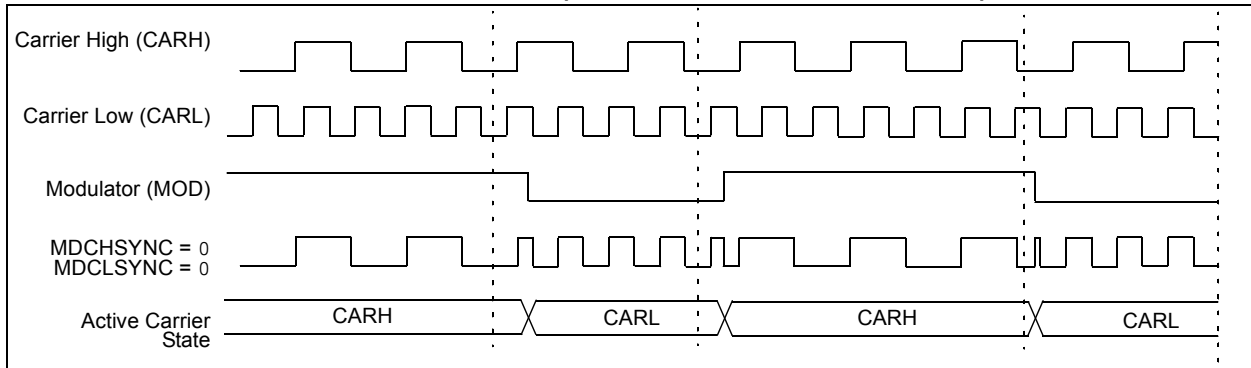
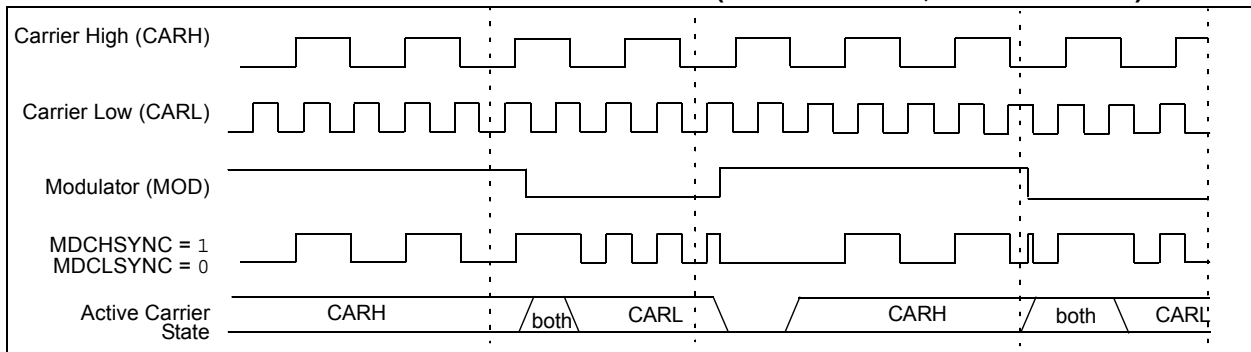


FIGURE 23-3: CARRIER HIGH SYNCHRONIZATION (MDSHSYNC = 1, MDCLSYNC = 0)



When one device is transmitting a logical one, or letting the line float, and a second device is transmitting a logical zero, or holding the line low, the first device can detect that the line is not a logical one. This detection, when used on the SCL line, is called clock stretching. Clock stretching gives slave devices a mechanism to control the flow of data. When this detection is used on the SDA line, it is called arbitration. Arbitration ensures that there is only one master device communicating at any single time.

25.3.1 CLOCK STRETCHING

When a slave device has not completed processing data, it can delay the transfer of more data through the process of Clock Stretching. An addressed slave device may hold the SCL clock line low after receiving or sending a bit, indicating that it is not yet ready to continue. The master that is communicating with the slave will attempt to raise the SCL line in order to transfer the next bit, but will detect that the clock line has not yet been released. Because the SCL connection is open-drain, the slave has the ability to hold that line low until it is ready to continue communicating.

Clock stretching allows receivers that cannot keep up with a transmitter to control the flow of incoming data.

25.3.2 ARBITRATION

Each master device must monitor the bus for Start and Stop bits. If the device detects that the bus is busy, it cannot begin a new message until the bus returns to an Idle state.

However, two master devices may try to initiate a transmission on or about the same time. When this occurs, the process of arbitration begins. Each transmitter checks the level of the SDA data line and compares it to the level that it expects to find. The first transmitter to observe that the two levels don't match, loses arbitration, and must stop transmitting on the SDA line.

For example, if one transmitter holds the SDA line to a logical one (lets it float) and a second transmitter holds it to a logical zero (pulls it low), the result is that the SDA line will be low. The first transmitter then observes that the level of the line is different than expected and concludes that another transmitter is communicating.

The first transmitter to notice this difference is the one that loses arbitration and must stop driving the SDA line. If this transmitter is also a master device, it also must stop driving the SCL line. It then can monitor the lines for a Stop condition before trying to reissue its transmission. In the meantime, the other device that has not noticed any difference between the expected and actual levels on the SDA line continues with its original transmission. It can do so without any complications, because so far, the transmission appears exactly as expected with no other transmitter disturbing the message.

Slave Transmit mode can also be arbitrated, when a master addresses multiple slaves, but this is less common.

If two master devices are sending a message to two different slave devices at the address stage, the master sending the lower slave address always wins arbitration. When two master devices send messages to the same slave address, and addresses can sometimes refer to multiple slaves, the arbitration process must continue into the data stage.

Arbitration usually occurs very rarely, but it is a necessary process for proper multi-master support.

25.4 I²C Mode Operation

All MSSP1 I²C communication is byte oriented and shifted out MSb first. Six SFR registers and 2 interrupt flags interface the module with the PIC[®] microcontroller and user software. Two pins, SDA and SCL, are exercised by the module to communicate with other external I²C devices.

25.4.1 BYTE FORMAT

All communication in I²C is done in 9-bit segments. A byte is sent from a Master to a Slave or vice-versa, followed by an Acknowledge bit sent back. After the 8th falling edge of the SCL line, the device outputting data on the SDA changes that pin to an input and reads in an acknowledge value on the next clock pulse.

The clock signal, SCL, is provided by the master. Data is valid to change while the SCL signal is low, and sampled on the rising edge of the clock. Changes on the SDA line while the SCL line is high define special conditions on the bus, explained below.

25.4.2 DEFINITION OF I²C TERMINOLOGY

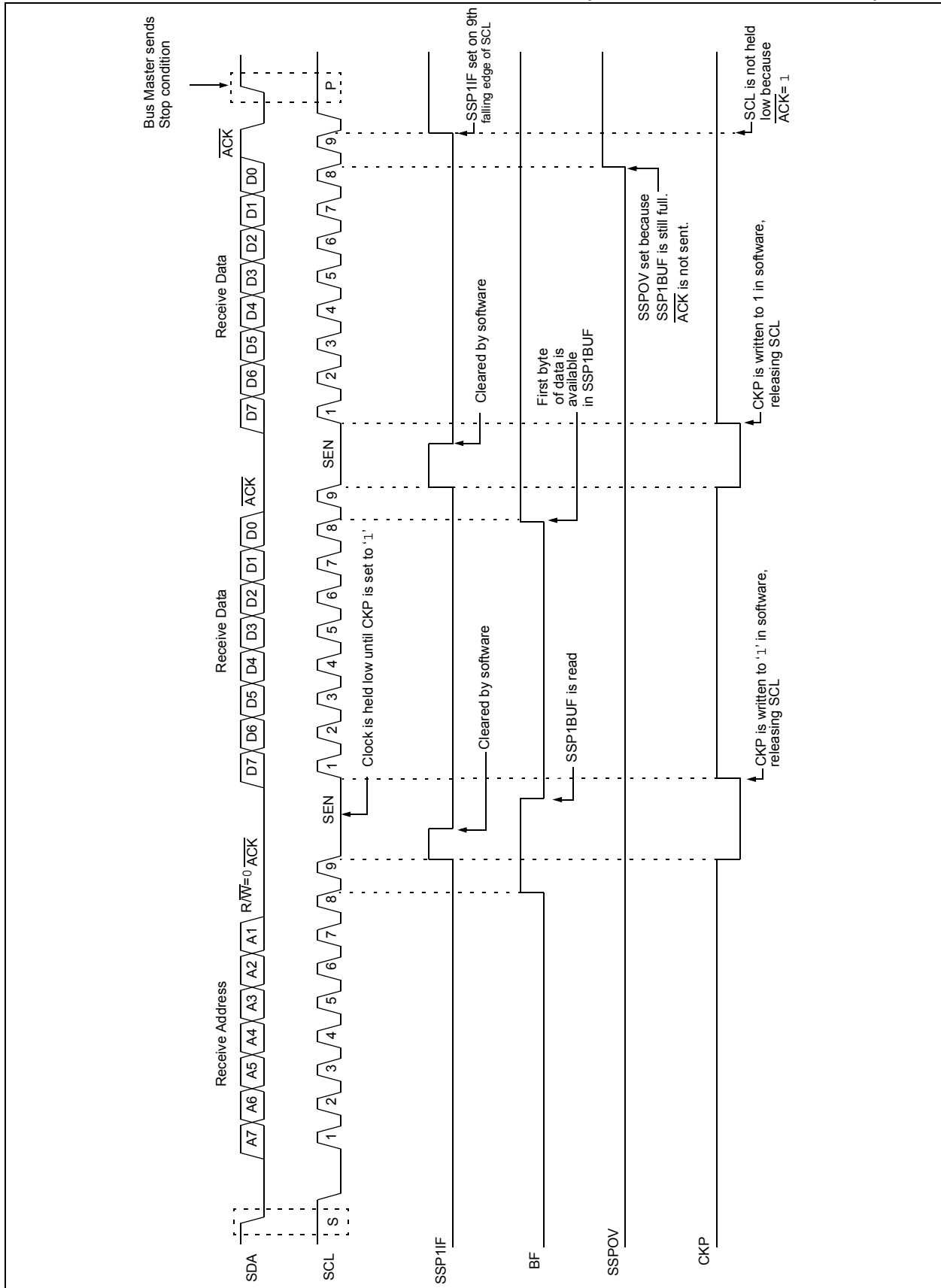
There is language and terminology in the description of I²C communication that have definitions specific to I²C. That word usage is defined below and may be used in the rest of this document without explanation. This table was adapted from the Phillips I²C specification.

25.4.3 SDA AND SCL PINS

Selection of any I²C mode with the SSP1EN bit set, forces the SCL and SDA pins to be open-drain. These pins should be set by the user to inputs by setting the appropriate TRIS bits.

Note: Data is tied to output zero when an I²C mode is enabled.

FIGURE 25-15: I²C SLAVE, 7-BIT ADDRESS, RECEPTION (SEN = 1, AHEN = 0, DHEN = 0)



26.3.4 BREAK CHARACTER SEQUENCE

The EUSART module has the capability of sending the special Break character sequences that are required by the LIN bus standard. A Break character consists of a Start bit, followed by 12 '0' bits and a Stop bit.

To send a Break character, set the SENDB and TXEN bits of the TXSTA register. The Break character transmission is then initiated by a write to the TXREG. The value of data written to TXREG will be ignored and all '0's will be transmitted.

The SENDB bit is automatically reset by hardware after the corresponding Stop bit is sent. This allows the user to preload the transmit FIFO with the next transmit byte following the Break character (typically, the Sync character in the LIN specification).

The TRMT bit of the TXSTA register indicates when the transmit operation is active or Idle, just as it does during normal transmission. See Figure 26-9 for the timing of the Break character sequence.

26.3.4.1 Break and Sync Transmit Sequence

The following sequence will start a message frame header made up of a Break, followed by an auto-baud Sync byte. This sequence is typical of a LIN bus master.

1. Configure the EUSART for the desired mode.
2. Set the TXEN and SENDB bits to enable the Break sequence.
3. Load the TXREG with a dummy character to initiate transmission (the value is ignored).
4. Write '55h' to TXREG to load the Sync character into the transmit FIFO buffer.
5. After the Break has been sent, the SENDB bit is reset by hardware and the Sync character is then transmitted.

When the TXREG becomes empty, as indicated by the TXIF, the next data byte can be written to TXREG.

26.3.5 RECEIVING A BREAK CHARACTER

The Enhanced EUSART module can receive a Break character in two ways.

The first method to detect a Break character uses the FERR bit of the RCSTA register and the Received data as indicated by RCREG. The Baud Rate Generator is assumed to have been initialized to the expected baud rate.

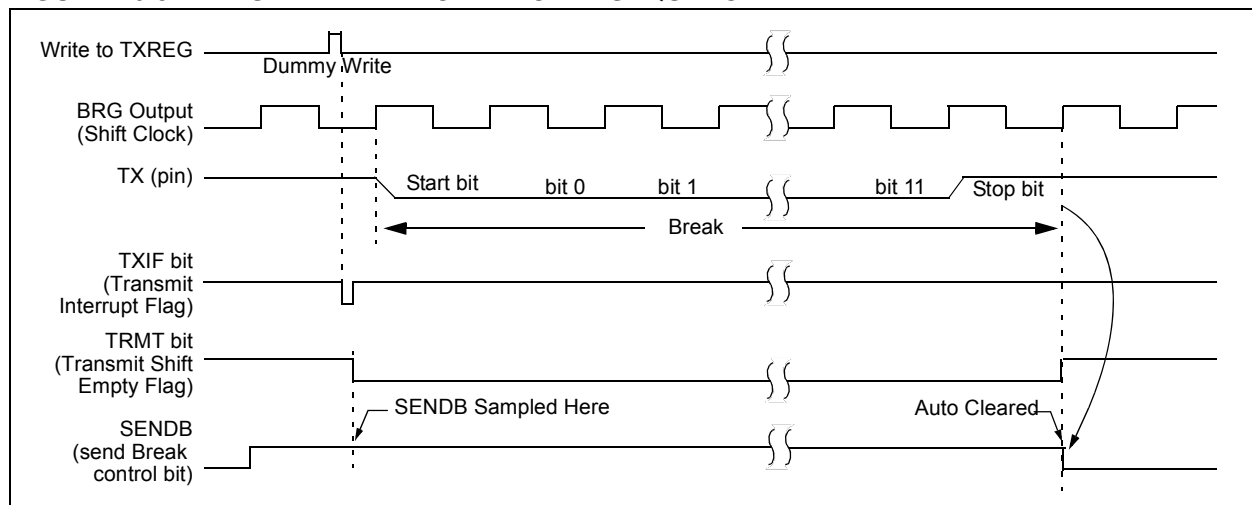
A Break character has been received when;

- RCIF bit is set
- FERR bit is set
- RCREG = 00h

The second method uses the Auto-Wake-up feature described in **Section 26.3.3 "Auto-Wake-up on Break"**. By enabling this feature, the EUSART will sample the next two transitions on RX/DT, cause an RCIF interrupt, and receive the next data byte followed by another interrupt.

Note that following a Break character, the user will typically want to enable the Auto-Baud Detect feature. For both methods, the user can set the ABDEN bit of the BAUDCON register before placing the EUSART in Sleep mode.

FIGURE 26-9: SEND BREAK CHARACTER SEQUENCE



26.4.2.3 EUSART Synchronous Slave Reception

The operation of the Synchronous Master and Slave modes is identical (**Section 26.4.1.5 “Synchronous Master Reception”**), with the following exceptions:

- Sleep
- CREN bit is always set, therefore the receiver is never Idle
- SREN bit, which is a “don’t care” in Slave mode

A character may be received while in Sleep mode by setting the CREN bit prior to entering Sleep. Once the word is received, the RSR register will transfer the data to the RCREG register. If the RCIE enable bit is set, the interrupt generated will wake the device from Sleep and execute the next instruction. If the GIE bit is also set, the program will branch to the interrupt vector.

26.4.2.4 Synchronous Slave Reception Setup:

1. Set the SYNC and SPEN bits and clear the CSRC bit.
2. Clear the ANSEL bit for both the CK and DT pins (if applicable).
3. If interrupts are desired, set the RCIE bit of the PIE1 register and the GIE and PEIE bits of the INTCON register.
4. If 9-bit reception is desired, set the RX9 bit.
5. Set the CREN bit to enable reception.
6. The RCIF bit will be set when reception is complete. An interrupt will be generated if the RCIE bit was set.
7. If 9-bit mode is enabled, retrieve the Most Significant bit from the RX9D bit of the RCSTA register.
8. Retrieve the eight Least Significant bits from the receive FIFO by reading the RCREG register.
9. If an overrun error occurs, clear the error by either clearing the CREN bit of the RCSTA register or by clearing the SPEN bit which resets the EUSART.

TABLE 26-10: SUMMARY OF REGISTERS ASSOCIATED WITH SYNCHRONOUS SLAVE RECEPTION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
APFCON0	RXDTSEL	SDOSEL ⁽¹⁾	SSSEL ⁽¹⁾	—	T1GSEL	TXCKSEL	—	—	117
BAUDCON	ABDOVF	RCIDL	—	SCKP	BRG16	—	WUE	ABDEN	296
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	89
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	90
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	93
RCREG	EUSART Receive Data Register								290*
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	295
TXSTA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	294

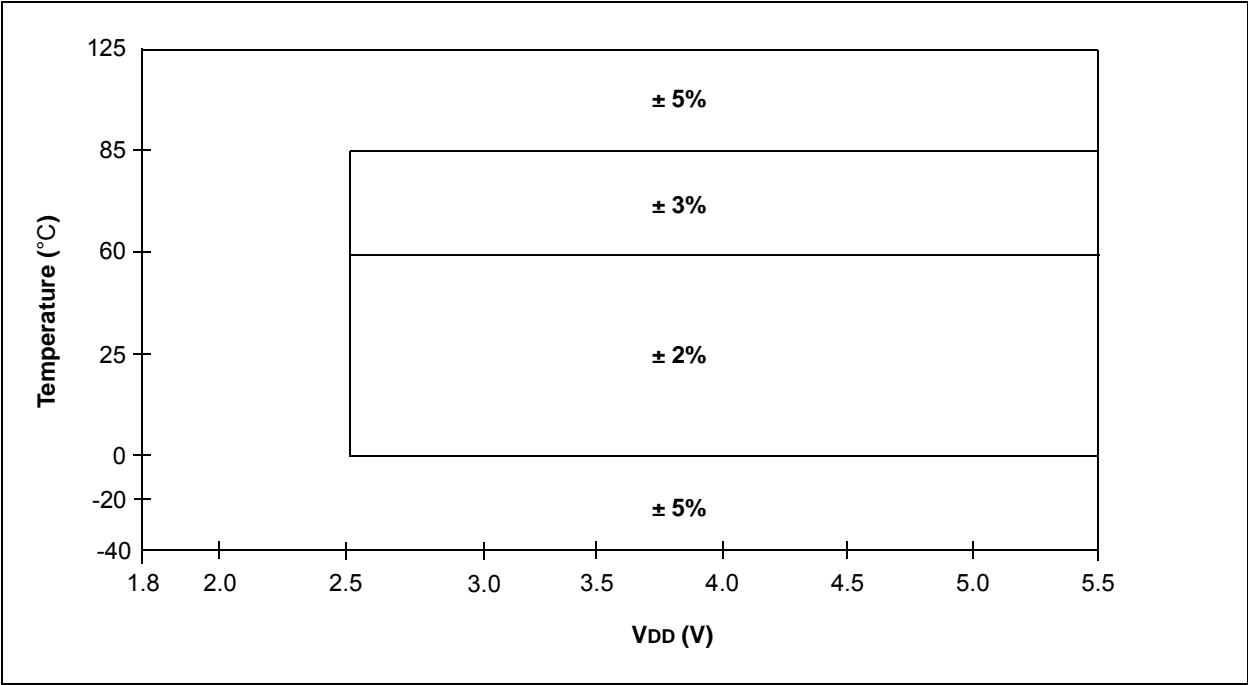
Legend: — = unimplemented location, read as ‘0’. Shaded cells are not used for synchronous slave reception.

* Page provides register information.

Note 1: PIC16(L)F1824 only.

PIC16(L)F1824/8

FIGURE 30-3: HFINTOSC FREQUENCY ACCURACY OVER DEVICE VDD AND TEMPERATURE



PIC16(L)F1824/8

30.3 DC Characteristics: PIC16(L)F1824/8-I/E (Power-Down)

PIC16LF1824/8			Standard Operating Conditions (unless otherwise stated)					
			Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended					
PIC16F1824/8			Standard Operating Conditions (unless otherwise stated)					
			Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended					
Param No.	Device Characteristics	Min.	Typ†	Max. +85°C	Max. +125°C	Units	Conditions	
							VDD	Note
D022	Power-down Base Current (IPD) ⁽²⁾							
		—	0.02	1.0	2.4	μA	1.8	WDT, BOR, FVR, and T1OSC disabled, all Peripherals Inactive
		—	0.03	1.5	3.0	μA	3.0	
D022		—	18	37	44	μA	1.8	WDT, BOR, FVR, and T1OSC disabled, all Peripherals Inactive
		—	20	42	48	μA	3.0	
		—	22	45	65	μA	5.0	
D023		—	0.2	2.0	3.0	μA	1.8	LPWDT Current (Note 1)
		—	0.5	2.0	4.0	μA	3.0	
D023		—	18	38	44	μA	1.8	LPWDT Current (Note 1)
		—	21	43	48	μA	3.0	
		—	22	46	65	μA	5.0	
D023A		—	12	22	25	μA	1.8	FVR current
		—	13	24	27	μA	3.0	
D023A		—	33	62	65	μA	1.8	FVR current
		—	40	72	75	μA	3.0	
		—	68	115	120	μA	5.0	
D024		—	7.0	14	16	μA	3.0	BOR Current (Note 1)
D024		—	24	47	50	μA	3.0	BOR Current (Note 1)
		—	29	55	70	μA	5.0	
D025		—	0.65	3.5	4.0	μA	1.8	T1OSC Current (Note 1)
		—	2.3	4.0	4.5	μA	3.0	
D025		—	19	39	45	μA	1.8	T1OSC Current (Note 1)
		—	21	43	59	μA	3.0	
		—	23	55	75	μA	5.0	
D026		—	0.03	1.5	3.0	μA	1.8	A/D Current (Note 1, 3), no conversion in progress
		—	0.04	2.0	3.5	μA	3.0	
D026		—	18	38	45	μA	1.8	A/D Current (Note 1, 3), no conversion in progress
		—	20	43	49	μA	3.0	
		—	22	46	65	μA	5.0	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

- Note 1:** The peripheral current is the sum of the base IDD or IPD and the additional current consumed when this peripheral is enabled. The peripheral Δ current can be determined by subtracting the base IDD or IPD current from this limit. Max values should be used when calculating total current consumption.
- Note 2:** The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD.
- Note 3:** A/D oscillator source is FRC.

TABLE 30-14: SPI MODE REQUIREMENTS

Param No.	Symbol	Characteristic	Min.	Typ†	Max.	Units	Conditions
SP70*	TssL2scH, TssL2scL	$\overline{SSx}\downarrow$ to SCKx \downarrow or SCKx \uparrow input	2.25 Tcy	—	—	ns	
SP71*	Tsch	SCKx input high time (Slave mode)	Tcy + 20	—	—	ns	
SP72*	TscL	SCKx input low time (Slave mode)	Tcy + 20	—	—	ns	
SP73*	TdIV2scH, TdIV2scL	Setup time of SDIx data input to SCKx edge	100	—	—	ns	
SP74*	Tsch2dIL, TscL2dIL	Hold time of SDIx data input to SCKx edge	100	—	—	ns	
SP75*	TdoR	SDO data output rise time	3.0-5.5V	—	10	25	ns
			1.8-5.5V	—	25	50	ns
SP76*	TdoF	SDOx data output fall time	—	10	25	ns	
SP77*	TssH2doZ	$\overline{SSx}\uparrow$ to SDOx output high-impedance	10	—	50	ns	
SP78*	Tscr	SCKx output rise time (Master mode)	3.0-5.5V	—	10	25	ns
			1.8-5.5V	—	25	50	ns
SP79*	TscF	SCKx output fall time (Master mode)	—	10	25	ns	
SP80*	Tsch2doV, TscL2doV	SDOx data output valid after SCKx edge	3.0-5.5V	—	—	50	ns
			1.8-5.5V	—	—	145	ns
SP81*	TdoV2scH, TdoV2scL	SDOx data output setup to SCKx edge	Tcy	—	—	ns	
SP82*	TssL2doV	SDOx data output valid after $\overline{SS}\downarrow$ edge	—	—	50	ns	
SP83*	Tsch2ssH, TscL2ssH	$\overline{SSx}\uparrow$ after SCKx edge	1.5Tcy + 40	—	—	ns	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 31-31: I_{PD}, CAPACITIVE SENSING (CPS) MODULE, LOW-CURRENT RANGE, CPSRM = 0, PIC16LF1824/8 ONLY

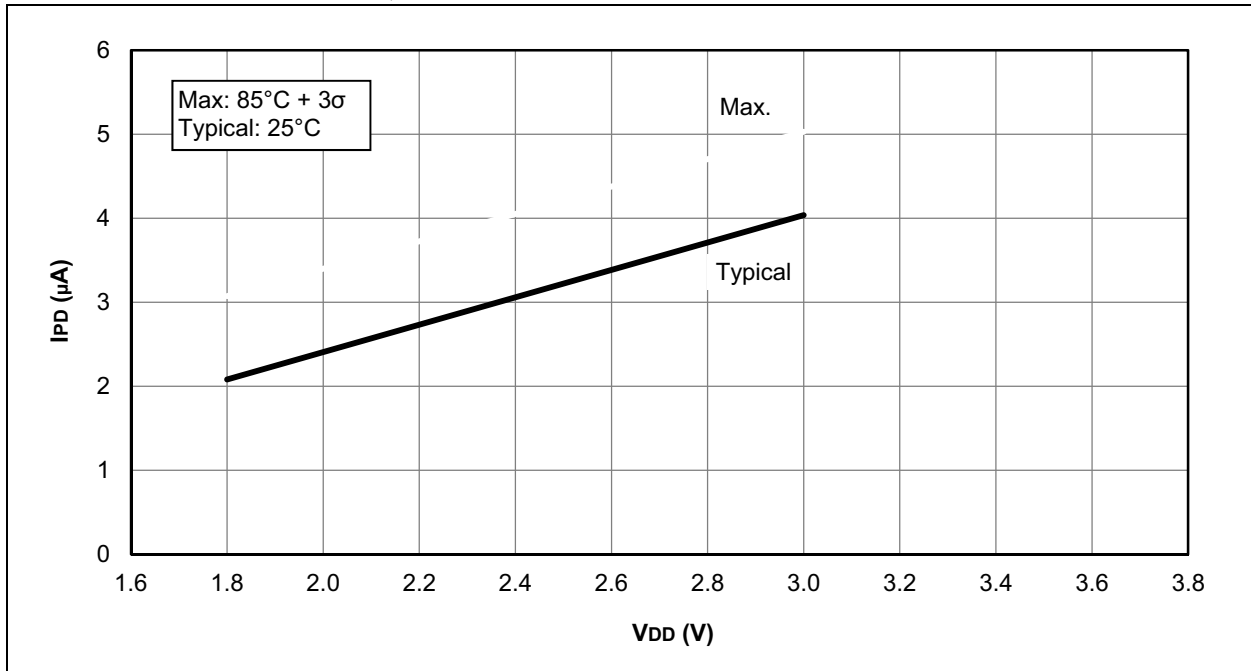
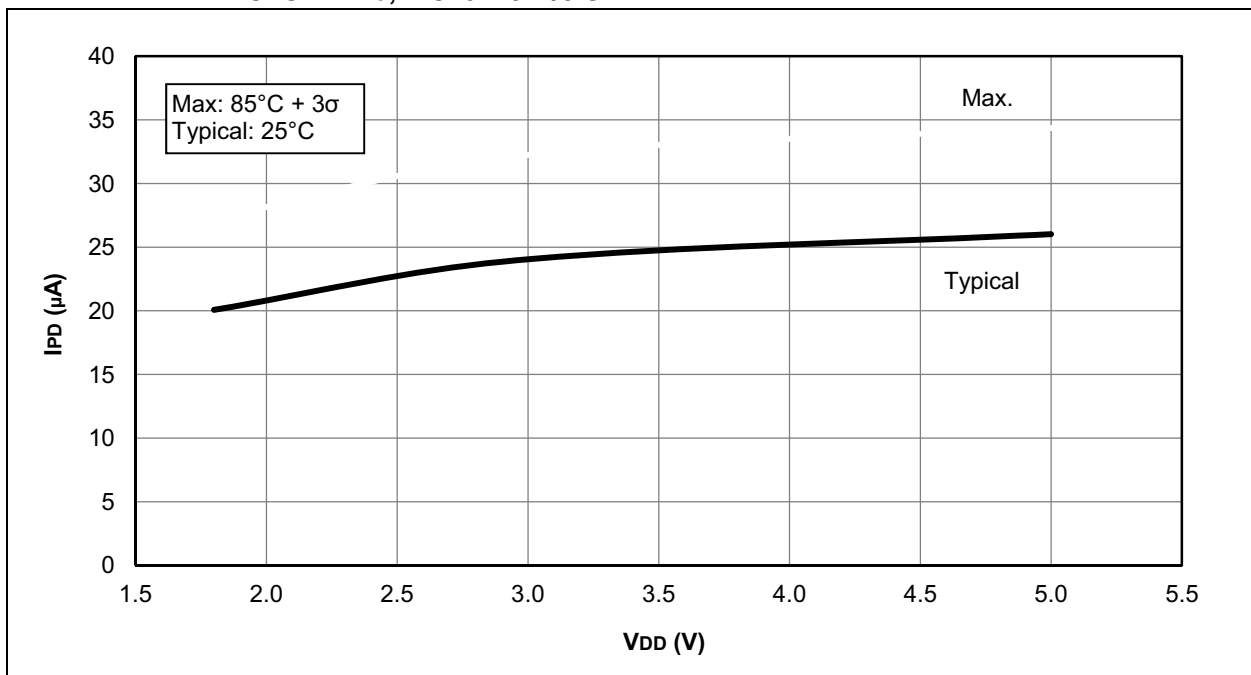


FIGURE 31-32: I_{PD}, CAPACITIVE SENSING (CPS) MODULE, LOW-CURRENT RANGE, CPSRM = 0, PIC16F1824/8 ONLY



PIC16(L)F1824/8

FIGURE 31-49: BROWN-OUT RESET VOLTAGE, BORV = 1

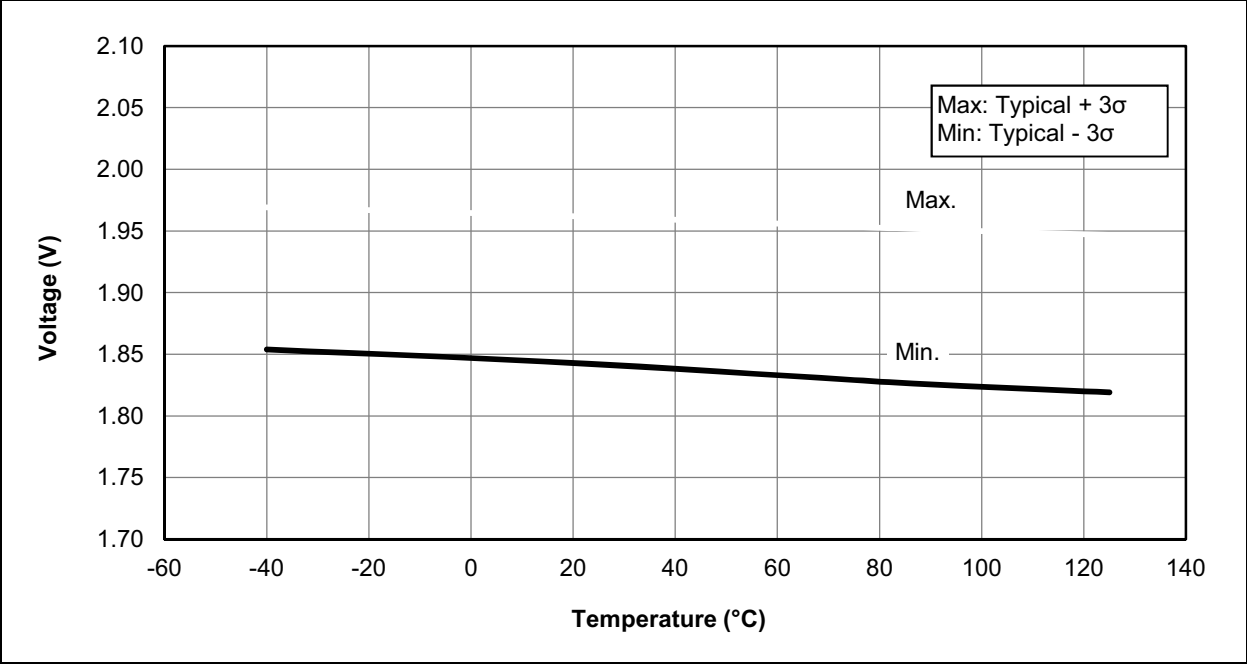
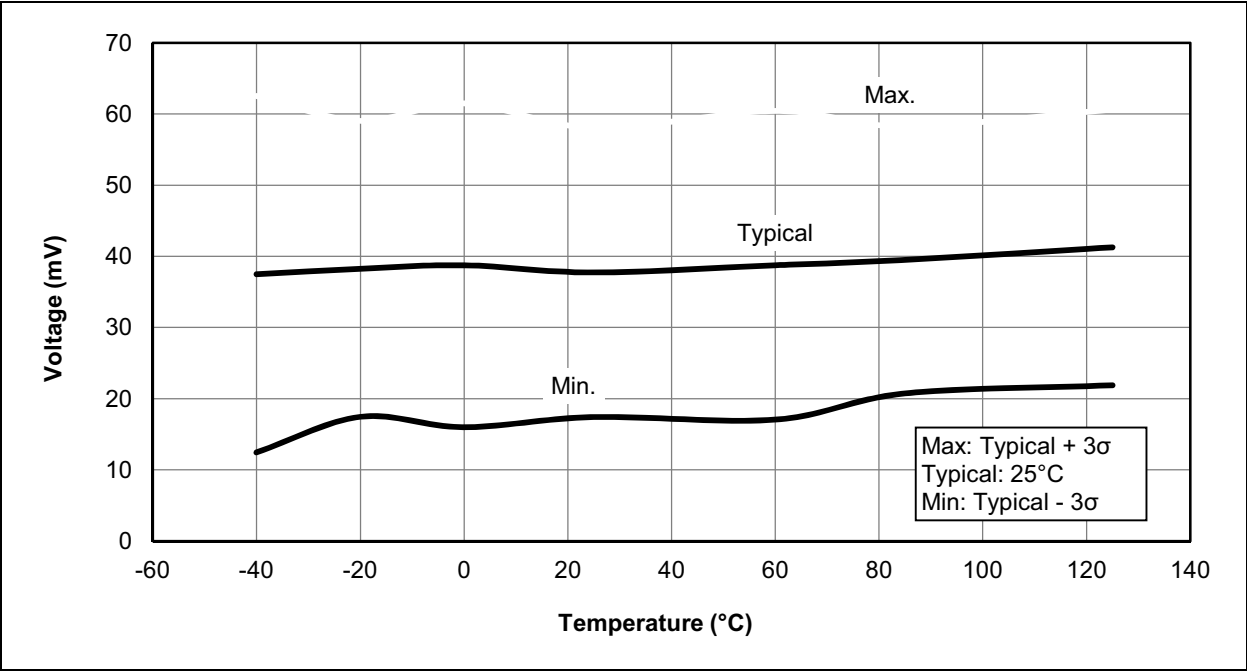
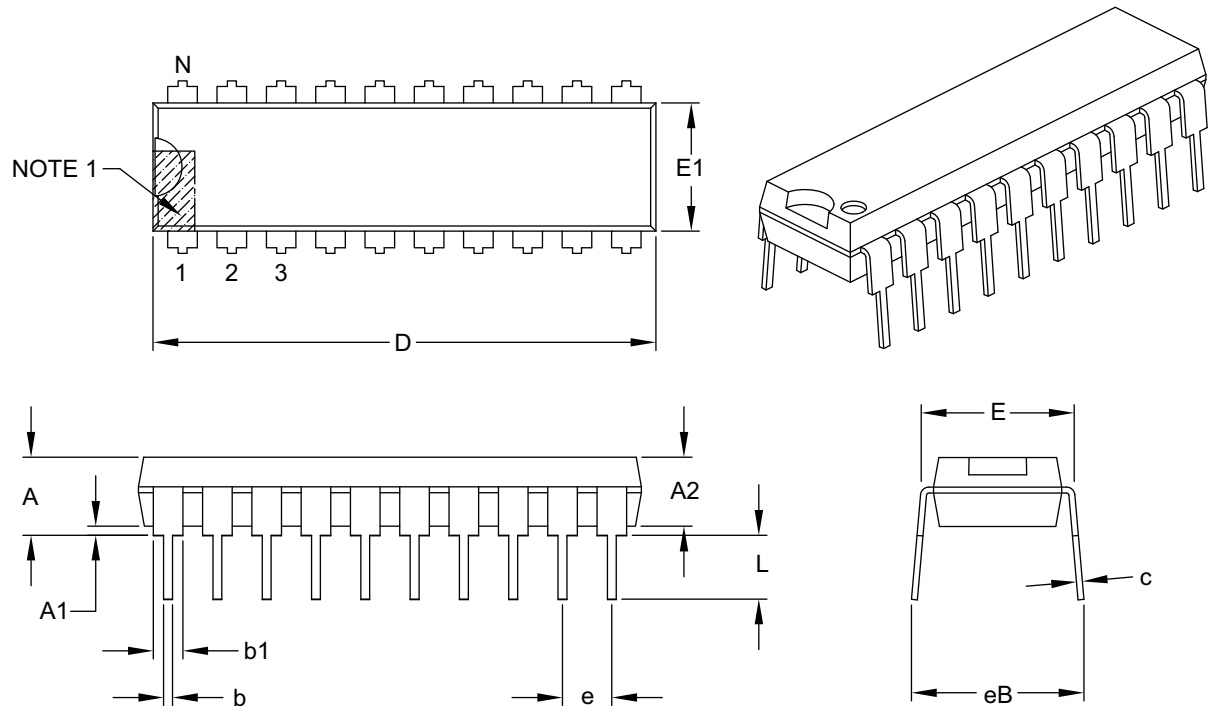


FIGURE 31-50: BROWN-OUT RESET HYSTERESIS, BORV = 1



20-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	20		
Pitch	e	.100 BSC		
Top to Seating Plane	A	–	–	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.300	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.980	1.030	1.060
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.045	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
- Dimensioning and tolerancing per ASME Y14.5M.
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-019B