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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	17
Program Memory Size	7KB (4K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	20-DIP (0.300", 7.62mm)
Supplier Device Package	20-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf1828-i-p

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Name	Function	Input Type	Output Type	Description
RA0/AN0/CPS0/C1IN+/VREF-/	RA0	TTL	CMOS	General purpose I/O.
	AN0	AN	_	A/D Channel 0 input.
ICSPDAT/ICDDAT	CPS0	AN	_	Capacitive sensing input 0.
	C1IN+	AN	—	Comparator C1 positive input.
	VREF-	AN	—	A/D and DAC Negative Voltage Reference input.
	DACOUT	_	AN	Digital-to-Analog Converter output.
	ТΧ	—	CMOS	USART asynchronous transmit.
	СК	ST	CMOS	USART synchronous clock.
	ICSPDAT	ST	CMOS	ICSP™ Data I/O.
	ICDDAT	ST	CMOS	In-Circuit Data I/O.
RA1/AN1/CPS1/C12IN0-/VREF+/	RA1	TTL	CMOS	General purpose I/O.
SRI/RX ⁽¹⁾ /DT ⁽¹⁾ /ICSPCLK/	AN1	AN	—	A/D Channel 1 input.
ICDCLK	CPS1	AN	—	Capacitive sensing input 1.
	C12IN0-	AN	—	Comparator C1 or C2 negative input.
	VREF+	AN	—	A/D and DAC Positive Voltage Reference input.
	SRI	ST	—	SR latch input.
	RX	ST	—	USART asynchronous input.
	DT	ST	CMOS	USART synchronous data.
	ICSPCLK	ST	—	Serial Programming Clock.
	ICDCLK	ST	—	In-Circuit Debug Clock.
RA2/AN2/CPS2/T0CKI/INT/	RA2	ST	CMOS	General purpose I/O.
C1OUT/SRQ/CCP3/FLT0	AN2	AN	—	A/D Channel 2 input.
	CPS2	AN	—	Capacitive sensing input 2.
	TOCKI	ST	—	Timer0 clock input.
	INT	ST	—	External interrupt.
	C10UT	_	CMOS	Comparator C1 output.
	SRQ	—	CMOS	SR latch non-inverting output.
	CCP3	ST	CMOS	Capture/Compare/PWM3.
	FLT0	ST	—	ECCP Auto-Shutdown Fault input.
RA3/SS ⁽¹⁾ /T1G ⁽¹⁾ /VPP/MCLR	RA3	TTL	—	General purpose input.
	SS	ST	_	Slave Select input.
	T1G	ST	—	Timer1 Gate input.
	Vpp	HV	_	Programming voltage.
	MCLR	ST		Master Clear with internal pull-up.

TABLE 1-2: PIC16(L)F1824 PINOUT DESCRIPTION

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open Drain TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I²C[™] = Schmitt Trigger input with I²C HV = High Voltage XTAL = Crystal levels

Note 1: Pin functions can be moved using the APFCONO and APFCON1 registers (Register 12-1 and Register 12-2). 2: Default function location.

FIGURE 2-1: CORE BLOCK DIAGRAM



11.3 Flash Program Memory Overview

It is important to understand the Flash program memory structure for erase and programming operations. Flash program memory is arranged in rows. A row consists of a fixed number of 14-bit program memory words. A row is the minimum block size that can be erased by user software.

Flash program memory may only be written or erased if the destination address is in a segment of memory that is not write-protected, as defined in bits WRT<1:0> of Configuration Word 2.

After a row has been erased, the user can reprogram all or a portion of this row. Data to be written into the program memory row is written to 14-bit wide data write latches. These write latches are not directly accessible to the user, but may be loaded via sequential writes to the EEDATH:EEDATL register pair.

Note:	If the user wants to modify only a portion
	of a previously programmed row, then the
	contents of the entire row must be read
	and saved in RAM prior to the erase.

The number of data write latches is not equivalent to the number of row locations. During programming, user software will need to fill the set of write latches and initiate a programming operation multiple times in order to fully reprogram an erased row. For example, a device with a row size of 32 words and eight write latches will need to load the write latches with data and initiate a programming operation four times.

The size of a program memory row and the number of program memory write latches may vary by device. See Table 11-1 for details.

TABLE 11-1:FLASH MEMORY
ORGANIZATION BY DEVICE

Device	Erase Block (Row) Size/ Boundary	Number of Write Latches/ Boundary
PIC16(L)F1824	32 words,	32 words,
PIC16(L)F1828	EEADRL<4:0>	EEADRL<4:0>
	= 00000	= 00000

11.3.1 READING THE FLASH PROGRAM MEMORY

To read a program memory location, the user must:

- 1. Write the Least and Most Significant address bits to the EEADRH:EEADRL register pair.
- 2. Clear the CFGS bit of the EECON1 register.
- 3. Set the EEPGD control bit of the EECON1 register.
- 4. Then, set control bit RD of the EECON1 register.

Once the read control bit is set, the program memory Flash controller will use the second instruction cycle to read the data. This causes the second instruction immediately following the "BSF EECON1, RD" instruction to be ignored. The data is available in the very next cycle, in the EEDATH:EEDATL register pair; therefore, it can be read as two bytes in the following instructions.

EEDATH:EEDATL register pair will hold this value until another read or until it is written to by the user.

- Note 1: The two instructions following a program memory read are required to be NOPS. This prevents the user from executing a two-cycle instruction on the next instruction after the RD bit is set.
 - 2: Flash program memory can be read regardless of the setting of the CP bit.

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u			
	ADRES<9:2>									
bit 7							bit 0			
Legend:										
R = Readable	bit	W = Writable I	bit	U = Unimpler	nented bit, read	d as '0'				
u = Bit is uncha	anged	x = Bit is unkn	iown	-n/n = Value a	at POR and BC	R/Value at all	other Resets			
'1' = Bit is set		'0' = Bit is clea	ared							

REGISTER 16-3: ADRESH: ADC RESULT REGISTER HIGH (ADRESH) ADFM = 0

bit 7-0 **ADRES<9:2>**: ADC Result Register bits Upper eight bits of 10-bit conversion result

REGISTER 16-4: ADRESL: ADC RESULT REGISTER LOW (ADRESL) ADFM = 0

| R/W-x/u |
|---------|---------|---------|---------|---------|---------|---------|---------|
| ADRE | S<1:0> | — | — | — | — | — | — |
| bit 7 | | | | | | | bit 0 |

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-6 ADRES<1:0>: ADC Result Register bits Lower 2 bits of 10-bit conversion result bit 5-0 Reserved: Do not use.

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REGISTER 16-5: ADRESH: ADC RESULT REGISTER HIGH (ADRESH) ADFM = 1

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
—	—	—	_	—	—	ADRES<9:8>	
bit 7							bit 0
Legend:							
R = Readable bit W = Writable bit			bit	U = Unimplemented bit, read as '0'			
u = Bit is uncha	u = Bit is unchanged x = Bit is unknown		iown	-n/n = Value at POR and BOR/Value at all other Resets			
'1' = Bit is set		'0' = Bit is clea	ared				

bit 7-2 Reserved: Do not use.

bit 1-0 ADRES<9:8>: ADC Result Register bits Upper two bits of 10-bit conversion result

REGISTER 16-6: ADRESL: ADC RESULT REGISTER LOW (ADRESL) ADFM = 1

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	
ADRES<7:0>								
bit 7							bit 0	

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 ADRES<7:0>: ADC Result Register bits Lower eight bits of 10-bit conversion result

FIGURE 16-4: ANALOG INPUT MODEL







R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	U-0	U-0	R/W-0/0	R/W-0/0
CxINTP	CxINTN	CxPCH<1:0>		—	—	CxNC	H<1:0>
bit 7						•	bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, read	d as '0'	
u = Bit is unch	anged	x = Bit is unkr	nown	-n/n = Value a	at POR and BO	R/Value at all o	other Resets
'1' = Bit is set		'0' = Bit is clea	ared				
TT = Bit is set '0' = Bit is cleared bit 7 CxINTP: Comparator Interrupt on Positive Going Edge Enable bits 1 = The CxIF interrupt flag will be set upon a positive going edge of the CxOUT bit 0 = No interrupt flag will be set on a positive going edge of the CxOUT bit bit 6 CxINTN: Comparator Interrupt on Negative Going Edge Enable bits 1 = The CxIF interrupt flag will be set upon a negative going edge of the CxOUT bit 0 = No interrupt flag will be set on a negative going edge of the CxOUT bit 0 = No interrupt flag will be set on a negative going edge of the CxOUT bit 0 = No interrupt flag will be set on a negative going edge of the CxOUT bit 0 = No interrupt flag will be set on a negative going edge of the CxOUT bit 0 = No interrupt flag will be set on a negative going edge of the CxOUT bit 0 = No interrupt flag will be set on a negative going edge of the CxOUT bit 0 = CxVP connects to CxIN+ pin 0 = CxVP connects to DAC Voltage Reference 1 = CxVP connects to FVR Voltage Reference 1 = CxVP connects to FVR Voltage Reference 1 = CxVP connects to FVR Voltage Reference							
bit 3-2	Unimplemen	ted: Read as '	0'				
bit 1-0	CxNCH<1:0>: Comparator Negative Input Channel Select bits 00 = CxVN connects to C12IN0- pin 01 = CxVN connects to C12IN1- pin 10 = CxVN connects to C12IN2- pin 11 = CxVN connects to C12IN3- pin						

REGISTER 19-2: CMxCON1: COMPARATOR CX CONTROL REGISTER 1

REGISTER 19-3: CMOUT: COMPARATOR OUTPUT REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	R-0/0	R-0/0
	—	—	—	—	—	MC2OUT	MC10UT
bit 7	•			•			bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-2	Unimplemented: Read as '0'
---------	----------------------------

- bit 1 MC2OUT: Mirror Copy of C2OUT bit
- bit 0 MC10UT: Mirror Copy of C10UT bit

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
CPSCON0	CPSON	CPSRM	_		CPSRNG<1:0>		CPSOUT	T0XCS	319
FVRCON	FVREN	FVRRDY	TSEN	TSRNG	CDAFVR<1:0>		ADFVR<1:0>		141
INLVLA	_	_	INLVLA5	INLVLA4	INLVLA3	INLVLA2	INLVLA1	INLVLA0	123
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	89
OPTION_REG	WPUEN	INTEDG	TMR0CS	TMR0SE	PSA F		PS<2:0>		176
TMR0	Timer0 Module Register								174*
TRISA	—	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	121

Legend: — = Unimplemented location, read as '0'. Shaded cells are not used by the Timer0 module.

* Page provides register information.



FIGURE 21-4: TIMER1 GATE TOGGLE MODE





22.5 Timer2 Control Register

U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
		TxOUTI	PS<3:0>		TMRxON	TxCKP	S<1:0>
bit 7						L	bit 0
Legend:							
R = Readab	le bit	W = Writable	bit	U = Unimpler	nented bit, read	d as '0'	
u = Bit is un	changed	x = Bit is unkr	nown	-n/n = Value a	at POR and BO	R/Value at all	other Resets
'1' = Bit is se	et	'0' = Bit is clea	ared				
bit 7	Unimpleme	nted: Read as '	0'				
bit 6-3	TxOUTPS<3	3:0>: Timerx Ou	tput Postscale	er Select bits			
	1111 = 1:16	Postscaler					
	1110 = 1:15	Postscaler					
	1101 = 1:14	Postscaler					
	1100 = 1.13	Postscaler					
	1011 = 1.12	Postscaler					
	1010 = 1.11 1001 = 1.10	Postscaler					
	1000 = 1:9 F	Postscaler					
	0111 = 1 :8 F	Postscaler					
	0110 = 1:7 F	Postscaler					
	0101 = 1:6 F	Postscaler					
	0100 = 1:5 F	Postscaler					
	0011 = 1 :4 F	Postscaler					
	0010 = 1:3 F	Postscaler					
	0001 = 1:2F						
hit 0							
DIL 2	1 = Timory i						
	0 = Timerx i	is off					
bit 1-0	TxCKPS<1:	0>: Timer2-tvpe	Clock Presca	ale Select bits			
	11 = Presca	ler is 64					
	10 =Prescal	er is 16					
	01 =Prescal	er is 4					
	00 =Prescal	er is 1					

REGISTER 22-1: TXCON: TIMER2/TIMER4/TIMER6 CONTROL REGISTER

24.4.1 HALF-BRIDGE MODE

In Half-Bridge mode, two pins are used as outputs to drive push-pull loads. The PWM output signal is output on the CCPx/PxA pin, while the complementary PWM output signal is output on the PxB pin (see Figure 24-9). This mode can be used for Half-Bridge applications, as shown in Figure 24-9, or for Full-Bridge applications, where four power switches are being modulated with two PWM signals.

In Half-Bridge mode, the programmable dead-band delay can be used to prevent shoot-through current in Half-Bridge power devices. The value of the PDC<6:0> bits of the PWMxCON register sets the number of instruction cycles before the output is driven active. If the value is greater than the duty cycle, the corresponding output remains inactive during the entire cycle. See **Section 24.4.5 "Programmable Dead-Band Delay Mode"** for more details of the dead-band delay operations. Since the PxA and PxB outputs are multiplexed with the PORT data latches, the associated TRIS bits must be cleared to configure PxA and PxB as outputs.





FIGURE 24-9: EXAMPLE OF HALF-BRIDGE APPLICATIONS



The I^2C interface supports the following modes and features:

- Master mode
- Slave mode
- Byte NACKing (Slave mode)
- · Limited multi-master support
- 7-bit and 10-bit addressing
- · Start and Stop interrupts
- · Interrupt masking
- Clock stretching
- · Bus collision detection
- · General call address matching
- Address masking
- · Address Hold and Data Hold modes
- · Selectable SDA hold times

Figure 25-2 is a block diagram of the I^2C interface module in Master mode. Figure 25-3 is a diagram of the I^2C interface module in Slave mode.

FIGURE 25-2: MSSP1 BLOCK DIAGRAM (I²C[™] MASTER MODE)





25.6.7 I²C MASTER MODE RECEPTION

Master mode reception is enabled by programming the Receive Enable bit, RCEN bit of the SSP1CON2 register.

Note:	The MSSP1 module must be in an Idle
	state before the RCEN bit is set or the
	RCEN bit will be disregarded.

The Baud Rate Generator begins counting and on each rollover, the state of the SCL pin changes (high-to-low/low-to-high) and data is shifted into the SSP1SR. After the falling edge of the eighth clock, the receive enable flag is automatically cleared, the contents of the SSP1SR are loaded into the SSP1BUF, the BF flag bit is set, the SSP1IF flag bit is set and the Baud Rate Generator is suspended from counting, holding SCL low. The MSSP1 is now in Idle state awaiting the next command. When the buffer is read by the CPU, the BF flag bit is automatically cleared. The user can then send an Acknowledge bit at the end of reception by setting the Acknowledge Sequence Enable, ACKEN bit of the SSP1CON2 register.

25.6.7.1 BF Status Flag

In receive operation, the BF bit is set when an address or data byte is loaded into SSP1BUF from SSP1SR. It is cleared when the SSP1BUF register is read.

25.6.7.2 SSPOV Status Flag

In receive operation, the SSPOV bit is set when eight bits are received into the SSP1SR and the BF flag bit is already set from a previous reception.

25.6.7.3 WCOL Status Flag

If the user writes the SSP1BUF when a receive is already in progress (i.e., SSP1SR is still shifting in a data byte), the WCOL bit is set and the contents of the buffer are unchanged (the write does not occur). 25.6.7.4 Typical Receive Sequence:

- 1. The user generates a Start condition by setting the SEN bit of the SSP1CON2 register.
- 2. SSP1IF is set by hardware on completion of the Start.
- 3. SSP1IF is cleared by software.
- 4. User writes SSP1BUF with the slave address to transmit and the R/W bit set.
- 5. Address is shifted out the SDA pin until all eight bits are transmitted. Transmission begins as soon as SSP1BUF is written to.
- The MSSP1 module shifts in the ACK bit from the slave device and writes its value into the ACKSTAT bit of the SSP1CON2 register.
- The MSSP1 module generates an interrupt at the end of the ninth clock cycle by setting the SSP1IF bit.
- 8. User sets the RCEN bit of the SSP1CON2 register and the master clocks in a byte from the slave.
- 9. After the eighth falling edge of SCL, SSP1IF and BF are set.
- 10. Master clears SSP1IF and reads the received byte from SSP1UF, clears BF.
- Master sets ACK value sent to slave in ACKDT bit of the SSP1CON2 register and initiates the ACK by setting the ACKEN bit.
- 12. Masters ACK is clocked out to the slave and SSP1IF is set.
- 13. User clears SSP1IF.
- 14. Steps 8-13 are repeated for each received byte from the slave.
- 15. Master sends a not ACK or Stop to end communication.

26.4.1.5 Synchronous Master Reception

Data is received at the RX/DT pin. The RX/DT pin output driver is automatically disabled when the EUSART is configured for synchronous master receive operation.

In Synchronous mode, reception is enabled by setting either the Single Receive Enable bit (SREN of the RCSTA register) or the Continuous Receive Enable bit (CREN of the RCSTA register).

When SREN is set and CREN is clear, only as many clock cycles are generated as there are data bits in a single character. The SREN bit is automatically cleared at the completion of one character. When CREN is set, clocks are continuously generated until CREN is cleared. If CREN is cleared in the middle of a character the CK clock stops immediately and the partial character is discarded. If SREN and CREN are both set, then SREN is cleared at the completion of the first character and CREN takes precedence.

To initiate reception, set either SREN or CREN. Data is sampled at the RX/DT pin on the trailing edge of the TX/CK clock pin and is shifted into the Receive Shift Register (RSR). When a complete character is received into the RSR, the RCIF bit is set and the character is automatically transferred to the two character receive FIFO. The Least Significant eight bits of the top character in the receive FIFO are available in RCREG. The RCIF bit remains set as long as there are unread characters in the receive FIFO.

Note:	If the RX/DT function is on an analog pin,							
	the corresponding ANSEL bit must be							
	cleared for the receiver to function.							

26.4.1.6 Slave Clock

Synchronous data transfers use a separate clock line, which is synchronous with the data. A device configured as a slave receives the clock on the TX/CK line. The TX/CK pin output driver is automatically disabled when the device is configured for synchronous slave transmit or receive operation. Serial data bits change on the leading edge to ensure they are valid at the trailing edge of each clock. One data bit is transferred for each clock cycle. Only as many clock cycles should be received as there are data bits.

Note: If the device is configured as a slave and the TX/CK function is on an analog pin, the corresponding ANSEL bit must be cleared.

26.4.1.7 Receive Overrun Error

The receive FIFO buffer can hold two characters. An overrun error will be generated if a third character, in its entirety, is received before RCREG is read to access the FIFO. When this happens the OERR bit of the RCSTA register is set. Previous data in the FIFO will not be overwritten. The two characters in the FIFO buffer can be read, however, no additional characters will be received until the error is cleared. The OERR bit can only be cleared by clearing the overrun condition. If the overrun error occurred when the SREN bit is set and CREN is clear then the error is cleared by reading RCREG. If the overrun occurred when the CREN bit is set then the error condition is cleared by either clearing the CREN bit of the RCSTA register or by clearing the SPEN bit which resets the EUSART.

26.4.1.8 Receiving 9-bit Characters

The EUSART supports 9-bit character reception. When the RX9 bit of the RCSTA register is set the EUSART will shift 9-bits into the RSR for each character received. The RX9D bit of the RCSTA register is the ninth, and Most Significant, data bit of the top unread character in the receive FIFO. When reading 9-bit data from the receive FIFO buffer, the RX9D data bit must be read before reading the eight Least Significant bits from the RCREG.

26.4.1.9 Synchronous Master Reception Setup:

- 1. Initialize the SPBRGH, SPBRGL register pair for the appropriate baud rate. Set or clear the BRGH and BRG16 bits, as required, to achieve the desired baud rate.
- 2. Clear the ANSEL bit for the RX pin (if applicable).
- 3. Enable the synchronous master serial port by setting bits SYNC, SPEN and CSRC.
- 4. Ensure bits CREN and SREN are clear.
- 5. If interrupts are desired, set the RCIE bit of the PIE1 register and the GIE and PEIE bits of the INTCON register.
- 6. If 9-bit reception is desired, set bit RX9.
- 7. Start reception by setting the SREN bit or for continuous reception, set the CREN bit.
- 8. Interrupt flag bit RCIF will be set when reception of a character is complete. An interrupt will be generated if the enable bit RCIE was set.
- 9. Read the RCSTA register to get the ninth bit (if enabled) and determine if any error occurred during reception.
- 10. Read the 8-bit received data by reading the RCREG register.
- 11. If an overrun error occurs, clear the error by either clearing the CREN bit of the RCSTA register or by clearing the SPEN bit which resets the EUSART.

FIGURE 27-2: CAPACITIVE SENSING OSCILLATOR BLOCK DIAGRAM



30.7 Timing Parameter Symbology

The timing parameter symbols have been created with one of the following formats:

- 1. TppS2ppS
- 2. TppS

T			
F	Frequency	т	Time
Lowerc	case letters (pp) and their meanings:		
рр			
сс	CCP1	osc	OSC1
ck	CLKOUT	rd	RD
CS	CS	rw	RD or WR
di	SDIx	sc	SCKx
do	SDO	ss	SS
dt	Data in	tO	TOCKI
io	I/O PORT	t1	T1CKI
mc	MCLR	wr	WR
Upperc	case letters and their meanings:	·	
S			
F	Fall	Р	Period
Н	High	R	Rise
I	Invalid (High-impedance)	V	Valid
L	Low	Z	High-impedance

FIGURE 30-5: LOAD CONDITIONS



TABLE 30-8: PIC16(L)F1824/8 A/D CONVERTER (ADC) CHARACTERISTICS (NOTE 1, 2, 3)

Operating Conditions (unless otherwise stated) VDD = 3.0V, TA = 25°C										
Param No.	Sym.	Characteristic	Min.	Тур†	Max.	Units	Conditions			
AD01	NR	Resolution		_	10	bit				
AD02	EIL	Integral Error	I		±1.7	LSb	VREF = 3.0V			
AD03	Edl	Differential Error			±1	LSb	No missing codes VREF = 3.0V			
AD04	EOFF	Offset Error	I		±2.5	LSb	VREF = 3.0V			
AD05	Egn	Gain Error	l		±2.0	LSb	VREF = 3.0V			
AD06	VREF	Reference Voltage ⁽⁴⁾	1.8		Vdd	V	VREF = (VREF+ minus VREF-)			
AD07	VAIN	Full-Scale Range	Vss		VREF	V				
AD08	ZAIN	Recommended Impedance of Analog Voltage Source			10	kΩ	Can go higher if external 0.01µF capacitor is present on input pin.			
*	Thor	a parameters are oberectorized but	not toot	od						

These parameters are characterized but not tested.

t Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Total Absolute Error includes integral, differential, offset and gain errors.

2: The A/D conversion result never decreases with an increase in the input voltage and has no missing codes.

3: ADC VREF is from external VREF, VDD pin or FVR, whichever is selected as reference input.

4: ADC Reference Voltage (REF+) is the selected input, VREF+ pin, VDD pin or the FVR Buffer1. When the FVR is selected as the reference input, the FVR Buffer1 output selection must be 2.048 or 4.096V (ADFVR<1:0> = 1x).

TABLE 30-9: PIC16(L)F1824/8 A/D CONVERSION REQUIREMENTS

Operating Conditions (unless otherwise stated) VDD = 3.0V, TA = 25°C										
Param No.	Sym.	Characteristic	Min.	Тур†	Max.	Units	Conditions			
AD130*	Tad	A/D Clock Period	1.0	_	9.0	μS	Tosc-based			
		A/D Internal RC Oscillator Period	1.0	2.5	6.0	μS	ADCS<1:0> = 11 (ADRC mode)			
AD131	TCNV	Conversion Time (not including Acquisition Time) ⁽¹⁾	-	11	—	TAD	Set GO/DONE bit to conversion complete			
AD132*	TACQ	Acquisition Time	—	5.0		μS				

These parameters are characterized but not tested.

Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not t tested.

Note 1: The ADRES register may be read on the following TCY cycle.

PIC16F1824/8			Standard Operating Conditions: (unless otherwise stated) Operating Temperature: $-40^{\circ}C \le TA \le +150^{\circ}C$ for High Temperature					
Param No.	Sym.	Characteristics	Min.	Тур.	Max.	Units	Condition	
D001	Vdd	Supply Voltage	2.5	_	5.5	V	Fosc ≤ 32 MHz (Note 2)	
D002*	Vdr	RAM Data Retention Voltage ⁽¹⁾	2.1	_	5.5	V	Device in Sleep mode	
D003	VADFVR	Fixed Voltage Reference Voltage for ADC	-10	_	8	%	$\begin{array}{l} 1.024V, \mbox{ Vdd} \geq 2.5V \\ 2.048V, \mbox{ Vdd} \geq 2.5V \\ 4.096V, \mbox{ Vdd} \geq 4.75V \end{array}$	
D003A	VCDAFV R	Fixed Voltage Reference Voltage for ADC	-13	_	9	%	$\begin{array}{l} 1.024V, \mbox{ Vdd} \geq 2.5V \\ 2.048V, \mbox{ Vdd} \geq 2.5V \\ 4.096V, \mbox{ Vdd} \geq 4.75V \end{array}$	

TABLE 30-19: DC CHARACTERISTICS FOR PIC16F1824/8-H (High Temp.)

These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in Sleep mode without losing RAM data.

2: PLL required for 32 MHz operation.

TABLE 30-20: DC CHARACTERISTICS FOR IDD SPECIFICATIONS FOR PIC16F1824/8-H (High Temp.)

PIC16F1824/8		Standard Operating Conditions: (unless otherwise stated) Operating Temperature: $-40^{\circ}C \le TA \le +150^{\circ}C$ for High Temperature							
Param	Device Characteristics	Min	Тур.	Max.	Units	Condition			
No.		win.				Vdd	Note		
	Supply Voltage (IDD) ^(1,2)								
D010A		_		70	μA	3.0	Fosc ≤ 32 kHz		
		—		75	μA	5.0	LP Oscillator mode		
D015		_		75	μA	3.0	Fosc ≤ 31 kHz		
		—		80	μA	5.0	LFINTOSC mode		

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD; MCLR = VDD; WDT disabled.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rage, oscillator type, internal code execution pattern, and temperature, also have an impact on the current consumption.