



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	17
Program Memory Size	7KB (4K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf1828-i-so

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong





4.2 Code Protection

Code protection allows the device to be protected from unauthorized access. Program memory protection and data EEPROM protection are controlled independently. Internal access to the program memory and data EEPROM are unaffected by any code protection setting.

4.2.1 PROGRAM MEMORY PROTECTION

The entire program memory space is protected from external reads and writes by the \overline{CP} bit in Configuration Word 1. When $\overline{CP} = 0$, external reads and writes of program memory are inhibited and a read will return all '0's. The CPU can continue to read program memory, regardless of the protection bit settings. Writing the program memory is dependent upon the write protection setting. See **Section 4.3** "Write **Protection**" for more information.

4.2.2 DATA EEPROM PROTECTION

The entire data EEPROM is protected from external reads and writes by the CPD bit. When CPD = 0, external reads and writes of data EEPROM are inhibited. The CPU can continue to read and write data EEPROM regardless of the protection bit settings.

4.3 Write Protection

Write protection allows the device to be protected from unintended self-writes. Applications, such as bootloader software, can be protected while allowing other regions of the program memory to be modified.

The WRT<1:0> bits in Configuration Word 2 define the size of the program memory block that is protected.

4.4 User ID

Four memory locations (8000h-8003h) are designated as ID locations where the user can store checksum or other code identification numbers. These locations are readable and writable during normal execution. See **Section 11.5 "User ID, Device ID and Configuration Word Access"** for more information on accessing these memory locations. For more information on checksum calculation, see the "*PIC16F/LF182X/PIC12F/LF1822 Memory Programming Specification*" (DS41390).

U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
— — TUN<5:0>							
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimplen	nented bit, read	d as '0'	
u = Bit is unch	anged	x = Bit is unkr	nown	-n/n = Value a	t POR and BO	R/Value at all	other Resets
'1' = Bit is set		'0' = Bit is clea	ared				
bit 7-6	Unimplemer	nted: Read as '	0'				
bit 5-0	TUN<4:0>: F	requency Tunir	ng bits				
	011111 = M	laximum freque	ncy				
	011110 =						
	•						
	•						
	000001 =						
	000000 = O	scillator module	e is running at	the factory-cali	prated frequen	cy.	
111111 =							
	•						
	•						
	• $100000 = M$	linimum frequer					
	T00000 - IV	minium nequei	icy				

REGISTER 5-3: OSCTUNE: OSCILLATOR TUNING REGISTER

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
OSCCON	SPLLEN		IRCI	=<3:0>		—	SCS	<1:0>	68
OSCSTAT	T10SCR	PLLR	OSTS	HFIOFR	HFIOFL	MFIOFR	LFIOFR	HFIOFS	69
OSCTUNE	—	_		TUN<5:0>					70
PIE2	OSFIE	C2IE	C1IE	EEIE	BCL1IE	—	—	CCP2IE	91
PIR2	OSFIF	C2IF	C1IF	EEIF	BCL1IF	—	—	CCP2IF	94
T1CON	TMR1C	S<1:0>	<1:0> T1CKPS<1:0>		T10SCEN	T1SYNC	_	TMR10N	186

TABLE 5-2: SUMMARY OF REGISTERS ASSOCIATED WITH CLOCK SOURCES

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by clock sources.

TABLE 5-3: SUMMARY OF CONFIGURATION WORD WITH CLOCK SOURCES

Name	Bits	Bit -/7	Bit -/6	Bit 13/5	Bit 12/4	Bit 11/3	Bit 10/2	Bit 9/1	Bit 8/0	Register on Page
0015104	13:8	—	—	FCMEN	IESO	CLKOUTEN	BORE	N<1:0>	CPD	40
7:0 CP MCLRE PWRTE		WDTE	WDTE<1:0>		FOSC<2:0>					

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by clock sources.

7.3 MCLR

The $\overline{\text{MCLR}}$ is an optional external input that can reset the device. The $\overline{\text{MCLR}}$ function is controlled by the MCLRE bit of Configuration Word 1 and the LVP bit of Configuration Word 2 (Table 7-2).

TABLE 7-2:	MCLR	CONFIGURATION

MCLRE	LVP	MCLR
0	0	Disabled
1	0	Enabled
x	1	Enabled

7.3.1 MCLR ENABLED

When MCLR is enabled and the pin is held low, the device is held in Reset. The MCLR pin is connected to VDD through an internal weak pull-up.

The device has a noise filter in the $\overline{\text{MCLR}}$ Reset path. The filter will detect and ignore small pulses.

Note: A Reset does not drive the MCLR pin lo	W.
---	----

7.3.2 MCLR DISABLED

When MCLR is disabled, the pin functions as a general purpose input and the internal weak pull-up is under software control. See **Section 12.2 "PORTA Registers"** for more information.

7.4 Watchdog Timer (WDT) Reset

The Watchdog Timer generates a Reset if the firmware does not issue a CLRWDT instruction within the time-out period. The TO and PD bits in the STATUS register are changed to indicate the WDT Reset. See **Section 10.0** "**Watchdog Timer**" for more information.

7.5 RESET Instruction

A RESET instruction will cause a device Reset. The \overline{RI} bit in the PCON register will be set to '0'. See Table 7-4 for default conditions after a RESET instruction has occurred.

7.6 Stack Overflow/Underflow Reset

The device can reset when the Stack Overflows or Underflows. The STKOVF or STKUNF bits of the PCON register indicate the Reset condition. These Resets are enabled by setting the STVREN bit in Configuration Word 2. See **Section 3.4.2** "**Overflow/Underflow Reset**" for more information.

7.7 Programming Mode Exit

Upon exit of Programming mode, the device will behave as if a POR had just occurred.

7.8 Power-up Timer

The Power-up Timer optionally delays device execution after a BOR or POR event. This timer is typically used to allow VDD to stabilize before allowing the device to start running.

The Power-up Timer is controlled by the $\overrightarrow{\text{PWRTE}}$ bit of Configuration Word 1.

7.9 Start-up Sequence

Upon the release of a POR or BOR, the following must occur before the device will begin executing:

- 1. Power-up Timer runs to completion (if enabled).
- 2. Oscillator start-up timer runs to completion (if required for oscillator source).
- 3. MCLR must be released (if enabled).

The total time-out will vary based on oscillator configuration and Power-up Timer configuration. See Section 5.0 "Oscillator Module (With Fail-Safe Clock Monitor)" for more information.

The Power-up Timer and oscillator start-up timer run independently of MCLR Reset. If MCLR is kept low long enough, the Power-up Timer and oscillator start-up timer will expire. Upon bringing MCLR high, the device will begin execution immediately (see Figure 7-4). This is useful for testing purposes or to synchronize more than one device operating in parallel.

Even if the flag bits were checked before executing a SLEEP instruction, it may be possible for flag bits to become set before the SLEEP instruction completes. To determine whether a SLEEP instruction executed, test the PD bit. If the PD bit is set, the SLEEP instruction was executed as a NOP.

FIGURE 9-1: WAKE-UP FROM SLEEP THROUGH INTERRUPT



Note 1: XT, HS or LP Oscillator mode assumed.

2: CLKOUT is not available in XT, HS, or LP Oscillator modes, but shown here for timing reference.

3: Tost = 1024 Tosc (drawing not to scale). This delay applies only to XT, HS or LP Oscillator modes.

4: GIE = 1 assumed. In this case after wake-up, the processor calls the ISR at 0004h. If GIE = 0, execution will continue in-line.

TABLE 9-1: SUMMARY OF REGISTERS ASSOCIATED WITH POWER-DOWN MODE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	89
IOCAF	_	—	IOCAF5	IOCAF4	IOCAF3	IOCAF2	IOCAF1	IOCAF0	137
IOCAN	_	—	IOCAN5	IOCAN4	IOCAN3	IOCAN2	IOCAN1	IOCAN0	137
IOCAP	_	—	IOCAP5	IOCAP4	IOCAP3	IOCAP2	IOCAP1	IOCAP0	137
IOCBF ⁽¹⁾	IOCBF7	IOCBF6	IOCBF5	IOCBF4	—	—	—	—	139
IOCBN ⁽¹⁾	IOCBN7	IOCBN6	IOCBN5	IOCBN4	—	—	—	—	138
IOCBP ⁽¹⁾	IOCBP7	IOCBP6	IOCBP5	IOCBP4	—	—	—	—	138
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	90
PIE2	OSFIE	C2IE	C1IE	EEIE	BCL1IE	—	—	CCP2IE	91
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	93
PIR2	OSFIF	C2IF	C1IF	EEIF	BCL1IF	—	—	CCP2IF	94
STATUS	_	—	—	TO	PD	Z	DC	С	22
WDTCON		_	WDTPS4	WDTPS3	WDTPS2	WDTPS1	WDTPS0	SWDTEN	101

Legend: — = unimplemented, read as '0'. Shaded cells are not used in Power-Down mode.

Note 1: PIC16(L)F1828 only.

16.2.6 A/D CONVERSION PROCEDURE

This is an example procedure for using the ADC to perform an Analog-to-Digital conversion:

- 1. Configure Port:
 - Disable pin output driver (Refer to the TRIS register)
 - Configure pin as analog (Refer to the ANSEL register)
- 2. Configure the ADC module:
 - Select ADC conversion clock
 - Configure voltage reference
 - Select ADC input channel
 - Turn on ADC module
- 3. Configure ADC interrupt (optional):
 - Clear ADC interrupt flag
 - · Enable ADC interrupt
 - Enable peripheral interrupt
 - Enable global interrupt⁽¹⁾
- 4. Wait the required acquisition time⁽²⁾.
- 5. Start conversion by setting the GO/DONE bit.
- 6. Wait for ADC conversion to complete by one of the following:
 - Polling the GO/DONE bit
 - Waiting for the ADC interrupt (interrupts enabled)
- 7. Read ADC Result.
- 8. Clear the ADC interrupt flag (required if interrupt is enabled).

Note 1: The global interrupt can be disabled if the user is attempting to wake-up from Sleep and resume in-line code execution.

2: Refer to Section 16.3 "A/D Acquisition Requirements".

EXAMPLE 16-1: A/D CONVERSION

;This code block configures the ADC ; for polling, Vdd and Vss references, Frc ;clock and ANO input. ;Conversion start & polling for completion ; are included. BANKSEL ADCON1 ; B'11110000' ;Right justify, Frc MOVLW ;clock MOVWF ADCON1 ;Vdd and Vss Vref BANKSEL TRISA ; BSF TRISA,0 ;Set RA0 to input BANKSEL ANSEL ; BSF ANSEL,0 ;Set RA0 to analog BANKSEL ADCON0 B'00000001' ;Select channel ANO MOVLW ;Turn ADC On MOVWE ADCON0 SampleTime ; Acquisiton delay CALL ADCON0, ADGO ; Start conversion BSF BTFSC ADCON0, ADGO ; Is conversion done? GOTO \$-1 ;No, test again ADRESH ; BANKSEL ADRESH,W ;Read upper 2 bits MOVF RESULTHI MOVWF ;store in GPR space BANKSEL ADRESL ; ADRESL,W MOVF ;Read lower 8 bits RESULTLO ;Store in GPR space MOVWE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ANSELA	—	—	-	ANSA4	—	ANSA2	ANSA1	ANSA0	122
CCP1CON	P1M	<1:0>	DC1B	3<1:0>		CCP1N	1<3:0>		225
CCP2CON	P2M·	<:0>1	DC2B	8<1:0>		CCP2N	1<3:0>		225
INLVLA	—	—	INLVLA5	INLVLA4	INLVLA3	INLVLA2	INLVLA1	INLVLA0	123
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	89
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	90
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	93
TMR1H	Holding Regi	ster for the M	ost Significan	t Byte of the	16-bit TMR1 F	Register			182*
TMR1L	Holding Regi	ster for the Le	ast Significa	nt Byte of the	16-bit TMR1	Register			182*
TRISA	—	—	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	121
T1CON	TMR1CS1	TMR1CS0	T1CKP	S<1:0>	T10SCEN	T1SYNC	—	TMR10N	186
T1GCON	TMR1GE	T1GPOL	T1GTM	T1GSPM	T1GGO/ DONE	T1GVAL	T1GSS1	T1GSS0	187

TABLE 21-5: SUMMARY OF REGISTERS ASSOCIATED WITH TIMER1

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by the Timer1 module.

* Page provides register information.

Note 1: PIC16(L)F1828 only.

25.3 I²C Mode Overview

The Inter-Integrated Circuit Bus (I²C) is a multi-master serial data communication bus. Devices communicate in a master/slave environment where the master devices initiate the communication. A Slave device is controlled through addressing.

The I²C bus specifies two signal connections:

- · Serial Clock (SCL)
- · Serial Data (SDA)

Figure 25-2 and Figure 25-3 shows the block diagram of the MSSP1 module when operating in I²C Mode.

Both the SCL and SDA connections are bidirectional open-drain lines, each requiring pull-up resistors for the supply voltage. Pulling the line to ground is considered a logical zero and letting the line float is considered a logical one.

Figure 25-11 shows a typical connection between two processors configured as master and slave devices.

The I^2C bus can operate with one or more master devices and one or more slave devices.

There are four potential modes of operation for a given device:

- Master Transmit mode
 (master is transmitting data to a slave)
- Master Receive mode
 (master is receiving data from a slave)
- Slave Transmit mode (slave is transmitting data to a master)
- Slave Receive mode (slave is receiving data from the master)

To begin communication, a master device starts out in Master Transmit mode. The master device sends out a Start bit followed by the address byte of the slave it intends to communicate with. This is followed by a single Read/Write bit, which determines whether the master intends to transmit to or receive data from the slave device.

If the requested slave exists on the bus, it will respond with an Acknowledge bit, otherwise known as an ACK. The master then continues in either Transmit mode or Receive mode and the slave continues in the complement, either in Receive mode or Transmit mode, respectively.

A Start bit is indicated by a high-to-low transition of the SDA line while the SCL line is held high. Address and data bytes are sent out, Most Significant bit (MSb) first. The Read/Write bit is sent out as a logical one when the master intends to read data from the slave, and is sent out as a logical zero when it intends to write data to the slave.

FIGURE 25-11: I²C MASTER/ SLAVE CONNECTION



The Acknowledge bit (\overline{ACK}) is an active-low signal, which holds the SDA line low to indicate to the transmitter that the slave device has received the transmitted data and is ready to receive more.

The transition of a data bit is always performed while the SCL line is held low. Transitions that occur while the SCL line is held high are used to indicate Start and Stop bits.

If the master intends to write to the slave, then it repeatedly sends out a byte of data, with the slave responding after each byte with an \overline{ACK} bit. In this example, the master device is in Master Transmit mode and the slave is in Slave Receive mode.

If the master intends to read from the slave, then it repeatedly receives a byte of data from the slave, and responds after each byte with an ACK bit. In this example, the master device is in Master Receive mode and the slave is Slave Transmit mode.

On the last byte of data communicated, the master device may end the transmission by sending a Stop bit. If the master device is in Receive mode, it sends the Stop bit in place of the last ACK bit. A Stop bit is indicated by a low-to-high transition of the SDA line while the SCL line is held high.

In some cases, the master may want to maintain control of the bus and re-initiate another transmission. If so, the master device may send another Start bit in place of the Stop bit or last ACK bit when it is in receive mode.

The I²C bus specifies three message protocols;

- Single message where a master writes data to a slave.
- Single message where a master reads data from a slave.
- Combined message where a master initiates a minimum of two writes, or two reads, or a combination of writes and reads, to one or more slaves.



25.6.5 I²C MASTER MODE REPEATED START CONDITION TIMING

A Repeated Start condition occurs when the RSEN bit of the SSP1CON2 register is programmed high and the Master state machine is no longer active. When the RSEN bit is set, the SCL pin is asserted low. When the SCL pin is sampled low, the Baud Rate Generator is loaded and begins counting. The SDA pin is released (brought high) for one Baud Rate Generator count (TBRG). When the Baud Rate Generator times out, if SDA is sampled high, the SCL pin will be deasserted (brought high). When SCL is sampled high, the Baud Rate Generator is reloaded and begins counting. SDA and SCL must be sampled high for one TBRG. This action is then followed by assertion of the SDA pin (SDA = 0) for one TBRG while SCL is high. SCL is asserted low. Following this, the RSEN bit of the SSP1CON2 register will be automatically cleared and the Baud Rate Generator will not be reloaded, leaving the SDA pin held low. As soon as a Start condition is detected on the SDA and SCL pins, the S bit of the SSP1STAT register will be set. The SSP1IF bit will not be set until the Baud Rate Generator has timed out.

- Note 1: If RSEN is programmed while any other event is in progress, it will not take effect.
 - **2:** A bus collision during the Repeated Start condition occurs if:
 - SDA is sampled low when SCL goes from low-to-high.
 - SCL goes low before SDA is asserted low. This may indicate that another master is attempting to transmit a data '1'.





25.6.6 I²C MASTER MODE TRANSMISSION

Transmission of a data byte, a 7-bit address or the other half of a 10-bit address is accomplished by simply writing a value to the SSP1BUF register. This action will set the Buffer Full flag bit, BF and allow the Baud Rate Generator to begin counting and start the next transmission. Each bit of address/data will be shifted out onto the SDA pin after the falling edge of SCL is asserted. SCL is held low for one Baud Rate Generator rollover count (TBRG). Data should be valid before SCL is released high. When the SCL pin is released high, it is held that way for TBRG. The data on the SDA pin must remain stable for that duration and some hold time after the next falling edge of SCL. After the eighth bit is shifted out (the falling edge of the eighth clock), the BF flag is cleared and the master releases SDA. This allows the slave device being addressed to respond with an \overline{ACK} bit during the ninth bit time if an address match occurred, or if data was received properly. The status of \overline{ACK} is written into the ACKSTAT bit on the rising edge of the ninth clock. If the master receives an Acknowledge, the Acknowledge Status bit, ACKSTAT, is cleared. If not, the bit is set. After the ninth clock, the SSP1IF bit is set and the master clock (Baud Rate Generator) is suspended until the next data byte is loaded into the SSP1BUF, leaving SCL low and SDA unchanged (Figure 25-28).

After the write to the SSP1BUF, each bit of the address will be shifted out on the falling edge of SCL until all seven address bits and the R/W bit are completed. On the falling edge of the eighth clock, the master will release the SDA pin, allowing the slave to respond with an Acknowledge. On the falling edge of the ninth clock, the master will sample the SDA pin to see if the address was recognized by a slave. The status of the ACK bit is loaded into the ACKSTAT Status bit of the SSP1CON2 register. Following the falling edge of the ninth clock transmission of the address, the SSP1IF is set, the BF flag is cleared and the Baud Rate Generator is turned off until another write to the SSP1BUF takes place, holding SCL low and allowing SDA to float.

25.6.6.1 BF Status Flag

In Transmit mode, the BF bit of the SSP1STAT register is set when the CPU writes to SSP1BUF and is cleared when all eight bits are shifted out.

25.6.6.2 WCOL Status Flag

If the user writes the SSP1BUF when a transmit is already in progress (i.e., SSP1SR is still shifting out a data byte), the WCOL bit is set and the contents of the buffer are unchanged (the write does not occur).

WCOL must be cleared by software before the next transmission.

25.6.6.3 ACKSTAT Status Flag

In Transmit mode, the ACKSTAT bit of the SSP1CON2 register is cleared when the slave has sent an Acknowledge ($\overrightarrow{ACK} = 0$) and is set when the slave does not Acknowledge ($\overrightarrow{ACK} = 1$). A slave sends an Acknowledge when it has recognized its address (including a general call), or when the slave has properly received its data.

25.6.6.4 Typical Transmit Sequence:

- 1. The user generates a Start condition by setting the SEN bit of the SSP1CON2 register.
- 2. SSP1IF is set by hardware on completion of the Start.
- 3. SSP1IF is cleared by software.
- 4. The MSSP1 module will wait the required start time before any other operation takes place.
- 5. The user loads the SSP1BUF with the slave address to transmit.
- Address is shifted out the SDA pin until all eight bits are transmitted. Transmission begins as soon as SSP1BUF is written to.
- 7. The MSSP1 module shifts in the ACK bit from the slave device and writes its value into the ACKSTAT bit of the SSP1CON2 register.
- The MSSP1 module generates an interrupt at the end of the ninth clock cycle by setting the SSP1IF bit.
- 9. The user loads the SSP1BUF with eight bits of data.
- 10. Data is shifted out the SDA pin until all eight bits are transmitted.
- 11. The MSSP1 module shifts in the ACK bit from the slave device and writes its value into the ACKSTAT bit of the SSP1CON2 register.
- 12. Steps 8-11 are repeated for all transmitted data bytes.
- 13. The user generates a Stop or Restart condition by setting the PEN or RSEN bits of the SSP1CON2 register. Interrupt is generated once the Stop/Restart condition is complete.

FIGURE 27-2: CAPACITIVE SENSING OSCILLATOR BLOCK DIAGRAM



RRF	Rotate Right f through Carry					
Syntax:	[<i>label</i>] RRF f,d					
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ d \in [0,1] \end{array}$					
Operation:	See description below					
Status Affected:	С					
Description:	The contents of register 'f' are rotated one bit to the right through the Carry flag. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.					



SUBLW	Subtract W from literal					
Syntax:	[<i>label</i>] SUBLW k					
Operands:	$0 \leq k \leq 255$					
Operation:	$k - (W) \to (W)$					
Status Affected:	C, DC, Z					
Description:	The W register is subtracted (2's com- plement method) from the 8-bit literal 'k'. The result is placed in the W regis- ter.					
	C = 0 W > k					
	C = 1 W ≤ k					

DC = 0

DC = 1

W<3:0> > k<3:0>

 $W<3:0> \le k<3:0>$

SLEEP	Enter Sleep mode
Syntax:	[label] SLEEP
Operands:	None
Operation:	$\begin{array}{l} 00h \rightarrow WDT, \\ 0 \rightarrow \underline{W}DT \text{ prescaler}, \\ 1 \rightarrow \underline{TO}, \\ 0 \rightarrow PD \end{array}$
Status Affected:	TO, PD
Description:	The power-down Status bit, \overline{PD} is cleared. Time-out Status bit, \overline{TO} is set. Watchdog Timer and its prescaler are cleared. The processor is put into Sleep mode with the oscillator stopped.

SUBWF	Subtract W	from f						
Syntax:	[label] SU	IBWF f,d						
Operands:	$\begin{array}{l} 0 \leq f \leq 127 \\ d \in [0,1] \end{array}$							
Operation:	(f) - (W) \rightarrow (d	estination)						
Status Affected:	C, DC, Z							
Description:	Subtract (2's complement method) W register from register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f.							
	C = 0	W > f						
	C = 1	$W \leq f$						
	DC = 0 W<3:0> > f<3:0							
	DC = 1 W<3:0> ≤ f<3:0>							

SUBWFB	Subtract W from f with Borrow
Syntax:	SUBWFB f {,d}
Operands:	$\begin{array}{l} 0\leq f\leq 127\\ d\in [0,1] \end{array}$
Operation:	$(f) - (W) - (\overline{B}) \rightarrow dest$
Status Affected:	C, DC, Z
Description:	Subtract W and the BORROW flag (CARRY) from register 'f' (2's comple- ment method). If 'd' is '0', the result is stored in W. If 'd' is '1', the result is stored back in register 'f'.

30.2 DC Characteristics: PIC16(L)F1824/8-I/E (Industrial, Extended) (Continued)

PIC16LF	1824/8	$\begin{array}{llllllllllllllllllllllllllllllllllll$						
PIC16F1	324/8	Standard Operating	d Operati g tempera	n g Condi t iture	ti ons (unl 40°C ≤ TA 40°C ≤ TA	ess otherwise stated) $A \le +85^{\circ}C$ for industrial $A \le +125^{\circ}C$ for extended		
Param	Device	Min	Tynt	Max	Units		Conditions	
No.	Characteristics		1961	max.	onto	VDD	Note	
	Supply Current (IDD) ^{(1,}	2)						
D014		_	187	250	μA	1.8	Fosc = 4 MHz	
		—	324	430	μA	3.0	Medium-Power mode	
D014			206	275	μA	1.8	Fosc = 4 MHz	
			350	450	μA	3.0	EC Oscillator mode Medium-Power mode	
		—	410	650	μA	5.0		
D015		_	6	18	μA	1.8	Fosc = 31 kHz	
		—	8	20	μA	3.0	LFINTOSC mode, $-40^{\circ}C \le IA \le +85^{\circ}C$	
D015			21	58	μA	1.8	Fosc = 31 kHz	
			27	65	μA	3.0	LFINTOSC mode, $-40^{\circ}C \le IA \le +85^{\circ}C$	
		_	28	70	μA	5.0		
D016		_	113	165	μA	1.8	Fosc = 500 kHz	
		—	140	190	μA	3.0	MFINTOSC mode	
D016			124	180	μA	1.8	Fosc = 500 kHz	
			150	210	μA	3.0		
			190	270	μA	5.0		
D017*			0.44	0.70	mA	1.8	Fosc = 8 MHz	
		_	0.70	1.10	mA	3.0		
D017*			0.48	0.75	mA	1.8	Fosc = 8 MHz	
			0.74	1.15	mA	3.0		
			0.82	1.35	mA	5.0		
D018			0.70	1.20	mA	1.8	Fosc = 16 MHz	
			1.10	1.80	mA	3.0		
D018			0.70	1.20	mA	1.8	Fosc = 16 MHz HEINTOSC mode	
			1.10	1.80	mA	3.0		
		—	1.40	2.00	mA	5.0		
D019			2.10	3.30	mA	3.0	Fosc = 32 MHz	
		—	3.20	3.60	mA	3.6		

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The test conditions for all IDD measurements in active operation mode are: OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD; MCLR = VDD; WDT disabled.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption.

3: 8 MHz internal oscillator with 4xPLL enabled.

4: 8 MHz crystal oscillator with 4xPLL enabled.

5: For RC oscillator configurations, current through REXT is not included. The current through the resistor can be extended by the formula IR = VDD/2REXT (mA) with REXT in kΩ..

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +125^{\circ}C$					
Param No.	Sym.	Characteristic	Min.	Тур†	Max.	Units	Conditions	
		Program Memory High Voltage Programming Specifications						
D110	Vінн	Voltage on MCLR/VPP/RA5 pin	8.0	—	9.0	V	(Note 3, 4)	
D111	IDDVPP	Programming/Erase Current on VPP, High Voltage Programming	—	—	10	mA		
D112	VBE	VDD for Bulk Erase	2.7	—	VDDMAX	V		
D113	VPEW	VDD for Write or Row Erase	VDDMIN	_	VDDMAX	V		
D114	IPPPGM	Programming/Erase Current on VPP, Low Voltage Programming	—	1.0	—	mA		
D115	IDDPGM	Programming/Erase Current on VDD, High or Low Voltage Programming	—	5.0	—	mA		
		Data EEPROM Memory						
D116	ED	Byte Endurance	100K	—	—	E/W	-40°C to +85°C	
D117	Vdrw	VDD for Read/Write	VDDMIN	—	VDDMAX	V		
D118	TDEW	Erase/Write Cycle Time	—	4.0	5.0	ms		
D119	TRETD	Characteristic Retention	—	40	—	Year	Provided no other specifications are violated	
D120	TREF	Number of Total Erase/Write Cycles before Refresh ⁽²⁾	1M	10M	—	E/W	-40°C to +85°C	
		Program Flash Memory						
D121	Eр	Cell Endurance	10K	_	_	E/W	-40°C to +85°C (Note 1)	
D122	VPRW	VDD for Read/Write	VDDMIN	—	VDDMAX	V		
D123	Tiw	Self-timed Write Cycle Time	—	2	2.5	ms		
D124	Tretd	Characteristic Retention	—	40	—	Year	Provided no other specifications are violated	

30.5 Memory Programming Requirements

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Self-write and Block Erase.

2: Refer to Section 11.2 "Using the Data EEPROM" for a more detailed discussion on data EEPROM endurance.

3: Required only if single-supply programming is disabled.

4: The MPLAB[®] ICD 2 does not support variable VPP output. Circuitry to limit the ICD 2 VPP voltage must be placed between the ICD 2 and target system when programming or debugging with the ICD 2.

TABLE 30-4: C	LKOUT	and I/O	TIMING	PARAM	ETERS
---------------	-------	---------	--------	-------	-------

Standard Operating Conditions (unless otherwise stated)Operating Temperature $-40^{\circ}C \le TA \le +125^{\circ}C$									
Param No.	Sym.	Characteristic	Min.	Тур†	Max.	Units	Conditions		
OS11	TosH2ckL	Fosc↑ to CLKOUT↓ ⁽¹⁾			70	ns	VDD = 3.0-5.0V		
OS12	TosH2ckH	Fosc↑ to CLKOUT ^{↑(1)}			72	ns	VDD = 3.0-5.0V		
OS13	TckL2ioV	CLKOUT↓ to Port out valid ⁽¹⁾			20	ns			
OS14	TioV2ckH	Port input valid before CLKOUT↑ ⁽¹⁾	Tosc + 200 ns	_	_	ns			
OS15	TosH2ioV	Fosc↑ (Q1 cycle) to Port out valid	—	50	70*	ns	VDD = 3.0-5.0V		
OS16	TosH2iol	Fosc↑ (Q2 cycle) to Port input invalid (I/O in hold time)	50	_	_	ns	VDD = 3.0-5.0V		
OS17	TioV2osH	Port input valid to Fosc↑ (Q2 cycle) (I/O in setup time)	20	_	_	ns			
OS18*	TioR	Port output rise time	—	40	72	ns	VDD = 1.8V		
			_	15	32		VDD = 3.0-5.0V		
OS19*	TioF	Port output fall time	_	28	55	ns	VDD = 1.8V		
			—	15	30		VDD = 3.0-5.0V		
OS20*	Tinp	INT pin input high or low time	25		_	ns			
OS21*	Tioc	Interrupt-on-change new input level time	25	—	—	ns			

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated.

Note 1: Measurements are taken in RC mode where CLKOUT output is 4 x Tosc.













TABLE 30-21: DC CHARACTERISTICS FOR IPD SPECIFICATIONS FOR PIC16F1824/8-H (High Temp.)

PIC16F	1824/8	Standard Operating Conditions: (unless otherwise stated) Operating Temperature: $-40^{\circ}C \le TA \le +150^{\circ}C$ for High Temperature							
Param Device Observation			-	Massa	l les ltes	Condition			
No.	Device Characteristics	Min.	тур.	wax.	Units	Vdd	Note		
	Power-Down Base Curren	t (IPD) ⁽²⁾		•	•				
D022		—	_	60	μA	3.0	WDT, BOR, FVR, and T1OSC		
		—		75	μA	5.0	disabled, all Peripherals Inactive		
D023			_	60	μΑ	3.0	LPWDT Current (Note 1)		
		—		75	μA	5.0			
D023A			_	75	μA	3.0	FVR current (Note 1)		
		—	—	120	μA	5.0			
D024			_	55	μA	3.0	BOR Current (Note 1)		
		—	—	75	μA	5.0			
D025			—	65	μA	3.0	T1OSC Current (Note 1)		
		—	—	80	μA	5.0			
D026			_	55	μA	3.0	A/D Current (Note 1, Note 3),		
		—	_	70	μA	5.0	no conversion in progress		
D027		_	_	_	_	_	Cap Sense module is not intended for use in high temperature devices		
D028			_	70	μA	3.0	Comparator Current, Low-		
		—	_	90	μA	5.0	Power mode (Note 1)		
D028B		—	_	100	μA	3.0	Comparator Current, High-		
		_	_	115	μA	5.0	Power mode (Note 1)		

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The peripheral current is the sum of the base IDD or IPD and the additional current consumed when this peripheral is enabled. The peripheral Δ current can be determined by subtracting the base IDD or IPD current from this limit. Max values should be used when calculating total current consumption.

2: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins set to inputs state and tied to VDD.

3: A/D oscillator source is FRC.

FIGURE 31-33: IPD, CAPACITIVE SENSING (CPS) MODULE, MEDIUM-CURRENT RANGE, CPSRM = 0, PIC16LF1824/8 ONLY



FIGURE 31-34: IPD, CAPACITIVE SENSING (CPS) MODULE, MEDIUM-CURRENT RANGE, CPSRM = 0, PIC16F1824/8 ONLY



16-Lead Ultra Thin Plastic Quad Flat, No Lead Package (JQ) - 4x4x0.5 mm Body [UQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	MILLIMETERS					
Dimension	MIN	NOM	MAX			
Number of Pins	N	16				
Pitch	е		0.65 BSC			
Overall Height	Α	0.45	0.50	0.55		
Standoff	A1	0.00	0.02	0.05		
Terminal Thickness	A3	0.127 REF				
Overall Width	E	4.00 BSC				
Exposed Pad Width	E2	2.50 2.60 2.70				
Overall Length	D	4.00 BSC				
Exposed Pad Length	D2	2.50 2.60 2.70				
Terminal Width	b	0.25 0.30 0.35				
Terminal Length	L	0.30 0.40 0.50				
Terminal-to-Exposed-Pad	К	0.20	-	-		

Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. Package is saw singulated
- 3. Dimensioning and tolerancing per ASME Y14.5M
 - BSC: Basic Dimension. Theoretically exact value shown without tolerances. REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-257A Sheet 2 of 2