Renesas Electronics America Inc - R5F21346WJFP#U0 Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	CANbus, I²C, IEBus, LINbus, SIO, SSU, UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	43
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	2.5K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21346wjfp-u0

Table 1.3 Specifications for R8C/34X Group (1)

Item	Function	Specification
CPU	Central processing unit	R8C CPU core • Number of fundamental instructions: 89 • Minimum instruction execution time: 50 ns (f(XIN) = 20 MHz, VCC = 2.7 to 5.5 V) • Multiplier: 16 bits × 16 bits → 32 bits • Multiply-accumulate instruction: 16 bits × 16 bits + 32 bits → 32 bits • Operating mode: Single-chip mode (address space: 1 Mbyte)
Memory	ROM, RAM, Data flash	Refer to **Table 1.10 Product List for R8C/34X Group**.
Power Supply Voltage Detection	Voltage detection circuit	• Power-on reset • Voltage detection 3 (detection level of voltage detection 1 selectable)
I/O Ports	Programmable I/O ports	• Input-only: 1 pin • CMOS I/O ports: 43, selectable pull-up resistor
Clock	Clock generation circuits	3 circuits: XIN clock oscillation circuit (with on-chip feedback resistor), High-speed on-chip oscillator (with frequency adjustment function), Low-speed on-chip oscillator • Oscillation stop detection: XIN clock oscillation stop detection function • Frequency divider circuit: Dividing selectable 1, 2, 4, 8, and 16 • Low power consumption modes: Standard operating mode (high-speed clock, high-speed on-chip oscillator, low-speed on-chip oscillator), wait mode, stop mode
Interrupts		• Interrupt vectors: 69 • External: 9 sources ($\overline{\text{INT}}$ × 5, key input × 4) • Priority levels: 7 levels
Watchdog Timer		• 14 bits × 1 (with prescaler) • Reset start selectable • Low-speed on-chip oscillator for watchdog timer selectable
DTC (Data Transfer Controller)		• 1 channel • Activation sources: 31 • Transfer modes: 2 (normal mode, repeat mode)
Timer	Timer RA	8 bits (with 8-bit prescaler) × 1 Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode
	Timer RB	8 bits (with 8-bit prescaler) × 1 Timer mode (period timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode
	Timer RC	16 bits (with 4 capture/compare registers) × 1 Timer mode (input capture function, output compare function), PWM mode (output 3 pins), PWM2 mode (PWM output pin)
	Timer RD	16 bits (with 4 capture/compare registers) × 2 Timer mode (input capture function, output compare function), PWM mode (output 6 pins), reset synchronous PWM mode (output three-phase waveforms (6 pins), sawtooth wave modulation), complementary PWM mode (output three-phase waveforms (6 pins), triangular wave modulation), PWM3 mode (PWM output 2 pins with fixed period)
	Timer RE	8 bits × 1 Output compare mode

Table 1.4 Specifications for R8C/34X Group (2)

Item	Function	Specification
Serial Interface	UART0	1 channel Clock synchronous serial I/O, UART
	UART2	1 channel Clock synchronous serial I/O, UART, I^2C mode (I^2C-bus), IE mode (IEBus), multiprocessor communication function
Synchronous Serial Communication Unit (SSU)		1 channel
LIN Module		Hardware LIN: 1 (timer RA, UART0)
CAN Module		1 channel, 16 Mailboxes (conforms to the ISO 11898-1)
A/D Converter		10-bit resolution × 12 channels, includes sample and hold function, with sweep mode
Flash Memory		• Programming and erasure voltage: VCC = 2.7 to 5.5 V • Programming and erasure endurance: 100 times (program ROM) • Program security: ROM code protect, ID code check • Debug functions: On-chip debug, on-board flash rewrite function
Operating Frequency/Supply Voltage		f(XIN) = 20 MHz (VCC = 2.7 to 5.5 V)
Current Consumption		Typ. 7 mA (VCC = 5.0 V, f(XIN) = 20 MHz)
Operating Ambient Temperature		-40 to 85°C (J version) -40 to 125°C (K version) (1)
Package		48-pin LQFP Package code: PLQP0048KB-A (previous code: 48P6Q-A)

Note:
1. Specify the K version if K version functions are to be used.

Table 1.10 Product List for R8C/34X Group **Current of Jan 2013**

Part No.	ROM Capacity Program ROM	RAM Capacity	Package Type	Remarks
R5F21346XJFP	32 Kbytes	2.5 Kbytes	PLQP0048KB-A	J version
R5F21347XJFP	48 Kbytes	4 Kbytes	PLQP0048KB-A	
R5F21348XJFP	64 Kbytes	6 Kbytes	PLQP0048KB-A	
R5F2134AXJFP	96 Kbytes	8 Kbytes	PLQP0048KB-A	
R5F2134CXJFP	128 Kbytes	10 Kbytes	PLQP0048KB-A	
R5F21346XKFP	32 Kbytes	2.5 Kbytes	PLQP0048KB-A	K version
R5F21347XKFP	48 Kbytes	4 Kbytes	PLQP0048KB-A	
R5F21348XKFP	64 Kbytes	6 Kbytes	PLQP0048KB-A	
R5F2134AXKFP	96 Kbytes	8 Kbytes	PLQP0048KB-A	
R5F2134CXKFP	128 Kbytes	10 Kbytes	PLQP0048KB-A	

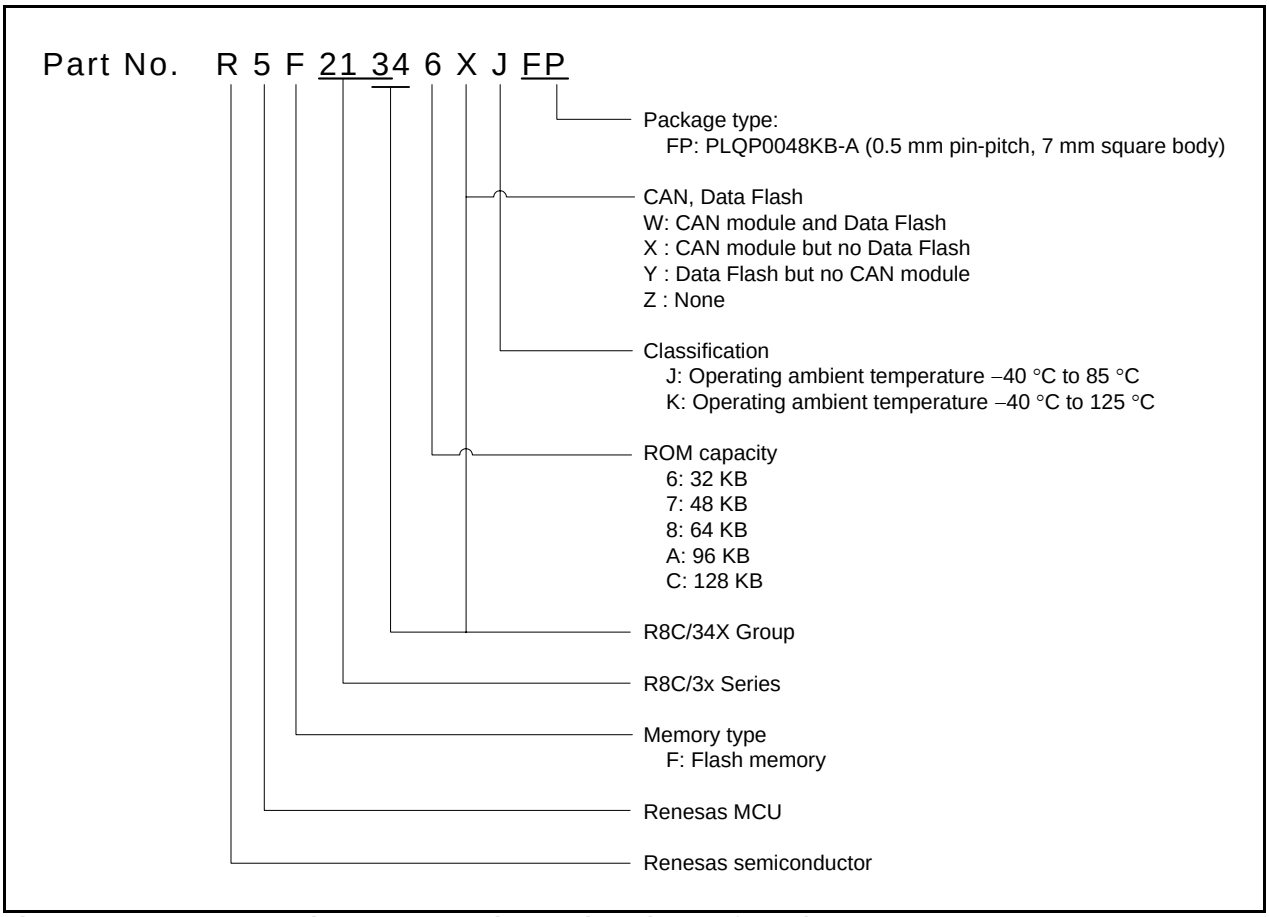


Figure 1.2 Part Number, Memory Size, and Package of R8C/34X Group

Table 1.11 Product List for R8C/34Y Group **Current of Jan 2013**

Part No.	ROM Capacity		RAM Capacity	Package Type	Remarks
	Program ROM	Data flash			
R5F21346YJFP	32 Kbytes	1 Kbyte × 4	2.5 Kbytes	PLQP0048KB-A	J version
R5F21347YJFP	48 Kbytes	1 Kbyte × 4	4 Kbytes	PLQP0048KB-A	
R5F21348YJFP	64 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0048KB-A	
R5F2134AYJFP	96 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0048KB-A	
R5F2134CYJFP	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0048KB-A	
R5F21346YKFP	32 Kbytes	1 Kbyte × 4	2.5 Kbytes	PLQP0048KB-A	K version
R5F21347YKFP	48 Kbytes	1 Kbyte × 4	4 Kbytes	PLQP0048KB-A	
R5F21348YKFP	64 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0048KB-A	
R5F2134AYKFP	96 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0048KB-A	
R5F2134CYKFP	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0048KB-A	

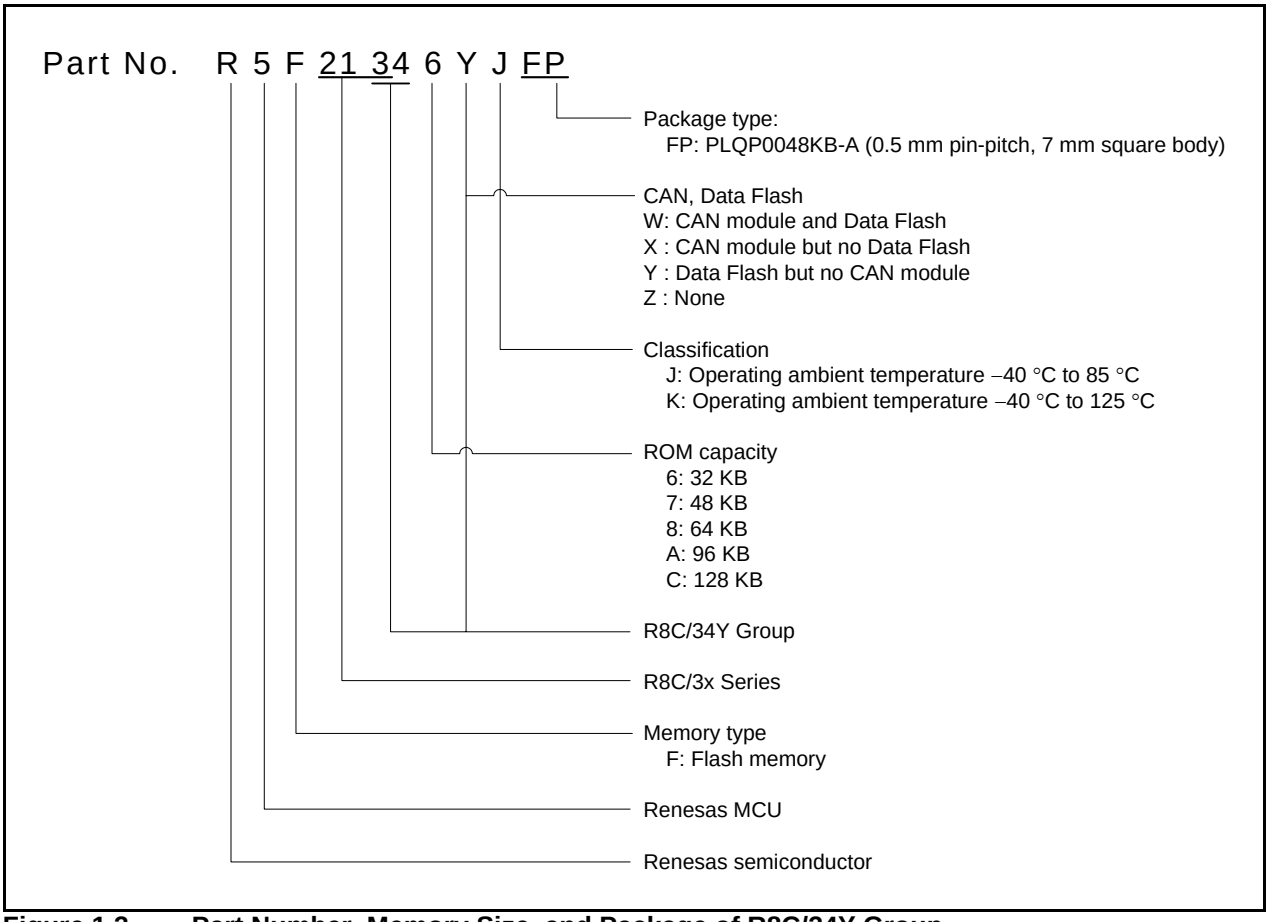


Figure 1.3 Part Number, Memory Size, and Package of R8C/34Y Group

1.3 Block Diagram

Figure 1.5 shows a Block Diagram.

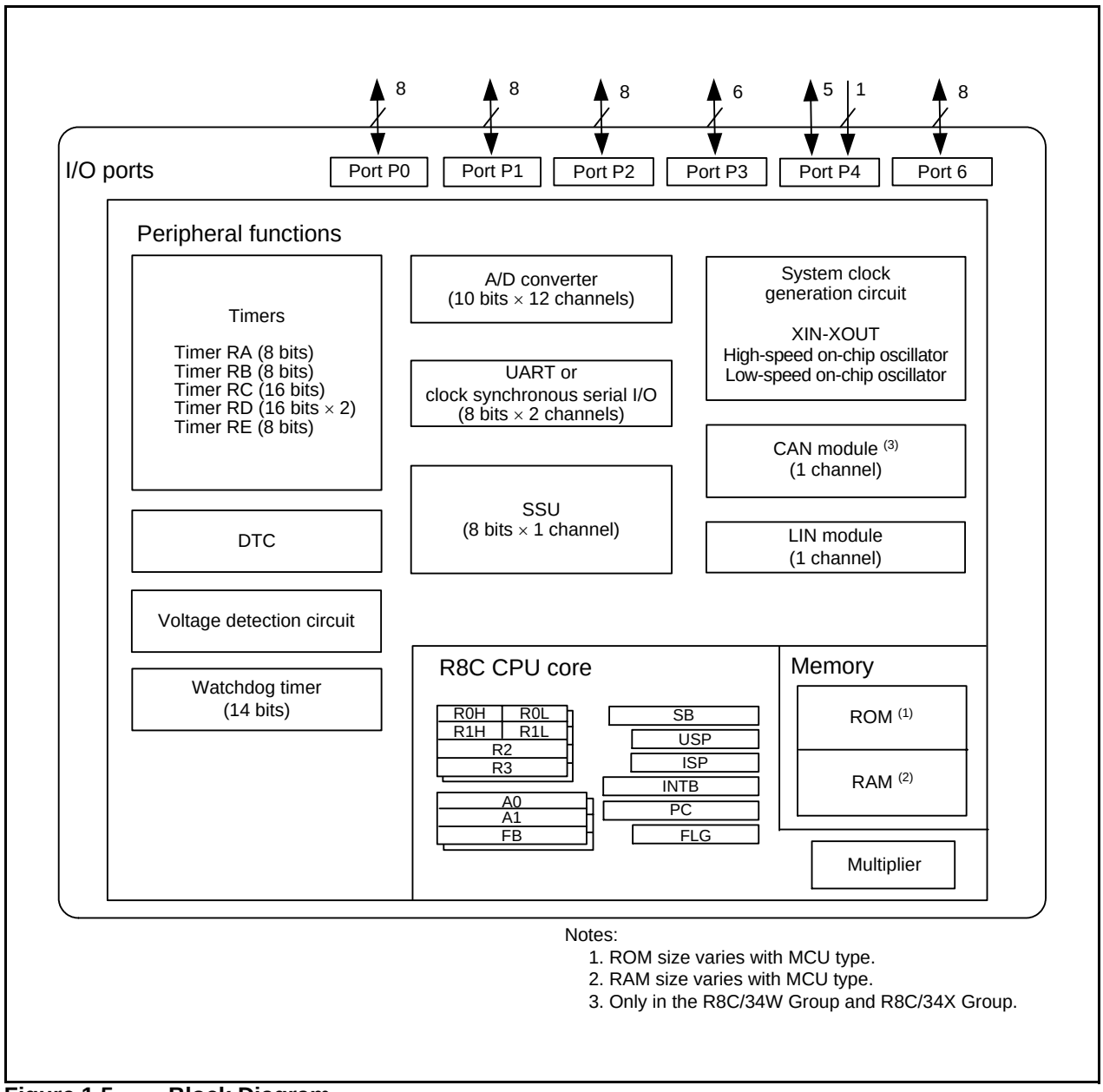
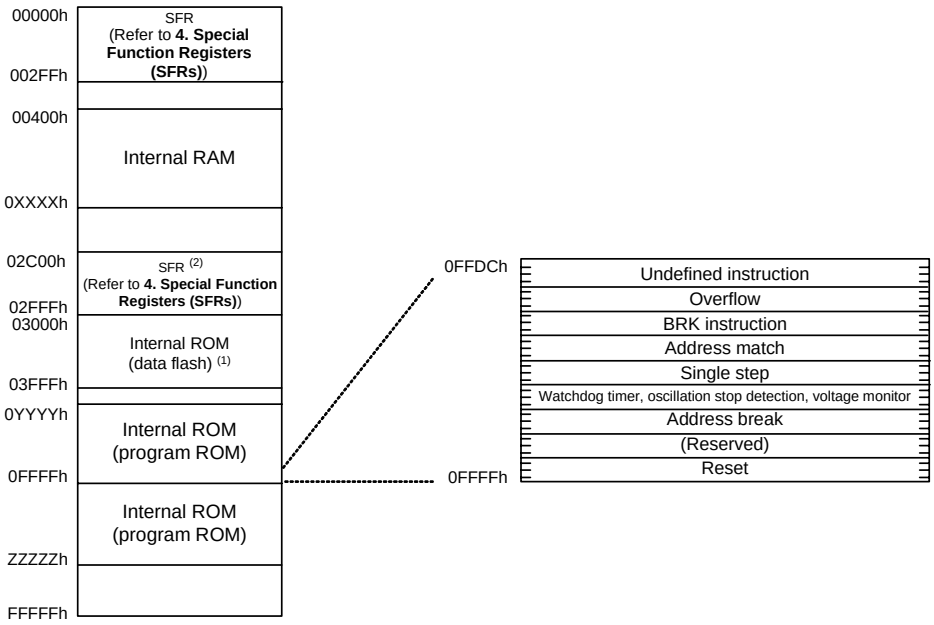


Figure 1.5 Block Diagram

3. Memory

3.1 R8C/34W Group

Figure 3.1 is a Memory Map of R8C/34W Group. The R8C/34W Group has a 1-Mbyte address space from addresses 00000h to FFFFFh. The internal ROM (program ROM) is allocated lower addresses, beginning with address 0FFFFh. For example, a 48-Kbyte internal ROM area is allocated addresses 04000h to 0FFFFh.
The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. The starting address of each interrupt routine is stored here.
The internal ROM (data flash) is allocated addresses 03000h to 03FFFh.
The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 4-Kbyte internal RAM area is allocated addresses 00400h to 013FFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.
Special function registers (SFRs) are allocated addresses 00000h to 002FFh and 02C00h to 02FFFh (the SFR areas for the CAN, DTC, and other modules). Peripheral function control registers are allocated here. All unallocated spaces within the SFRs are reserved and cannot be accessed by users.



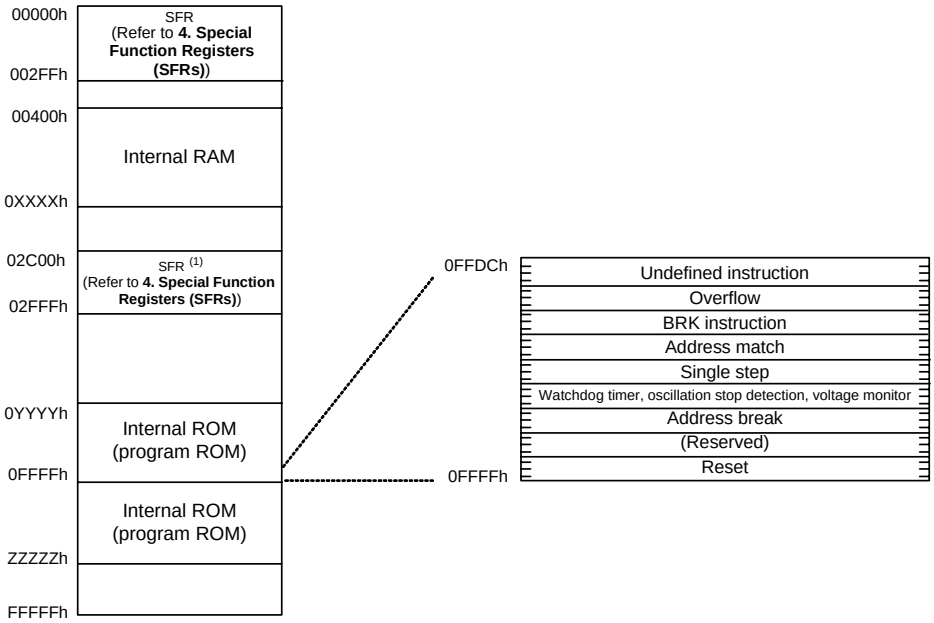
Notes:
1. The Data Flash memory indicates blocks A (1 Kbyte), B (1 Kbyte), C (1 Kbyte), and D (1 Kbyte).
2. The SFR areas for the CAN, DTC and other modules are allocated to addresses 02C00h to 02FFFh.
3. The blank areas are reserved and cannot be accessed by users.

Part Number	Internal ROM			Internal RAM	
	Size	Address 0YYYYh	Address ZZZZZh	Size	Address 0XXXXh
R5F21346WJFP, R5F21346WKFP	32 Kbytes	08000h	—	2.5 Kbytes	00DFFh
R5F21347WJFP, R5F21347WKFP	48 Kbytes	04000h	—	4 Kbytes	013FFh
R5F21348WJFP, R5F21348WKFP	64 Kbytes	04000h	13FFFh	6 Kbytes	01BFFh
R5F2134AWJFP, R5F2134AWKFP	96 Kbytes	04000h	1BFFFh	8 Kbytes	023FFh
R5F2134CWJFP, R5F2134CWKFP	128 Kbytes	04000h	23FFFh	10 Kbytes	02BFFh

Figure 3.1 Memory Map of R8C/34W Group

3.4 R8C/34Z Group

Figure 3.4 is a Memory Map of R8C/34Z Group. The R8C/34Z Group has a 1-Mbyte address space from addresses 00000h to FFFFFh. The internal ROM (program ROM) is allocated lower addresses, beginning with address 0FFFFh. For example, a 48-Kbyte internal ROM area is allocated addresses 04000h to 0FFFFh.
The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. The starting address of each interrupt routine is stored here.
The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 4-Kbyte internal RAM area is allocated addresses 00400h to 013FFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.
Special function registers (SFRs) are allocated addresses 00000h to 002FFh and 02C00h to 02FFFh (the SFR areas for the DTC and other modules). Peripheral function control registers are allocated here. All unallocated spaces within the SFRs are reserved and cannot be accessed by users.



Notes:
1. The SFR areas for the DTC and other modules are allocated to addresses 02C00h to 02FFFh.
2. The blank areas are reserved and cannot be accessed by users.

Part Number	Internal ROM			Internal RAM	
	Size	Address 0YYYYh	Address ZZZZZh	Size	Address 0XXXXh
R5F21346ZJFP, R5F21346ZKFP	32 Kbytes	08000h	—	2.5 Kbytes	00DFFh
R5F21347ZJFP, R5F21347ZKFP	48 Kbytes	04000h	—	4 Kbytes	013FFh
R5F21348ZJFP, R5F21348ZKFP	64 Kbytes	04000h	13FFFh	6 Kbytes	01BFFh
R5F2134AZJFP, R5F2134AZKFP	96 Kbytes	04000h	1BFFFh	8 Kbytes	023FFh
R5F2134CZJFP, R5F2134CZKFP	128 Kbytes	04000h	23FFFh	10 Kbytes	02BFFh

Figure 3.4 Memory Map of R8C/34Z Group

Table 4.4 SFR Information (4) (1)

Address	Register	Symbol	After reset
00C0h	A/D Register 0	AD0	XXh
00C1h			000000XXb
00C2h	A/D Register 1	AD1	XXh
00C3h			000000XXb
00C4h	A/D Register 2	AD2	XXh
00C5h			000000XXb
00C6h	A/D Register 3	AD3	XXh
00C7h			000000XXb
00C8h	A/D Register 4	AD4	XXh
00C9h			000000XXb
00CAh	A/D Register 5	AD5	XXh
00CBh			000000XXb
00CCh	A/D Register 6	AD6	XXh
00CDh			000000XXb
00CEh	A/D Register 7	AD7	XXh
00CFh			000000XXb
00D0h			
00D1h			
00D2h			
00D3h			
00D4h	A/D Mode Register	ADMOD	00h
00D5h	A/D Input Select Register	ADINSEL	11000000b
00D6h	A/D Control Register 0	ADCON0	00h
00D7h	A/D Control Register 1	ADCON1	00h
00D8h			
00D9h			
00DAh			
00DBh			
00DCh			
00DDh			
00DEh			
00DFh			
00E0h	Port P0 Register	P0	XXh
00E1h	Port P1 Register	P1	XXh
00E2h	Port P0 Direction Register	PD0	00h
00E3h	Port P1 Direction Register	PD1	00h
00E4h	Port P2 Register	P2	XXh
00E5h	Port P3 Register	P3	XXh
00E6h	Port P2 Direction Register	PD2	00h
00E7h	Port P3 Direction Register	PD3	00h
00E8h	Port P4 Register	P4	XXh
00E9h			
00EAh	Port P4 Direction Register	PD4	00h
00EBh			
00ECh	Port P6 Register	P6	XXh
00EDh			
00EEh	Port P6 Direction Register	PD6	00h
00EFh			
00F0h			
00F1h			
00F2h			
00F3h			
00F4h			
00F5h			
00F6h			
00F7h			
00F8h			
00F9h			
00FAh			
00FBh			
00FCh			
00FDh			
00FEh			
00FFh			

X: Undefined
Note:
1. The blank areas are reserved and cannot be accessed by users.

Table 4.6 SFR Information (6) (1)

Address	Register	Symbol	After reset
0140h	Timer RD Control Register 0	TRDCR0	00h
0141h	Timer RD I/O Control Register A0	TRDIORA0	10001000b
0142h	Timer RD I/O Control Register C0	TRDIORC0	10001000b
0143h	Timer RD Status Register 0	TRDSR0	11100000b
0144h	Timer RD Interrupt Enable Register 0	TRDIER0	11100000b
0145h	Timer RD PWM Mode Output Level Control Register 0	TRDPOCR0	11111000b
0146h	Timer RD Counter 0	TRD0	00h
0147h			00h
0148h	Timer RD General Register A0	TRDGRA0	FFh
0149h			FFh
014Ah	Timer RD General Register B0	TRDGRB0	FFh
014Bh			FFh
014Ch	Timer RD General Register C0	TRDGRC0	FFh
014Dh			FFh
014Eh	Timer RD General Register D0	TRDGRD0	FFh
014Fh			FFh
0150h	Timer RD Control Register 1	TRDCR1	00h
0151h	Timer RD I/O Control Register A1	TRDIORA1	10001000b
0152h	Timer RD I/O Control Register C1	TRDIORC1	10001000b
0153h	Timer RD Status Register 1	TRDSR1	11000000b
0154h	Timer RD Interrupt Enable Register 1	TRDIER1	11100000b
0155h	Timer RD PWM Mode Output Level Control Register 1	TRDPOCR1	11111000b
0156h	Timer RD Counter 1	TRD1	00h
0157h			00h
0158h	Timer RD General Register A1	TRDGRA1	FFh
0159h			FFh
015Ah	Timer RD General Register B1	TRDGRB1	FFh
015Bh			FFh
015Ch	Timer RD General Register C1	TRDGRC1	FFh
015Dh			FFh
015Eh	Timer RD General Register D1	TRDGRD1	FFh
015Fh			FFh
0160h			
0161h			
0162h			
0163h			
0164h			
0165h			
0166h			
0167h			
0168h			
0169h			
016Ah			
016Bh			
016Ch			
016Dh			
016Eh			
016Fh			
0170h			
0171h			
0172h			
0173h			
0174h			
0175h			
0176h			
0177h			
0178h			
0179h			
017Ah			
017Bh			
017Ch			
017Dh			
017Eh			
017Fh			

X: Undefined
Note:
1. The blank areas are reserved and cannot be accessed by users.

Table 4.9 SFR Information (9) (1)

Address	Register	Symbol	After reset
2C00h	DTC Transfer Vector Area		XXh
2C01h	DTC Transfer Vector Area		XXh
2C02h	DTC Transfer Vector Area		XXh
2C03h	DTC Transfer Vector Area		XXh
2C04h	DTC Transfer Vector Area		XXh
2C05h			
2C06h			
2C07h			
2C08h	DTC Transfer Vector Area		XXh
2C09h	DTC Transfer Vector Area		XXh
2C0Ah	DTC Transfer Vector Area		XXh
:	DTC Transfer Vector Area		XXh
:	DTC Transfer Vector Area		XXh
2C3Ah			
2C3Bh			
2C3Ch			
2C3Dh			
2C3Eh			
2C3Fh			
2C40h	DTC Control Data 0	DTCD0	XXh
2C41h			XXh
2C42h			XXh
2C43h			XXh
2C44h			XXh
2C45h			XXh
2C46h			XXh
2C47h			XXh
2C48h	DTC Control Data 1	DTCD1	XXh
2C49h			XXh
2C4Ah			XXh
2C4Bh			XXh
2C4Ch			XXh
2C4Dh			XXh
2C4Eh			XXh
2C4Fh			XXh
2C50h	DTC Control Data 2	DTCD2	XXh
2C51h			XXh
2C52h			XXh
2C53h			XXh
2C54h			XXh
2C55h			XXh
2C56h			XXh
2C57h			XXh
2C58h	DTC Control Data 3	DTCD3	XXh
2C59h			XXh
2C5Ah			XXh
2C5Bh			XXh
2C5Ch			XXh
2C5Dh			XXh
2C5Eh			XXh
2C5Fh			XXh
2C60h	DTC Control Data 4	DTCD4	XXh
2C61h			XXh
2C62h			XXh
2C63h			XXh
2C64h			XXh
2C65h			XXh
2C66h			XXh
2C67h			XXh
2C68h	DTC Control Data 5	DTCD5	XXh
2C69h			XXh
2C6Ah			XXh
2C6Bh			XXh
2C6Ch			XXh
2C6Dh			XXh
2C6Eh			XXh
2C6Fh			XXh

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.10 SFR Information (10) (1)

Address	Register	Symbol	After reset
2C70h	DTC Control Data 6	DTCD6	XXh
2C71h			XXh
2C72h			XXh
2C73h			XXh
2C74h			XXh
2C75h			XXh
2C76h			XXh
2C77h			XXh
2C78h	DTC Control Data 7	DTCD7	XXh
2C79h			XXh
2C7Ah			XXh
2C7Bh			XXh
2C7Ch			XXh
2C7Dh			XXh
2C7Eh			XXh
2C7Fh			XXh
2C80h	DTC Control Data 8	DTCD8	XXh
2C81h			XXh
2C82h			XXh
2C83h			XXh
2C84h			XXh
2C85h			XXh
2C86h			XXh
2C87h			XXh
2C88h	DTC Control Data 9	DTCD9	XXh
2C89h			XXh
2C8Ah			XXh
2C8Bh			XXh
2C8Ch			XXh
2C8Dh			XXh
2C8Eh			XXh
2C8Fh			XXh
2C90h	DTC Control Data 10	DTCD10	XXh
2C91h			XXh
2C92h			XXh
2C93h			XXh
2C94h			XXh
2C95h			XXh
2C96h			XXh
2C97h			XXh
2C98h	DTC Control Data 11	DTCD11	XXh
2C99h			XXh
2C9Ah			XXh
2C9Bh			XXh
2C9Ch			XXh
2C9Dh			XXh
2C9Eh			XXh
2C9Fh			XXh
2CA0h	DTC Control Data 12	DTCD12	XXh
2CA1h			XXh
2CA2h			XXh
2CA3h			XXh
2CA4h			XXh
2CA5h			XXh
2CA6h			XXh
2CA7h			XXh
2CA8h	DTC Control Data 13	DTCD13	XXh
2CA9h			XXh
2CAAh			XXh
2CABh			XXh
2CACh			XXh
2CADh			XXh
2CAEh			XXh
2CAFh			XXh

X: Undefined
Note:
1. The blank areas are reserved and cannot be accessed by users.

Table 4.15 SFR Information (15) (1)

Address	Register	Symbol	After reset
2EB0h	CAN0 Mailbox11 : Message ID	C0MB11	XXh
2EB1h			XXh
2EB2h			XXh
2EB3h			XXh
2EB4h			
2EB5h	CAN0 Mailbox11 : Data length		XXh
2EB6h	CAN0 Mailbox11 : Data field		XXh
2EB7h			XXh
2EB8h			XXh
2EB9h			XXh
2EBAh			XXh
2EBBh			XXh
2EBCh			XXh
2EBDh			XXh
2EBEh	CAN0 Mailbox11 : Time stamp		XXh
2EBFh			XXh
2EC0h	CAN0 Mailbox12 : Message ID	C0MB12	XXh
2EC1h			XXh
2EC2h			XXh
2EC3h			XXh
2EC4h			
2EC5h	CAN0 Mailbox12 : Data length		XXh
2EC6h	CAN0 Mailbox12 : Data field		XXh
2EC7h			XXh
2EC8h			XXh
2EC9h			XXh
2ECAh			XXh
2ECBh			XXh
2ECCh			XXh
2ECDh			XXh
2ECEh	CAN0 Mailbox12 : Time stamp		XXh
2ECFh			XXh
2ED0h	CAN0 Mailbox13 : Message ID	C0MB13	XXh
2ED1h			XXh
2ED2h			XXh
2ED3h			XXh
2ED4h			
2ED5h	CAN0 Mailbox13 : Data length		XXh
2ED6h	CAN0 Mailbox13 : Data field		XXh
2ED7h			XXh
2ED8h			XXh
2ED9h			XXh
2EDAh			XXh
2EDBh			XXh
2EDCh			XXh
2EDDh			XXh
2EDEh	CAN0 Mailbox13 : Time stamp		XXh
2EDFh			XXh
2EE0h	CAN0 Mailbox14 : Message ID	C0MB14	XXh
2EE1h			XXh
2EE2h			XXh
2EE3h			XXh
2EE4h			
2EE5h	CAN0 Mailbox14 : Data length		XXh
2EE6h	CAN0 Mailbox14 : Data field		XXh
2EE7h			XXh
2EE8h			XXh
2EE9h			XXh
2EEAh			XXh
2EEBh			XXh
2EECh			XXh
2EEDh			XXh
2EEEh	CAN0 Mailbox14 : Time stamp		XXh
2EEFh			XXh

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

5. Electrical Characteristics

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter	Condition	Rated Value	Unit
V_{CC}/AV_{CC}	Supply voltage		–0.3 to 6.5	V
V_I	Input voltage (1)		–0.3 to V_{CC} + 0.3	V
IIN	Input current (1)	(2, 3, 4)	–4 to 4	mA
V_O	Output voltage		–0.3 to V_{CC} + 0.3	V
P_d	Power dissipation	–40 °C ≤ T_{opr} < 85 °C	300	mW
		85 °C ≤ T_{opr} < 125 °C	125	mW
T_{opr}	Operating ambient temperature		–40 to 85 (J version) / –40 to 125 (K version)	°C
T_{stg}	Storage temperature		–65 to 150	°C

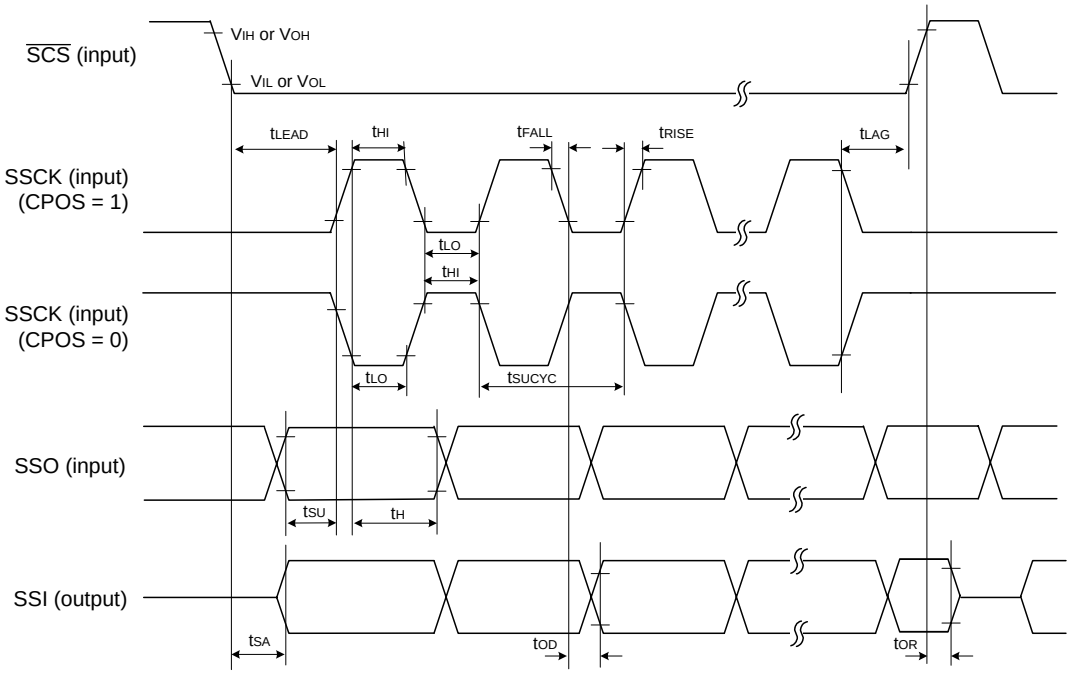
Notes:
1. Meet the specified range for the input voltage or the input current.
2. Applicable ports: P0 to P2, P3_0, P3_1, P3_3 to P3_5, P3_7, P4_3 to P4_5, P6
3. The total input current must be 12 mA or less.
4. Even if no voltage is supplied to Vcc, the input current may cause the MCU to be powered on and operate. When a voltage is supplied to Vcc, the input current may cause the supply voltage to rise. Since operations in any cases other than above are not guaranteed, use the power supply circuit in the system to ensure the supply voltage for the MCU is stable within the specified range.

Table 5.14 Timing Requirements of SSU (1)

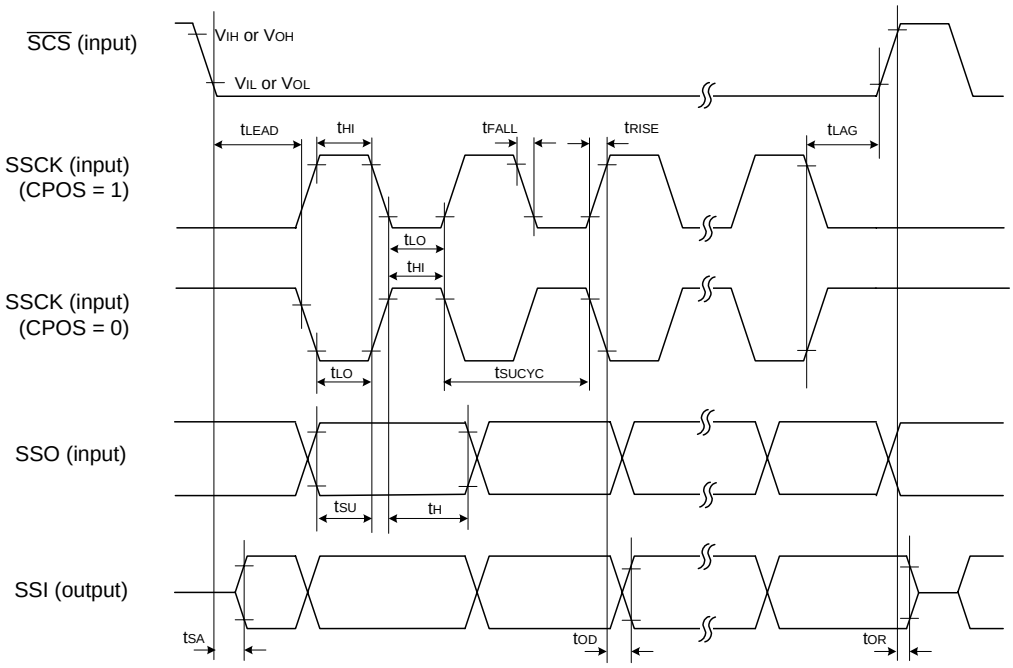
Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
t_{SUCYC}	SSCK clock cycle time			4	–	–	t_{CYC} (2)
t_{HI}	SSCK clock “H” width			0.4	–	0.6	t_{SUCYC}
t_{LO}	SSCK clock “L” width			0.4	–	0.6	t_{SUCYC}
t_{RISE}	SSCK clock rising time	Master		–	–	1	t_{CYC} (2)
		Slave		–	–	1	µs
t_{FALL}	SSCK clock falling time	Master		–	–	1	t_{CYC} (2)
		Slave		–	–	1	µs
t_{SU}	SSO, SSI data input setup time			100	–	–	ns
t_{H}	SSO, SSI data input hold time			1	–	–	t_{CYC} (2)
t_{LEAD}	$\overline{SCS}$ setup time	Slave		$1t_{CYC}$ + 50	–	–	ns
t_{LAG}	$\overline{SCS}$ hold time	Slave		$1t_{CYC}$ + 50	–	–	ns
t_{OD}	SSO, SSI data output delay time			–	–	1	t_{CYC} (2)
t_{SA}	SSI slave access time		2.7 V ≤ V_{CC} ≤ 5.5 V	–	–	$1.5t_{CYC}$ + 100	ns
t_{OR}	SSI slave out open time		2.7 V ≤ V_{CC} ≤ 5.5 V	–	–	$1.5t_{CYC}$ + 100	ns

Notes:
1. The measurement condition is V_{CC} = 2.7 to 5.5 V and T_{opr} = –40 to 85°C (J version) / –40 to 125°C (K version).
2. $1t_{CYC}$ = 1/f1(s)

4-Wire Bus Communication Mode, Slave, CPHS = 1



4-Wire Bus Communication Mode, Slave, CPHS = 0



CPHS, CPOS: Bits in SSMR register

Figure 5.5 I/O Timing of SSU (Slave)

Table 5.16 Electrical Characteristics (2) [3.3 V ≤ Vcc ≤ 5.5 V]
(Topr = –40 to 85°C (J version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
Icc	Power supply current (Vcc = 3.3 to 5.5 V) Single-chip mode, output pins are open, other pins are Vss	High-speed clock mode (1)	XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	7.0	15	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	5.6	12.5	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	3.6	–	mA
			XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	3.0	–	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	2.2	–	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	1.5	–	mA
		High-speed on-chip oscillator mode (1)	XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	7.0	15	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	3.0	–	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR27 = 1, VCA20 = 0	–	90	180	µA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	15	110	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	5	100	µA
		Stop mode	XIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	2.0	5.0	µA
			XIN clock off, Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	15.0	–	µA

Note:
1. The typical value (Typ.) indicates the current value when the CPU and the memory operate.
The maximum value (Max.) indicates the current when the CPU, the memory, and the peripheral functions operate and the flash memory is programmed/erased.

Timing Requirements
(Unless Otherwise Specified: Vcc = 5 V, Vss = 0 V at Topr = –40°C to 85°C (J ver)/–40°C to 125°C (K ver))

Table 5.18 External clock input (XOUT)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XOUT)}$	XOUT input cycle time	50	–	ns
$t_{WH(XOUT)}$	XOUT input “H” width	24	–	ns
$t_{WL(XOUT)}$	XOUT input “L” width	24	–	ns

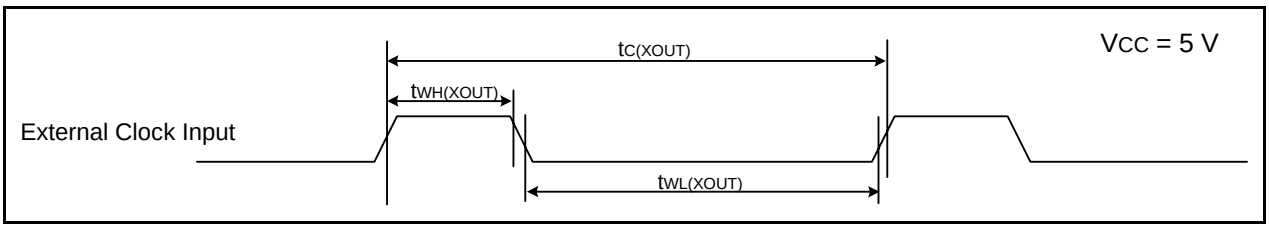


Figure 5.7 External Clock Input Timing Diagram when Vcc = 5 V

Table 5.19 TRAIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	100	–	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	40	–	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	40	–	ns

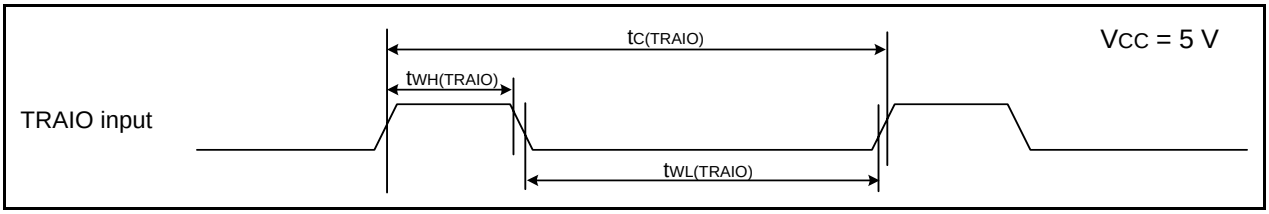


Figure 5.8 TRAIO Input Timing Diagram when Vcc = 5 V

Table 5.24 Electrical Characteristics (4) [2.7 V ≤ Vcc < 3.3 V] (Topr = –40 to 125°C (K version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
Icc	Power supply current (Vcc = 2.7 to 3.3 V) Single-chip mode, output pins are open, other pins are Vss	High-speed clock mode (1)	XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	7.0	14.5	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	5.6	12.0	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	3.6	–	mA
			XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	3.0	–	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	2.2	–	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	1.5	–	mA
		High-speed on-chip oscillator mode (1)	XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	7.0	14.5	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	3.0	–	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR27 = 1, VCA20 = 0	–	85	390	µA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	15	320	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	5	310	µA
		Stop mode	XIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	2.0	5.0	µA
			XIN clock off, Topr = 125°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	55.0	–	µA

Note:
1. The typical value (Typ.) indicates the current value when the CPU and the memory operate.
The maximum value (Max.) indicates the current when the CPU, the memory, and the peripheral functions operate and the flash memory is programmed/erased.

REVISION HISTORY	R8C/34W Group, R8C/34X Group, R8C/34Y Group, R8C/34Z Group Datasheet

Rev.	Date	Description	
		Page	Summary
0.10	Apr 09, 2010	—	First Edition issued
1.00	Nov 24, 2010	All	"Preliminary" and "Under development" deleted
		14	Figure 1.5 "Voltage detection circuit" added
		28	Table 4.2 006Ch, 006Dh, 0072h, and 0073h revised
		38 to 43	Tables 4.12 to 4.17 "After Reset" notation revised
		46	Table 5.3 "VI > VSS" → "VI < VSS", Note 1 revised
		47	Table 5.4 t_{SAMP} revised
		48	Table 5.5 "1,000 times" → "100 times"
		51	Figure 5.3 Note 1 revised
		57	Table 5.15 "V_{CC} = 5.0 V" added
		61	Table 5.20 revised
		62	Table 5.22 "V_{CC} = 3.0 V" added, "[2.7 V ≤ Vcc ≤ 4.2 V]" → "[2.7 V ≤ Vcc < 4.2 V]"
		63, 64	Tables 5.23 and 5.24 "[2.7 V ≤ Vcc ≤ 3.3 V]" → "[2.7 V ≤ Vcc < 3.3 V]"
		65	Table 5.27 revised
1.10	Jan 31, 2013	15	Figure 1.6 revised

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