Renesas Electronics America Inc - R5F21346XJFP#U0 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	CANbus, I²C, LINbus, SIO, SSU, UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	43
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2.5K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21346xjfp-u0

Table 1.6 Specifications for R8C/34Y Group (2)

Item	Function	Specification
Serial Interface	UART0	1 channel Clock synchronous serial I/O, UART
	UART2	1 channel Clock synchronous serial I/O, UART, I^2C mode (I^2C-bus), IE mode (IEBus), multiprocessor communication function
Synchronous Serial Communication Unit (SSU)		1 channel
LIN Module		Hardware LIN: 1 (timer RA, UART0)
A/D Converter		10-bit resolution × 12 channels, includes sample and hold function, with sweep mode
Flash Memory		• Programming and erasure voltage: VCC = 2.7 to 5.5 V • Programming and erasure endurance: 10,000 times (data flash) 1,000 times (program ROM) • Program security: ROM code protect, ID code check • Debug functions: On-chip debug, on-board flash rewrite function • Background operation (BGO) function (data flash)
Operating Frequency/Supply Voltage		f(XIN) = 20 MHz (VCC = 2.7 to 5.5 V)
Current Consumption		Typ. 7 mA (VCC = 5.0 V, f(XIN) = 20 MHz)
Operating Ambient Temperature		-40 to 85°C (J version) -40 to 125°C (K version) (1)
Package		48-pin LQFP Package code: PLQP0048KB-A (previous code: 48P6Q-A)

Note:
1. Specify the K version if K version functions are to be used.

Table 1.11 Product List for R8C/34Y Group **Current of Jan 2013**

Part No.	ROM Capacity		RAM Capacity	Package Type	Remarks
	Program ROM	Data flash			
R5F21346YJFP	32 Kbytes	1 Kbyte × 4	2.5 Kbytes	PLQP0048KB-A	J version
R5F21347YJFP	48 Kbytes	1 Kbyte × 4	4 Kbytes	PLQP0048KB-A	
R5F21348YJFP	64 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0048KB-A	
R5F2134AYJFP	96 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0048KB-A	
R5F2134CYJFP	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0048KB-A	
R5F21346YKFP	32 Kbytes	1 Kbyte × 4	2.5 Kbytes	PLQP0048KB-A	K version
R5F21347YKFP	48 Kbytes	1 Kbyte × 4	4 Kbytes	PLQP0048KB-A	
R5F21348YKFP	64 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0048KB-A	
R5F2134AYKFP	96 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0048KB-A	
R5F2134CYKFP	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0048KB-A	

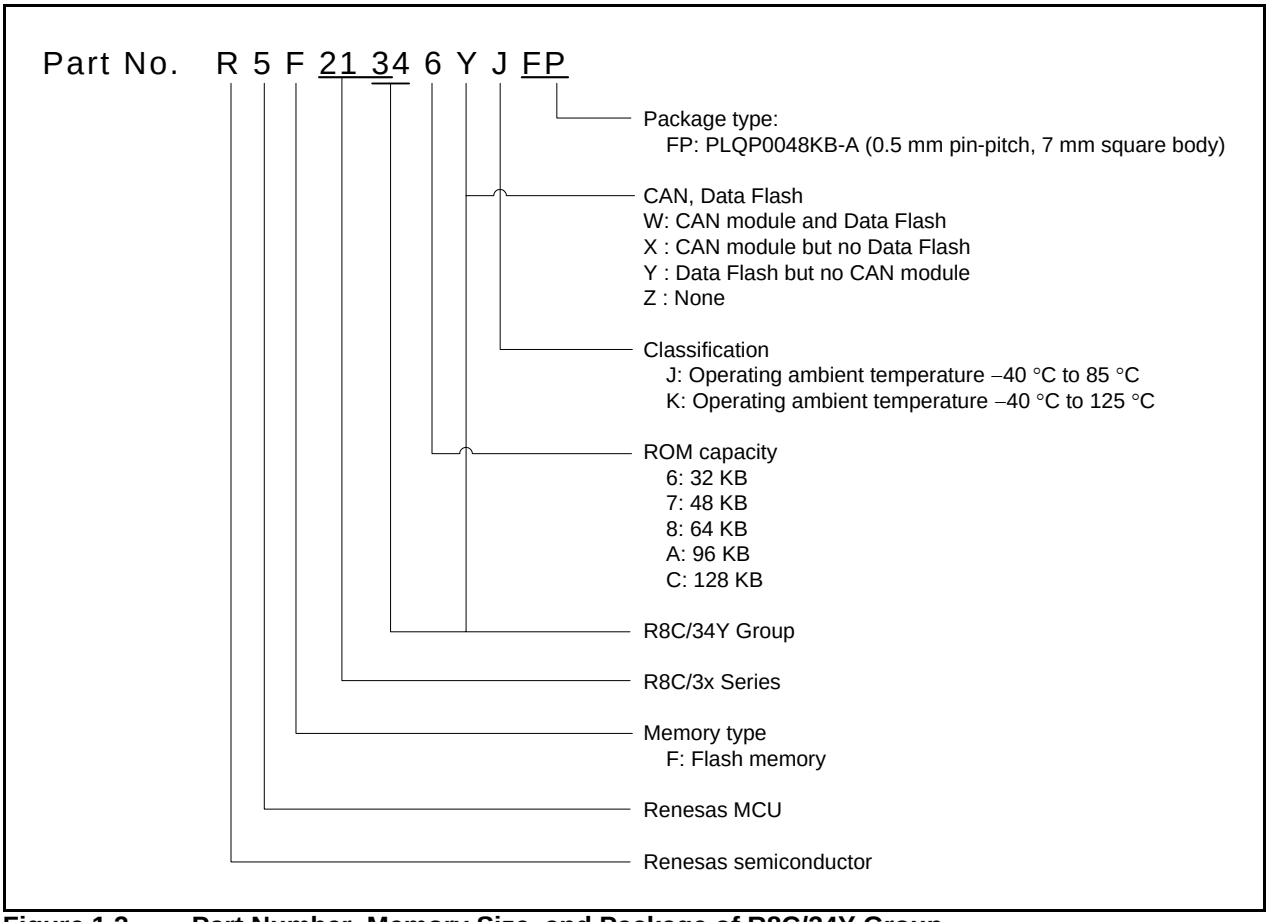
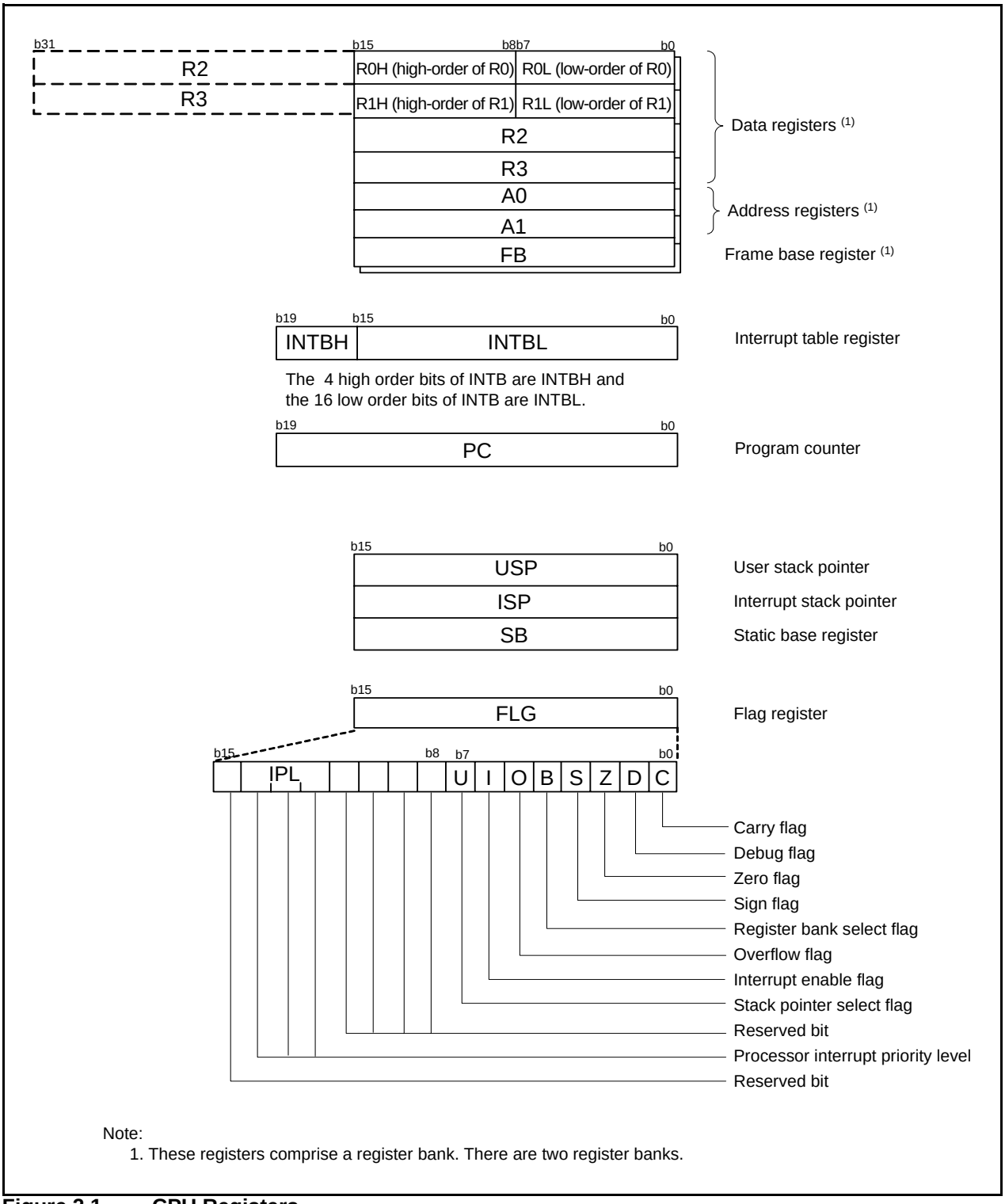


Figure 1.3 Part Number, Memory Size, and Package of R8C/34Y Group

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU Registers. The CPU contains 13 registers. R0, R1, R2, R3, A0, A1, and FB configure a register bank. There are two sets of register bank.



Note:
1. These registers comprise a register bank. There are two register banks.

Figure 2.1 CPU Registers

2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 is analogous to A0. A1 can be combined with A0 and as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC is 20 bits wide and indicates the address of the next instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP, and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

2.8 Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

2.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

2.8.5 Register Bank Select Flag (B)

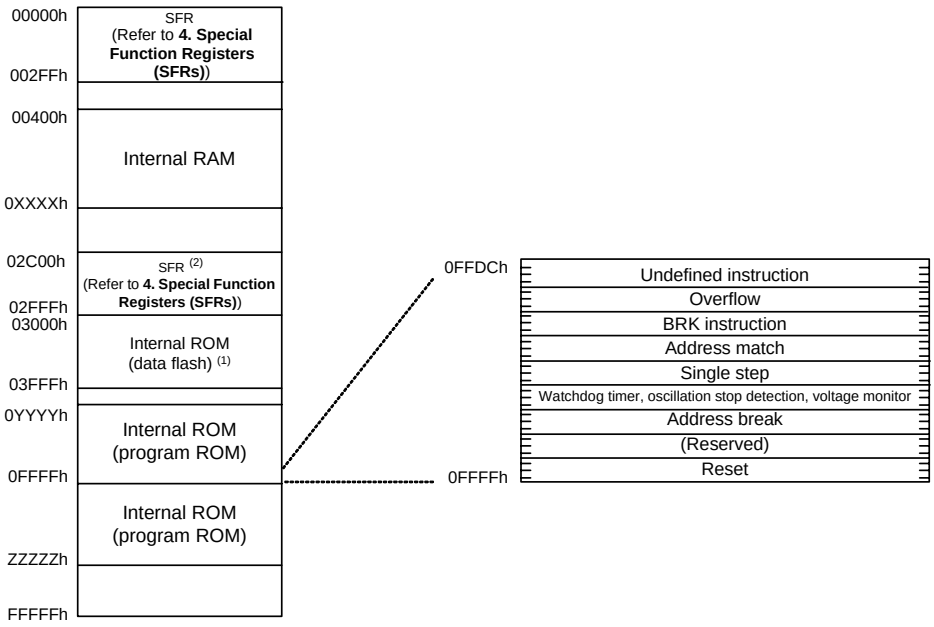
Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow; otherwise to 0.

3.3 R8C/34Y Group

Figure 3.3 is a Memory Map of R8C/34Y Group. The R8C/34Y Group has a 1-Mbyte address space from addresses 00000h to FFFFFh. The internal ROM (program ROM) is allocated lower addresses, beginning with address 0FFFFh. For example, a 48-Kbyte internal ROM area is allocated addresses 04000h to 0FFFFh.
The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. The starting address of each interrupt routine is stored here.
The internal ROM (data flash) is allocated addresses 03000h to 03FFFh.
The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 4-Kbyte internal RAM area is allocated addresses 00400h to 013FFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.
Special function registers (SFRs) are allocated addresses 00000h to 002FFh and 02C00h to 02FFFh (the SFR areas for the DTC and other modules). Peripheral function control registers are allocated here. All unallocated spaces within the SFRs are reserved and cannot be accessed by users.



Notes:
1. The Data Flash memory indicates blocks A (1 Kbyte), B (1 Kbyte), C (1 Kbyte), and D (1 Kbyte).
2. The SFR areas for the DTC and other modules are allocated to addresses 02C00h to 02FFFh.
3. The blank areas are reserved and cannot be accessed by users.

Part Number	Internal ROM			Internal RAM	
	Size	Address 0YYYYh	Address ZZZZZh	Size	Address 0XXXXh
R5F21346YJFP, R5F21346YKFP	32 Kbytes	08000h	—	2.5 Kbytes	00DFFh
R5F21347YJFP, R5F21347YKFP	48 Kbytes	04000h	—	4 Kbytes	013FFh
R5F21348YJFP, R5F21348YKFP	64 Kbytes	04000h	13FFFh	6 Kbytes	01BFFh
R5F2134AYJFP, R5F2134AYKFP	96 Kbytes	04000h	1BFFFh	8 Kbytes	023FFh
R5F2134CYJFP, R5F2134CYKFP	128 Kbytes	04000h	23FFFh	10 Kbytes	02BFFh

Figure 3.3 Memory Map of R8C/34Y Group

4. Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function. Tables 4.1 to 4.17 list the special function registers. Table 4.18 lists the ID Code Areas and Option Function Select Area.

Table 4.1 SFR Information (1) (1)

Address	Register	Symbol	After reset
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	00h
0005h	Processor Mode Register 1	PM1	00h
0006h	System Clock Control Register 0	CM0	00101000b
0007h	System Clock Control Register 1	CM1	00100000b
0008h	Module Standby Control Register	MSTCR	00h
0009h	System Clock Control Register 3	CM3	00h
000Ah	Protect Register	PRCR	00h
000Bh	Reset Source Determination Register	RSTFR	0XXXXXXXb (2)
000Ch	Oscillation Stop Detection Register	OCD	00000100b
000Dh	Watchdog Timer Reset Register	WDTR	XXh
000Eh	Watchdog Timer Start Register	WDTS	XXh
000Fh	Watchdog Timer Control Register	WDTC	00111111b
0010h			
0011h			
0012h			
0013h			
0014h			
0015h	High-Speed On-Chip Oscillator Control Register 7	FRA7	When shipping
0016h			
0017h			
0018h			
0019h			
001Ah			
001Bh			
001Ch	Count Source Protection Mode Register	CSPR	00h 10000000b (3)
001Dh			
001Eh			
001Fh			
0020h			
0021h			
0022h			
0023h	High-Speed On-Chip Oscillator Control Register 0	FRA0	00h
0024h	High-Speed On-Chip Oscillator Control Register 1	FRA1	When shipping
0025h	High-Speed On-Chip Oscillator Control Register 2	FRA2	00h
0026h	On-Chip Reference Voltage Control Register	OCVREFCR	00h
0027h			
0028h			
0029h	High-Speed On-Chip Oscillator Control Register 4	FRA4	When Shipping
002Ah	High-Speed On-Chip Oscillator Control Register 5	FRA5	When Shipping
002Bh	High-Speed On-Chip Oscillator Control Register 6	FRA6	When Shipping
002Ch			
002Dh			
002Eh			
002Fh	High-Speed On-Chip Oscillator Control Register 3	FRA3	When shipping
0030h	Voltage Monitor Circuit Control Register	CMPA	00h
0031h	Voltage Monitor Circuit Edge Select Register	VCAC	00h
0032h			
0033h	Voltage Detect Register 1	VCA1	00001000b
0034h	Voltage Detect Register 2	VCA2	00h (4) 00100000b (5)
0035h			
0036h	Voltage Detection 1 Level Select Register	VD1LS	00000111b
0037h			
0038h	Voltage Monitor 0 Circuit Control Register	VW0C	1100X010b (4) 1100X011b (5)
0039h	Voltage Monitor 1 Circuit Control Register	VW1C	10001010b

X: Undefined

Notes:
1. The blank areas are reserved and cannot be accessed by users.
2. The CWR bit in the RSTFR register is set to 0 after power-on and voltage monitor 0 reset. Hardware reset, Software reset, or watchdog timer reset does not affect this bit.
3. The CSPROINI bit in the OFS register is set to 0.
4. The LVDAS bit in the OFS register is set to 1.
5. The LVDAS bit in the OFS register is set to 0.

Table 4.3 SFR Information (3) (1)

Address	Register	Symbol	After reset
0080h	DTC Activation Control Register	DTCTL	00h
0081h			
0082h			
0083h			
0084h			
0085h			
0086h			
0087h			
0088h	DTC Activation Enable Register 0	DTCEN0	00h
0089h	DTC Activation Enable Register 1	DTCEN1	00h
008Ah	DTC Activation Enable Register 2	DTCEN2	00h
008Bh	DTC Activation Enable Register 3	DTCEN3	00h
008Ch	DTC Activation Enable Register 4	DTCEN4	00h
008Dh	DTC Activation Enable Register 5	DTCEN5	00h
008Eh	DTC Activation Enable Register 6	DTCEN6	00h
008Fh			
0090h			
0091h			
0092h			
0093h			
0094h			
0095h			
0096h			
0097h			
0098h			
0099h			
009Ah			
009Bh			
009Ch			
009Dh			
009Eh			
009Fh			
00A0h	UART0 Transmit/Receive Mode Register	U0MR	00h
00A1h	UART0 Bit Rate Register	U0BRG	XXh
00A2h	UART0 Transmit Buffer Register	U0TB	XXh
00A3h			XXh
00A4h	UART0 Transmit/Receive Control Register 0	U0C0	00001000b
00A5h	UART0 Transmit/Receive Control Register 1	U0C1	00000010b
00A6h	UART0 Receive Buffer Register	U0RB	XXh
00A7h			XXh
00A8h	UART2 Transmit/Receive Mode Register	U2MR	00h
00A9h	UART2 Bit Rate Register	U2BRG	XXh
00AAh	UART2 Transmit Buffer Register	U2TB	XXh
00ABh			XXh
00ACh	UART2 Transmit/Receive Control Register 0	U2C0	00001000b
00ADh	UART2 Transmit/Receive Control Register 1	U2C1	00000010b
00AEh	UART2 Receive Buffer Register	U2RB	XXh
00AFh			XXh
00B0h	UART2 Digital Filter Function Select Register	URXDF	00h
00B1h			
00B2h			
00B3h			
00B4h			
00B5h			
00B6h			
00B7h			
00B8h			
00B9h			
00BAh			
00BBh	UART2 Special Mode Register 5	U2SMR5	00h
00BCh	UART2 Special Mode Register 4	U2SMR4	00h
00BDh	UART2 Special Mode Register 3	U2SMR3	000X0X0Xb
00BEh	UART2 Special Mode Register 2	U2SMR2	X0000000b
00BFh	UART2 Special Mode Register	U2SMR	X0000000b

X: Undefined
Note:
1. The blank areas are reserved and cannot be accessed by users.

Table 4.7 SFR Information (7) (1)

Address	Register	Symbol	After reset
0180h	Timer RA Pin Select Register	TRASR	00h
0181h	Timer RB/RC Pin Select Register	TRBRCSR	00h
0182h	Timer RC Pin Select Register 0	TRCPSR0	00h
0183h	Timer RC Pin Select Register 1	TRCPSR1	00h
0184h	Timer RD Pin Select Register 0	TRDPSR0	00h
0185h	Timer RD Pin Select Register 1	TRDPSR1	00h
0186h	Timer Pin Select Register	TIMSR	00h
0187h			
0188h	UART0 Pin Select Register	U0SR	00h
0189h			
018Ah	UART2 Pin Select Register 0	U2SR0	00h
018Bh	UART2 Pin Select Register 1	U2SR1	00h
018Ch	SSU Pin Select Register	SSUIICSR	00h
018Dh			
018Eh	INT Interrupt Input Pin Select Register	INTSR	00h
018Fh	I/O Function Pin Select Register	PINSR	00h
0190h			
0191h			
0192h			
0193h	SS Bit Counter Register	SSBR	11111000b
0194h	SS Transmit Data Register	SSTDR	FFh
0195h			FFh
0196h	SS Receive Data Register	SSRDR	FFh
0197h			FFh
0198h	SS Control Register H	SSCRH	00h
0199h	SS Control Register L	SSCRL	01111101b
019Ah	SS Mode Register	SSMR	00010000b
019Bh	SS Enable Register	SSER	00h
019Ch	SS Status Register	SSSR	00h
019Dh	SS Mode Register 2	SSMR2	00h
019Eh			
019Fh			
01A0h			
01A1h			
01A2h			
01A3h			
01A4h			
01A5h			
01A6h			
01A7h			
01A8h			
01A9h			
01AAh			
01ABh			
01ACh			
01ADh			
01AEh			
01AFh			
01B0h			
01B1h			
01B2h	Flash Memory Status Register	FST	10000X00b
01B3h			
01B4h	Flash Memory Control Register 0	FMR0	00h
01B5h	Flash Memory Control Register 1	FMR1	00h
01B6h	Flash Memory Control Register 2	FMR2	00h
01B7h			
01B8h			
01B9h			
01BAh			
01BBh			
01BCh			
01BDh			
01BEh			
01BFh			

X: Undefined
Note:
1. The blank areas are reserved and cannot be accessed by users.

Table 4.9 SFR Information (9) (1)

Address	Register	Symbol	After reset
2C00h	DTC Transfer Vector Area		XXh
2C01h	DTC Transfer Vector Area		XXh
2C02h	DTC Transfer Vector Area		XXh
2C03h	DTC Transfer Vector Area		XXh
2C04h	DTC Transfer Vector Area		XXh
2C05h			
2C06h			
2C07h			
2C08h	DTC Transfer Vector Area		XXh
2C09h	DTC Transfer Vector Area		XXh
2C0Ah	DTC Transfer Vector Area		XXh
:	DTC Transfer Vector Area		XXh
:	DTC Transfer Vector Area		XXh
2C3Ah			
2C3Bh			
2C3Ch			
2C3Dh			
2C3Eh			
2C3Fh			
2C40h	DTC Control Data 0	DTCD0	XXh
2C41h			XXh
2C42h			XXh
2C43h			XXh
2C44h			XXh
2C45h			XXh
2C46h			XXh
2C47h			XXh
2C48h	DTC Control Data 1	DTCD1	XXh
2C49h			XXh
2C4Ah			XXh
2C4Bh			XXh
2C4Ch			XXh
2C4Dh			XXh
2C4Eh			XXh
2C4Fh			XXh
2C50h	DTC Control Data 2	DTCD2	XXh
2C51h			XXh
2C52h			XXh
2C53h			XXh
2C54h			XXh
2C55h			XXh
2C56h			XXh
2C57h			XXh
2C58h	DTC Control Data 3	DTCD3	XXh
2C59h			XXh
2C5Ah			XXh
2C5Bh			XXh
2C5Ch			XXh
2C5Dh			XXh
2C5Eh			XXh
2C5Fh			XXh
2C60h	DTC Control Data 4	DTCD4	XXh
2C61h			XXh
2C62h			XXh
2C63h			XXh
2C64h			XXh
2C65h			XXh
2C66h			XXh
2C67h			XXh
2C68h	DTC Control Data 5	DTCD5	XXh
2C69h			XXh
2C6Ah			XXh
2C6Bh			XXh
2C6Ch			XXh
2C6Dh			XXh
2C6Eh			XXh
2C6Fh			XXh

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.10 SFR Information (10) (1)

Address	Register	Symbol	After reset
2C70h	DTC Control Data 6	DTCD6	XXh
2C71h			XXh
2C72h			XXh
2C73h			XXh
2C74h			XXh
2C75h			XXh
2C76h			XXh
2C77h			XXh
2C78h	DTC Control Data 7	DTCD7	XXh
2C79h			XXh
2C7Ah			XXh
2C7Bh			XXh
2C7Ch			XXh
2C7Dh			XXh
2C7Eh			XXh
2C7Fh			XXh
2C80h	DTC Control Data 8	DTCD8	XXh
2C81h			XXh
2C82h			XXh
2C83h			XXh
2C84h			XXh
2C85h			XXh
2C86h			XXh
2C87h			XXh
2C88h	DTC Control Data 9	DTCD9	XXh
2C89h			XXh
2C8Ah			XXh
2C8Bh			XXh
2C8Ch			XXh
2C8Dh			XXh
2C8Eh			XXh
2C8Fh			XXh
2C90h	DTC Control Data 10	DTCD10	XXh
2C91h			XXh
2C92h			XXh
2C93h			XXh
2C94h			XXh
2C95h			XXh
2C96h			XXh
2C97h			XXh
2C98h	DTC Control Data 11	DTCD11	XXh
2C99h			XXh
2C9Ah			XXh
2C9Bh			XXh
2C9Ch			XXh
2C9Dh			XXh
2C9Eh			XXh
2C9Fh			XXh
2CA0h	DTC Control Data 12	DTCD12	XXh
2CA1h			XXh
2CA2h			XXh
2CA3h			XXh
2CA4h			XXh
2CA5h			XXh
2CA6h			XXh
2CA7h			XXh
2CA8h	DTC Control Data 13	DTCD13	XXh
2CA9h			XXh
2CAAh			XXh
2CABh			XXh
2CACh			XXh
2CADh			XXh
2CAEh			XXh
2CAFh			XXh

X: Undefined
Note:
1. The blank areas are reserved and cannot be accessed by users.

Table 4.12 SFR Information (12) (1)

Address	Register	Symbol	After reset
2CF0h	DTC Control Data 22	DTCD22	XXh
2CF1h			XXh
2CF2h			XXh
2CF3h			XXh
2CF4h			XXh
2CF5h			XXh
2CF6h			XXh
2CF7h			XXh
2CF8h	DTC Control Data 23	DTCD23	XXh
2CF9h			XXh
2CFAh			XXh
2CFBh			XXh
2CFCh			XXh
2CFDh			XXh
2CFEh			XXh
2CFFh			XXh
2D00h			
2D01h			
:			
2E00h	CAN0 Mailbox 0 : Message ID	C0MB0	XXh
2E01h			XXh
2E02h			XXh
2E03h			XXh
2E04h			
2E05h	CAN0 Mailbox 0 : Data length		XXh
2E06h	CAN0 Mailbox 0 : Data field		XXh
2E07h			XXh
2E08h			XXh
2E09h			XXh
2E0Ah			XXh
2E0Bh			XXh
2E0Ch			XXh
2E0Dh			XXh
2E0Eh	CAN0 Mailbox 0 : Time stamp		XXh
2E0Fh			XXh
2E10h	CAN0 Mailbox 1 : Message ID	C0MB1	XXh
2E11h			XXh
2E12h			XXh
2E13h			XXh
2E14h			
2E15h	CAN0 Mailbox 1 : Data length		XXh
2E16h	CAN0 Mailbox 1 : Data field		XXh
2E17h			XXh
2E18h			XXh
2E19h			XXh
2E1Ah			XXh
2E1Bh			XXh
2E1Ch			XXh
2E1Dh			XXh
2E1Eh	CAN0 Mailbox 1 : Time stamp		XXh
2E1Fh			XXh
2E20h	CAN0 Mailbox 2 : Message ID	C0MB2	XXh
2E21h			XXh
2E22h			XXh
2E23h			XXh
2E24h			
2E25h	CAN0 Mailbox 2 : Data length		XXh
2E26h	CAN0 Mailbox 2 : Data field		XXh
2E27h			XXh
2E28h			XXh
2E29h			XXh
2E2Ah			XXh
2E2Bh			XXh
2E2Ch			XXh
2E2Dh			XXh
2E2Eh	CAN0 Mailbox 2 : Time stamp		XXh
2E2Fh			XXh

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 5.2 Recommended Operating Conditions (1)

Symbol	Parameter				Conditions	Standard			Unit
						Min.	Typ.	Max.	
V_{CC}/AV_{CC}	Supply voltage					2.7	–	5.5	V
V_{SS}/AV_{SS}	Supply voltage					–	0	–	V
V_{IH}	Input “H” voltage	Other than CMOS input				0.8 V_{CC}	–	V_{CC}	V
		CMOS input	Input level switching function (I/O port)	Input level selection : 0.35 V_{CC}	4.0 V ≤ V_{CC} ≤ 5.5 V	0.5 V_{CC}	–	V_{CC}	V
					2.7 V ≤ V_{CC} < 4.0 V	0.55 V_{CC}	–	V_{CC}	V
				Input level selection : 0.5 V_{CC}	4.0 V ≤ V_{CC} ≤ 5.5 V	0.65 V_{CC}	–	V_{CC}	V
					2.7 V ≤ V_{CC} < 4.0 V	0.7 V_{CC}	–	V_{CC}	V
				Input level selection : 0.7 V_{CC}	4.0 V ≤ V_{CC} ≤ 5.5 V	0.85 V_{CC}	–	V_{CC}	V
					2.7 V ≤ V_{CC} < 4.0 V	0.85 V_{CC}	–	V_{CC}	V
		External clock input (XOUT)				1.2	–	V_{CC}	V
V_{IL}	Input “L” voltage	Other than CMOS input				0	–	0.2 V_{CC}	V
		CMOS input	Input level switching function (I/O port)	Input level selection : 0.35 V_{CC}	4.0 V ≤ V_{CC} ≤ 5.5 V	0	–	0.2 V_{CC}	V
					2.7 V ≤ V_{CC} < 4.0 V	0	–	0.2 V_{CC}	V
				Input level selection : 0.5 V_{CC}	4.0 V ≤ V_{CC} ≤ 5.5 V	0	–	0.4 V_{CC}	V
					2.7 V ≤ V_{CC} < 4.0 V	0	–	0.3 V_{CC}	V
				Input level selection : 0.7 V_{CC}	4.0 V ≤ V_{CC} ≤ 5.5 V	0	–	0.55 V_{CC}	V
					2.7 V ≤ V_{CC} < 4.0 V	0	–	0.45 V_{CC}	V
		External clock input (XOUT)				0	–	0.4	V
$I_{OH(sum)}$	Peak sum output “H”	Sum of all pins $I_{OH(peak)}$				–	–	–80	mA
$I_{OH(sum)}$	Average sum output “H”	Sum of all pins $I_{OH(avg)}$				–	–	–40	mA
$I_{OH(peak)}$	Peak output “H” current					–	–	–10	mA
$I_{OH(avg)}$	Average output “H” current					–	–	–5	mA
$I_{OL(sum)}$	Peak sum output “L”	Sum of all pins $I_{OL(peak)}$				–	–	80	mA
$I_{OL(sum)}$	Average sum output “L”	Sum of all pins $I_{OL(avg)}$				–	–	40	mA
$I_{OL(peak)}$	Peak output “L” current					–	–	10	mA
$I_{OL(avg)}$	Average output “L” current					–	–	5	mA
$f_{(XIN)}$	XIN clock input oscillation frequency				2.7 V ≤ V_{CC} ≤ 5.5 V	–	–	20	MHz
fOCO40M	When used as the count source for timer RC or timer RD				2.7 V ≤ V_{CC} ≤ 5.5 V	32	–	40	MHz
fOCO-F	fOCO-F frequency				2.7 V ≤ V_{CC} ≤ 5.5 V	–	–	20	MHz
–	System clock frequency				2.7 V ≤ V_{CC} ≤ 5.5 V	–	–	20	MHz
$f_{(BCLK)}$	CPU clock frequency				2.7 V ≤ V_{CC} ≤ 5.5 V	–	–	20	MHz

Notes:
1. V_{CC} = 2.7 to 5.5 V at T_{opr} = –40 to 85°C (J version) / –40 to 125°C (K version), unless otherwise specified.
2. The average output current indicates the average value of current measured during 100 ms.

Table 5.4 A/D Converter Characteristics

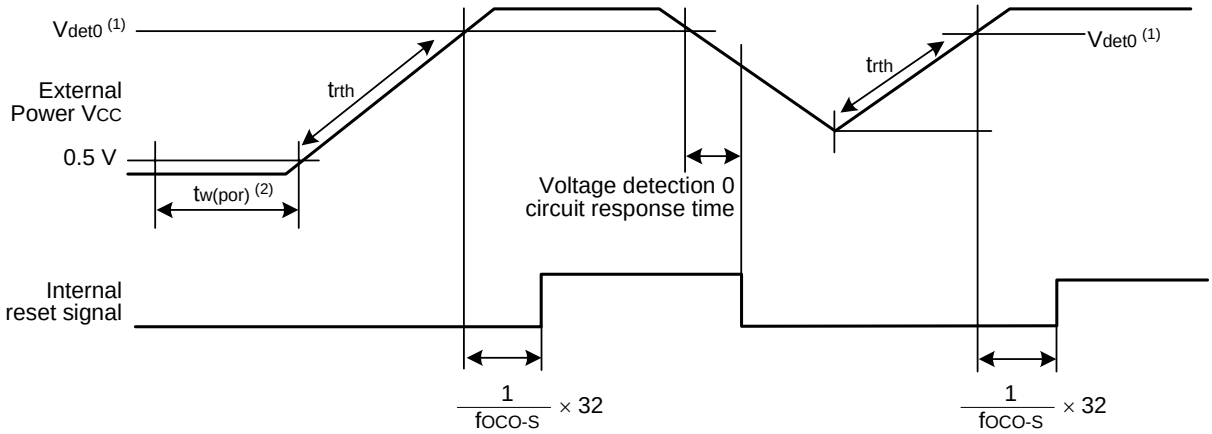
Symbol	Parameter		Conditions		Standard			Unit
					Min.	Typ.	Max.	
–	Resolution		V_{ref} = AV_{CC}		–	–	10	Bit
–	Absolute accuracy	10-bit mode	V_{ref} = AV_{CC} = 5.0 V	AN0 to AN7 input, AN8 to AN11 input	–	–	±3	LSB
			V_{ref} = AV_{CC} = 3.0 V	AN0 to AN7 input, AN8 to AN11 input	–	–	±5	LSB
		8-bit mode	V_{ref} = AV_{CC} = 5.0 V	AN0 to AN7 input, AN8 to AN11 input	–	–	±2	LSB
			V_{ref} = AV_{CC} = 3.0 V	AN0 to AN7 input, AN8 to AN11 input	–	–	±2	LSB
ϕAD	A/D conversion clock		4.0 ≤ V_{ref} = AV_{CC} = ≤ 5.5 (2)		2	–	20	MHz
			2.7 ≤ V_{ref} = AV_{CC} = ≤ 5.5 (2)		2	–	10	MHz
–	Tolerance level impedance				–	3	–	kΩ
I_{vref}	V_{ref} current		V_{CC} = 5.0 V, XIN = f1 = ϕAD = 20 MHz		–	45	–	µA
t_{CONV}	Conversion time	10-bit mode	V_{ref} = AV_{CC} = 5.0 V, ϕAD = 20 MHz		2.2	–	–	µs
		8-bit mode	V_{ref} = AV_{CC} = 5.0 V, ϕAD = 20 MHz		2.2	–	–	µs
t_{SAMP}	Sampling time		ϕAD = 20 MHz		0.8	–	–	µs
V_{ref}	Reference voltage				2.7	–	AV_{CC}	V
V_{IA}	Analog input voltage (3)				0	–	V_{ref}	V
OCVREF	On-chip reference voltage		2 MHz ≤ ϕAD ≤ 4 MHz		1.14	1.34	1.54	V

Notes:
1. V_{CC}/AV_{CC} = V_{ref} = 2.7 to 5.5 V, V_{SS} = 0 V at T_{opr} = –40 to 85°C (J version) / –40 to 125°C (K version), unless otherwise specified.
2. The A/D conversion result will be undefined in wait mode, stop mode, when the flash memory stops, and in low-consumption current mode. Do not perform A/D conversion in these states or transition to these states during A/D conversion.
3. When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

Table 5.10 Power-on Reset Circuit, Voltage Monitor 0 Reset Electrical Characteristics (2)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t_{rth}	External power V_{CC} rise gradient	(1)	0	–	50000	mV/msec

Notes:
1. The measurement condition is V_{CC} = 2.7 V to 5.5 V and T_{opr} = –40 to 85°C (J version) / –40 to 125°C (K version).
2. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.



Notes:
1. Vdet0 indicates the voltage detection level of the voltage detection 0 circuit. Refer to **6. Voltage Detection Circuit** of User's Manual: Hardware (R01UH0063EJ) for details.
2. tw(por) indicates the duration the external power VCC must be held below the valid voltage (0.5 V) to enable a power-on reset. When turning on the power after it falls with voltage monitor 0 reset disabled, maintain tw(por) for 1 ms or more.

Figure 5.3 Power-on Reset Circuit Electrical Characteristics

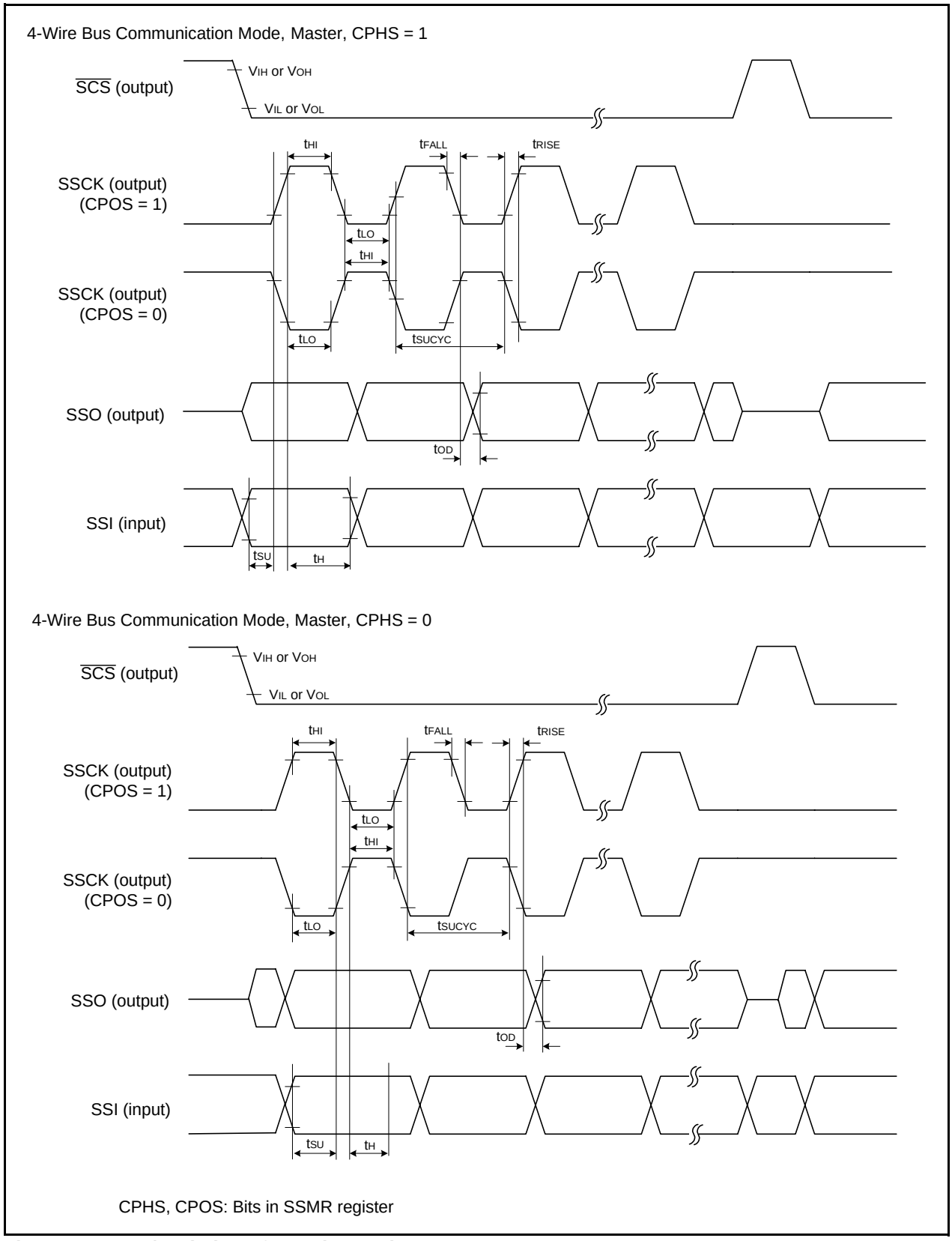


Figure 5.4 I/O Timing of SSU (Master)

Table 5.17 Electrical Characteristics (3) [3.3 V ≤ Vcc ≤ 5.5 V] (Topr = –40 to 125°C (K version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
Icc	Power supply current (Vcc = 3.3 to 5.5 V) Single-chip mode, output pins are open, other pins are Vss	High-speed clock mode (1)	XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	7.0	15	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	5.6	12.5	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	3.6	–	mA
			XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	3.0	–	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	2.2	–	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	1.5	–	mA
		High-speed on-chip oscillator mode (1)	XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	7.0	15	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	3.0	–	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR27 = 1, VCA20 = 0	–	90	400	µA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	15	330	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	5	320	µA
		Stop mode	XIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	2.0	5.0	µA
			XIN clock off, Topr = 125°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	60.0	–	µA

Note:
1. The typical value (Typ.) indicates the current value when the CPU and the memory operate.
The maximum value (Max.) indicates the current when the CPU, the memory, and the peripheral functions operate and the flash memory is programmed/erased.

Timing Requirements
(Unless Otherwise Specified: Vcc = 5 V, Vss = 0 V at Topr = –40°C to 85°C (J ver)/–40°C to 125°C (K ver))

Table 5.18 External clock input (XOUT)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XOUT)}$	XOUT input cycle time	50	–	ns
$t_{WH(XOUT)}$	XOUT input “H” width	24	–	ns
$t_{WL(XOUT)}$	XOUT input “L” width	24	–	ns

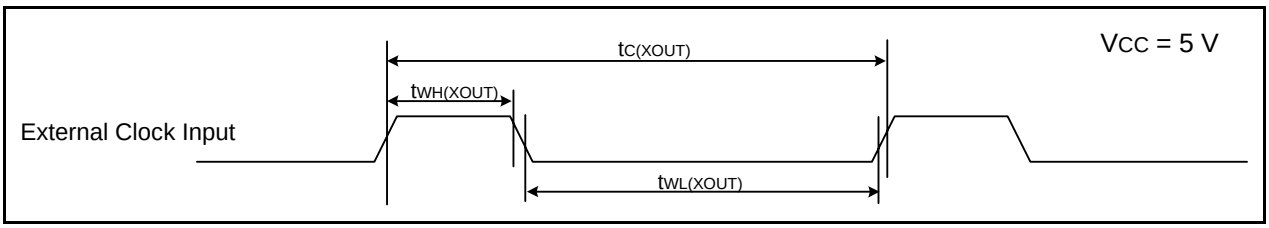


Figure 5.7 External Clock Input Timing Diagram when Vcc = 5 V

Table 5.19 TRAIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	100	–	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	40	–	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	40	–	ns

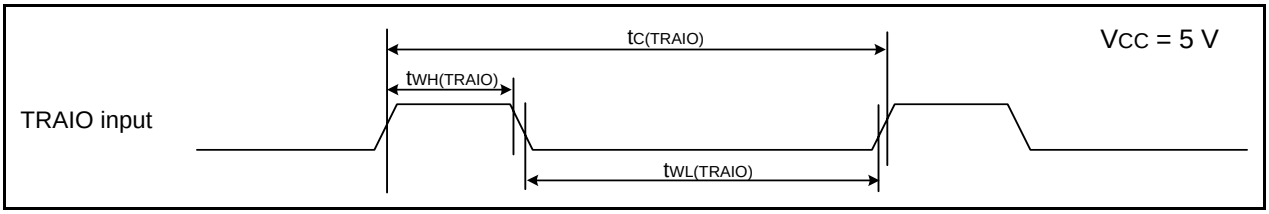


Figure 5.8 TRAIO Input Timing Diagram when Vcc = 5 V

Table 5.22 Electrical Characteristics (3) [2.7 V ≤ Vcc < 4.2 V]

Symbol	Parameter		Condition	Standard			Unit
				Min.	Typ.	Max.	
V_{OH}	Output “H” voltage	Other than XOUT	I_{OH} = –1 mA	V_{CC} – 0.5	–	V_{CC}	V
		XOUT	I_{OH} = –200 μA	1.0	–	V_{CC}	V
V_{OL}	Output “L” voltage	Other than XOUT	I_{OL} = 1 mA	–	–	0.5	V
		XOUT	I_{OL} = 200 μA	–	–	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$ to $\overline{INT4}$, $\overline{KI0}$ to $\overline{KI3}$, TRAIO, TRBO, TRCIOA to TRCIOD, TRDIOA0 to TRDIOD0, TRDIOA1 to TRDIOD1, TRCCLK, $\overline{TRDCLK}$, TRCTRG, $\overline{ADTRG}$, RXD0, RXD2, CLK0, CLK2, SSI, SCL2, SDA2, SSO		0.1	0.4	–	V
		$\overline{RESET}$		0.1	0.5	–	V
I_{IH}	Input “H” current		VI = 3 V, V_{CC} = 3.0 V	–	–	1.0	μA
I_{IL}	Input “L” current		VI = 0 V, V_{CC} = 3.0 V	–	–	–1.0	μA
R_{PULLUP}	Pull-up resistance		VI = 0 V, V_{CC} = 3.0 V	42	84	168	kΩ
R_{fXIN}	Feedback resistance	XIN		–	0.3	–	MΩ
V_{RAM}	RAM hold voltage		During stop mode	2.0	–	–	V

Note:
1. 2.7 V ≤ V_{CC} < 4.2 V at T_{opr} = –40 to 85°C (J version) / –40 to 125°C (K version), f(XIN) = 20 MHz, unless otherwise specified.

Table 5.24 Electrical Characteristics (4) [2.7 V ≤ Vcc < 3.3 V] (Topr = –40 to 125°C (K version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
Icc	Power supply current (Vcc = 2.7 to 3.3 V) Single-chip mode, output pins are open, other pins are Vss	High-speed clock mode (1)	XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	7.0	14.5	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	5.6	12.0	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	3.6	–	mA
			XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	3.0	–	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	2.2	–	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	1.5	–	mA
		High-speed on-chip oscillator mode (1)	XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	7.0	14.5	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	3.0	–	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR27 = 1, VCA20 = 0	–	85	390	µA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	15	320	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	5	310	µA
		Stop mode	XIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	2.0	5.0	µA
			XIN clock off, Topr = 125°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	55.0	–	µA

Note:
1. The typical value (Typ.) indicates the current value when the CPU and the memory operate.
The maximum value (Max.) indicates the current when the CPU, the memory, and the peripheral functions operate and the flash memory is programmed/erased.

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