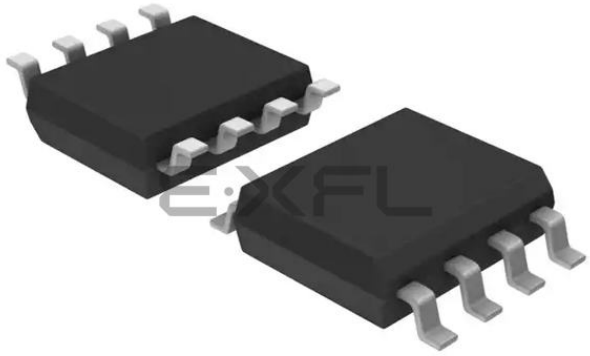

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Details	
Product Status	Active
Core Processor	M8C
Core Size	8-Bit
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Connectivity	I²C, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	6
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.25V
Data Converters	A/D 8x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	8-SOIC (0.154", 3.90mm Width)
Supplier Device Package	8-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c21123-24sxi

Contents

Pin Information

This section describes, lists, and illustrates the CY8C21x23 PSoC device pins and pinout configurations. Every port pin (labeled with a “P”) is capable of Digital I/O. However, V_{SS}, V_{DD}, SMP, and XRES are not capable of Digital I/O.

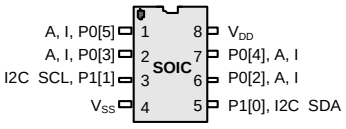
8-Pin Part Pinout

Table 2. Pin Definitions – CY8C21123 8-Pin SOIC

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O	I	P0[5]	Analog column mux input
2	I/O	I	P0[3]	Analog column mux input
3	I/O		P1[1]	I^2C serial clock (SCL), ISSP-SCLK[3]
4	Power		V_{SS}	Ground connection
5	I/O		P1[0]	I^2C serial data (SDA), ISSP-SDATA[3]
6	I/O	I	P0[2]	Analog column mux input
7	I/O	I	P0[4]	Analog column mux input
8	Power		V_{DD}	Supply voltage

LEGEND: A = Analog, I = Input, and O = Output.

Figure 3. CY8C21123 8-Pin SOIC



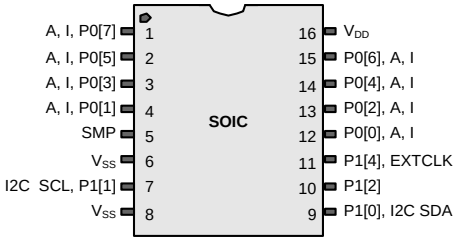
16-Pin Part Pinout

Table 3. Pin Definitions – CY8C21223 16-Pin SOIC

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O	I	P0[7]	Analog column mux input
2	I/O	I	P0[5]	Analog column mux input
3	I/O	I	P0[3]	Analog column mux input
4	I/O	I	P0[1]	Analog column mux input
5	Power		SMP	SMP connection to required external components
6	Power		V_{SS}	Ground connection
7	I/O		P1[1]	I^2C SCL, ISSP-SCLK[3]
8	Power		V_{SS}	Ground connection
9	I/O		P1[0]	I^2C SDA, ISSP-SDATA[3]
10	I/O		P1[2]	
11	I/O		P1[4]	Optional external clock input (EXTCLK)
12	I/O	I	P0[0]	Analog column mux input
13	I/O	I	P0[2]	Analog column mux input
14	I/O	I	P0[4]	Analog column mux input
15	I/O	I	P0[6]	Analog column mux input
16	Power		V_{DD}	Supply voltage

LEGEND A = Analog, I = Input, and O = Output.

Figure 4. CY8C21223 16-Pin SOIC



Note
3. These are the ISSP pins, which are not high Z at POR (power on reset). See the PSoC Technical Reference Manual for details.

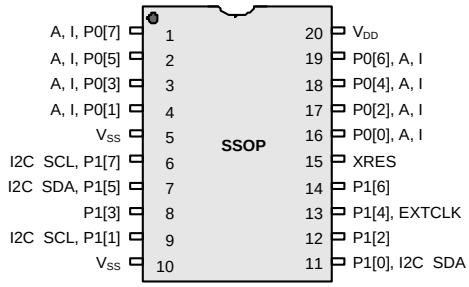
20-Pin Part Pinout

Table 5. Pin Definitions – CY8C21323 20-Pin SSOP

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O	I	P0[7]	Analog column mux input
2	I/O	I	P0[5]	Analog column mux input
3	I/O	I	P0[3]	Analog column mux input
4	I/O	I	P0[1]	Analog column mux input
5	Power		V_{SS}	Ground connection[6]
6	I/O		P1[7]	I^2C SCL
7	I/O		P1[5]	I^2C SDA
8	I/O		P1[3]	
9	I/O		P1[1]	I^2C SCL, ISSP-SCLK[7]
10	Power		V_{SS}	Ground connection[6]
11	I/O		P1[0]	I^2C SDA, ISSP-SDATA[7]
12	I/O		P1[2]	
13	I/O		P1[4]	Optional EXTCLK input
14	I/O		P1[6]	
15	Input		XRES	Active high external reset with internal pull-down
16	I/O	I	P0[0]	Analog column mux input
17	I/O	I	P0[2]	Analog column mux input
18	I/O	I	P0[4]	Analog column mux input
19	I/O	I	P0[6]	Analog column mux input
20	Power		V_{DD}	Supply voltage

LEGEND A = Analog, I = Input, and O = Output.

Figure 6. CY8C21323 20-Pin SSOP



Notes
6. All V_{SS} pins should be brought out to one common GND plane.
7. These are the ISSP pins, which are not high Z at POR (power on reset). See the PSoC Technical Reference Manual for details.

Table 8. Register Map Bank 0 Table: User Space (continued)

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
	30			70		RDI0RI	B0	RW		F0	
	31			71		RDI0SYN	B1	RW		F1	
	32		ACE00CR1	72	RW	RDI0IS	B2	RW		F2	
	33		ACE00CR2	73	RW	RDI0LT0	B3	RW		F3	
	34			74		RDI0LT1	B4	RW		F4	
	35			75		RDI0RO0	B5	RW		F5	
	36		ACE01CR1	76	RW	RDI0RO1	B6	RW		F6	
	37		ACE01CR2	77	RW		B7		CPU_F	F7	RL
	38			78			B8			F8	
	39			79			B9			F9	
	3A			7A			BA			FA	
	3B			7B			BB			FB	
	3C			7C			BC			FC	
	3D			7D			BD			FD	
	3E			7E			BE		CPU_SCR1	FE	#
	3F			7F			BF		CPU_SCR0	FF	#

Blank fields are Reserved and must not be accessed. # Access is bit specific.

Table 9. Register Map Bank 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW		40		ASE10CR0	80	RW		C0	
PRT0DM1	01	RW		41			81			C1	
PRT0IC0	02	RW		42			82			C2	
PRT0IC1	03	RW		43			83			C3	
PRT1DM0	04	RW		44		ASE11CR0	84	RW		C4	
PRT1DM1	05	RW		45			85			C5	
PRT1IC0	06	RW		46			86			C6	
PRT1IC1	07	RW		47			87			C7	
	08			48			88			C8	
	09			49			89			C9	
	0A			4A			8A			CA	
	0B			4B			8B			CB	
	0C			4C			8C			CC	
	0D			4D			8D			CD	
	0E			4E			8E			CE	
	0F			4F			8F			CF	
	10			50			90		GDI_O_IN	D0	RW
	11			51			91		GDI_E_IN	D1	RW
	12			52			92		GDI_O_OU	D2	RW
	13			53			93		GDI_E_OU	D3	RW
	14			54			94			D4	
	15			55			95			D5	
	16			56			96			D6	
	17			57			97			D7	
	18			58			98			D8	
	19			59			99			D9	
	1A			5A			9A			DA	
	1B			5B			9B			DB	

Blank fields are Reserved and must not be accessed. # Access is bit specific.

DC Amplifier Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 15. 5-V DC Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input offset voltage (absolute value)	–	2.5	15	mV	
TCV_{OSOA}	Average input offset voltage drift	–	10	–	µV/°C	
I_{EBOA}	Input leakage current (port 0 analog pins)	–	200	–	pA	Gross tested to 1 µA
C_{INOA}	Input capacitance (port 0 analog pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25 °C
V_{CMOA}	Common mode voltage range	0.0	–	V_{DD} – 1	V	
G_{OLOA}	Open loop gain	80	–	–	dB	
I_{SOA}	Amplifier supply current	–	10	30	µA	

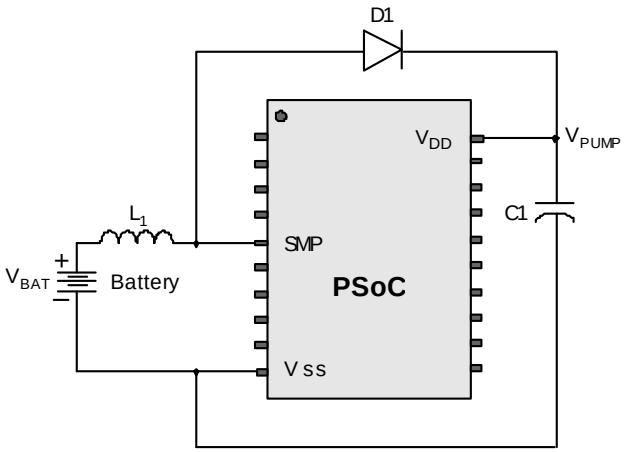
Table 16. 3.3-V DC Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input offset voltage (absolute value)	–	2.5	15	mV	
TCV_{OSOA}	Average input offset voltage drift	–	10	–	µV/°C	
I_{EBOA}	Input leakage current (port 0 analog pins)	–	200	–	pA	Gross tested to 1 µA
C_{INOA}	Input capacitance (port 0 analog pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25 °C
V_{CMOA}	Common mode voltage range	0	–	V_{DD} – 1	V	
G_{OLOA}	Open loop gain	80	–	–	dB	
I_{SOA}	Amplifier supply current	–	10	30	µA	

Table 17. 2.7V DC Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input offset voltage (absolute value)	–	2.5	15	mV	
TCV_{OSOA}	Average input offset voltage drift	–	10	–	µV/°C	
I_{EBOA}	Input leakage current (port 0 analog pins)	–	200	–	pA	Gross tested to 1 µA
C_{INOA}	Input capacitance (port 0 analog pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25 °C
V_{CMOA}	Common mode voltage range	0	–	V_{DD} – 1	V	
G_{OLOA}	Open loop gain	80	–	–	dB	
I_{SOA}	Amplifier supply current	–	10	30	µA	

Figure 12. Basic Switch Mode Pump Circuit



DC POR and LVD Specifications

Table 19 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 19. DC POR and LVD Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
	V_{DD} value for PPOR trip					V_{DD} must be greater than or equal to 2.5 V during startup, reset from the XRES pin, or reset from watchdog.
V_{PPOR0}	PORLEV[1:0] = 00b	–	2.36	2.40	V	
V_{PPOR1}	PORLEV[1:0] = 01b	–	2.82	2.95	V	
V_{PPOR2}	PORLEV[1:0] = 10b	–	4.55	4.70	V	
	V_{DD} value for LVD trip					
V_{LVD0}	VM[2:0] = 000b	2.40	2.45	2.51[12]	V	
V_{LVD1}	VM[2:0] = 001b	2.85	2.92	2.99[13]	V	
V_{LVD2}	VM[2:0] = 010b	2.95	3.02	3.09	V	
V_{LVD3}	VM[2:0] = 011b	3.06	3.13	3.20	V	
V_{LVD4}	VM[2:0] = 100b	4.37	4.48	4.55	V	
V_{LVD5}	VM[2:0] = 101b	4.50	4.64	4.75	V	
V_{LVD6}	VM[2:0] = 110b	4.62	4.73	4.83	V	
V_{LVD7}	VM[2:0] = 111b	4.71	4.81	4.95	V	
	V_{DD} value for PUMP trip					
V_{PUMP0}	VM[2:0] = 000b	2.45	2.55	2.62[14]	V	
V_{PUMP1}	VM[2:0] = 001b	2.96	3.02	3.09	V	
V_{PUMP2}	VM[2:0] = 010b	3.03	3.10	3.16	V	
V_{PUMP3}	VM[2:0] = 011b	3.18	3.25	3.32[15]	V	
V_{PUMP4}	VM[2:0] = 100b	4.54	4.64	4.74	V	
V_{PUMP5}	VM[2:0] = 101b	4.62	4.73	4.83	V	
V_{PUMP6}	VM[2:0] = 110b	4.71	4.82	4.92	V	
V_{PUMP7}	VM[2:0] = 111b	4.89	5.00	5.12	V	

Notes
12. Always greater than 50 mV above V_{PPOR} (PORLEV = 00) for falling supply.
13. Always greater than 50 mV above V_{PPOR} (PORLEV = 01) for falling supply.
14. Always greater than 50 mV above V_{LVD0}.
15. Always greater than 50 mV above V_{LVD3}.

DC Programming Specifications

Table 20 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 20. DC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{DDP}	V_{DD} for programming and erase	4.5	5.0	5.5	V	This specification applies to the functional requirements of external programmer tools
V_{DDLV}	Low V_{DD} for verify	2.4	2.5	2.6	V	This specification applies to the functional requirements of external programmer tools
V_{DDHV}	High V_{DD} for verify	5.1	5.2	5.3	V	This specification applies to the functional requirements of external programmer tools
$V_{DDIWRITE}$	Supply voltage for flash write operations	2.70	–	5.25	V	This specification applies to this device when it is executing internal flash writes
I_{DDP}	Supply current during programming or verify	–	5	25	mA	
V_{ILP}	Input low voltage during programming or verify	–	–	0.8	V	
V_{IHP}	Input high voltage during programming or verify	2.2	–	–	V	
I_{ILP}	Input current when applying V_{ILP} to P1[0] or P1[1] during programming or verify	–	–	0.2	mA	Driving internal pull-down resistor
I_{IHP}	Input current when applying V_{IHP} to P1[0] or P1[1] during programming or verify	–	–	1.5	mA	Driving internal pull-down resistor
V_{OLV}	Output low voltage during programming or verify	–	–	V_{SS} + 0.75	V	
V_{OHV}	Output high voltage during programming or verify	V_{DD} – 1.0	–	V_{DD}	V	
$Flash_{ENPB}$	Flash endurance (per block)	50,000[16]	–	–	–	Erase/write cycles per block
$Flash_{ENT}$	Flash endurance (total)[17]	1,800,000	–	–	–	Erase/write cycles
$Flash_{DR}$	Flash data retention	10	–	–	Years	

DC I^2C Specifications

Table 20 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 21. DC I^2C Specifications[18]

Symbol	Description	Min	Typ	Max	Units	Notes
V_{ILI2C}	Input low level	–	–	0.3 × V_{DD}	V	2.4 V ≤ V_{DD} ≤ 3.6 V
		–	–	0.25 × V_{DD}	V	4.75 V ≤ V_{DD} ≤ 5.25 V
V_{IHI2C}	Input high level	0.7 × V_{DD}	–	–	V	2.4 V ≤ V_{DD} ≤ 5.25 V

Notes

16. The 50,000 cycle flash endurance per block is guaranteed if the flash is operating within one voltage range. Voltage ranges are 2.4 V to 3.0 V, 3.0 V to 3.6 V, and 4.75 V to 5.25 V.
17. A maximum of 36 × 50,000 block endurance cycles is allowed. This may be balanced between operations on 36 × 1 blocks of 50,000 maximum cycles each, 36 × 2 blocks of 25,000 maximum cycles each, or 36 × 4 blocks of 12,500 maximum cycles each (and so forth to limit the total number of cycles to 36 × 50,000 and that no single block ever sees more than 50,000 cycles).For the full industrial range, you must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the application note, Design Aids — Reading and Writing PSoC® Flash – AN2015 for more information on Flash APIs.
18. All GPIO meet the DC GPIO V_{IL} and V_{IH} specifications mentioned in section DC GPIO Specifications on page 18. The I^2C GPIO pins also meet the mentioned specs.

AC General Purpose I/O Specifications

Table 24 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

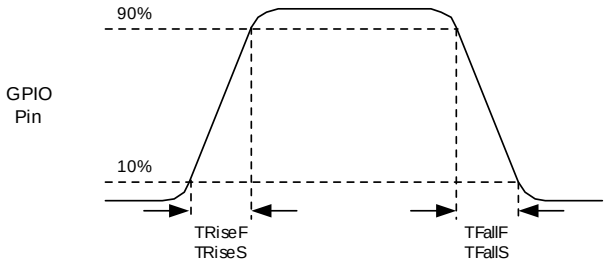
Table 24. 5-V and 3.3-V AC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{GPIO}	GPIO operating frequency	0	–	12	MHz	Normal strong mode
tRiseF	Rise time, normal strong mode, Cload = 50 pF	3	–	18	ns	V_{DD} = 4.5 V to 5.25 V, 10% to 90%
tFallF	Fall time, normal strong mode, Cload = 50 pF	2	–	18	ns	V_{DD} = 4.5 V to 5.25 V, 10% to 90%
tRiseS	Rise time, slow strong mode, Cload = 50 pF	10	27	–	ns	V_{DD} = 3 V to 5.25 V, 10% to 90%
tFallS	Fall time, slow strong mode, Cload = 50 pF	10	22	–	ns	V_{DD} = 3 V to 5.25 V, 10% to 90%

Table 25. 2.7-V AC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{GPIO}	GPIO operating frequency	0	–	3	MHz	Normal strong mode
tRiseF	Rise time, normal strong mode, Cload = 50 pF	6	–	50	ns	V_{DD} = 2.4 V to 3.0 V, 10% to 90%
tFallF	Fall time, normal strong mode, Cload = 50 pF	6	–	50	ns	V_{DD} = 2.4 V to 3.0 V, 10% to 90%
tRiseS	Rise time, slow strong mode, Cload = 50 pF	18	40	120	ns	V_{DD} = 2.4 V to 3.0 V, 10% to 90%
tFallS	Fall time, slow strong mode, Cload = 50 pF	18	40	120	ns	V_{DD} = 2.4 V to 3.0 V, 10% to 90%

Figure 13. GPIO Timing Diagram



AC Amplifier Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Settling times, slew rates, and gain bandwidth are based on the analog continuous time PSoC block.

Table 26. 5-V and 3.3-V AC Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units
t_{COMP1}	Comparator mode response time, 50 mVpp signal centered on Ref	–	–	100	ns
t_{COMP2}	Comparator mode response time, 2.5 V input, 0.5 V overdrive	–	–	300	ns

Table 27. 2.7-V AC Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units
t_{COMP1}	Comparator mode response time, 50 mVpp signal centered on Ref	–	–	600	ns
t_{COMP2}	Comparator mode response time, 1.5 V input, 0.5 V overdrive	–	–	300	ns

Table 29. 2.7-V AC Digital Block Specifications

Function	Description	Min	Typ	Max	Units	Notes
All functions	Block input clock frequency	–	–	12.7	MHz	2.4 V < V_{DD} < 3.0 V.
Timer	Capture pulse width	100[28]	–	–	ns	
	Input clock frequency, with or without capture	–	–	12.7	MHz	
Counter	Enable input pulse width	100	–	–	ns	
	Input clock frequency, no enable input	–	–	12.7	MHz	
	Input clock frequency, enable input	–	–	12.7	MHz	
Dead band	Kill pulse width:					
	Asynchronous restart mode	20	–	–	ns	
	Synchronous restart mode	100	–	–	ns	
	Disable mode	100	–	–	ns	
	Input clock frequency	–	–	12.7	MHz	
CRCPRS (PRS mode)	Input clock frequency	–	–	12.7	MHz	
CRCPRS (CRC mode)	Input clock frequency	–	–	12.7	MHz	
SPIM	Input clock frequency	–	–	6.35	MHz	The SPI serial clock (SCLK) frequency is equal to the input clock frequency divided by 2.
SPIS	Input clock (SCLK) frequency	–	–	4.1	MHz	
	Width of SS_ Negated between transmissions	100	–	–	ns	
Transmitter	Input clock frequency	–	–	12.7	MHz	The baud rate is equal to the input clock frequency divided by 8.
Receiver	Input clock frequency	–	–	12.7	MHz	The baud rate is equal to the input clock frequency divided by 8.

Note
28. 100 ns minimum input pulse width is based on the input synchronizers running at 12 MHz (84 ns nominal period).

AC External Clock Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 30. 5-V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency	0.093	–	24.6	MHz	
–	High period	20.6	–	5300	ns	
–	Low period	20.6	–	–	ns	
–	Power-up IMO to switch	150	–	–	µs	

Table 31. 3.3-V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency with CPU clock divide by 1	0.093	–	12.3	MHz	Maximum CPU frequency is 12 MHz at 3.3 V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements.
F_{OSCEXT}	Frequency with CPU clock divide by 2 or greater	0.186	–	24.6	MHz	If the frequency of the external clock is greater than 12 MHz, the CPU clock divider must be set to 2 or greater. In this case, the CPU clock divider ensures that the fifty percent duty cycle requirement is met.
–	High period with CPU clock divide by 1	41.7	–	5300	ns	
–	Low period with CPU clock divide by 1	41.7	–	–	ns	
–	Power-up IMO to switch	150	–	–	µs	

Table 32. 2.7-V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency with CPU clock divide by 1	0.093	–	6.06	MHz	Maximum CPU frequency is 3 MHz at 2.7 V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements.
F_{OSCEXT}	Frequency with CPU clock divide by 2 or greater	0.186	–	12.12	MHz	If the frequency of the external clock is greater than 3 MHz, the CPU clock divider must be set to 2 or greater. In this case, the CPU clock divider ensures that the fifty percent duty cycle requirement is met.
–	High period with CPU clock divide by 1	83.4	–	5300	ns	
–	Low period with CPU clock divide by 1	83.4	–	–	ns	
–	Power-up IMO to switch	150	–	–	µs	

Figure 16. 16-Pin (150-Mil) SOIC

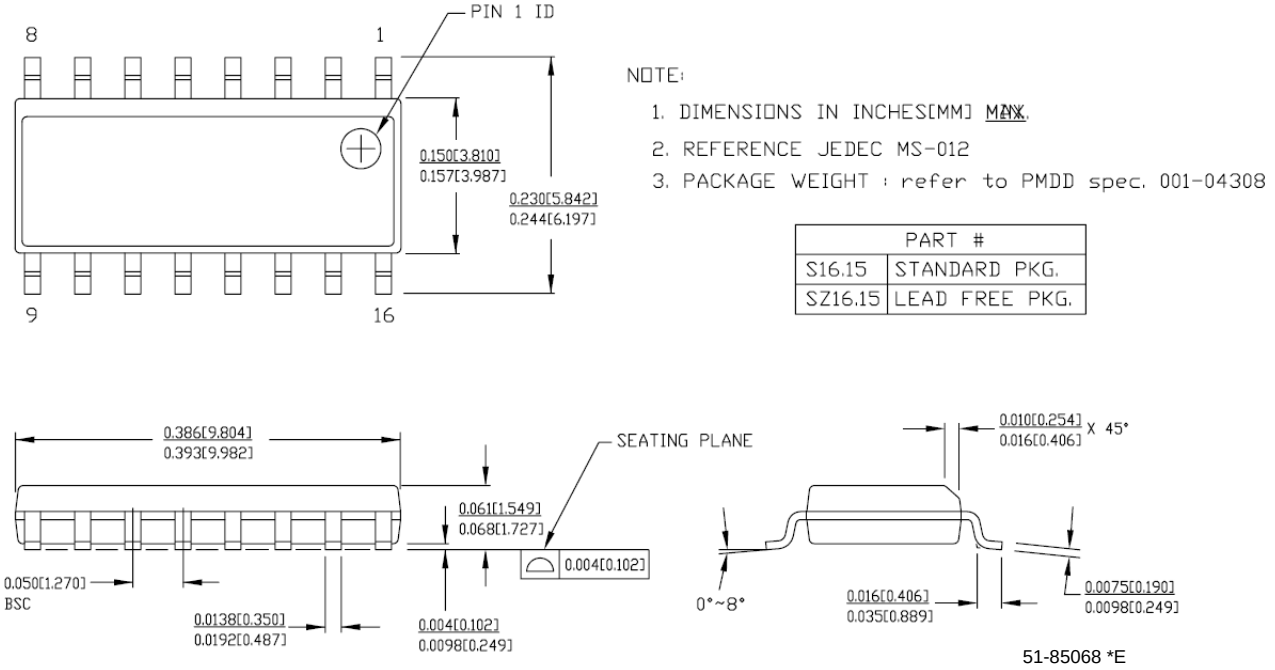
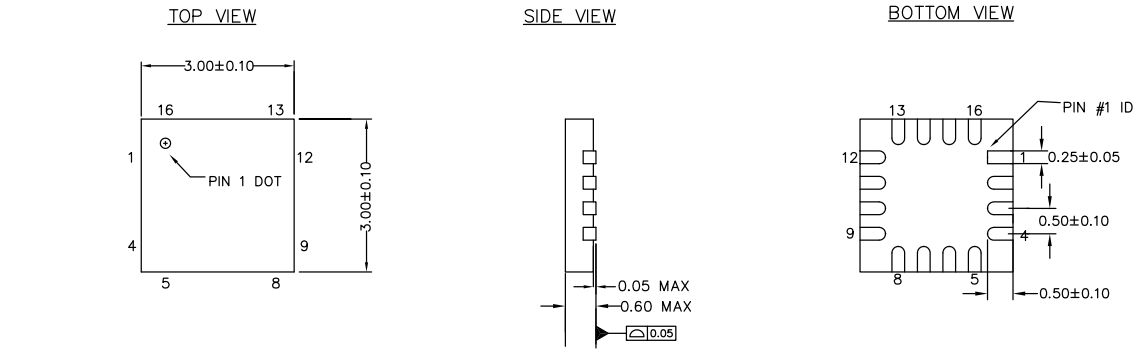


Figure 17. 16-Pin QFN with no E-Pad



NOTES
1. REFERENCE JEDEC # MO-220
2. ALL DIMENSIONS ARE IN MILLIMETERS

001-09116 *J

Figure 18. 20-pin SSOP (210 Mils) O20.21 Package Outline, 51-85077

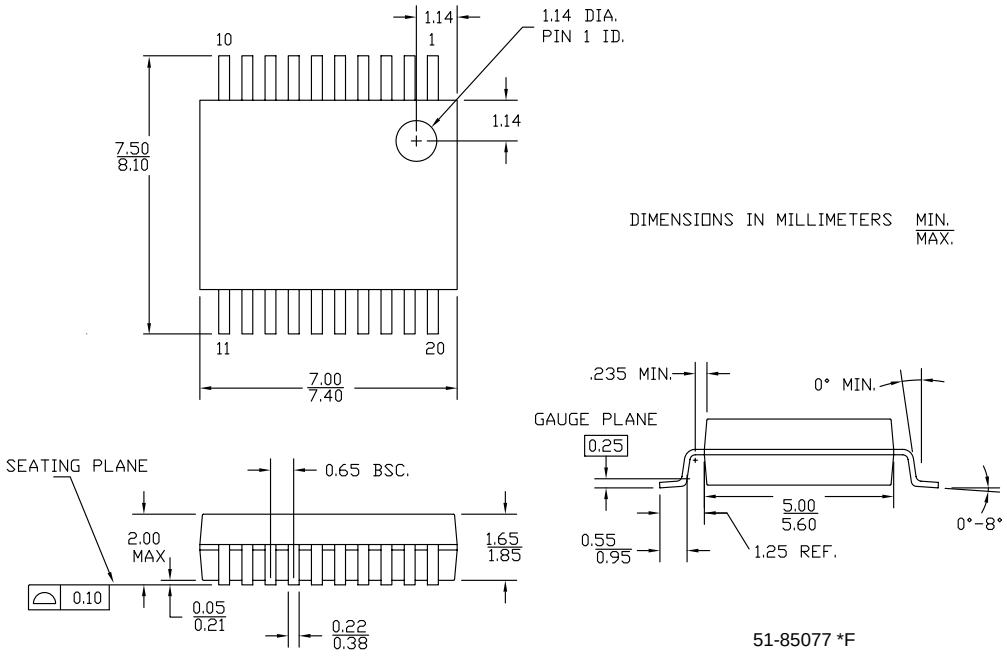
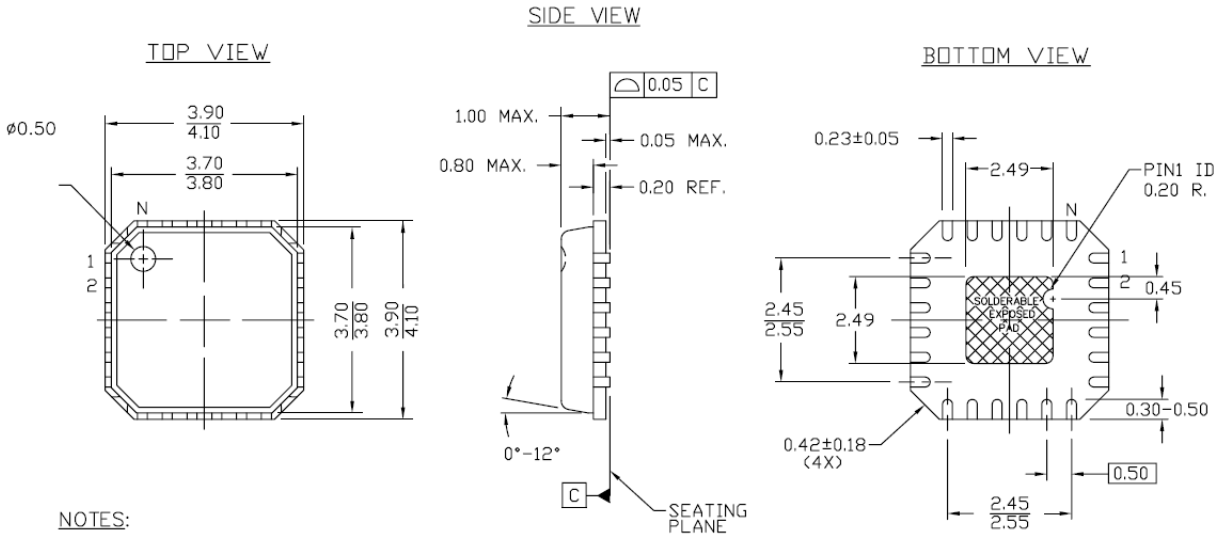


Figure 19. 24-Pin (4 × 4) QFN (Punched)



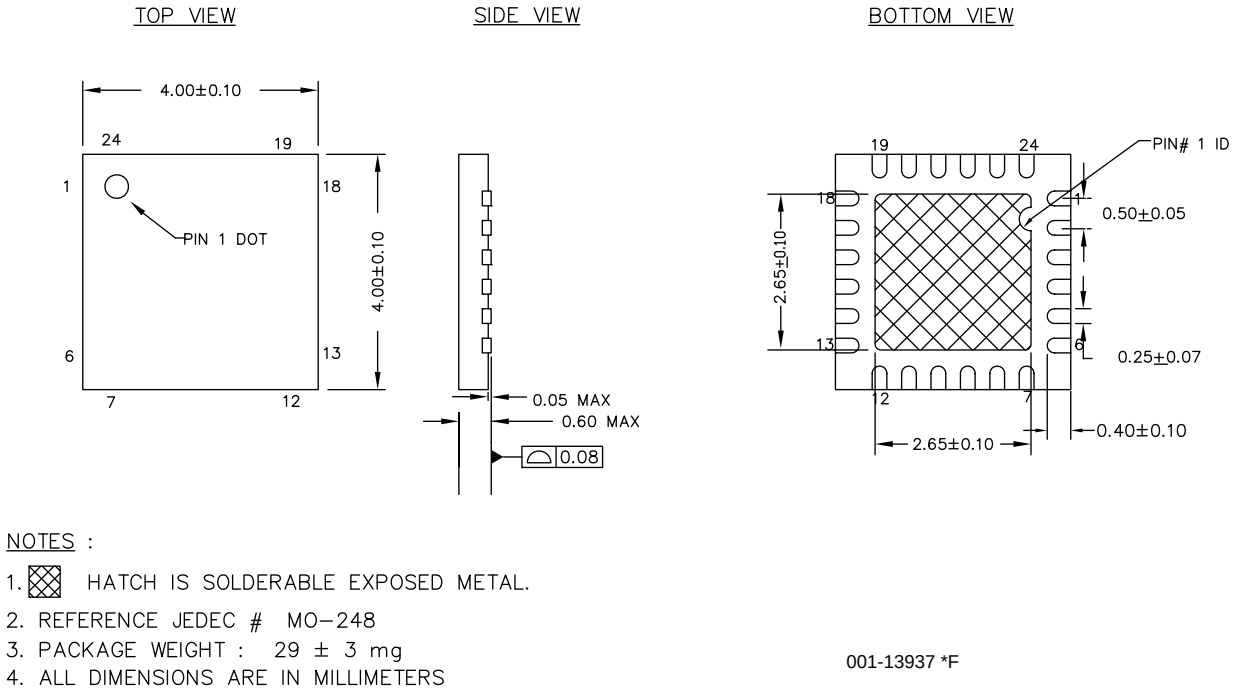
NOTES:

1. HATCH IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO-220
3. PACKAGE WEIGHT: REFER TO PMDD SPEC.
4. ALL DIMENSIONS ARE IN MM [MIN/MAX]
5. PACKAGE CODE

PART #	DESCRIPTION
LF24A	STANDARD
LY24A	LEAD FREE

51-85203 *D

Figure 20. 24-Pin (4 × 4) QFN (Sawn)



NOTES :

1. HATCH IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC # MO−248
3. PACKAGE WEIGHT : 29 ± 3 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-13937 *F

Important Note For information on the preferred dimensions for mounting QFN packages, refer the application note, Application Notes for Surface Mount Assembly of Amkor's MicroLeadFrame (MLF) Packages available at http://www.amkor.com.

Note that pinned vias for thermal conduction are not required for the low power 24, 32, and 48-pin QFN PSoC devices.

Thermal Impedances

Table 36. Thermal Impedances per Package

Package	Typical θ_{JA} [31]
8-pin SOIC	186 °C/W
16-pin SOIC	125 °C/W
16-pin QFN	46 °C/W
20-pin SSOP	117 °C/W
24-pin QFN[32]	40 °C/W

Solder Reflow Specifications

Table 37 shows the solder reflow temperature limits that must not be exceeded.

Table 37. Solder Reflow Specifications

Package	Maximum Peak Temperature (T_C)	Maximum Time above T_C – 5 °C
8-pin SOIC	260 °C	30 seconds
16-pin SOIC	260 °C	30 seconds
16-pin QFN	260 °C	30 seconds
20-pin SSOP	260 °C	30 seconds
24-pin QFN	260 °C	30 seconds

Notes
31. $T_J = T_A + POWER \times \theta_{JA}$
32. To achieve the thermal impedance specified for the QFN package, refer to "Application Notes for Surface Mount Assembly of Amkor's MicroLeadFrame (MLF) Packages" available at http://www.amkor.com.
33. Higher temperatures may be required based on the solder melting point. Typical temperatures for solder are 220+/-5 °C with Sn-Pb or 245+/-5 °C with Sn-Ag-Cu paste. Refer to the solder manufacturer specifications.

Glossary (continued)

shift register	A memory storage device that sequentially shifts a word either left or right to output a stream of serial data.
slave device	A device that allows another device to control the timing for data exchanges between two devices. Or when devices are cascaded in width, the slave device is the one that allows another device to control the timing of data exchanges between the cascaded devices and an external interface. The controlling device is called the master device.
SRAM	An acronym for static random access memory. A memory device where you can store and retrieve data at a high rate of speed. The term static is used because, after a value is loaded into an SRAM cell, it remains unchanged until it is explicitly altered or until power is removed from the device.
SROM	An acronym for supervisory read only memory. The SROM holds code that is used to boot the device, calibrate circuitry, and perform Flash operations. The functions of the SROM may be accessed in normal user code, operating from Flash.
stop bit	A signal following a character or block that prepares the receiving device to receive the next character or block.
synchronous	1. A signal whose data is not acknowledged or acted upon until the next active edge of a clock signal. 2. A system whose operation is synchronized by a clock signal.
tri-state	A function whose output can adopt three states: 0, 1, and Z (high-impedance). The function does not drive any value in the Z state and, in many respects, may be considered to be disconnected from the rest of the circuit, allowing another output to drive the same net.
UART	A UART or universal asynchronous receiver-transmitter translates between parallel bits of data and serial bits.
user modules	Pre-build, pre-tested hardware/firmware peripheral functions that take care of managing and configuring the lower level Analog and Digital PSoC Blocks. User Modules also provide high level ***API (Application Programming Interface)*** for the peripheral function.
user space	The bank 0 space of the register map. The registers in this bank are more likely to be modified during normal program execution and not just during initialization. Registers in bank 1 are most likely to be modified only during the initialization phase of the program.
V_{DD}	A name for a power net meaning "voltage drain." The most positive power supply signal. Usually 5 V or 3.3 V.
V_{SS}	A name for a power net meaning "voltage source." The most negative power supply signal.
watchdog timer	A timer that must be serviced periodically. If it is not serviced, the CPU resets after a specified period of time.

Errata

This section describes the errata for the CY8C21x23 PSoC® programmable system-on-chip family. Details include errata trigger conditions, scope of impact, available workarounds, and silicon revision applicability.

Contact your local Cypress Sales Representative if you have questions.

Part Numbers Affected

Part Number	Ordering Information
CY8C21123	CY8C21123-24SXI
	CY8C21123-24SXIT
	CY8C21223-24SXI
	CY8C21223-24SXIT
	CY8C21323-24PVXI
	CY8C21323-24PVXIT
	CY8C21323-24LFXI
	CY8C21323-24LFXIT
	CY8C21323-24LQXI
	CY8C21323-24LQXIT

CY8C21123 Qualification Status

Product Status: Production

CY8C21123 Errata Summary

The following table defines the errata applicability to available CY8C21123 family devices. An "X" indicates that the errata pertains to the selected device.

Note Errata items, in the table below, are hyperlinked. Click on any item entry to jump to its description.

Items	Part Number	Silicon Revision	Fix Status
[1.] Internal Main Oscillator (IMO) Tolerance Deviation at Temperature Extremes	CY8C21123	A	No silicon fix is planned. Workaround is required.

1. Internal Main Oscillator (IMO) Tolerance Deviation at Temperature Extremes

- **Problem Definition**
  Asynchronous Digital Communications Interfaces may fail framing beyond 0 to 70 °C. This problem does not affect end-product usage between 0 and 70 °C.
- **Parameters Affected**
  The IMO frequency tolerance. The worst case deviation when operated below 0 °C and above +70 °C and within the upper and lower datasheet temperature range is ±5%.
- **Trigger Condition(S)**
  The asynchronous Rx/Tx clock source IMO frequency tolerance may deviate beyond the data sheet limit of ±2.5% when operated beyond the temperature range of 0 to +70 °C.
- **Scope of Impact**
  This problem may affect UART, IrDA, and FSK implementations.
- **Workaround**
  Implement a quartz crystal stabilized clock source on at least one end of the asynchronous digital communications interface.
- **Fix Status**
  No silicon fix is planned. The workaround mentioned above should be used.

Document History Page

Document Title: CY8C21123/CY8C21223/CY8C21323, PSoC® Programmable System-on-Chip™ Document Number: 38-12022				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	133248	NWJ	See ECN	New silicon and document (Revision **).
*A	208900	NWJ	See ECN	Add new part, new package and update all ordering codes to Pb-free.
*B	212081	NWJ	See ECN	Expand and prepare Preliminary version.
*C	227321	CMS Team	See ECN	Update specs., data, format.
*D	235973	SFV	See ECN	Updated Overview and Electrical Spec. chapters, along with 24-pin pinout. Added CMP_GO_EN register (1,64h) to mapping table.
*E	290991	HMT	See ECN	Update datasheet standards per SFV memo. Fix device table. Add part numbers to pinouts and fine tune. Change 20-pin SSOP to CY8C21323. Add Reflow Temp. table. Update diagrams and specs.
*F	301636	HMT	See ECN	DC Chip-Level Specification changes. Update links to new CY.com Portal.
*G	324073	HMT	See ECN	Obtained clearer 16 SOIC package. Update Thermal Impedances and Solder Reflow tables. Re-add pinout ISSP notation. Fix ADC type-o. Fix TMP register names. Update Electrical Specifications. Add CY logo. Update CY copyright. Make datasheet Final.
*H	2588457	KET / HMI / AESA	10/22/2008	New package information on page 9. Converted datasheet to new template. Added 16-Pin OFN package diagram.
*I	2618175	OGNE / PYRS	12/09/2008	Added Note in Ordering Information Section. Changed title from PSoC Mixed-Signal Array to PSoC Programmable System-on-Chip. Updated ‘Development Tools’ and ‘Designing with PSoC Designer’ sections on pages 5 and 6
*J	2682782	MAXK / AESA	04/03/2009	Corrected 16 COL pinout.
*K	2699713	MAXK	04/29/2009	Minor ECN to correct paragraph style of 16 COL Pinout. No change in content.
*L	2762497	JVY	09/11/2009	Updated DC GPIO, AC Chip-Level, and AC Programming Specifications as follows: Modified F_{IMO6} and T_{WRITE} specifications. Replaced T_{RAMP} time) specification with SR_{POWER_UP} (slew rate) specification. Added note [11] to Flash Endurance specification. Added I_{OH}, I_{OL}, DC_{ILO}, F_{32K_U}, $T_{POWERUP}$, $T_{ERASEALL}$, $T_{PROGRAM\_HOT}$, and $T_{PROGRAM\_COLD}$ specifications..
*M	2792630	TTO	10/26/2009	Updated ordering information for CY8C21223-24LGXI to indicate availability of XRES pin.
*N	2901653	NJF	03/30/2010	Changed 16-pin COL to 16-pin QFN in the datasheet. Added Contents. Updated links in Sales, Solutions, and Legal Information Updated Cypress website links. Added $T_{BAKETEMP}$ and $T_{BAKETIME}$ parameters in Absolute Maximum Ratings Updated 5-V and 3.3-V AC Chip-Level Specifications Updated Notes in Packaging Information and package diagrams. Updated Ordering Code Definitions
*O	2928895	YJI	05/06/2010	No technical updates. Included with EROS spec.

Document History Page (continued)

Document Title: CY8C21123/CY8C21223/CY8C21323, PSoC® Programmable System-on-Chip™ Document Number: 38-12022				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*P	3044869	NJF	10/01/2010	Added PSoC Device Characteristics table. Added DC I^2C Specifications table. Added F_{32K_U} max limit. Added Tjit_IMO specification, removed existing jitter specifications. Updated Units of Measure, Acronyms, Glossary, and References sections. Updated solder reflow specifications. No specific changes were made to AC Digital Block Specifications table and I^2C Timing Diagram. They were updated for clearer understanding. Updated Figure 13 since the labelling for y-axis was incorrect. Template and styles update.
*Q	3263669	YJI	05/23/2011	Updated 16-pin SOIC and 20-pin SSOP package diagrams. Updated Development Tool Selection and Designing with PSoC Designer sections.
*R	3383787	GIR	09/26/2011	The text “Pin must be left floating” is included under Description of NC pin in Table 6 on page 11. Updated Table 37 on page 35 for improved clarity.
*S	3558729	RJVB	03/22/2012	Updated 16-pin SOIC package.
*T	3598261	LURE / XZNG	04/24/2012	Changed the PWM description string from “8- to 32-bit” to “8- and 16-bit”.
*U	3649990	BVI / YLIU	06/19/2012	Updated description of NC pin as “No Connection. Pin must be left floating”
*V	3873870	UVS	01/18/2013	Updated Packaging Information: spec 51-85068 – Changed revision from *D to *E. spec 001-09116 – Changed revision from *F to *G. spec 51-85203 – Changed revision from *C to *D.
*W	3993321	UVS	05/07/2013	Added Errata.
*X	4067216	UVS	07/18/2013	Added Errata footnotes (Note 19). Updated Features: Replaced 2.5% with 5% under “Precision, programmable clocking”. Updated Electrical Specifications: Updated AC Electrical Characteristics: Updated AC Chip-Level Specifications: Added Note 19 and referred the same note in F_{IMO24} parameter. Updated minimum and maximum values of F_{IMO24} parameter. Updated AC Digital Block Specifications: Replaced all instances of maximum value “49.2” with “50.4” and “24.6” with “25.2” in Table 28. Updated Packaging Information: spec 51-85066 – Changed revision from *E to *F. spec 001-09116 – Changed revision from *G to *H. Updated to new template.
*Y	4479648	RJVB	08/20/2014	Updated Errata: Updated CY8C21123 Errata Summary: Updated details in “Fix Status” column in the table. Updated details in “Fix Status” bulleted point below the table.

Document History Page (continued)

Document Title: CY8C21123/CY8C21223/CY8C21323, PSoC® Programmable System-on-Chip™ Document Number: 38-12022				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*Z	4623500	DIMA	01/14/2015	Updated Pin Information: Updated 20-Pin Part Pinout: Updated Table 5: Added Note 6 and referred the same note in description of pin 5 and pin 10. Updated 24-Pin Part Pinout: Updated Table 6: Added Note 9 and referred the same note in description of pin 3, pin 9 and pin 21. Updated Packaging Information: spec 51-85066 – Changed revision from *F to *G. spec 51-85077 – Changed revision from *E to *F. Completing Sunset Review.
AA	5090662	ARVI	01/18/2016	Updated Ordering Information, Ordering Code Definitions, and Errata. Upated figure title in Figure 19. Updated Table 38. Updated Figure 15 (spec 51-85066 *G to *H) in Packaging Information. Added Figure 20 (spec 001-13937 *F) in Packaging Information.

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