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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	6
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.25V
Data Converters	A/D 8x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	8-SOIC (0.154", 3.90mm Width)
Supplier Device Package	8-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c21123-24sxit

Contents

Analog System

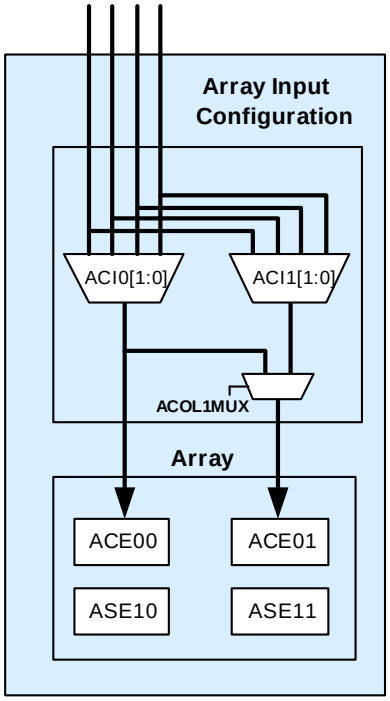
The analog system consists of four configurable blocks to allow creation of complex analog signal flows. Analog peripherals are very flexible and may be customized to support specific application requirements. Some of the more common PSoC analog functions (most available as user modules) are:

- Analog-to-digital converters (single or dual, with 8-bit or 10-bit resolution)
- Pin-to-pin comparators (one)
- Single-ended comparators (up to 2) with absolute (1.3 V) reference or 8-bit DAC reference
- 1.3 V reference (as a system resource)

In most PSoC devices, analog blocks are provided in columns of three, which includes one CT (continuous time) and two SC (switched capacitor) blocks. The CY8C21x23 devices provide limited functionality Type “E” analog blocks. Each column contains one CT block and one SC block.

The number of blocks on the device family is listed in Table 1 on page 5.

Figure 2. CY8C21x23 Analog System Block Diagram



Additional System Resources

System resources, some of which listed in the previous sections, provide additional capability useful to complete systems. Additional resources include a switch mode pump, low voltage detection, and power on reset. The merits of each system resource are.

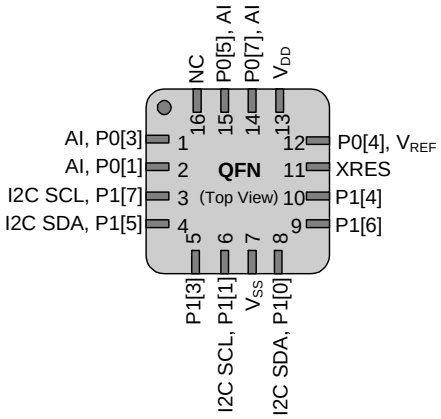
- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks can be routed to both the digital and analog systems. Additional clocks can be generated using digital PSoC blocks as clock dividers.
- The I^2C module provides 100 and 400 kHz communication over two wires. Slave, master, and multi-master modes are all supported.
- LVD interrupts can signal the application of falling voltage levels, while the advanced POR (power on reset) circuit eliminates the need for a system supervisor.
- An internal 1.3 V voltage reference provides an absolute reference for the analog system, including ADCs and DACs.
- An integrated switch mode pump (SMP) generates normal operating voltages from a single 1.2 V battery cell, providing a low cost boost converter.

Table 4. Pin Definitions – CY8C21223 16-Pin QFN with no E-Pad [4]

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O	I	P0[3]	Analog column mux input
2	I/O	I	P0[1]	Analog column mux input
3	I/O		P1[7]	I^2C SCL
4	I/O		P1[5]	I^2C SDA
5	I/O		P1[3]	
6	I/O		P1[1]	I^2C SCL, ISSP-SCLK[5]
7	Power		V_{SS}	Ground connection
8	I/O		P1[0]	I^2C SDA, ISSP-SDATA[5]
9	I/O		P1[6]	
10	I/O		P1[4]	EXTCLK
11	Input		XRES	Active high external reset with internal pull-down
12	I/O	I	P0[4]	V_{REF}
13	Power		V_{DD}	Supply voltage
14	I/O	I	P0[7]	Analog column mux input
15	I/O	I	P0[5]	Analog column mux input
16			NC	No Connection. Pin must be left floating

LEGEND A = Analog, I = Input, and O = Output.

Figure 5. CY8C21223 16-Pin QFN



Notes
4. The center pad on the QFN package must be connected to ground (Vss) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.
5. These are the ISSP pins, which are not high Z at POR (power on reset). See the PSoC Technical Reference Manual for details.

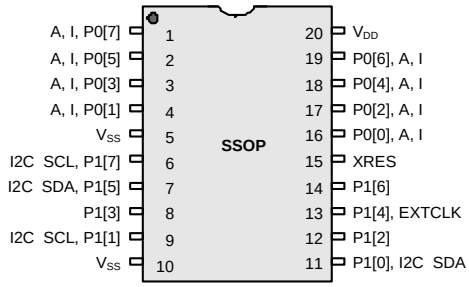
20-Pin Part Pinout

Table 5. Pin Definitions – CY8C21323 20-Pin SSOP

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O	I	P0[7]	Analog column mux input
2	I/O	I	P0[5]	Analog column mux input
3	I/O	I	P0[3]	Analog column mux input
4	I/O	I	P0[1]	Analog column mux input
5	Power		V_{SS}	Ground connection[6]
6	I/O		P1[7]	I^2C SCL
7	I/O		P1[5]	I^2C SDA
8	I/O		P1[3]	
9	I/O		P1[1]	I^2C SCL, ISSP-SCLK[7]
10	Power		V_{SS}	Ground connection[6]
11	I/O		P1[0]	I^2C SDA, ISSP-SDATA[7]
12	I/O		P1[2]	
13	I/O		P1[4]	Optional EXTCLK input
14	I/O		P1[6]	
15	Input		XRES	Active high external reset with internal pull-down
16	I/O	I	P0[0]	Analog column mux input
17	I/O	I	P0[2]	Analog column mux input
18	I/O	I	P0[4]	Analog column mux input
19	I/O	I	P0[6]	Analog column mux input
20	Power		V_{DD}	Supply voltage

LEGEND A = Analog, I = Input, and O = Output.

Figure 6. CY8C21323 20-Pin SSOP



Notes
6. All V_{SS} pins should be brought out to one common GND plane.
7. These are the ISSP pins, which are not high Z at POR (power on reset). See the PSoC Technical Reference Manual for details.

Table 8. Register Map Bank 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW		40		ASE10CR0	80	RW		C0	
PRT0IE	01	RW		41			81			C1	
PRT0GS	02	RW		42			82			C2	
PRT0DM2	03	RW		43			83			C3	
PRT1DR	04	RW		44		ASE11CR0	84	RW		C4	
PRT1IE	05	RW		45			85			C5	
PRT1GS	06	RW		46			86			C6	
PRT1DM2	07	RW		47			87			C7	
	08			48			88			C8	
	09			49			89			C9	
	0A			4A			8A			CA	
	0B			4B			8B			CB	
	0C			4C			8C			CC	
	0D			4D			8D			CD	
	0E			4E			8E			CE	
	0F			4F			8F			CF	
	10			50			90			D0	
	11			51			91			D1	
	12			52			92			D2	
	13			53			93			D3	
	14			54			94			D4	
	15			55			95			D5	
	16			56			96		I2C_CFG	D6	RW
	17			57			97		I2C_SCR	D7	#
	18			58			98		I2C_DR	D8	RW
	19			59			99		I2C_MSCR	D9	#
	1A			5A			9A		INT_CLR0	DA	RW
	1B			5B			9B		INT_CLR1	DB	RW
	1C			5C			9C			DC	
	1D			5D			9D		INT_CLR3	DD	RW
	1E			5E			9E		INT_MSK3	DE	RW
	1F			5F			9F			DF	
DBB00DR0	20	#	AMX_IN	60	RW		A0		INT_MSK0	E0	RW
DBB00DR1	21	W		61			A1		INT_MSK1	E1	RW
DBB00DR2	22	RW	PWM_CR	62	RW		A2		INT_VC	E2	RC
DBB00CR0	23	#		63			A3		RES_WDT	E3	W
DBB01DR0	24	#	CMP_CR0	64	#		A4			E4	
DBB01DR1	25	W		65			A5			E5	
DBB01DR2	26	RW	CMP_CR1	66	RW		A6		DEC_CR0	E6	RW
DBB01CR0	27	#		67			A7		DEC_CR1	E7	RW
DCB02DR0	28	#	ADC0_CR	68	#		A8			E8	
DCB02DR1	29	W	ADC1_CR	69	#		A9			E9	
DCB02DR2	2A	RW		6A			AA			EA	
DCB02CR0	2B	#		6B			AB			EB	
DCB03DR0	2C	#	TMP_DR0	6C	RW		AC			EC	
DCB03DR1	2D	W	TMP_DR1	6D	RW		AD			ED	
DCB03DR2	2E	RW	TMP_DR2	6E	RW		AE			EE	
DCB03CR0	2F	#	TMP_DR3	6F	RW		AF			EF	

Blank fields are Reserved and must not be accessed. # Access is bit specific.

Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8C21x23 PSoC device. For up to date electrical specifications, check if you have the latest datasheet by visiting the web at http://www.cypress.com.

Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted.

Refer to Table 24 on page 25 for the electrical specifications on the IMO using SLIMO mode.

Figure 10. Voltage versus CPU Frequency

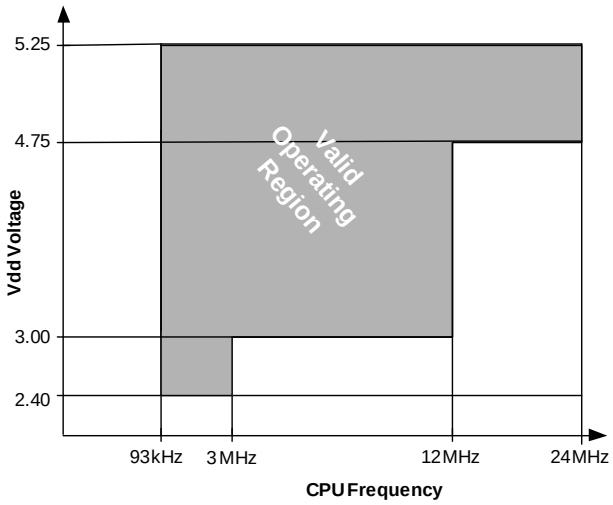
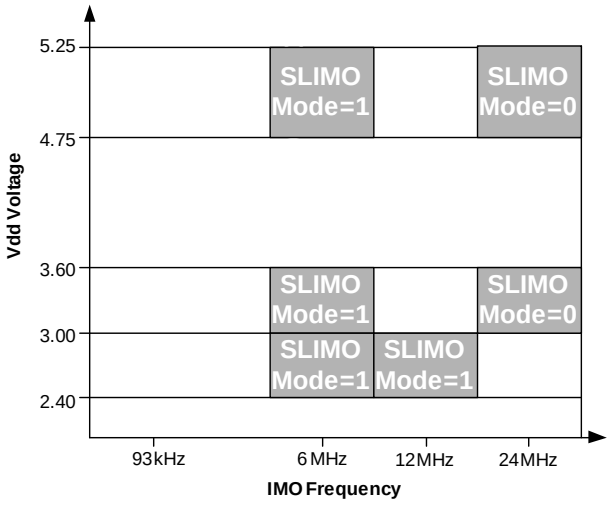


Figure 11. Voltage versus IMO Frequency



Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Table 10. Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units	Notes
T_{STG}	Storage temperature	–55	–	+100	°C	Higher storage temperatures reduce data retention time. Recommended storage temperature is +25 °C ± 25 °C. Extended duration storage temperatures higher than 65 °C degrade reliability.
$T_{BAKETEMP}$	Bake temperature	–	125	See package label	°C	
$t_{BAKETIME}$	Bake time	See package label	–	72	Hours	
T_A	Ambient temperature with power applied	–40	–	+85	°C	
V_{DD}	Supply voltage on V_{DD} relative to V_{SS}	–0.5	–	+6.0	V	
V_{IO}	DC input voltage	V_{SS} – 0.5	–	V_{DD} + 0.5	V	
V_{IOZ}	DC voltage applied to tristate	V_{SS} – 0.5	–	V_{DD} + 0.5	V	
I_{MIO}	Maximum current into any port pin	–25	–	+50	mA	
ESD	Electro static discharge voltage	2000	–	–	V	Human body model ESD
LU	Latch-up current	–	–	200	mA	

Operating Temperature

Table 11. Operating Temperature

Symbol	Description	Min	Typ	Max	Units	Notes
T_A	Ambient temperature	–40	–	+85	°C	
T_J	Junction temperature	–40	–	+100	°C	The temperature rise from ambient to junction is package specific. See Table 36 on page 35. You must limit the power consumption to comply with this requirement.

DC Electrical Characteristics

DC Chip-Level Specifications

Table 12 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 12. DC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{DD}	Supply voltage	2.40	–	5.25	V	See DC POR and LVD specifications, Table 19 on page 21.
I_{DD}	Supply current, IMO = 24 MHz	–	3	4	mA	Conditions are V_{DD} = 5.0 V, 25 °C, CPU = 3 MHz, SYSCLK doubler disabled. VC1 = 1.5 MHz VC2 = 93.75 kHz VC3 = 0.366 kHz
I_{DD3}	Supply current, IMO = 6 MHz	–	1.2	2	mA	Conditions are V_{DD} = 3.3 V, 25 °C, CPU = 3 MHz, clock doubler disabled. VC1 = 375 kHz VC2 = 23.4 kHz VC3 = 0.091 kHz
I_{DD27}	Supply current, IMO = 6 MHz	–	1.1	1.5	mA	Conditions are V_{DD} = 2.55 V, 25 °C, CPU = 3 MHz, clock doubler disabled. VC1 = 375 kHz VC2 = 23.4 kHz VC3 = 0.091 kHz
I_{SB27}	Sleep (mode) current with POR, LVD, sleep timer, WDT, and internal slow oscillator active. Mid temperature range.	–	2.6	4	µA	V_{DD} = 2.55 V, 0 °C to 40 °C
I_{SB}	Sleep (mode) current with POR, LVD, sleep timer, WDT, and internal slow oscillator active.	–	2.8	5	µA	V_{DD} = 3.3 V, –40 °C ≤ T_A ≤ 85 °C
V_{REF}	Reference voltage (bandgap)	1.28	1.30	1.32	V	Trimmed for appropriate V_{DD}. V_{DD} = 3.0 V to 5.25 V
V_{REF27}	Reference voltage (bandgap)	1.16	1.30	1.330	V	Trimmed for appropriate V_{DD}. V_{DD} = 2.4 V to 3.0 V
AGND	Analog ground	V_{REF} – 0.003	V_{REF}	V_{REF} + 0.003	V	

DC Switch Mode Pump Specifications

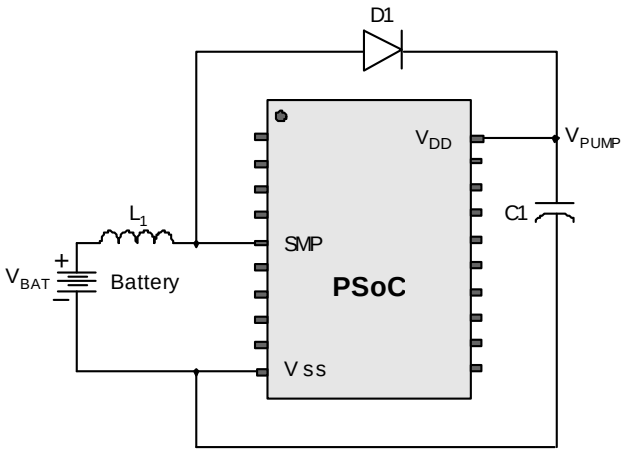
Table 18 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 18. DC Switch Mode Pump (SMP) Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{PUMP5V}	5 V output voltage from pump	4.75	5.0	5.25	V	Configuration of footnote.[11] Average, neglecting ripple. SMP trip voltage is set to 5.0 V.
V_{PUMP3V}	3.3 V output voltage from pump	3.00	3.25	3.60	V	Configuration of footnote.[11] Average, neglecting ripple. SMP trip voltage is set to 3.25 V.
V_{PUMP2V}	2.6 V output voltage from pump	2.45	2.55	2.80	V	Configuration of footnote.[11] Average, neglecting ripple. SMP trip voltage is set to 2.55 V.
I_{PUMP}	Available output current V_{BAT} = 1.8 V, V_{PUMP} = 5.0 V V_{BAT} = 1.5 V, V_{PUMP} = 3.25 V V_{BAT} = 1.3 V, V_{PUMP} = 2.55 V	 5 8 8	 – – –	 – – –	 mA mA mA	Configuration of footnote.[11] SMP trip voltage is set to 5.0 V. SMP trip voltage is set to 3.25 V. SMP trip voltage is set to 2.55 V.
V_{BAT5V}	Input voltage range from battery	1.8	–	5.0	V	Configuration of footnote.[11] SMP trip voltage is set to 5.0 V.
V_{BAT3V}	Input voltage range from battery	1.0	–	3.3	V	Configuration of footnote.[11] SMP trip voltage is set to 3.25 V.
V_{BAT2V}	Input voltage range from battery	1.0	–	2.8	V	Configuration of footnote.[11] SMP trip voltage is set to 2.55 V.
$V_{BATSTART}$	Minimum input voltage from battery to start pump	1.2	–	–	V	Configuration of footnote.[11] 0 °C ≤ T_A ≤ 100. 1.25 V at T_A = –40 °C.
ΔV_{PUMP_Line}	Line regulation (over Vi range)	–	5	–	$\%V_O$	Configuration of footnote.[11] V_O is the "V_{DD} Value for PUMP Trip" specified by the VM[2:0] setting in the DC POR and LVD Specification, Table 19 on page 21.
ΔV_{PUMP_Load}	Load regulation	–	5	–	$\%V_O$	Configuration of footnote.[11] V_O is the "V_{DD} Value for PUMP Trip" specified by the VM[2:0] setting in the DC POR and LVD Specification, Table 19 on page 21.
ΔV_{PUMP_Ripple}	Output voltage ripple (depends on cap/load)	–	100	–	mVpp	Configuration of footnote.[11] Load is 5 mA.
E_3	Efficiency	35	50	–	%	Configuration of footnote.[11] Load is 5 mA. SMP trip voltage is set to 3.25 V.
E_2	Efficiency	35	80	–	%	For I load = 1 mA, V_{PUMP} = 2.55 V, V_{BAT} = 1.3 V, 10 uH inductor, 1 uF capacitor, and Schottky diode.
F_{PUMP}	Switching frequency	–	1.3	–	MHz	
DC_{PUMP}	Switching duty cycle	–	50	–	%	

Note
11. L_1 = 2 mH inductor, C_1 = 10 mF capacitor, D_1 = Schottky diode. Refer to Figure 12 on page 21.

Figure 12. Basic Switch Mode Pump Circuit



DC POR and LVD Specifications

Table 19 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 19. DC POR and LVD Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
	V_{DD} value for PPOR trip					V_{DD} must be greater than or equal to 2.5 V during startup, reset from the XRES pin, or reset from watchdog.
V_{PPOR0}	PORLEV[1:0] = 00b	–	2.36	2.40	V	
V_{PPOR1}	PORLEV[1:0] = 01b	–	2.82	2.95	V	
V_{PPOR2}	PORLEV[1:0] = 10b	–	4.55	4.70	V	
	V_{DD} value for LVD trip					
V_{LVD0}	VM[2:0] = 000b	2.40	2.45	2.51[12]	V	
V_{LVD1}	VM[2:0] = 001b	2.85	2.92	2.99[13]	V	
V_{LVD2}	VM[2:0] = 010b	2.95	3.02	3.09	V	
V_{LVD3}	VM[2:0] = 011b	3.06	3.13	3.20	V	
V_{LVD4}	VM[2:0] = 100b	4.37	4.48	4.55	V	
V_{LVD5}	VM[2:0] = 101b	4.50	4.64	4.75	V	
V_{LVD6}	VM[2:0] = 110b	4.62	4.73	4.83	V	
V_{LVD7}	VM[2:0] = 111b	4.71	4.81	4.95	V	
	V_{DD} value for PUMP trip					
V_{PUMP0}	VM[2:0] = 000b	2.45	2.55	2.62[14]	V	
V_{PUMP1}	VM[2:0] = 001b	2.96	3.02	3.09	V	
V_{PUMP2}	VM[2:0] = 010b	3.03	3.10	3.16	V	
V_{PUMP3}	VM[2:0] = 011b	3.18	3.25	3.32[15]	V	
V_{PUMP4}	VM[2:0] = 100b	4.54	4.64	4.74	V	
V_{PUMP5}	VM[2:0] = 101b	4.62	4.73	4.83	V	
V_{PUMP6}	VM[2:0] = 110b	4.71	4.82	4.92	V	
V_{PUMP7}	VM[2:0] = 111b	4.89	5.00	5.12	V	

Notes
12. Always greater than 50 mV above V_{PPOR} (PORLEV = 00) for falling supply.
13. Always greater than 50 mV above V_{PPOR} (PORLEV = 01) for falling supply.
14. Always greater than 50 mV above V_{LVD0}.
15. Always greater than 50 mV above V_{LVD3}.

AC Electrical Characteristics

AC Chip-Level Specifications

Table 22 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 22. 5-V and 3.3-V AC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{IMO24} [19]	IMO frequency for 24 MHz	22.8	24	25.2 [20,21]	MHz	Trimmed for 5 V or 3.3 V operation using factory trim values. Refer to Figure 11 on page 16. SLIMO mode = 0.
F_{IMO6}	IMO frequency for 6 MHz	5.5	6	6.5[20,21]	MHz	Trimmed for 3.3 V operation using factory trim values. See Figure 11 on page 16. SLIMO mode = 1.
F_{CPU1}	CPU frequency (5 V nominal)	0.0937	24	24.6[20]	MHz	12 MHz only for SLIMO mode = 0.
F_{CPU2}	CPU frequency (3.3 V nominal)	0.0937	12	12.3[21]	MHz	SLIMO Mode = 0.
F_{BLK5}	Digital PSoC block frequency (5 V nominal)	0	48	49.2[20,22]	MHz	Refer to the section AC Digital Block Specifications on page 26.
F_{BLK33}	Digital PSoC block frequency (3.3 V nominal)	0	24	24.6[22]	MHz	
F_{32K1}	ILO frequency	15	32	64	kHz	
F_{32K_U}	ILO untrimmed frequency	5	–	100	kHz	After a reset and before the M8C starts to run, the ILO is not trimmed. See the system resets section of the PSoC Technical Reference Manual for details on this timing.
t_{XRST}	External reset pulse width	10	–	–	µs	
DC24M	24 MHz duty cycle	40	50	60	%	
DC_{ILO}	ILO duty cycle	20	50	80	%	
Step24M	24 MHz trim step size	–	50	–	kHz	
Fout48M	48 MHz output frequency	46.8	48.0	49.2[20,21]	MHz	Trimmed. Using factory trim values.
F_{MAX}	Maximum frequency of signal on row input or row output.	–	–	12.3	MHz	
SR_{POWER_UP}	Power supply slew rate	–	–	250	V/ms	V_{DD} slew rate during power-up.
$t_{POWERUP}$	Time from end of POR to CPU executing code	–	16	100	ms	Power-up from 0 V. See the system resets section of the PSoC Technical Reference Manual.
t_{jit_IMO}	24-MHz IMO cycle-to-cycle jitter (RMS) [23]	–	200	700	ps	
	24-MHz IMO long term N cycle-to-cycle jitter (RMS) [23]	–	300	900	ps	N = 32
	24-MHz IMO period jitter (RMS) [23]	–	100	400	ps	

Notes

19. Errata: When the device is operated within 0 °C to 70 °C, the frequency tolerance is reduced to ±2.5%, but if operated at extreme temperature (below 0 °C or above 70 °C), frequency tolerance deviates from ±2.5% to ±5%. For more information, see "Errata" on page 43.
20. 4.75 V < V_{DD} < 5.25 V.
21. 3.0 V < V_{DD} < 3.6 V. Refer to the application note, Adjusting PSoC Microcontroller Trims for Dual Voltage-Range Operation – AN2012 for more information on trimming for operation at 3.3 V.
22. See the individual user module datasheets for information on maximum frequencies for user modules.
23. Refer to the application note, Understanding Datasheet Jitter Specifications for Cypress Timing Products – AN5054 for more information on jitter specifications.

Table 23. 2.7-V AC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{IMO12}	IMO frequency for 12 MHz	11.5	12	12.7[24,25]	MHz	Trimmed for 2.7 V operation using factory trim values. See Figure 11 on page 16. SLIMO mode = 1.
F_{IMO6}	IMO frequency for 6 MHz	5.5	6	6.5[24,25]	MHz	Trimmed for 2.7 V operation using factory trim values. See Figure 11 on page 16. SLIMO mode = 1.
F_{CPU1}	CPU frequency (2.7 V nominal)	0.093	3	3.15[24]	MHz	24 MHz only for SLIMO mode = 0.
F_{BLK27}	Digital PSoC block frequency (2.7 V nominal)	0	12	12.5[24,25]	MHz	Refer to the section AC Digital Block Specifications on page 26.
F_{32K1}	ILO frequency	8	32	96	kHz	
F_{32K_U}	ILO untrimmed frequency	5	–	100	kHz	After a reset and before the M8C starts to run, the ILO is not trimmed. See the system resets section of the PSoC Technical Reference Manual for details on this timing.
t_{XRST}	External reset pulse width	10	–	–	µs	
DC_{ILO}	ILO duty cycle	20	50	80	%	
F_{MAX}	Maximum frequency of signal on row input or row output	–	–	12.3	MHz	
SR_{POWER_UP}	Power supply slew rate	–	–	250	V/ms	V_{DD} slew rate during power-up.
$t_{POWERUP}$	Time from end of POR to CPU executing code	–	16	100	ms	Power-up from 0 V. See the system resets section of the PSoC Technical Reference Manual.
t_{jit_IMO}	12-MHz IMO cycle-to-cycle jitter (RMS)[26]	–	400	1000	ps	
	12-MHz IMO long term N cycle-to-cycle jitter (RMS)[26]	–	600	1300	ps	N = 32
	12-MHz IMO period jitter (RMS)[26]	–	100	500	ps	

Notes
24. 2.4 V < V_{DD} < 3.0 V.
25. Refer to the application note Adjusting PSoC Microcontroller Trims for Dual Voltage-Range Operation – AN2012 for more information on maximum frequency for user modules.
26. Refer to the application note, Understanding Datasheet Jitter Specifications for Cypress Timing Products – AN5054 for more information on jitter specifications.

AC Digital Block Specifications

Table 28 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 28. 5-V and 3.3-V AC Digital Block Specifications

Function	Description	Min	Typ	Max	Unit	Notes
All functions	Block input clock frequency					
	V_{DD} ≥ 4.75 V	–	–	50.4	MHz	
	V_{DD} < 4.75 V	–	–	25.2	MHz	
Timer	Input clock frequency					
	No capture, V_{DD} ≥ 4.75 V	–	–	50.4	MHz	
	No capture, V_{DD} < 4.75 V	–	–	25.2	MHz	
	With capture	–	–	25.2	MHz	
	Capture pulse width	50[27]	–	–	ns	
Counter	Input clock frequency					
	No enable input, V_{DD} ≥ 4.75 V	–	–	50.4	MHz	
	No enable input, V_{DD} < 4.75 V	–	–	25.2	MHz	
	With enable input	–	–	25.2	MHz	
	Enable input pulse width	50[27]	–	–	ns	
Dead Band	Kill pulse width					
	Asynchronous restart mode	20	–	–	ns	
	Synchronous restart mode	50[27]	–	–	ns	
	Disable mode	50[27]	–	–	ns	
	Input clock frequency					
	V_{DD} ≥ 4.75 V	–	–	50.4	MHz	
	V_{DD} < 4.75 V	–	–	25.2	MHz	
CRCPRS (PRS Mode)	Input clock frequency					
	V_{DD} ≥ 4.75 V	–	–	50.4	MHz	
	V_{DD} < 4.75 V	–	–	25.2	MHz	
CRCPRS (CRC Mode)	Input clock frequency	–	–	25.2	MHz	
SPIM	Input clock frequency	–	–	8.2	MHz	The SPI serial clock (SCLK) frequency is equal to the input clock frequency divided by 2.
SPIS	Input clock (SCLK) frequency	–	–	4.1	MHz	The input clock is the SPI SCLK in SPIS mode.
	Width of SS_negated between transmissions	50[27]	–	–	ns	
Transmitter	Input clock frequency					The baud rate is equal to the input clock frequency divided by 8.
	V_{DD} ≥ 4.75 V, 2 stop bits	–	–	50.4	MHz	
	V_{DD} ≥ 4.75 V, 1 stop bit	–	–	25.2	MHz	
	V_{DD} < 4.75 V	–	–	25.2	MHz	
Receiver	Input clock frequency					The baud rate is equal to the input clock frequency divided by 8.
	V_{DD} ≥ 4.75 V, 2 stop bits	–	–	50.4	MHz	
	V_{DD} ≥ 4.75 V, 1 stop bit	–	–	25.2	MHz	
	V_{DD} < 4.75 V	–	–	25.2	MHz	

Note
27. 50 ns minimum input pulse width is based on the input synchronizers running at 24 MHz (42 ns nominal period).

AC External Clock Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 30. 5-V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency	0.093	–	24.6	MHz	
–	High period	20.6	–	5300	ns	
–	Low period	20.6	–	–	ns	
–	Power-up IMO to switch	150	–	–	µs	

Table 31. 3.3-V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency with CPU clock divide by 1	0.093	–	12.3	MHz	Maximum CPU frequency is 12 MHz at 3.3 V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements.
F_{OSCEXT}	Frequency with CPU clock divide by 2 or greater	0.186	–	24.6	MHz	If the frequency of the external clock is greater than 12 MHz, the CPU clock divider must be set to 2 or greater. In this case, the CPU clock divider ensures that the fifty percent duty cycle requirement is met.
–	High period with CPU clock divide by 1	41.7	–	5300	ns	
–	Low period with CPU clock divide by 1	41.7	–	–	ns	
–	Power-up IMO to switch	150	–	–	µs	

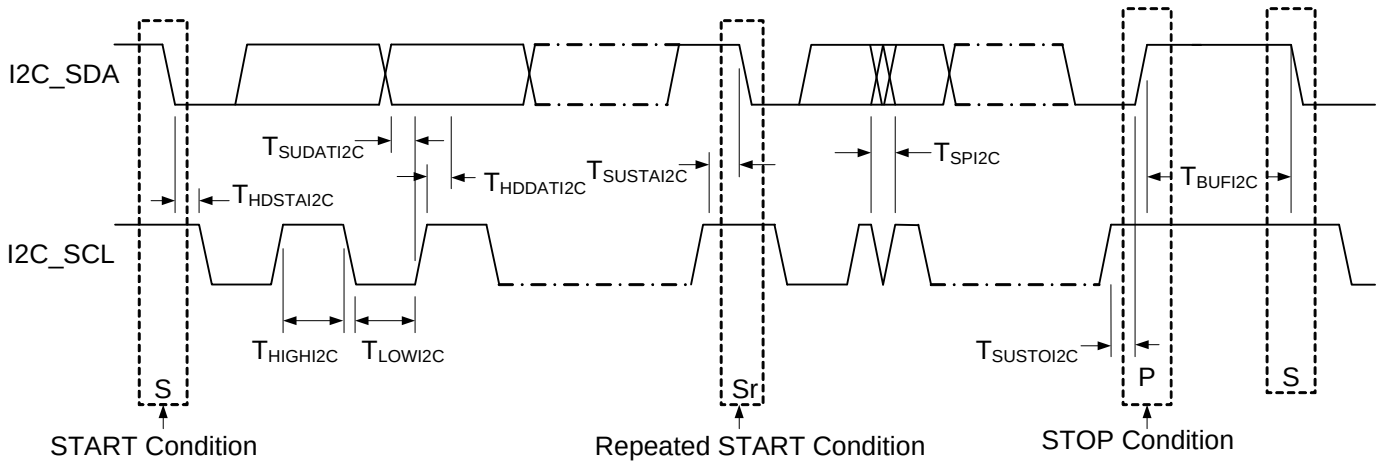
Table 32. 2.7-V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency with CPU clock divide by 1	0.093	–	6.06	MHz	Maximum CPU frequency is 3 MHz at 2.7 V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements.
F_{OSCEXT}	Frequency with CPU clock divide by 2 or greater	0.186	–	12.12	MHz	If the frequency of the external clock is greater than 3 MHz, the CPU clock divider must be set to 2 or greater. In this case, the CPU clock divider ensures that the fifty percent duty cycle requirement is met.
–	High period with CPU clock divide by 1	83.4	–	5300	ns	
–	Low period with CPU clock divide by 1	83.4	–	–	ns	
–	Power-up IMO to switch	150	–	–	µs	

Table 35. 2.7-V AC Characteristics of the I²C SDA and SCL Pins (Fast Mode Not Supported)

Symbol	Description	Standard Mode		Fast Mode		Units
		Min	Max	Min	Max	
F_{SCLI2C}	SCL clock frequency	0	100	–	–	kHz
$t_{HDSTAI2C}$	Hold time (repeated) START Condition. After this period, the first clock pulse is generated.	4.0	–	–	–	µs
t_{LOWI2C}	Low period of the SCL clock	4.7	–	–	–	µs
$t_{HIGHI2C}$	High period of the SCL clock	4.0	–	–	–	µs
$t_{SUSTAI2C}$	Setup time for a repeated START condition	4.7	–	–	–	µs
$t_{HDDATI2C}$	Data hold time	0	–	–	–	µs
$t_{SUDATI2C}$	Data setup time	250	–	–	–	ns
$t_{SUSTOI2C}$	Setup time for STOP condition	4.0	–	–	–	µs
t_{BUFI2C}	Bus free time between a STOP and START condition	4.7	–	–	–	µs
t_{SPI2C}	Pulse width of spikes are suppressed by the input filter.	–	–	–	–	ns

Figure 14. Definition for Timing for Fast/Standard Mode on the I²C Bus



Acronyms

Acronyms Used

Table 39 lists the acronyms that are used in this document.

Table 39. Acronyms Used in this Datasheet

Acronym	Description	Acronym	Description
AC	alternating current	PCB	printed circuit board
ADC	analog-to-digital converter	PGA	programmable gain amplifier
API	application programming interface	POR	power on reset
CMOS	complementary metal oxide semiconductor	PPOR	precision power on reset
CPU	central processing unit	PRS	pseudo-random sequence
CRC	cyclic redundancy check	PSoC®	Programmable System-on-Chip
CT	continuous time	PWM	pulse width modulator
DAC	digital-to-analog converter	QFN	quad flat no leads
DC	direct current	SC	switched capacitor
EEPROM	electrically erasable programmable read-only memory	SLIMO	slow IMO
GPIO	general purpose I/O	SMP	switch mode pump
ICE	in-circuit emulator	SOIC	small-outline integrated circuit
IDE	integrated development environment	SPI™	serial peripheral interface
ILO	internal low speed oscillator	SRAM	static random access memory
IMO	internal main oscillator	SROM	supervisory read only memory
I/O	input/output	SSOP	shrink small-outline package
IrDA	infrared data association	UART	universal asynchronous reciever / transmitter
ISSP	in-system serial programming	USB	universal serial bus
LVD	low voltage detect	WDT	watchdog timer
MCU	microcontroller unit	XRES	external reset
MIPS	million instructions per second		

Reference Documents

CY8CPLC20, CY8CLED16P01, CY8C29x66, CY8C27x43, CY8C24x94, CY8C24x23, CY8C24x23A, CY8C22x13, CY8C21x34, CY8C21x23, CY7C64215, CY7C603xx, CY8CNP1xx, and CYWUSB6953 PSoC® Programmable System-on-Chip Technical Reference Manual (TRM) (001-14463)

Design Aids – Reading and Writing PSoC® Flash – AN2015 (001-40459)

Adjusting PSoC® Trims for 3.3 V and 2.7 V Operation – AN2012 (001-17397)

Understanding Datasheet Jitter Specifications for Cypress Timing Products – AN5054 (001-14503)

Application Notes for Surface Mount Assembly of Amkor's MicroLeadFrame (MLF) Packages – available at http://www.amkor.com.

Glossary (continued)

bias	1. A systematic deviation of a value from a reference value. 2. The amount by which the average of a set of values departs from a reference value. 3. The electrical, mechanical, magnetic, or other force (field) applied to a device to establish a reference level to operate the device.
block	1. A functional unit that performs a single function, such as an oscillator. 2. A functional unit that may be configured to perform one of several functions, such as a digital PSoC block or an analog PSoC block.
buffer	1. A storage area for data that is used to compensate for a speed difference, when transferring data from one device to another. Usually refers to an area reserved for IO operations, into which data is read, or from which data is written. 2. A portion of memory set aside to store data, often before it is sent to an external device or as it is received from an external device. 3. An amplifier used to lower the output impedance of a system.
bus	1. A named connection of nets. Bundling nets together in a bus makes it easier to route nets with similar routing patterns. 2. A set of signals performing a common function and carrying similar data. Typically represented using vector notation; for example, address[7:0]. 3. One or more conductors that serve as a common connection for a group of related devices.
clock	The device that generates a periodic signal with a fixed frequency and duty cycle. A clock is sometimes used to synchronize different logic blocks.
comparator	An electronic circuit that produces an output voltage or current whenever two input levels simultaneously satisfy predetermined amplitude requirements.
compiler	A program that translates a high level language, such as C, into machine language.
configuration space	In PSoC devices, the register space accessed when the XIO bit, in the CPU_F register, is set to ‘1’.
crystal oscillator	An oscillator in which the frequency is controlled by a piezoelectric crystal. Typically a piezoelectric crystal is less sensitive to ambient temperature than other circuit components.
cyclic redundancy check (CRC)	A calculation used to detect errors in data communications, typically performed using a linear feedback shift register. Similar calculations may be used for a variety of other purposes such as data compression.
data bus	A bi-directional set of signals used by a computer to convey information from a memory location to the central processing unit and vice versa. More generally, a set of signals used to convey data between digital functions.
debugger	A hardware and software system that allows you to analyze the operation of the system under development. A debugger usually allows the developer to step through the firmware one step at a time, set break points, and analyze memory.
dead band	A period of time when neither of two or more signals are in their active state or in transition.
digital blocks	The 8-bit logic blocks that can act as a counter, timer, serial receiver, serial transmitter, CRC generator, pseudo-random number generator, or SPI.
digital-to-analog (DAC)	A device that changes a digital signal to an analog signal of corresponding magnitude. The analog-to-digital (ADC) converter performs the reverse operation.

Glossary (continued)

duty cycle	The relationship of a clock period high time to its low time, expressed as a percent.
emulator	Duplicates (provides an emulation of) the functions of one system with a different system, so that the second system appears to behave like the first system.
External Reset (XRES)	An active high signal that is driven into the PSoC device. It causes all operation of the CPU and blocks to stop and return to a pre-defined state.
Flash	An electrically programmable and erasable, non-volatile technology that provides you the programmability and data storage of EPROMs, plus in-system erasability. Non-volatile means that the data is retained when power is OFF.
Flash block	The smallest amount of Flash ROM space that may be programmed at one time and the smallest amount of Flash space that may be protected. A Flash block holds 64 bytes.
frequency	The number of cycles or events per unit of time, for a periodic function.
gain	The ratio of output current, voltage, or power to input current, voltage, or power, respectively. Gain is usually expressed in dB.
I^2C	A two-wire serial computer bus by Philips Semiconductors (now NXP Semiconductors). I2C is an Inter-Integrated Circuit. It is used to connect low-speed peripherals in an embedded system. The original system was created in the early 1980s as a battery control interface, but it was later used as a simple internal bus system for building control electronics. I2C uses only two bi-directional pins, clock and data, both running at +5 V and pulled high with resistors. The bus operates at 100 kbits/second in standard mode and 400 kbits/second in fast mode.
ICE	The in-circuit emulator that allows you to test the project in a hardware environment, while viewing the debugging device activity in a software environment (PSoC Designer).
input/output (I/O)	A device that introduces data into or extracts data from a system.
interrupt	A suspension of a process, such as the execution of a computer program, caused by an event external to that process, and performed in such a way that the process can be resumed.
interrupt service routine (ISR)	A block of code that normal code execution is diverted to when the M8C receives a hardware interrupt. Many interrupt sources may each exist with its own priority and individual ISR code block. Each ISR code block ends with the RETI instruction, returning the device to the point in the program where it left normal program execution.
jitter	1. A misplacement of the timing of a transition from its ideal position. A typical form of corruption that occurs on serial data streams. 2. The abrupt and unwanted variations of one or more signal characteristics, such as the interval between successive pulses, the amplitude of successive cycles, or the frequency or phase of successive cycles.
low-voltage detect (LVD)	A circuit that senses V_{DD} and provides an interrupt to the system when V_{DD} falls lower than a selected threshold.
M8C	An 8-bit Harvard-architecture microprocessor. The microprocessor coordinates all activity inside a PSoC by interfacing to the Flash, SRAM, and register space.
master device	A device that controls the timing for data exchanges between two devices. Or when devices are cascaded in width, the master device is the one that controls the timing for data exchanges between the cascaded devices and an external interface. The controlled device is called the ***slave device.***

Errata

This section describes the errata for the CY8C21x23 PSoC® programmable system-on-chip family. Details include errata trigger conditions, scope of impact, available workarounds, and silicon revision applicability.

Contact your local Cypress Sales Representative if you have questions.

Part Numbers Affected

Part Number	Ordering Information
CY8C21123	CY8C21123-24SXI
	CY8C21123-24SXIT
	CY8C21223-24SXI
	CY8C21223-24SXIT
	CY8C21323-24PVXI
	CY8C21323-24PVXIT
	CY8C21323-24LFXI
	CY8C21323-24LFXIT
	CY8C21323-24LQXI
	CY8C21323-24LQXIT

CY8C21123 Qualification Status

Product Status: Production

CY8C21123 Errata Summary

The following table defines the errata applicability to available CY8C21123 family devices. An "X" indicates that the errata pertains to the selected device.

Note Errata items, in the table below, are hyperlinked. Click on any item entry to jump to its description.

Items	Part Number	Silicon Revision	Fix Status
[1.] Internal Main Oscillator (IMO) Tolerance Deviation at Temperature Extremes	CY8C21123	A	No silicon fix is planned. Workaround is required.

1. Internal Main Oscillator (IMO) Tolerance Deviation at Temperature Extremes

- **Problem Definition**
  Asynchronous Digital Communications Interfaces may fail framing beyond 0 to 70 °C. This problem does not affect end-product usage between 0 and 70 °C.
- **Parameters Affected**
  The IMO frequency tolerance. The worst case deviation when operated below 0 °C and above +70 °C and within the upper and lower datasheet temperature range is ±5%.
- **Trigger Condition(S)**
  The asynchronous Rx/Tx clock source IMO frequency tolerance may deviate beyond the data sheet limit of ±2.5% when operated beyond the temperature range of 0 to +70 °C.
- **Scope of Impact**
  This problem may affect UART, IrDA, and FSK implementations.
- **Workaround**
  Implement a quartz crystal stabilized clock source on at least one end of the asynchronous digital communications interface.
- **Fix Status**
  No silicon fix is planned. The workaround mentioned above should be used.

Document History Page

Document Title: CY8C21123/CY8C21223/CY8C21323, PSoC® Programmable System-on-Chip™ Document Number: 38-12022				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	133248	NWJ	See ECN	New silicon and document (Revision **).
*A	208900	NWJ	See ECN	Add new part, new package and update all ordering codes to Pb-free.
*B	212081	NWJ	See ECN	Expand and prepare Preliminary version.
*C	227321	CMS Team	See ECN	Update specs., data, format.
*D	235973	SFV	See ECN	Updated Overview and Electrical Spec. chapters, along with 24-pin pinout. Added CMP_GO_EN register (1,64h) to mapping table.
*E	290991	HMT	See ECN	Update datasheet standards per SFV memo. Fix device table. Add part numbers to pinouts and fine tune. Change 20-pin SSOP to CY8C21323. Add Reflow Temp. table. Update diagrams and specs.
*F	301636	HMT	See ECN	DC Chip-Level Specification changes. Update links to new CY.com Portal.
*G	324073	HMT	See ECN	Obtained clearer 16 SOIC package. Update Thermal Impedances and Solder Reflow tables. Re-add pinout ISSP notation. Fix ADC type-o. Fix TMP register names. Update Electrical Specifications. Add CY logo. Update CY copyright. Make datasheet Final.
*H	2588457	KET / HMI / AESA	10/22/2008	New package information on page 9. Converted datasheet to new template. Added 16-Pin OFN package diagram.
*I	2618175	OGNE / PYRS	12/09/2008	Added Note in Ordering Information Section. Changed title from PSoC Mixed-Signal Array to PSoC Programmable System-on-Chip. Updated ‘Development Tools’ and ‘Designing with PSoC Designer’ sections on pages 5 and 6
*J	2682782	MAXK / AESA	04/03/2009	Corrected 16 COL pinout.
*K	2699713	MAXK	04/29/2009	Minor ECN to correct paragraph style of 16 COL Pinout. No change in content.
*L	2762497	JVY	09/11/2009	Updated DC GPIO, AC Chip-Level, and AC Programming Specifications as follows: Modified F_{IMO6} and T_{WRITE} specifications. Replaced T_{RAMP} time) specification with SR_{POWER_UP} (slew rate) specification. Added note [11] to Flash Endurance specification. Added I_{OH}, I_{OL}, DC_{ILO}, F_{32K_U}, $T_{POWERUP}$, $T_{ERASEALL}$, $T_{PROGRAM\_HOT}$, and $T_{PROGRAM\_COLD}$ specifications..
*M	2792630	TTO	10/26/2009	Updated ordering information for CY8C21223-24LGXI to indicate availability of XRES pin.
*N	2901653	NJF	03/30/2010	Changed 16-pin COL to 16-pin QFN in the datasheet. Added Contents. Updated links in Sales, Solutions, and Legal Information Updated Cypress website links. Added $T_{BAKETEMP}$ and $T_{BAKETIME}$ parameters in Absolute Maximum Ratings Updated 5-V and 3.3-V AC Chip-Level Specifications Updated Notes in Packaging Information and package diagrams. Updated Ordering Code Definitions
*O	2928895	YJI	05/06/2010	No technical updates. Included with EROS spec.

Document History Page (continued)

Document Title: CY8C21123/CY8C21223/CY8C21323, PSoC® Programmable System-on-Chip™ Document Number: 38-12022				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*P	3044869	NJF	10/01/2010	Added PSoC Device Characteristics table. Added DC I^2C Specifications table. Added F_{32K_U} max limit. Added Tjit_IMO specification, removed existing jitter specifications. Updated Units of Measure, Acronyms, Glossary, and References sections. Updated solder reflow specifications. No specific changes were made to AC Digital Block Specifications table and I^2C Timing Diagram. They were updated for clearer understanding. Updated Figure 13 since the labelling for y-axis was incorrect. Template and styles update.
*Q	3263669	YJI	05/23/2011	Updated 16-pin SOIC and 20-pin SSOP package diagrams. Updated Development Tool Selection and Designing with PSoC Designer sections.
*R	3383787	GIR	09/26/2011	The text “Pin must be left floating” is included under Description of NC pin in Table 6 on page 11. Updated Table 37 on page 35 for improved clarity.
*S	3558729	RJVB	03/22/2012	Updated 16-pin SOIC package.
*T	3598261	LURE / XZNG	04/24/2012	Changed the PWM description string from “8- to 32-bit” to “8- and 16-bit”.
*U	3649990	BVI / YLIU	06/19/2012	Updated description of NC pin as “No Connection. Pin must be left floating”
*V	3873870	UVS	01/18/2013	Updated Packaging Information: spec 51-85068 – Changed revision from *D to *E. spec 001-09116 – Changed revision from *F to *G. spec 51-85203 – Changed revision from *C to *D.
*W	3993321	UVS	05/07/2013	Added Errata.
*X	4067216	UVS	07/18/2013	Added Errata footnotes (Note 19). Updated Features: Replaced 2.5% with 5% under “Precision, programmable clocking”. Updated Electrical Specifications: Updated AC Electrical Characteristics: Updated AC Chip-Level Specifications: Added Note 19 and referred the same note in F_{IMO24} parameter. Updated minimum and maximum values of F_{IMO24} parameter. Updated AC Digital Block Specifications: Replaced all instances of maximum value “49.2” with “50.4” and “24.6” with “25.2” in Table 28. Updated Packaging Information: spec 51-85066 – Changed revision from *E to *F. spec 001-09116 – Changed revision from *G to *H. Updated to new template.
*Y	4479648	RJVB	08/20/2014	Updated Errata: Updated CY8C21123 Errata Summary: Updated details in “Fix Status” column in the table. Updated details in “Fix Status” bulleted point below the table.