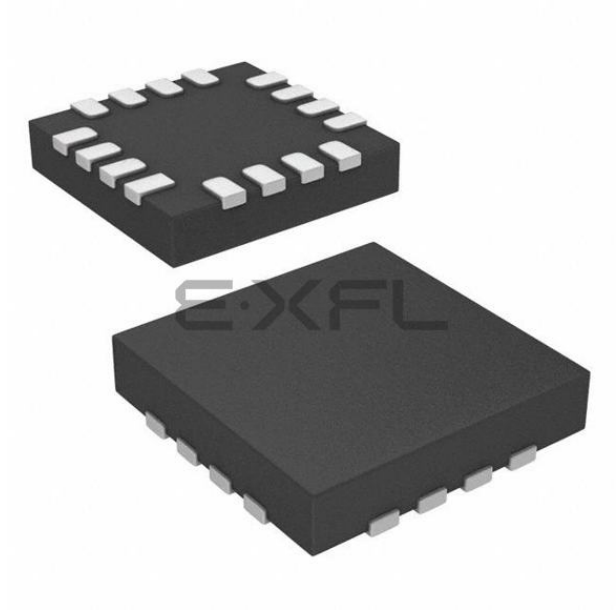

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	12
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.25V
Data Converters	A/D 8x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	16-UFQFN
Supplier Device Package	16-QFN (3x3)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c21223-24lgxi

Analog System

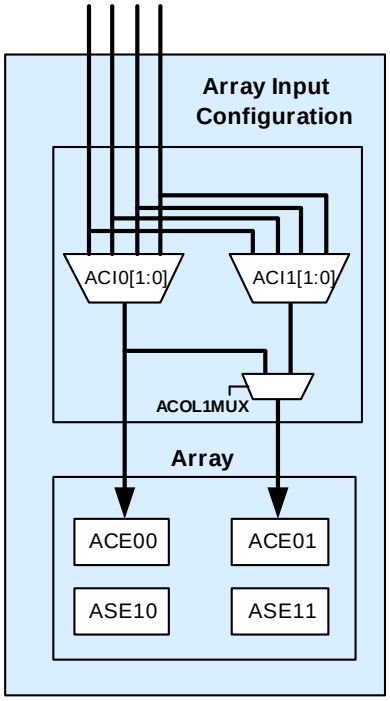
The analog system consists of four configurable blocks to allow creation of complex analog signal flows. Analog peripherals are very flexible and may be customized to support specific application requirements. Some of the more common PSoC analog functions (most available as user modules) are:

- Analog-to-digital converters (single or dual, with 8-bit or 10-bit resolution)
- Pin-to-pin comparators (one)
- Single-ended comparators (up to 2) with absolute (1.3 V) reference or 8-bit DAC reference
- 1.3 V reference (as a system resource)

In most PSoC devices, analog blocks are provided in columns of three, which includes one CT (continuous time) and two SC (switched capacitor) blocks. The CY8C21x23 devices provide limited functionality Type “E” analog blocks. Each column contains one CT block and one SC block.

The number of blocks on the device family is listed in Table 1 on page 5.

Figure 2. CY8C21x23 Analog System Block Diagram



Additional System Resources

System resources, some of which listed in the previous sections, provide additional capability useful to complete systems. Additional resources include a switch mode pump, low voltage detection, and power on reset. The merits of each system resource are.

- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks can be routed to both the digital and analog systems. Additional clocks can be generated using digital PSoC blocks as clock dividers.
- The I^2C module provides 100 and 400 kHz communication over two wires. Slave, master, and multi-master modes are all supported.
- LVD interrupts can signal the application of falling voltage levels, while the advanced POR (power on reset) circuit eliminates the need for a system supervisor.
- An internal 1.3 V voltage reference provides an absolute reference for the analog system, including ADCs and DACs.
- An integrated switch mode pump (SMP) generates normal operating voltages from a single 1.2 V battery cell, providing a low cost boost converter.

PSoC Device Characteristics

Depending on your PSoC device characteristics, the digital and analog systems can have 16, 8, or 4 digital blocks, and 12, 6, or 4 analog blocks. Table 1 lists the resources available for specific PSoC device groups. The PSoC device covered by this datasheet is highlighted.

Table 1. PSoC Device Characteristics

PSoC Part Number	Digital I/O	Digital Rows	Digital Blocks	Analog Inputs	Analog Outputs	Analog Columns	Analog Blocks	SRAM Size	Flash Size
CY8C29x66	up to 64	4	16	up to 12	4	4	12	2 K	32 K
CY8C28xxx	up to 44	up to 3	up to 12	up to 44	up to 4	up to 6	up to 12 + 4[1]	1 K	16 K
CY8C27x43	up to 44	2	8	up to 12	4	4	12	256	16 K
CY8C24x94	up to 56	1	4	up to 48	2	2	6	1 K	16 K
CY8C24x23A	up to 24	1	4	up to 12	2	2	6	256	4 K
CY8C23x33	up to 26	1	4	up to 12	2	2	4	256	8 K
CY8C22x45	up to 38	2	8	up to 38	0	4	6[1]	1 K	16 K
CY8C21x45	up to 24	1	4	up to 24	0	4	6[1]	512	8 K
CY8C21x34	up to 28	1	4	up to 28	0	2	4[1]	512	8 K
CY8C21x23	up to 16	1	4	up to 8	0	2	4[1]	256	4 K
CY8C20x34	up to 28	0	0	up to 28	0	0	3[1,2]	512	8 K
CY8C20xx6	up to 36	0	0	up to 36	0	0	3[1,2]	up to 2 K	up to 32 K

Getting Started

The quickest way to understand PSoC silicon is to read this datasheet and then use the PSoC Designer Integrated Development Environment (IDE). This datasheet is an overview of the PSoC integrated circuit and presents specific pin, register, and electrical specifications.

For in depth information, along with detailed programming details, see the Technical Reference Manual for this PSoC device.

For up to date ordering, packaging, and electrical specification information, see the latest PSoC device datasheets on the web at http://www.cypress.com.

Application Notes

Application notes are an excellent introduction to the wide variety of possible PSoC designs. They can be found at http://www.cypress.com.

Development Kits

PSoC Development Kits are available online from Cypress at http://www.cypress.com and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

Training

Free PSoC technical training (on demand, webinars, and workshops) is available online at http://www.cypress.com. The training covers a wide variety of topics and skill levels to assist you in your designs.

CYPros Consultants

Certified PSoC Consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC Consultant go to http://www.cypress.com and refer to CYPros Consultants.

Solutions Library

Visit our growing library of solution focused designs at http://www.cypress.com. Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

Technical Support

For assistance with technical issues, search KnowledgeBase articles and forums at http://www.cypress.com. If you cannot find an answer to your question, call technical support at 1-800-541-4736.

Notes
1. Limited analog functionality.
2. Two analog blocks and one CapSense®.

Designing with PSoC Designer

The development process for the PSoC device differs from that of a traditional fixed function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and by lowering inventory costs. These configurable resources, called PSoC Blocks, have the ability to implement a wide variety of user-selectable functions.

The PSoC development process can be summarized in the following four steps:

1. Select User Modules
2. Configure User Modules
3. Organize and Connect
4. Generate, Verify, and Debug

Select Components

PSoC Designer provides a library of pre-built, pre-tested hardware peripheral components called "user modules." User modules make selecting and implementing peripheral devices, both analog and digital, simple.

Configure Components

Each of the User Modules you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a PWM User Module configures one or more

digital PSoC blocks, one for each 8 bits of resolution. The user module parameters permit you to establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus. All the user modules are documented in datasheets that may be viewed directly in PSoC Designer or on the Cypress website. These user module datasheets explain the internal operation of the User Module and provide performance specifications. Each datasheet describes the use of each user module parameter, and other information you may need to successfully implement your design.

Organize and Connect

You build signal chains at the chip level by interconnecting user modules to each other and the I/O pins. You perform the selection, configuration, and routing so that you have complete control over all on-chip resources.

Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, you perform the "Generate Configuration Files" step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. The generated code provides application programming interfaces (APIs) with high-level functions to control and respond to hardware events at run time and interrupt service routines that you can adapt as needed.

A complete code development environment allows you to develop and customize your applications in C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer's Debugger (access by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition

to traditional single-step, run-to-breakpoint and watch-variable features, the debug interface provides a large trace buffer and allows you to define complex breakpoint events that include monitoring address and data bus values, memory locations and external signals.

Pin Information

This section describes, lists, and illustrates the CY8C21x23 PSoC device pins and pinout configurations. Every port pin (labeled with a “P”) is capable of Digital I/O. However, V_{SS}, V_{DD}, SMP, and XRES are not capable of Digital I/O.

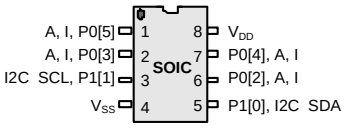
8-Pin Part Pinout

Table 2. Pin Definitions – CY8C21123 8-Pin SOIC

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O	I	P0[5]	Analog column mux input
2	I/O	I	P0[3]	Analog column mux input
3	I/O		P1[1]	I^2C serial clock (SCL), ISSP-SCLK[3]
4	Power		V_{SS}	Ground connection
5	I/O		P1[0]	I^2C serial data (SDA), ISSP-SDATA[3]
6	I/O	I	P0[2]	Analog column mux input
7	I/O	I	P0[4]	Analog column mux input
8	Power		V_{DD}	Supply voltage

LEGEND: A = Analog, I = Input, and O = Output.

Figure 3. CY8C21123 8-Pin SOIC



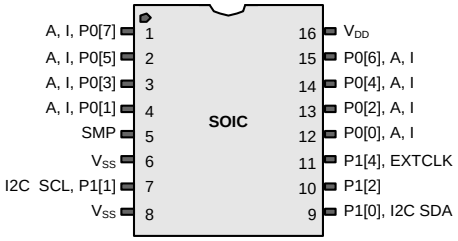
16-Pin Part Pinout

Table 3. Pin Definitions – CY8C21223 16-Pin SOIC

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O	I	P0[7]	Analog column mux input
2	I/O	I	P0[5]	Analog column mux input
3	I/O	I	P0[3]	Analog column mux input
4	I/O	I	P0[1]	Analog column mux input
5	Power		SMP	SMP connection to required external components
6	Power		V_{SS}	Ground connection
7	I/O		P1[1]	I^2C SCL, ISSP-SCLK[3]
8	Power		V_{SS}	Ground connection
9	I/O		P1[0]	I^2C SDA, ISSP-SDATA[3]
10	I/O		P1[2]	
11	I/O		P1[4]	Optional external clock input (EXTCLK)
12	I/O	I	P0[0]	Analog column mux input
13	I/O	I	P0[2]	Analog column mux input
14	I/O	I	P0[4]	Analog column mux input
15	I/O	I	P0[6]	Analog column mux input
16	Power		V_{DD}	Supply voltage

LEGEND A = Analog, I = Input, and O = Output.

Figure 4. CY8C21223 16-Pin SOIC



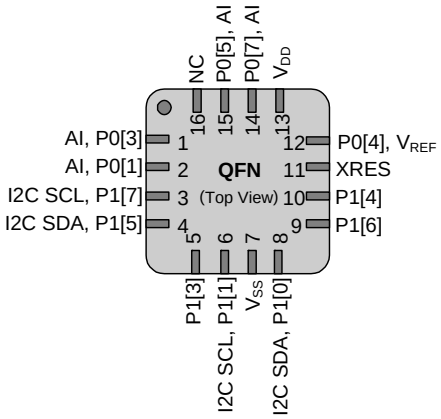
Note
3. These are the ISSP pins, which are not high Z at POR (power on reset). See the PSoC Technical Reference Manual for details.

Table 4. Pin Definitions – CY8C21223 16-Pin QFN with no E-Pad [4]

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O	I	P0[3]	Analog column mux input
2	I/O	I	P0[1]	Analog column mux input
3	I/O		P1[7]	I^2C SCL
4	I/O		P1[5]	I^2C SDA
5	I/O		P1[3]	
6	I/O		P1[1]	I^2C SCL, ISSP-SCLK[5]
7	Power		V_{SS}	Ground connection
8	I/O		P1[0]	I^2C SDA, ISSP-SDATA[5]
9	I/O		P1[6]	
10	I/O		P1[4]	EXTCLK
11	Input		XRES	Active high external reset with internal pull-down
12	I/O	I	P0[4]	V_{REF}
13	Power		V_{DD}	Supply voltage
14	I/O	I	P0[7]	Analog column mux input
15	I/O	I	P0[5]	Analog column mux input
16			NC	No Connection. Pin must be left floating

LEGEND A = Analog, I = Input, and O = Output.

Figure 5. CY8C21223 16-Pin QFN



Notes
4. The center pad on the QFN package must be connected to ground (Vss) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.
5. These are the ISSP pins, which are not high Z at POR (power on reset). See the PSoC Technical Reference Manual for details.

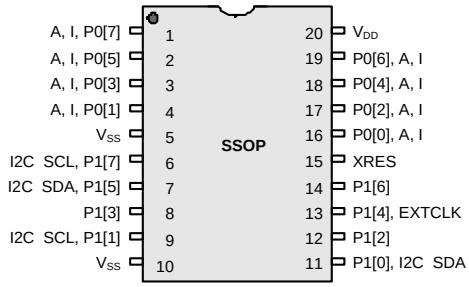
20-Pin Part Pinout

Table 5. Pin Definitions – CY8C21323 20-Pin SSOP

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O	I	P0[7]	Analog column mux input
2	I/O	I	P0[5]	Analog column mux input
3	I/O	I	P0[3]	Analog column mux input
4	I/O	I	P0[1]	Analog column mux input
5	Power		V_{SS}	Ground connection[6]
6	I/O		P1[7]	I^2C SCL
7	I/O		P1[5]	I^2C SDA
8	I/O		P1[3]	
9	I/O		P1[1]	I^2C SCL, ISSP-SCLK[7]
10	Power		V_{SS}	Ground connection[6]
11	I/O		P1[0]	I^2C SDA, ISSP-SDATA[7]
12	I/O		P1[2]	
13	I/O		P1[4]	Optional EXTCLK input
14	I/O		P1[6]	
15	Input		XRES	Active high external reset with internal pull-down
16	I/O	I	P0[0]	Analog column mux input
17	I/O	I	P0[2]	Analog column mux input
18	I/O	I	P0[4]	Analog column mux input
19	I/O	I	P0[6]	Analog column mux input
20	Power		V_{DD}	Supply voltage

LEGEND A = Analog, I = Input, and O = Output.

Figure 6. CY8C21323 20-Pin SSOP



Notes
6. All V_{SS} pins should be brought out to one common GND plane.
7. These are the ISSP pins, which are not high Z at POR (power on reset). See the PSoC Technical Reference Manual for details.

Table 8. Register Map Bank 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW		40		ASE10CR0	80	RW		C0	
PRT0IE	01	RW		41			81			C1	
PRT0GS	02	RW		42			82			C2	
PRT0DM2	03	RW		43			83			C3	
PRT1DR	04	RW		44		ASE11CR0	84	RW		C4	
PRT1IE	05	RW		45			85			C5	
PRT1GS	06	RW		46			86			C6	
PRT1DM2	07	RW		47			87			C7	
	08			48			88			C8	
	09			49			89			C9	
	0A			4A			8A			CA	
	0B			4B			8B			CB	
	0C			4C			8C			CC	
	0D			4D			8D			CD	
	0E			4E			8E			CE	
	0F			4F			8F			CF	
	10			50			90			D0	
	11			51			91			D1	
	12			52			92			D2	
	13			53			93			D3	
	14			54			94			D4	
	15			55			95			D5	
	16			56			96		I2C_CFG	D6	RW
	17			57			97		I2C_SCR	D7	#
	18			58			98		I2C_DR	D8	RW
	19			59			99		I2C_MSCR	D9	#
	1A			5A			9A		INT_CLR0	DA	RW
	1B			5B			9B		INT_CLR1	DB	RW
	1C			5C			9C			DC	
	1D			5D			9D		INT_CLR3	DD	RW
	1E			5E			9E		INT_MSK3	DE	RW
	1F			5F			9F			DF	
DBB00DR0	20	#	AMX_IN	60	RW		A0		INT_MSK0	E0	RW
DBB00DR1	21	W		61			A1		INT_MSK1	E1	RW
DBB00DR2	22	RW	PWM_CR	62	RW		A2		INT_VC	E2	RC
DBB00CR0	23	#		63			A3		RES_WDT	E3	W
DBB01DR0	24	#	CMP_CR0	64	#		A4			E4	
DBB01DR1	25	W		65			A5			E5	
DBB01DR2	26	RW	CMP_CR1	66	RW		A6		DEC_CR0	E6	RW
DBB01CR0	27	#		67			A7		DEC_CR1	E7	RW
DCB02DR0	28	#	ADC0_CR	68	#		A8			E8	
DCB02DR1	29	W	ADC1_CR	69	#		A9			E9	
DCB02DR2	2A	RW		6A			AA			EA	
DCB02CR0	2B	#		6B			AB			EB	
DCB03DR0	2C	#	TMP_DR0	6C	RW		AC			EC	
DCB03DR1	2D	W	TMP_DR1	6D	RW		AD			ED	
DCB03DR2	2E	RW	TMP_DR2	6E	RW		AE			EE	
DCB03CR0	2F	#	TMP_DR3	6F	RW		AF			EF	

Blank fields are Reserved and must not be accessed. # Access is bit specific.

Table 8. Register Map Bank 0 Table: User Space (continued)

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
	30			70		RDI0RI	B0	RW		F0	
	31			71		RDI0SYN	B1	RW		F1	
	32		ACE00CR1	72	RW	RDI0IS	B2	RW		F2	
	33		ACE00CR2	73	RW	RDI0LT0	B3	RW		F3	
	34			74		RDI0LT1	B4	RW		F4	
	35			75		RDI0RO0	B5	RW		F5	
	36		ACE01CR1	76	RW	RDI0RO1	B6	RW		F6	
	37		ACE01CR2	77	RW		B7		CPU_F	F7	RL
	38			78			B8			F8	
	39			79			B9			F9	
	3A			7A			BA			FA	
	3B			7B			BB			FB	
	3C			7C			BC			FC	
	3D			7D			BD			FD	
	3E			7E			BE		CPU_SCR1	FE	#
	3F			7F			BF		CPU_SCR0	FF	#

Blank fields are Reserved and must not be accessed. # Access is bit specific.

Table 9. Register Map Bank 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW		40		ASE10CR0	80	RW		C0	
PRT0DM1	01	RW		41			81			C1	
PRT0IC0	02	RW		42			82			C2	
PRT0IC1	03	RW		43			83			C3	
PRT1DM0	04	RW		44		ASE11CR0	84	RW		C4	
PRT1DM1	05	RW		45			85			C5	
PRT1IC0	06	RW		46			86			C6	
PRT1IC1	07	RW		47			87			C7	
	08			48			88			C8	
	09			49			89			C9	
	0A			4A			8A			CA	
	0B			4B			8B			CB	
	0C			4C			8C			CC	
	0D			4D			8D			CD	
	0E			4E			8E			CE	
	0F			4F			8F			CF	
	10			50			90		GDI_O_IN	D0	RW
	11			51			91		GDI_E_IN	D1	RW
	12			52			92		GDI_O_OU	D2	RW
	13			53			93		GDI_E_OU	D3	RW
	14			54			94			D4	
	15			55			95			D5	
	16			56			96			D6	
	17			57			97			D7	
	18			58			98			D8	
	19			59			99			D9	
	1A			5A			9A			DA	
	1B			5B			9B			DB	

Blank fields are Reserved and must not be accessed. # Access is bit specific.

Operating Temperature

Table 11. Operating Temperature

Symbol	Description	Min	Typ	Max	Units	Notes
T_A	Ambient temperature	–40	–	+85	°C	
T_J	Junction temperature	–40	–	+100	°C	The temperature rise from ambient to junction is package specific. See Table 36 on page 35. You must limit the power consumption to comply with this requirement.

DC Electrical Characteristics

DC Chip-Level Specifications

Table 12 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 12. DC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{DD}	Supply voltage	2.40	–	5.25	V	See DC POR and LVD specifications, Table 19 on page 21.
I_{DD}	Supply current, IMO = 24 MHz	–	3	4	mA	Conditions are V_{DD} = 5.0 V, 25 °C, CPU = 3 MHz, SYSCLK doubler disabled. VC1 = 1.5 MHz VC2 = 93.75 kHz VC3 = 0.366 kHz
I_{DD3}	Supply current, IMO = 6 MHz	–	1.2	2	mA	Conditions are V_{DD} = 3.3 V, 25 °C, CPU = 3 MHz, clock doubler disabled. VC1 = 375 kHz VC2 = 23.4 kHz VC3 = 0.091 kHz
I_{DD27}	Supply current, IMO = 6 MHz	–	1.1	1.5	mA	Conditions are V_{DD} = 2.55 V, 25 °C, CPU = 3 MHz, clock doubler disabled. VC1 = 375 kHz VC2 = 23.4 kHz VC3 = 0.091 kHz
I_{SB27}	Sleep (mode) current with POR, LVD, sleep timer, WDT, and internal slow oscillator active. Mid temperature range.	–	2.6	4	µA	V_{DD} = 2.55 V, 0 °C to 40 °C
I_{SB}	Sleep (mode) current with POR, LVD, sleep timer, WDT, and internal slow oscillator active.	–	2.8	5	µA	V_{DD} = 3.3 V, –40 °C ≤ T_A ≤ 85 °C
V_{REF}	Reference voltage (bandgap)	1.28	1.30	1.32	V	Trimmed for appropriate V_{DD}. V_{DD} = 3.0 V to 5.25 V
V_{REF27}	Reference voltage (bandgap)	1.16	1.30	1.330	V	Trimmed for appropriate V_{DD}. V_{DD} = 2.4 V to 3.0 V
AGND	Analog ground	V_{REF} – 0.003	V_{REF}	V_{REF} + 0.003	V	

DC GPIO Specifications

Table 13 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 13. 5-V and 3.3-V DC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{PU}	Pull-up resistor	4	5.6	8	kΩ	
R_{PD}	Pull-down resistor	4	5.6	8	kΩ	
V_{OH}	High output level	V_{DD} – 1.0	–	–	V	I_{OH} = 10 mA, V_{DD} = 4.75 to 5.25 V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])). 80 mA maximum combined I_{OH} budget.
V_{OL}	Low output level	–	–	0.75	V	I_{OL} = 25 mA, V_{DD} = 4.75 to 5.25 V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5])). 150 mA maximum combined I_{OL} budget.
I_{OH}	High level source current	10	–	–	mA	V_{OH} = V_{DD} – 1.0 V, see the limitations of the total current in the note for V_{OH}
I_{OL}	Low level sink current	25	–	–	mA	V_{OL} = 0.75 V, see the limitations of the total current in the note for V_{OL}
V_{IL}	Input low level	–	–	0.8	V	V_{DD} = 3.0 to 5.25
V_{IH}	Input high level	2.1	–		V	V_{DD} = 3.0 to 5.25
V_H	Input hysteresis	–	60	–	mV	
I_{IL}	Input leakage (absolute value)	–	1	–	nA	Gross tested to 1 µA
C_{IN}	Capacitive load on pins as input	–	3.5	10	pF	Package and pin dependent. Temp = 25 °C
C_{OUT}	Capacitive load on pins as output	–	3.5	10	pF	Package and pin dependent. Temp = 25 °C

Table 14 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C. Typical parameters apply to 2.7 V at 25 °C and are for design guidance only.

Table 14. 2.7-V DC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{PU}	Pull-up resistor	4	5.6	8	kΩ	
R_{PD}	Pull-down resistor	4	5.6	8	kΩ	
V_{OH}	High output level	V_{DD} – 0.4	–	–	V	I_{OH} = 2.5 mA (6.25 Typ), V_{DD} = 2.4 to 3.0 V (16 mA maximum, 50 mA Typ combined I_{OH} budget).
V_{OL}	Low output level	–	–	0.75	V	I_{OL} = 10 mA, V_{DD} = 2.4 to 3.0 V (90 mA maximum combined I_{OL} budget).
I_{OH}	High level source current	2.5	–	–	mA	V_{OH} = V_{DD} – 0.4 V, see the limitations of the total current in the note for V_{OH}
I_{OL}	Low level sink current	10	–	–	mA	V_{OL} = 0.75 V, see the limitations of the total current in the note for V_{OL}
V_{IL}	Input low level	–	–	0.75	V	V_{DD} = 2.4 to 3.0
V_{IH}	Input high level	2.0	–	–	V	V_{DD} = 2.4 to 3.0
V_H	Input hysteresis	–	60	–	mV	
I_{IL}	Input leakage (absolute value)	–	1	–	nA	Gross tested to 1 µA
C_{IN}	Capacitive load on pins as input	–	3.5	10	pF	Package and pin dependent. Temp = 25 °C
C_{OUT}	Capacitive load on pins as output	–	3.5	10	pF	Package and pin dependent. Temp = 25 °C

Table 23. 2.7-V AC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{IMO12}	IMO frequency for 12 MHz	11.5	12	12.7[24,25]	MHz	Trimmed for 2.7 V operation using factory trim values. See Figure 11 on page 16. SLIMO mode = 1.
F_{IMO6}	IMO frequency for 6 MHz	5.5	6	6.5[24,25]	MHz	Trimmed for 2.7 V operation using factory trim values. See Figure 11 on page 16. SLIMO mode = 1.
F_{CPU1}	CPU frequency (2.7 V nominal)	0.093	3	3.15[24]	MHz	24 MHz only for SLIMO mode = 0.
F_{BLK27}	Digital PSoC block frequency (2.7 V nominal)	0	12	12.5[24,25]	MHz	Refer to the section AC Digital Block Specifications on page 26.
F_{32K1}	ILO frequency	8	32	96	kHz	
F_{32K_U}	ILO untrimmed frequency	5	–	100	kHz	After a reset and before the M8C starts to run, the ILO is not trimmed. See the system resets section of the PSoC Technical Reference Manual for details on this timing.
t_{XRST}	External reset pulse width	10	–	–	µs	
DC_{ILO}	ILO duty cycle	20	50	80	%	
F_{MAX}	Maximum frequency of signal on row input or row output	–	–	12.3	MHz	
SR_{POWER_UP}	Power supply slew rate	–	–	250	V/ms	V_{DD} slew rate during power-up.
$t_{POWERUP}$	Time from end of POR to CPU executing code	–	16	100	ms	Power-up from 0 V. See the system resets section of the PSoC Technical Reference Manual.
t_{jit_IMO}	12-MHz IMO cycle-to-cycle jitter (RMS)[26]	–	400	1000	ps	
	12-MHz IMO long term N cycle-to-cycle jitter (RMS)[26]	–	600	1300	ps	N = 32
	12-MHz IMO period jitter (RMS)[26]	–	100	500	ps	

Notes
24. 2.4 V < V_{DD} < 3.0 V.
25. Refer to the application note Adjusting PSoC Microcontroller Trims for Dual Voltage-Range Operation – AN2012 for more information on maximum frequency for user modules.
26. Refer to the application note, Understanding Datasheet Jitter Specifications for Cypress Timing Products – AN5054 for more information on jitter specifications.

Table 29. 2.7-V AC Digital Block Specifications

Function	Description	Min	Typ	Max	Units	Notes
All functions	Block input clock frequency	–	–	12.7	MHz	2.4 V < V_{DD} < 3.0 V.
Timer	Capture pulse width	100[28]	–	–	ns	
	Input clock frequency, with or without capture	–	–	12.7	MHz	
Counter	Enable input pulse width	100	–	–	ns	
	Input clock frequency, no enable input	–	–	12.7	MHz	
	Input clock frequency, enable input	–	–	12.7	MHz	
Dead band	Kill pulse width:					
	Asynchronous restart mode	20	–	–	ns	
	Synchronous restart mode	100	–	–	ns	
	Disable mode	100	–	–	ns	
	Input clock frequency	–	–	12.7	MHz	
CRCPRS (PRS mode)	Input clock frequency	–	–	12.7	MHz	
CRCPRS (CRC mode)	Input clock frequency	–	–	12.7	MHz	
SPIM	Input clock frequency	–	–	6.35	MHz	The SPI serial clock (SCLK) frequency is equal to the input clock frequency divided by 2.
SPIS	Input clock (SCLK) frequency	–	–	4.1	MHz	
	Width of SS_ Negated between transmissions	100	–	–	ns	
Transmitter	Input clock frequency	–	–	12.7	MHz	The baud rate is equal to the input clock frequency divided by 8.
Receiver	Input clock frequency	–	–	12.7	MHz	The baud rate is equal to the input clock frequency divided by 8.

Note
28. 100 ns minimum input pulse width is based on the input synchronizers running at 12 MHz (84 ns nominal period).

AC External Clock Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 30. 5-V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency	0.093	–	24.6	MHz	
–	High period	20.6	–	5300	ns	
–	Low period	20.6	–	–	ns	
–	Power-up IMO to switch	150	–	–	µs	

Table 31. 3.3-V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency with CPU clock divide by 1	0.093	–	12.3	MHz	Maximum CPU frequency is 12 MHz at 3.3 V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements.
F_{OSCEXT}	Frequency with CPU clock divide by 2 or greater	0.186	–	24.6	MHz	If the frequency of the external clock is greater than 12 MHz, the CPU clock divider must be set to 2 or greater. In this case, the CPU clock divider ensures that the fifty percent duty cycle requirement is met.
–	High period with CPU clock divide by 1	41.7	–	5300	ns	
–	Low period with CPU clock divide by 1	41.7	–	–	ns	
–	Power-up IMO to switch	150	–	–	µs	

Table 32. 2.7-V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency with CPU clock divide by 1	0.093	–	6.06	MHz	Maximum CPU frequency is 3 MHz at 2.7 V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements.
F_{OSCEXT}	Frequency with CPU clock divide by 2 or greater	0.186	–	12.12	MHz	If the frequency of the external clock is greater than 3 MHz, the CPU clock divider must be set to 2 or greater. In this case, the CPU clock divider ensures that the fifty percent duty cycle requirement is met.
–	High period with CPU clock divide by 1	83.4	–	5300	ns	
–	Low period with CPU clock divide by 1	83.4	–	–	ns	
–	Power-up IMO to switch	150	–	–	µs	

Packaging Information

This section illustrates the packaging specifications for the CY8C21x23 PSoC device, along with the thermal impedances for each package and minimum solder reflow peak temperature.

Important Note Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the emulator pod drawings at http://www.cypress.com.

Packaging Dimensions

Figure 15. 8-pin SOIC (150 Mils) S0815/SZ815/SW815 Package Outline, 51-85066

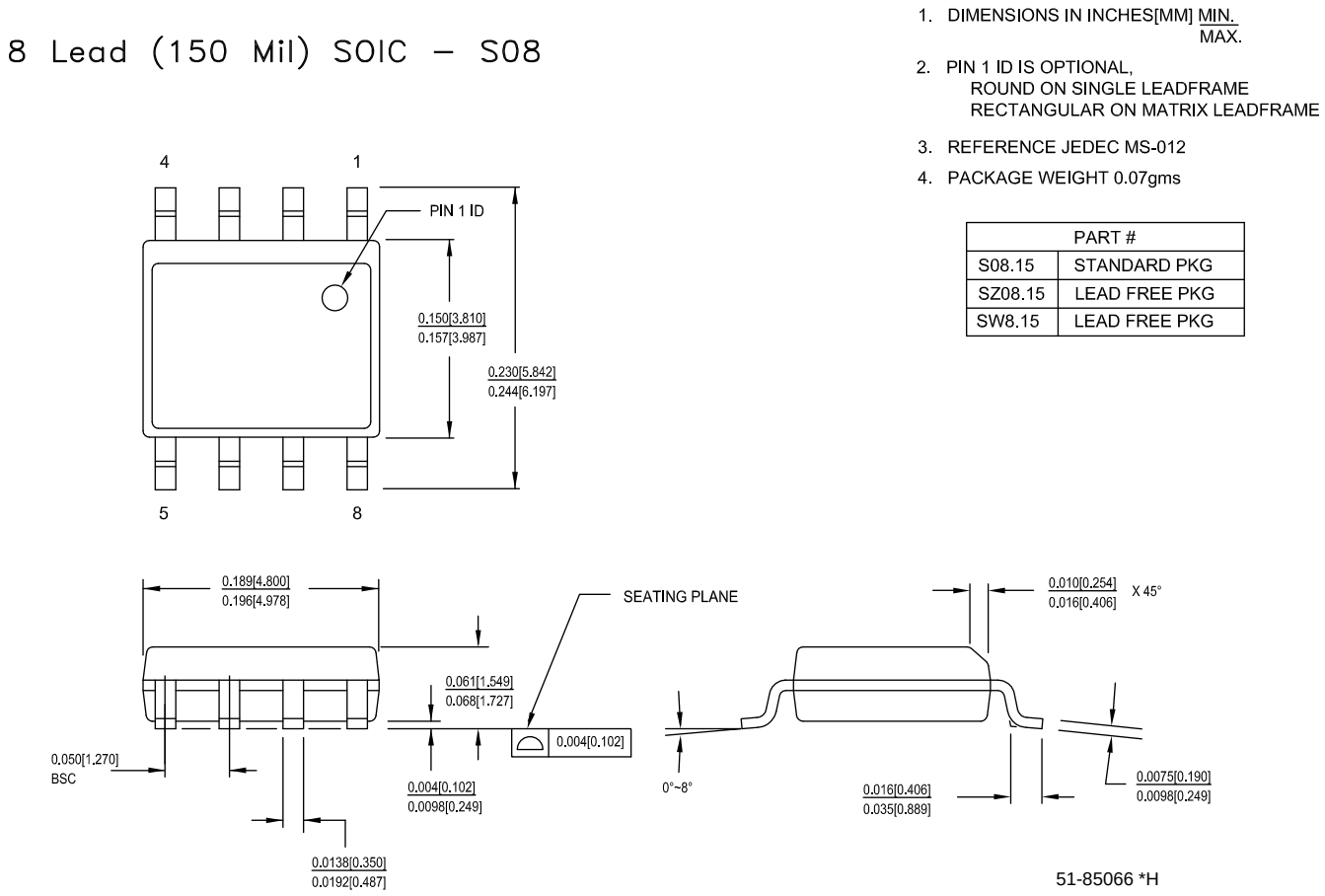


Figure 16. 16-Pin (150-Mil) SOIC

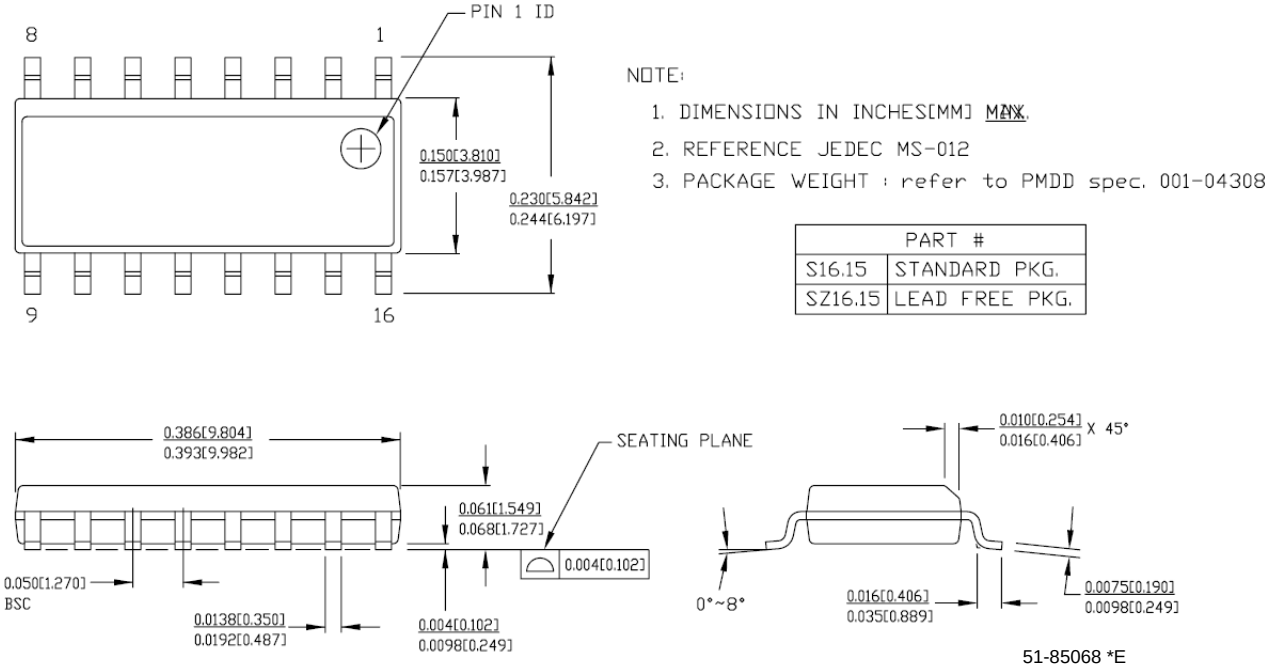
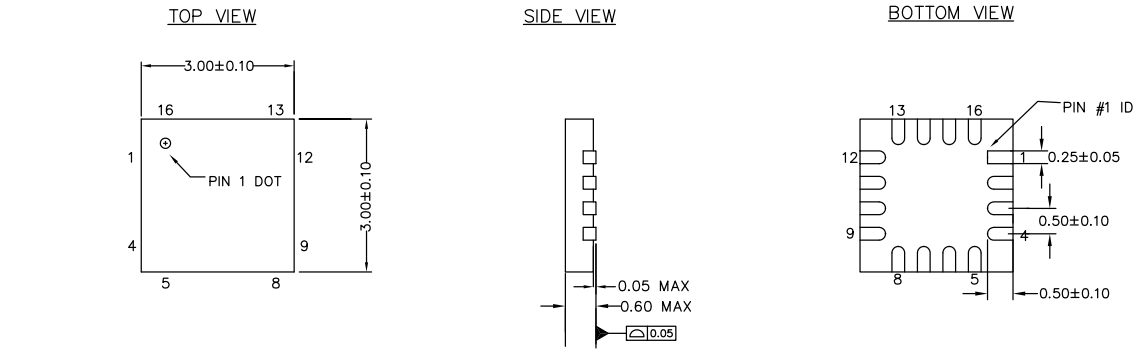


Figure 17. 16-Pin QFN with no E-Pad



NOTES
1. REFERENCE JEDEC # MO-220
2. ALL DIMENSIONS ARE IN MILLIMETERS

001-09116 *J

Thermal Impedances

Table 36. Thermal Impedances per Package

Package	Typical θ_{JA} [31]
8-pin SOIC	186 °C/W
16-pin SOIC	125 °C/W
16-pin QFN	46 °C/W
20-pin SSOP	117 °C/W
24-pin QFN[32]	40 °C/W

Solder Reflow Specifications

Table 37 shows the solder reflow temperature limits that must not be exceeded.

Table 37. Solder Reflow Specifications

Package	Maximum Peak Temperature (T_C)	Maximum Time above T_C – 5 °C
8-pin SOIC	260 °C	30 seconds
16-pin SOIC	260 °C	30 seconds
16-pin QFN	260 °C	30 seconds
20-pin SSOP	260 °C	30 seconds
24-pin QFN	260 °C	30 seconds

Notes
31. $T_J = T_A + POWER \times \theta_{JA}$
32. To achieve the thermal impedance specified for the QFN package, refer to "Application Notes for Surface Mount Assembly of Amkor's MicroLeadFrame (MLF) Packages" available at http://www.amkor.com.
33. Higher temperatures may be required based on the solder melting point. Typical temperatures for solder are 220+/-5 °C with Sn-Pb or 245+/-5 °C with Sn-Ag-Cu paste. Refer to the solder manufacturer specifications.

Document Conventions

Units of Measure

Table 40 lists the units of measures.

Table 40. Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure
dB	decibels	mH	millihenry
°C	degree Celsius	µH	microhenry
µF	microfarad	µs	microsecond
pF	picofarad	ms	millisecond
kHz	kilohertz	ns	nanosecond
MHz	megahertz	ps	picosecond
rt-Hz	root hertz	µV	microvolt
kΩ	kilohm	mV	millivolt
Ω	ohm	mVpp	millivolts peak-to-peak
µA	microampere	V	volt
mA	milliampere	W	watt
nA	nanoampere	mm	millimeter
pA	pikoampere	%	percent

Numeric Conventions

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase ‘h’ (for example, ‘14h’ or ‘3Ah’). Hexadecimal numbers may also be represented by a ‘0x’ prefix, the C coding convention. Binary numbers have an appended lowercase ‘b’ (for example, 01010100b’ or ‘01000011b’). Numbers not indicated by an ‘h’ or ‘b’ are decimals.

Glossary

active high	1. A logic signal having its asserted state as the logic 1 state. 2. A logic signal having the logic 1 state as the higher voltage of the two states.
analog blocks	The basic programmable opamp circuits. These are SC (switched capacitor) and CT (continuous time) blocks. These blocks can be interconnected to provide ADCs, DACs, multi-pole filters, gain stages, and much more.
analog-to-digital (ADC)	A device that changes an analog signal to a digital signal of corresponding magnitude. Typically, an ADC converts a voltage to a digital number. The digital-to-analog (DAC) converter performs the reverse operation.
Application programming interface (API)	A series of software routines that comprise an interface between a computer application and lower level services and functions (for example, user modules and libraries). APIs serve as building blocks for programmers that create software applications.
asynchronous	A signal whose data is acknowledged or acted upon immediately, irrespective of any clock signal.
bandgap reference	A stable voltage reference design that matches the positive temperature coefficient of VT with the negative temperature coefficient of VBE, to produce a zero temperature coefficient (ideally) reference.
bandwidth	1. The frequency range of a message or information processing system measured in hertz. 2. The width of the spectral region over which an amplifier (or absorber) has substantial gain (or loss); it is sometimes represented more specifically as, for example, full width at half maximum.

Glossary (continued)

shift register	A memory storage device that sequentially shifts a word either left or right to output a stream of serial data.
slave device	A device that allows another device to control the timing for data exchanges between two devices. Or when devices are cascaded in width, the slave device is the one that allows another device to control the timing of data exchanges between the cascaded devices and an external interface. The controlling device is called the master device.
SRAM	An acronym for static random access memory. A memory device where you can store and retrieve data at a high rate of speed. The term static is used because, after a value is loaded into an SRAM cell, it remains unchanged until it is explicitly altered or until power is removed from the device.
SROM	An acronym for supervisory read only memory. The SROM holds code that is used to boot the device, calibrate circuitry, and perform Flash operations. The functions of the SROM may be accessed in normal user code, operating from Flash.
stop bit	A signal following a character or block that prepares the receiving device to receive the next character or block.
synchronous	1. A signal whose data is not acknowledged or acted upon until the next active edge of a clock signal. 2. A system whose operation is synchronized by a clock signal.
tri-state	A function whose output can adopt three states: 0, 1, and Z (high-impedance). The function does not drive any value in the Z state and, in many respects, may be considered to be disconnected from the rest of the circuit, allowing another output to drive the same net.
UART	A UART or universal asynchronous receiver-transmitter translates between parallel bits of data and serial bits.
user modules	Pre-build, pre-tested hardware/firmware peripheral functions that take care of managing and configuring the lower level Analog and Digital PSoC Blocks. User Modules also provide high level ***API (Application Programming Interface)*** for the peripheral function.
user space	The bank 0 space of the register map. The registers in this bank are more likely to be modified during normal program execution and not just during initialization. Registers in bank 1 are most likely to be modified only during the initialization phase of the program.
V_{DD}	A name for a power net meaning "voltage drain." The most positive power supply signal. Usually 5 V or 3.3 V.
V_{SS}	A name for a power net meaning "voltage source." The most negative power supply signal.
watchdog timer	A timer that must be serviced periodically. If it is not serviced, the CPU resets after a specified period of time.

Document History Page

Document Title: CY8C21123/CY8C21223/CY8C21323, PSoC® Programmable System-on-Chip™ Document Number: 38-12022				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	133248	NWJ	See ECN	New silicon and document (Revision **).
*A	208900	NWJ	See ECN	Add new part, new package and update all ordering codes to Pb-free.
*B	212081	NWJ	See ECN	Expand and prepare Preliminary version.
*C	227321	CMS Team	See ECN	Update specs., data, format.
*D	235973	SFV	See ECN	Updated Overview and Electrical Spec. chapters, along with 24-pin pinout. Added CMP_GO_EN register (1,64h) to mapping table.
*E	290991	HMT	See ECN	Update datasheet standards per SFV memo. Fix device table. Add part numbers to pinouts and fine tune. Change 20-pin SSOP to CY8C21323. Add Reflow Temp. table. Update diagrams and specs.
*F	301636	HMT	See ECN	DC Chip-Level Specification changes. Update links to new CY.com Portal.
*G	324073	HMT	See ECN	Obtained clearer 16 SOIC package. Update Thermal Impedances and Solder Reflow tables. Re-add pinout ISSP notation. Fix ADC type-o. Fix TMP register names. Update Electrical Specifications. Add CY logo. Update CY copyright. Make datasheet Final.
*H	2588457	KET / HMI / AESA	10/22/2008	New package information on page 9. Converted datasheet to new template. Added 16-Pin OFN package diagram.
*I	2618175	OGNE / PYRS	12/09/2008	Added Note in Ordering Information Section. Changed title from PSoC Mixed-Signal Array to PSoC Programmable System-on-Chip. Updated ‘Development Tools’ and ‘Designing with PSoC Designer’ sections on pages 5 and 6
*J	2682782	MAXK / AESA	04/03/2009	Corrected 16 COL pinout.
*K	2699713	MAXK	04/29/2009	Minor ECN to correct paragraph style of 16 COL Pinout. No change in content.
*L	2762497	JVY	09/11/2009	Updated DC GPIO, AC Chip-Level, and AC Programming Specifications as follows: Modified F_{IMO6} and T_{WRITE} specifications. Replaced T_{RAMP} time) specification with SR_{POWER_UP} (slew rate) specification. Added note [11] to Flash Endurance specification. Added I_{OH}, I_{OL}, DC_{ILO}, F_{32K_U}, $T_{POWERUP}$, $T_{ERASEALL}$, $T_{PROGRAM\_HOT}$, and $T_{PROGRAM\_COLD}$ specifications..
*M	2792630	TTO	10/26/2009	Updated ordering information for CY8C21223-24LGXI to indicate availability of XRES pin.
*N	2901653	NJF	03/30/2010	Changed 16-pin COL to 16-pin QFN in the datasheet. Added Contents. Updated links in Sales, Solutions, and Legal Information Updated Cypress website links. Added $T_{BAKETEMP}$ and $T_{BAKETIME}$ parameters in Absolute Maximum Ratings Updated 5-V and 3.3-V AC Chip-Level Specifications Updated Notes in Packaging Information and package diagrams. Updated Ordering Code Definitions
*O	2928895	YJI	05/06/2010	No technical updates. Included with EROS spec.

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