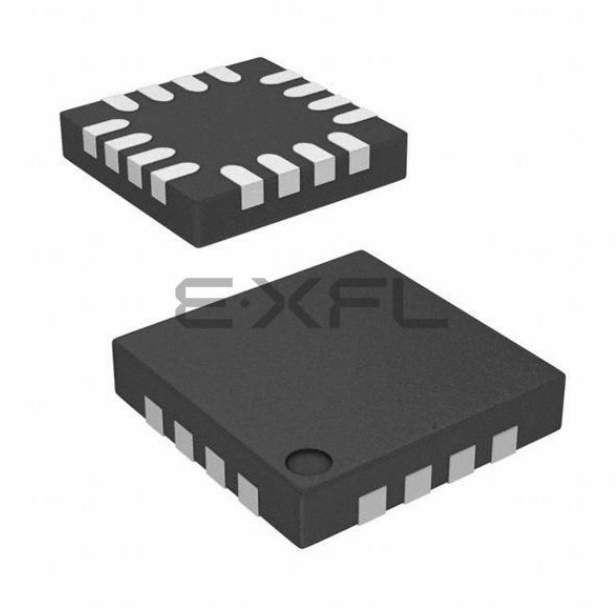

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	12
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.25V
Data Converters	A/D 8x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	16-UFQFN
Supplier Device Package	16-QFN (3x3)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c21223-24lgxit

PSoC Functional Overview

The PSoC family consists of many programmable system-on-chip controller devices. These devices are designed to replace multiple traditional MCU-based system components with a low cost single-chip programmable component. A PSoC device includes configurable blocks of analog and digital logic, and programmable interconnect. This architecture allows you to create customized peripheral configurations, to match the requirements of each individual application. Additionally, a fast CPU, Flash program memory, SRAM data memory, and configurable I/O are included in a range of convenient pinouts.

The PSoC architecture, as shown in Figure 1, consists of four main areas: the Core, the System Resources, the Digital System, and the Analog System. Configurable global bus resources allow the combining of all device resources into a complete custom system. Each PSoC device includes four digital blocks. Depending on the PSoC package, up to two analog comparators and up to 16 GPIO are also included. The GPIO provide access to the global digital and analog interconnects.

PSoC Core

The PSoC Core is a powerful engine that supports a rich instruction set. It encompasses SRAM for data storage, an interrupt controller, sleep and watchdog timers, and internal main oscillator (IMO), and internal low-speed oscillator (ILO). The CPU core, called the M8C, is a powerful processor with speeds up to 24 MHz. The M8C is a four MIPS 8-bit Harvard-architecture microprocessor.

System Resources provide additional capability, such as digital clocks or I^2C functionality for implementing an I^2C master, slave, MultiMaster, an internal voltage reference that provides an absolute value of 1.3 V to a number of PSoC subsystems, an SMP that generates normal operating voltages off a single battery cell, and various system resets supported by the M8C.

The digital system consists of an array of digital PSoC blocks, which can be configured into any number of digital peripherals. The digital blocks can be connected to the GPIO through a series of global bus that can route any signal to any pin. This frees designs from the constraints of a fixed peripheral controller.

The analog system consists of four analog PSoC blocks, supporting comparators and analog-to-digital conversion up to 10 bits of precision.

Digital System

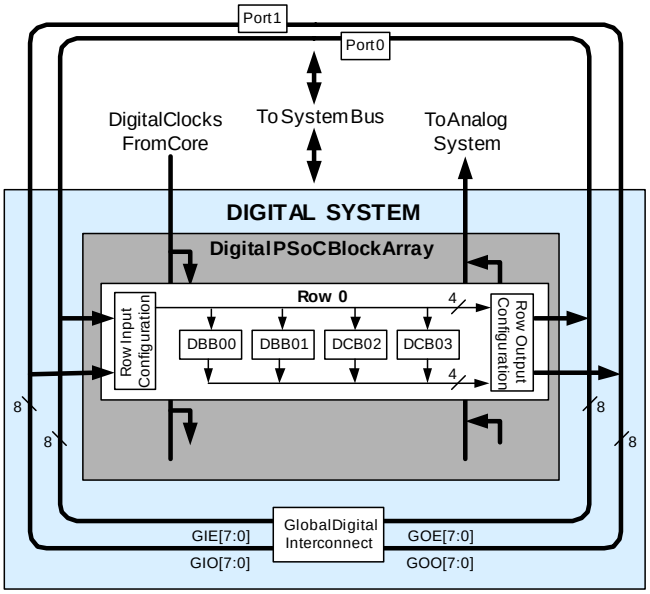
The digital system consists of four digital PSoC blocks. Each block is an 8-bit resource that can be used alone or combined with other blocks to form 8, 16, 24, and 32-bit peripherals, which are called user modules. Digital peripheral configurations include:

- PWMs (8- and 16-bit)
- PWMs with dead band (8- and 16-bit)
- Counters (8- to 32-bit)
- Timers (8- to 32-bit)
- UART 8-bit with selectable parity (up to two)
- SPI master and slave
- I^2C slave, master, multi-master (one available as a system resource)
- Cyclical redundancy checker/generator (8-bit)
- IrDA (up to two)
- Pseudo random sequence generators (8- to 32-bit)

The digital blocks can be connected to any GPIO through a series of global bus that can route any signal to any pin. The busses also allow for signal multiplexing and performing logic operations. This configurability frees your designs from the constraints of a fixed peripheral controller.

Digital blocks are provided in rows of four, where the number of blocks varies by PSoC device family. This provides an optimum choice of system resources for your application. Family resources are shown in Table 1 on page 5.

Figure 1. Digital System Block Diagram



Analog System

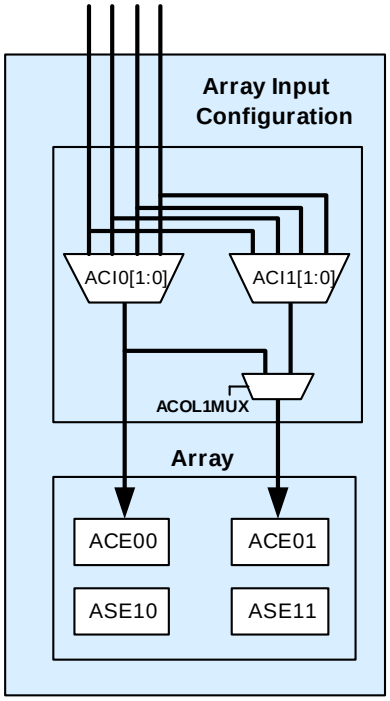
The analog system consists of four configurable blocks to allow creation of complex analog signal flows. Analog peripherals are very flexible and may be customized to support specific application requirements. Some of the more common PSoC analog functions (most available as user modules) are:

- Analog-to-digital converters (single or dual, with 8-bit or 10-bit resolution)
- Pin-to-pin comparators (one)
- Single-ended comparators (up to 2) with absolute (1.3 V) reference or 8-bit DAC reference
- 1.3 V reference (as a system resource)

In most PSoC devices, analog blocks are provided in columns of three, which includes one CT (continuous time) and two SC (switched capacitor) blocks. The CY8C21x23 devices provide limited functionality Type “E” analog blocks. Each column contains one CT block and one SC block.

The number of blocks on the device family is listed in Table 1 on page 5.

Figure 2. CY8C21x23 Analog System Block Diagram



Additional System Resources

System resources, some of which listed in the previous sections, provide additional capability useful to complete systems. Additional resources include a switch mode pump, low voltage detection, and power on reset. The merits of each system resource are.

- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks can be routed to both the digital and analog systems. Additional clocks can be generated using digital PSoC blocks as clock dividers.
- The I^2C module provides 100 and 400 kHz communication over two wires. Slave, master, and multi-master modes are all supported.
- LVD interrupts can signal the application of falling voltage levels, while the advanced POR (power on reset) circuit eliminates the need for a system supervisor.
- An internal 1.3 V voltage reference provides an absolute reference for the analog system, including ADCs and DACs.
- An integrated switch mode pump (SMP) generates normal operating voltages from a single 1.2 V battery cell, providing a low cost boost converter.

Pin Information

This section describes, lists, and illustrates the CY8C21x23 PSoC device pins and pinout configurations. Every port pin (labeled with a “P”) is capable of Digital I/O. However, V_{SS}, V_{DD}, SMP, and XRES are not capable of Digital I/O.

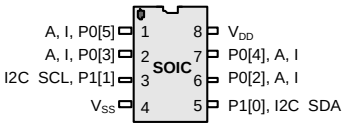
8-Pin Part Pinout

Table 2. Pin Definitions – CY8C21123 8-Pin SOIC

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O	I	P0[5]	Analog column mux input
2	I/O	I	P0[3]	Analog column mux input
3	I/O		P1[1]	I^2C serial clock (SCL), ISSP-SCLK[3]
4	Power		V_{SS}	Ground connection
5	I/O		P1[0]	I^2C serial data (SDA), ISSP-SDATA[3]
6	I/O	I	P0[2]	Analog column mux input
7	I/O	I	P0[4]	Analog column mux input
8	Power		V_{DD}	Supply voltage

LEGEND: A = Analog, I = Input, and O = Output.

Figure 3. CY8C21123 8-Pin SOIC



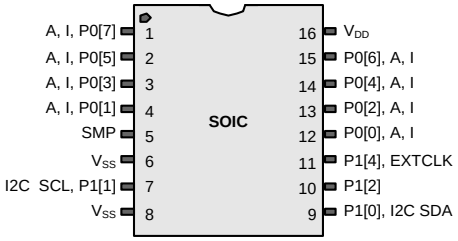
16-Pin Part Pinout

Table 3. Pin Definitions – CY8C21223 16-Pin SOIC

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O	I	P0[7]	Analog column mux input
2	I/O	I	P0[5]	Analog column mux input
3	I/O	I	P0[3]	Analog column mux input
4	I/O	I	P0[1]	Analog column mux input
5	Power		SMP	SMP connection to required external components
6	Power		V_{SS}	Ground connection
7	I/O		P1[1]	I^2C SCL, ISSP-SCLK[3]
8	Power		V_{SS}	Ground connection
9	I/O		P1[0]	I^2C SDA, ISSP-SDATA[3]
10	I/O		P1[2]	
11	I/O		P1[4]	Optional external clock input (EXTCLK)
12	I/O	I	P0[0]	Analog column mux input
13	I/O	I	P0[2]	Analog column mux input
14	I/O	I	P0[4]	Analog column mux input
15	I/O	I	P0[6]	Analog column mux input
16	Power		V_{DD}	Supply voltage

LEGEND A = Analog, I = Input, and O = Output.

Figure 4. CY8C21223 16-Pin SOIC



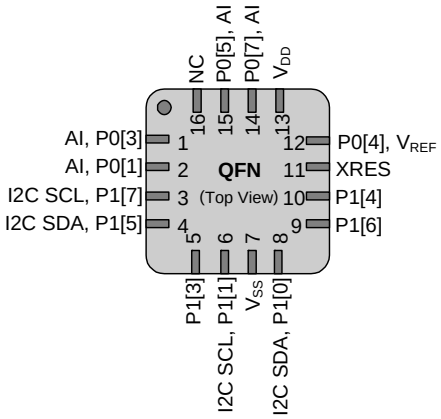
Note
3. These are the ISSP pins, which are not high Z at POR (power on reset). See the PSoC Technical Reference Manual for details.

Table 4. Pin Definitions – CY8C21223 16-Pin QFN with no E-Pad [4]

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O	I	P0[3]	Analog column mux input
2	I/O	I	P0[1]	Analog column mux input
3	I/O		P1[7]	I^2C SCL
4	I/O		P1[5]	I^2C SDA
5	I/O		P1[3]	
6	I/O		P1[1]	I^2C SCL, ISSP-SCLK[5]
7	Power		V_{SS}	Ground connection
8	I/O		P1[0]	I^2C SDA, ISSP-SDATA[5]
9	I/O		P1[6]	
10	I/O		P1[4]	EXTCLK
11	Input		XRES	Active high external reset with internal pull-down
12	I/O	I	P0[4]	V_{REF}
13	Power		V_{DD}	Supply voltage
14	I/O	I	P0[7]	Analog column mux input
15	I/O	I	P0[5]	Analog column mux input
16			NC	No Connection. Pin must be left floating

LEGEND A = Analog, I = Input, and O = Output.

Figure 5. CY8C21223 16-Pin QFN



Notes
4. The center pad on the QFN package must be connected to ground (Vss) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.
5. These are the ISSP pins, which are not high Z at POR (power on reset). See the PSoC Technical Reference Manual for details.

Register Reference

This section lists the registers of the CY8C21x23 PSoC device. For detailed register information, refer the PSoC Technical Reference Manual.

Register Conventions

The register conventions specific to this section are listed in the following table.

Table 7. Register Conventions

Convention	Description
R	Read register or bit(s)
W	Write register or bit(s)
L	Logical register or bit(s)
C	Clearable register or bit(s)
#	Access is bit specific

Register Mapping Tables

The PSoC device has a total register address space of 512 bytes. The register space is referred to as I/O space and is divided into two banks. The XOI bit in the Flag register (CPU_F) determines the bank you are currently in. When the XOI bit is set, you are in Bank 1.

Note In the following register mapping tables, blank fields are Reserved and must not be accessed.

Table 9. Register Map Bank 1 Table: Configuration Space (continued)

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
	1C			5C			9C			DC	
	1D			5D			9D		OSC_GO_EN	DD	RW
	1E			5E			9E		OSC_CR4	DE	RW
	1F			5F			9F		OSC_CR3	DF	RW
DBB00FN	20	RW	CLK_CR0	60	RW		A0		OSC_CR0	E0	RW
DBB00IN	21	RW	CLK_CR1	61	RW		A1		OSC_CR1	E1	RW
DBB00OU	22	RW	ABF_CR0	62	RW		A2		OSC_CR2	E2	RW
	23		AMD_CR0	63	RW		A3		VLT_CR	E3	RW
DBB01FN	24	RW	CMP_GO_EN	64	RW		A4		VLT_CMP	E4	R
DBB01IN	25	RW		65			A5		ADC0_TR	E5	RW
DBB01OU	26	RW	AMD_CR1	66	RW		A6		ADC1_TR	E6	RW
	27		ALT_CR0	67	RW		A7			E7	
DCB02FN	28	RW		68			A8		IMO_TR	E8	W
DCB02IN	29	RW		69			A9		ILO_TR	E9	W
DCB02OU	2A	RW		6A			AA		BDG_TR	EA	RW
	2B		CLK_CR3	6B	RW		AB		ECO_TR	EB	W
DCB03FN	2C	RW	TMP_DR0	6C	RW		AC			EC	
DCB03IN	2D	RW	TMP_DR1	6D	RW		AD			ED	
DCB03OU	2E	RW	TMP_DR2	6E	RW		AE			EE	
	2F		TMP_DR3	6F	RW		AF			EF	
	30			70		RDI0RI	B0	RW		F0	
	31			71		RDI0SYN	B1	RW		F1	
	32		ACE00CR1	72	RW	RDI0IS	B2	RW		F2	
	33		ACE00CR2	73	RW	RDI0LT0	B3	RW		F3	
	34			74		RDI0LT1	B4	RW		F4	
	35			75		RDI0RO0	B5	RW		F5	
	36		ACE01CR1	76	RW	RDI0RO1	B6	RW		F6	
	37		ACE01CR2	77	RW		B7		CPU_F	F7	RL
	38			78			B8			F8	
	39			79			B9			F9	
	3A			7A			BA		FLS_PR1	FA	RW
	3B			7B			BB			FB	
	3C			7C			BC			FC	
	3D			7D			BD			FD	
	3E			7E			BE		CPU_SCR1	FE	#
	3F			7F			BF		CPU_SCR0	FF	#

Blank fields are Reserved and must not be accessed. # Access is bit specific.

Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8C21x23 PSoC device. For up to date electrical specifications, check if you have the latest datasheet by visiting the web at http://www.cypress.com.

Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted.

Refer to Table 24 on page 25 for the electrical specifications on the IMO using SLIMO mode.

Figure 10. Voltage versus CPU Frequency

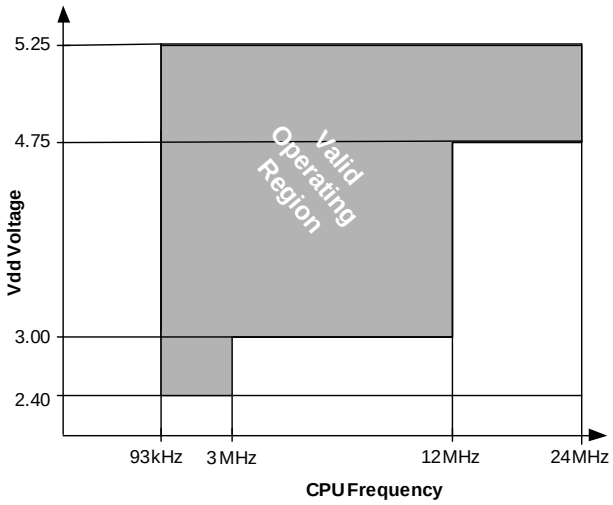
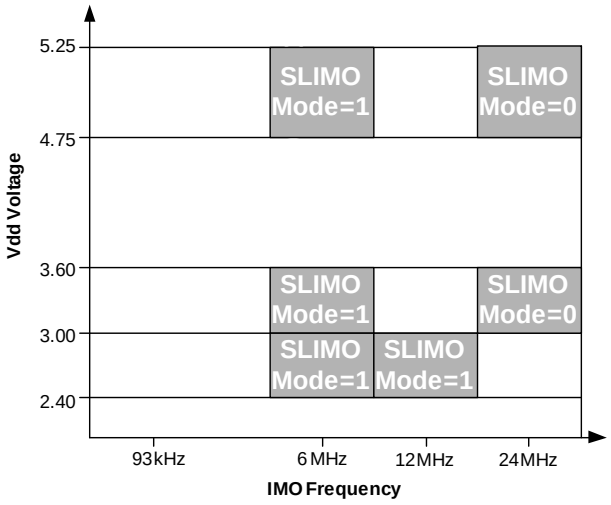


Figure 11. Voltage versus IMO Frequency



Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Table 10. Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units	Notes
T_{STG}	Storage temperature	–55	–	+100	°C	Higher storage temperatures reduce data retention time. Recommended storage temperature is +25 °C ± 25 °C. Extended duration storage temperatures higher than 65 °C degrade reliability.
$T_{BAKETEMP}$	Bake temperature	–	125	See package label	°C	
$t_{BAKETIME}$	Bake time	See package label	–	72	Hours	
T_A	Ambient temperature with power applied	–40	–	+85	°C	
V_{DD}	Supply voltage on V_{DD} relative to V_{SS}	–0.5	–	+6.0	V	
V_{IO}	DC input voltage	V_{SS} – 0.5	–	V_{DD} + 0.5	V	
V_{IOZ}	DC voltage applied to tristate	V_{SS} – 0.5	–	V_{DD} + 0.5	V	
I_{MIO}	Maximum current into any port pin	–25	–	+50	mA	
ESD	Electro static discharge voltage	2000	–	–	V	Human body model ESD
LU	Latch-up current	–	–	200	mA	

Table 23. 2.7-V AC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{IMO12}	IMO frequency for 12 MHz	11.5	12	12.7[24,25]	MHz	Trimmed for 2.7 V operation using factory trim values. See Figure 11 on page 16. SLIMO mode = 1.
F_{IMO6}	IMO frequency for 6 MHz	5.5	6	6.5[24,25]	MHz	Trimmed for 2.7 V operation using factory trim values. See Figure 11 on page 16. SLIMO mode = 1.
F_{CPU1}	CPU frequency (2.7 V nominal)	0.093	3	3.15[24]	MHz	24 MHz only for SLIMO mode = 0.
F_{BLK27}	Digital PSoC block frequency (2.7 V nominal)	0	12	12.5[24,25]	MHz	Refer to the section AC Digital Block Specifications on page 26.
F_{32K1}	ILO frequency	8	32	96	kHz	
F_{32K_U}	ILO untrimmed frequency	5	–	100	kHz	After a reset and before the M8C starts to run, the ILO is not trimmed. See the system resets section of the PSoC Technical Reference Manual for details on this timing.
t_{XRST}	External reset pulse width	10	–	–	µs	
DC_{ILO}	ILO duty cycle	20	50	80	%	
F_{MAX}	Maximum frequency of signal on row input or row output	–	–	12.3	MHz	
SR_{POWER_UP}	Power supply slew rate	–	–	250	V/ms	V_{DD} slew rate during power-up.
$t_{POWERUP}$	Time from end of POR to CPU executing code	–	16	100	ms	Power-up from 0 V. See the system resets section of the PSoC Technical Reference Manual.
t_{jit_IMO}	12-MHz IMO cycle-to-cycle jitter (RMS)[26]	–	400	1000	ps	
	12-MHz IMO long term N cycle-to-cycle jitter (RMS)[26]	–	600	1300	ps	N = 32
	12-MHz IMO period jitter (RMS)[26]	–	100	500	ps	

Notes
24. 2.4 V < V_{DD} < 3.0 V.
25. Refer to the application note Adjusting PSoC Microcontroller Trims for Dual Voltage-Range Operation – AN2012 for more information on maximum frequency for user modules.
26. Refer to the application note, Understanding Datasheet Jitter Specifications for Cypress Timing Products – AN5054 for more information on jitter specifications.

AC Digital Block Specifications

Table 28 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 28. 5-V and 3.3-V AC Digital Block Specifications

Function	Description	Min	Typ	Max	Unit	Notes
All functions	Block input clock frequency					
	V_{DD} ≥ 4.75 V	–	–	50.4	MHz	
	V_{DD} < 4.75 V	–	–	25.2	MHz	
Timer	Input clock frequency					
	No capture, V_{DD} ≥ 4.75 V	–	–	50.4	MHz	
	No capture, V_{DD} < 4.75 V	–	–	25.2	MHz	
	With capture	–	–	25.2	MHz	
	Capture pulse width	50[27]	–	–	ns	
Counter	Input clock frequency					
	No enable input, V_{DD} ≥ 4.75 V	–	–	50.4	MHz	
	No enable input, V_{DD} < 4.75 V	–	–	25.2	MHz	
	With enable input	–	–	25.2	MHz	
	Enable input pulse width	50[27]	–	–	ns	
Dead Band	Kill pulse width					
	Asynchronous restart mode	20	–	–	ns	
	Synchronous restart mode	50[27]	–	–	ns	
	Disable mode	50[27]	–	–	ns	
	Input clock frequency					
	V_{DD} ≥ 4.75 V	–	–	50.4	MHz	
	V_{DD} < 4.75 V	–	–	25.2	MHz	
CRCPRS (PRS Mode)	Input clock frequency					
	V_{DD} ≥ 4.75 V	–	–	50.4	MHz	
	V_{DD} < 4.75 V	–	–	25.2	MHz	
CRCPRS (CRC Mode)	Input clock frequency	–	–	25.2	MHz	
SPIM	Input clock frequency	–	–	8.2	MHz	The SPI serial clock (SCLK) frequency is equal to the input clock frequency divided by 2.
SPIS	Input clock (SCLK) frequency	–	–	4.1	MHz	The input clock is the SPI SCLK in SPIS mode.
	Width of SS_negated between transmissions	50[27]	–	–	ns	
Transmitter	Input clock frequency					The baud rate is equal to the input clock frequency divided by 8.
	V_{DD} ≥ 4.75 V, 2 stop bits	–	–	50.4	MHz	
	V_{DD} ≥ 4.75 V, 1 stop bit	–	–	25.2	MHz	
	V_{DD} < 4.75 V	–	–	25.2	MHz	
Receiver	Input clock frequency					The baud rate is equal to the input clock frequency divided by 8.
	V_{DD} ≥ 4.75 V, 2 stop bits	–	–	50.4	MHz	
	V_{DD} ≥ 4.75 V, 1 stop bit	–	–	25.2	MHz	
	V_{DD} < 4.75 V	–	–	25.2	MHz	

Note
27. 50 ns minimum input pulse width is based on the input synchronizers running at 24 MHz (42 ns nominal period).

AC Programming Specifications

Table 33 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 33. AC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{RSCLK}	Rise time of SCLK	1	–	20	ns	
t_{FSCLK}	Fall time of SCLK	1	–	20	ns	
t_{SSCLK}	Data set up time to falling edge of SCLK	40	–	–	ns	
t_{HSCLK}	Data hold time from falling edge of SCLK	40	–	–	ns	
F_{SCLK}	Frequency of SCLK	0	–	8	MHz	
t_{ERASEB}	Flash erase time (block)	–	10	–	ms	
t_{WRITE}	Flash block write time	–	80	–	ms	
t_{DSCLK3}	Data out delay from falling edge of SCLK	–	–	50	ns	3.0 ≤ V_{DD} ≤ 3.6.
t_{DSCLK2}	Data out delay from falling edge of SCLK	–	–	70	ns	2.4 ≤ V_{DD} ≤ 3.0.
$t_{ERASEALL}$	Flash erase time (bulk)	–	20	–	ms	Erase all blocks and protection fields at once.
$t_{PROGRAM\_HOT}$	Flash block erase + flash block write time	–	–	180[30]	ms	0 °C ≤ Tj ≤ 100 °C.
$t_{PROGRAM\_COLD}$	Flash block erase + flash block write time	–	–	360[30]	ms	–40 °C ≤ Tj ≤ 0 °C.

AC I^2C Specifications

Table 34 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 34. AC Characteristics of the I^2C SDA and SCL Pins for V_{CC} ≥ 3.0 V

Symbol	Description	Standard Mode		Fast Mode		Units
		Min	Max	Min	Max	
F_{SCLI2C}	SCL clock frequency	0	100	0	400	kHz
$t_{HDSTAI2C}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	4.0	–	0.6	–	µs
t_{LOWI2C}	Low period of the SCL clock	4.7	–	1.3	–	µs
$t_{HIGHI2C}$	High period of the SCL clock	4.0	–	0.6	–	µs
$t_{SUSTAI2C}$	Setup time for a repeated START condition	4.7	–	0.6	–	µs
$t_{HDDATI2C}$	Data hold time	0	–	0	–	µs
$t_{SUDATI2C}$	Data setup time	250	–	100[29]	–	ns
$t_{SUSTOI2C}$	Setup time for STOP condition	4.0	–	0.6	–	µs
t_{BUFI2C}	Bus free time between a STOP and START condition	4.7	–	1.3	–	µs
t_{SPI2C}	Pulse width of spikes are suppressed by the input filter	–	–	0	50	ns

Notes

29. A fast-mode I^2C-bus device can be used in a standard-mode I^2C-bus system, but the requirement t_{SUDAT} ≥ 250 ns must then be met. This automatically becomes the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t_{rmax} + t_{SUDAT} = 1000 + 250 = 1250 ns (according to the standard-mode I^2C-bus specification) before the SCL line is released.
30. For the full industrial range, you must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the application note, Design Aids — Reading and Writing PSoC® Flash – AN2015 for more information on Flash APIs.

Packaging Information

This section illustrates the packaging specifications for the CY8C21x23 PSoC device, along with the thermal impedances for each package and minimum solder reflow peak temperature.

Important Note Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the emulator pod drawings at http://www.cypress.com.

Packaging Dimensions

Figure 15. 8-pin SOIC (150 Mils) S0815/SZ815/SW815 Package Outline, 51-85066

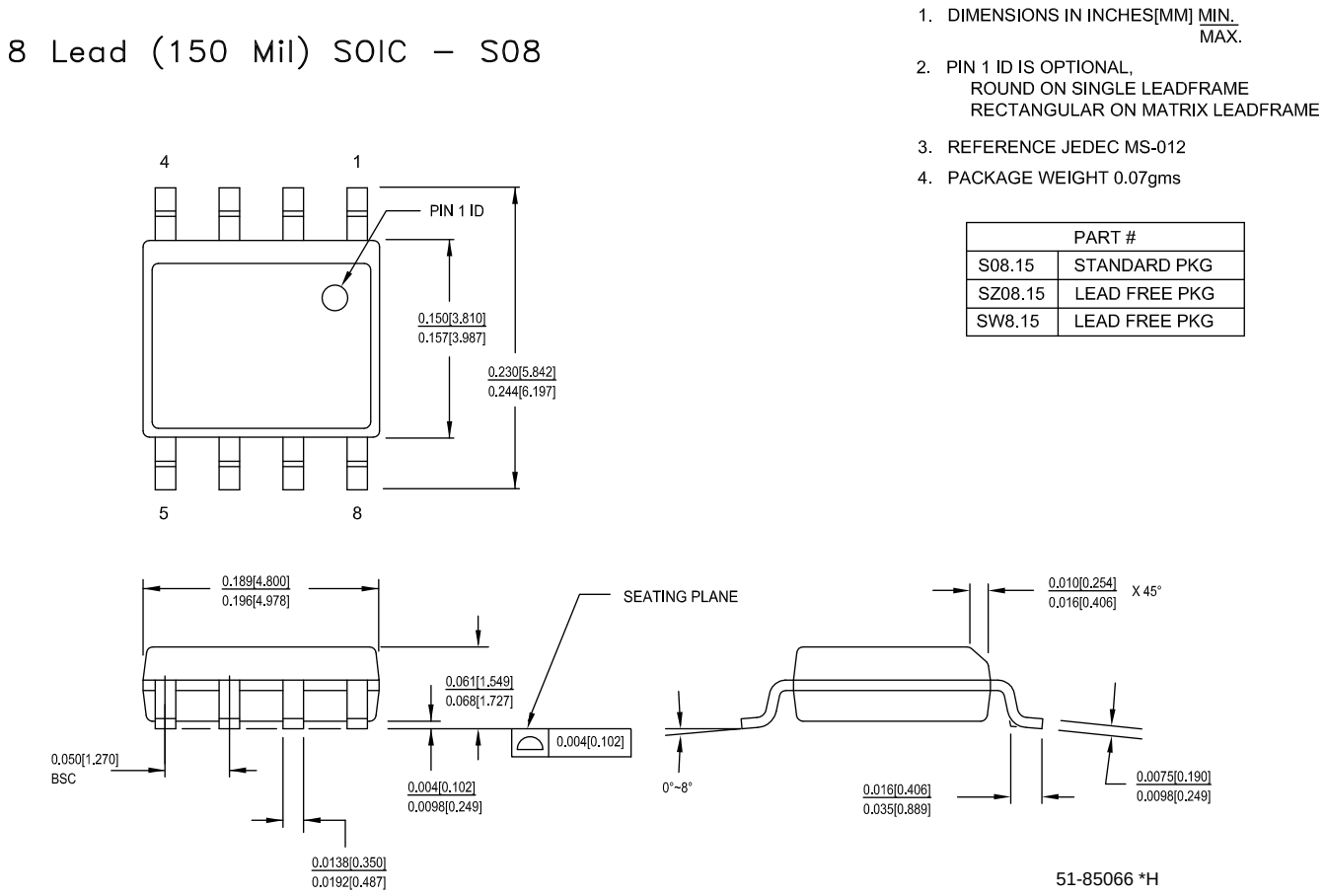


Figure 16. 16-Pin (150-Mil) SOIC

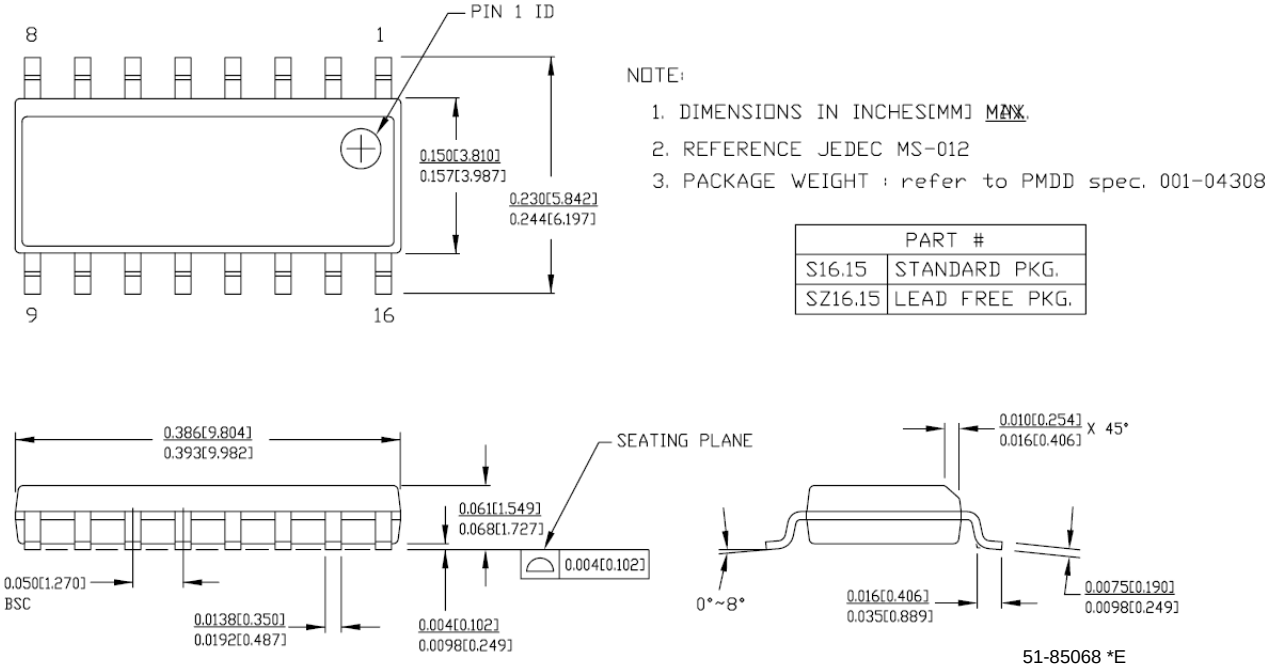
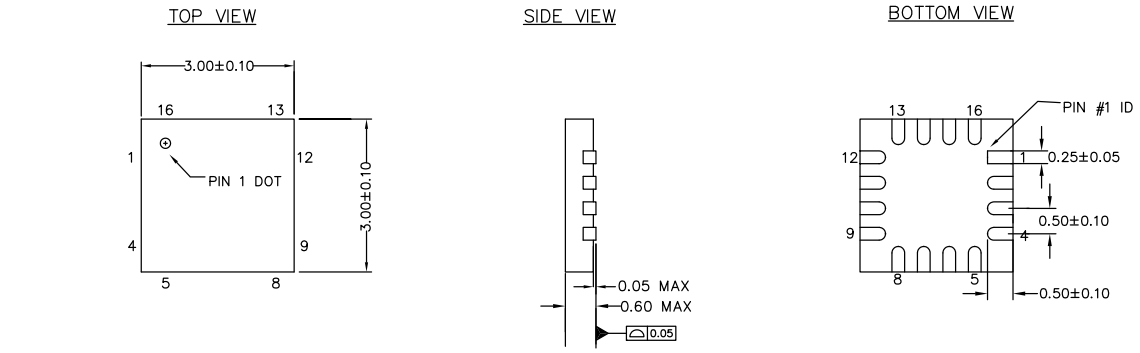


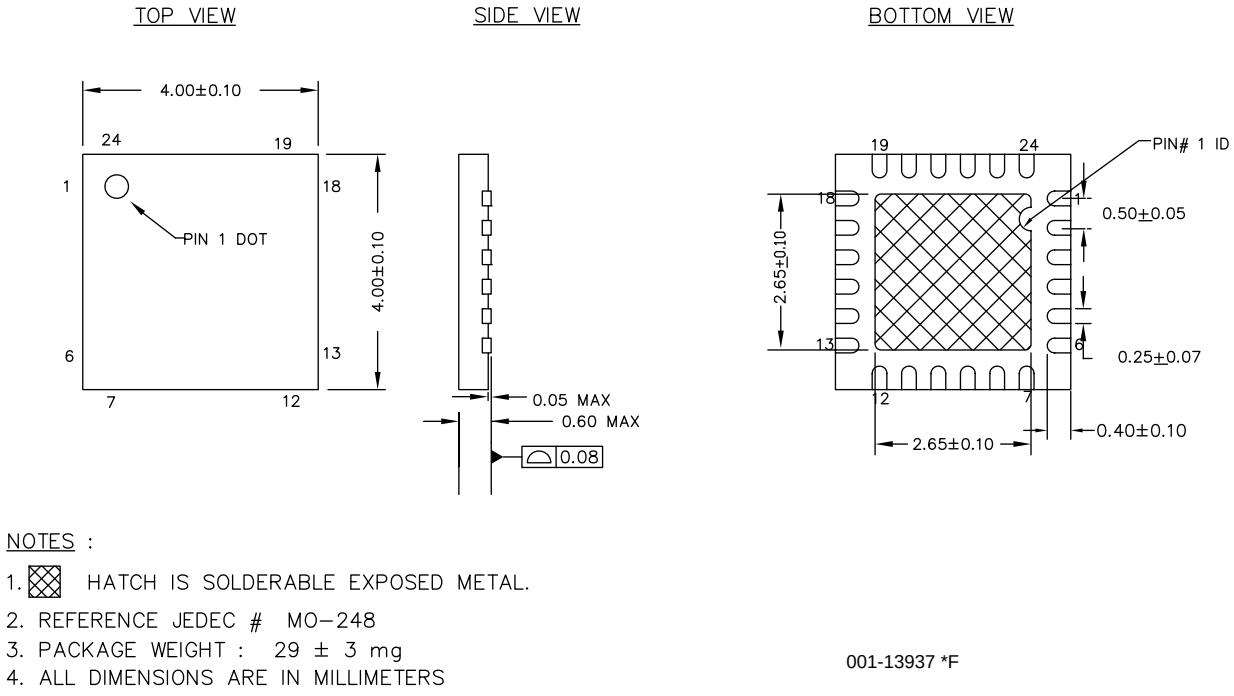
Figure 17. 16-Pin QFN with no E-Pad



NOTES
1. REFERENCE JEDEC # MO-220
2. ALL DIMENSIONS ARE IN MILLIMETERS

001-09116 *J

Figure 20. 24-Pin (4 × 4) QFN (Sawn)



NOTES :

1. HATCH IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC # MO−248
3. PACKAGE WEIGHT : 29 ± 3 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-13937 *F

Important Note For information on the preferred dimensions for mounting QFN packages, refer the application note, Application Notes for Surface Mount Assembly of Amkor's MicroLeadFrame (MLF) Packages available at http://www.amkor.com.

Note that pinned vias for thermal conduction are not required for the low power 24, 32, and 48-pin QFN PSoC devices.

Ordering Information

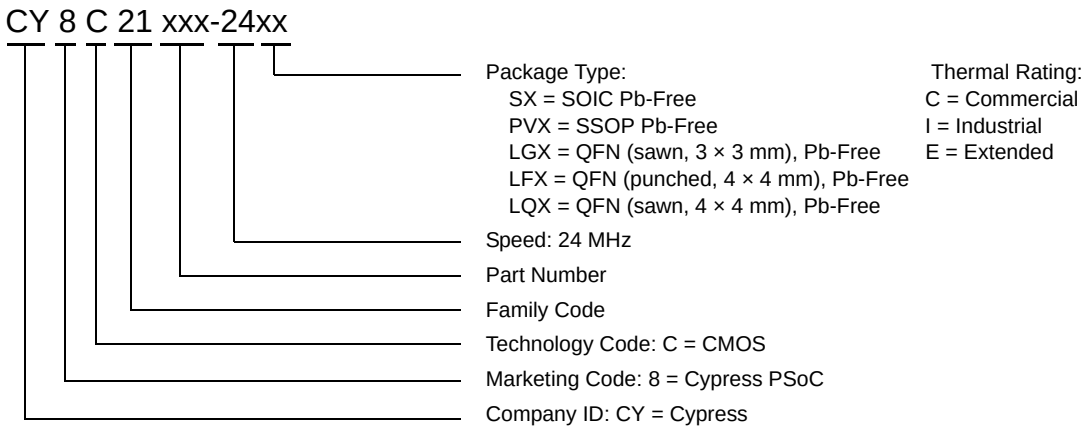
The following table lists the CY8C21x23 PSoC device's key package features and ordering codes.

Table 38. CY8C21x23 PSoC Device Key Features and Ordering Information

Package	Ordering Code	Flash (Bytes)	RAM (Bytes)	Switch Mode Pump	Temperature Range	Digital PSoC Blocks	Analog Blocks	Digital I/O Pins	Analog Inputs	Analog Outputs	XRES Pin
8-Pin (150-Mil) SOIC	CY8C21123-24SXI	4 K	256	No	–40 °C to +85 °C	4	4	6	4	0	No
8-Pin (150-Mil) SOIC (Tape and Reel)	CY8C21123-24SXIT	4 K	256	No	–40 °C to +85 °C	4	4	6	4	0	No
16-Pin (150-Mil) SOIC	CY8C21223-24SXI	4 K	256	Yes	–40 °C to +85 °C	4	4	12	8	0	No
16-Pin (150-Mil) SOIC (Tape and Reel)	CY8C21223-24SXIT	4 K	256	Yes	–40 °C to +85 °C	4	4	12	8	0	No
16-Pin (3 × 3) QFN with no E-Pad	CY8C21223-24LGXI	4 K	256	No	–40 °C to +85 °C	4	4	12	8	0	Yes
20-Pin (210-Mil) SSOP	CY8C21323-24PVXI	4 K	256	No	–40 °C to +85 °C	4	4	16	8	0	Yes
20-Pin (210-Mil) SSOP (Tape and Reel)	CY8C21323-24PVXIT	4 K	256	No	–40 °C to +85 °C	4	4	16	8	0	Yes
24-Pin (4 × 4) QFN (Punched)	CY8C21323-24LFXI	4 K	256	Yes	–40 °C to +85 °C	4	4	16	8	0	Yes
24-Pin (4 × 4) QFN (Punched) (Tape and Reel)	CY8C21323-24LFXIT	4 K	256	Yes	–40 °C to +85 °C	4	4	16	8	0	Yes
24-Pin (4 × 4) QFN (Sawn)	CY8C21323-24LQXI	4 K	256	Yes	–40 °C to +85 °C	4	4	16	8	0	Yes
24-Pin (4 × 4) QFN (Sawn) (Tape and Reel)	CY8C21323-24LQXIT	4 K	256	Yes	–40 °C to +85 °C	4	4	16	8	0	Yes

Note For Die sales information, contact a local Cypress sales office or Field Applications Engineer (FAE).

Ordering Code Definitions



Acronyms

Acronyms Used

Table 39 lists the acronyms that are used in this document.

Table 39. Acronyms Used in this Datasheet

Acronym	Description	Acronym	Description
AC	alternating current	PCB	printed circuit board
ADC	analog-to-digital converter	PGA	programmable gain amplifier
API	application programming interface	POR	power on reset
CMOS	complementary metal oxide semiconductor	PPOR	precision power on reset
CPU	central processing unit	PRS	pseudo-random sequence
CRC	cyclic redundancy check	PSoC®	Programmable System-on-Chip
CT	continuous time	PWM	pulse width modulator
DAC	digital-to-analog converter	QFN	quad flat no leads
DC	direct current	SC	switched capacitor
EEPROM	electrically erasable programmable read-only memory	SLIMO	slow IMO
GPIO	general purpose I/O	SMP	switch mode pump
ICE	in-circuit emulator	SOIC	small-outline integrated circuit
IDE	integrated development environment	SPI™	serial peripheral interface
ILO	internal low speed oscillator	SRAM	static random access memory
IMO	internal main oscillator	SROM	supervisory read only memory
I/O	input/output	SSOP	shrink small-outline package
IrDA	infrared data association	UART	universal asynchronous reciever / transmitter
ISSP	in-system serial programming	USB	universal serial bus
LVD	low voltage detect	WDT	watchdog timer
MCU	microcontroller unit	XRES	external reset
MIPS	million instructions per second		

Reference Documents

CY8CPLC20, CY8CLED16P01, CY8C29x66, CY8C27x43, CY8C24x94, CY8C24x23, CY8C24x23A, CY8C22x13, CY8C21x34, CY8C21x23, CY7C64215, CY7C603xx, CY8CNP1xx, and CYWUSB6953 PSoC® Programmable System-on-Chip Technical Reference Manual (TRM) (001-14463)

Design Aids – Reading and Writing PSoC® Flash – AN2015 (001-40459)

Adjusting PSoC® Trims for 3.3 V and 2.7 V Operation – AN2012 (001-17397)

Understanding Datasheet Jitter Specifications for Cypress Timing Products – AN5054 (001-14503)

Application Notes for Surface Mount Assembly of Amkor's MicroLeadFrame (MLF) Packages – available at http://www.amkor.com.

Glossary (continued)

microcontroller	An integrated circuit chip that is designed primarily for control systems and products. In addition to a CPU, a microcontroller typically includes memory, timing circuits, and IO circuitry. The reason for this is to permit the realization of a controller with a minimal quantity of chips, thus achieving maximal possible miniaturization. This in turn, reduces the volume and the cost of the controller. The microcontroller is normally not used for general-purpose computation as is a microprocessor.
mixed-signal	The reference to a circuit containing both analog and digital techniques and components.
modulator	A device that imposes a signal on a carrier.
noise	1. A disturbance that affects a signal and that may distort the information carried by the signal. 2. The random variations of one or more characteristics of any entity such as voltage, current, or data.
oscillator	A circuit that may be crystal controlled and is used to generate a clock frequency.
parity	A technique for testing transmitting data. Typically, a binary digit is added to the data to make the sum of all the digits of the binary data either always even (even parity) or always odd (odd parity).
Phase-locked loop (PLL)	An electronic circuit that controls an ***oscillator*** so that it maintains a constant phase angle relative to a reference signal.
pinouts	The pin number assignment: the relation between the logical inputs and outputs of the PSoC device and their physical counterparts in the printed circuit board (PCB) package. Pinouts involve pin numbers as a link between schematic and PCB design (both being computer generated files) and may also involve pin names.
port	A group of pins, usually eight.
Power on reset (POR)	A circuit that forces the PSoC device to reset when the voltage is lower than a pre-set level. This is one type of hardware reset.
PSoC®	Cypress Semiconductor's PSoC® is a registered trademark and Programmable System-on-Chip™ is a trademark of Cypress.
PSoC Designer™	The software for Cypress' Programmable System-on-Chip technology.
pulse width modulator (PWM)	An output in the form of duty cycle which varies as a function of the applied measurand.
RAM	An acronym for random access memory. A data-storage device from which data can be read out and new data can be written in.
register	A storage device with a specific capacity, such as a bit or byte.
reset	A means of bringing a system back to a know state. See hardware reset and software reset.
ROM	An acronym for read only memory. A data-storage device from which data can be read out, but new data cannot be written in.
serial	1. Pertaining to a process in which all events occur one after the other. 2. Pertaining to the sequential or consecutive occurrence of two or more related activities in a single device or channel.
settling time	The time it takes for an output signal or value to stabilize after the input has changed from one value to another.

Glossary (continued)

shift register	A memory storage device that sequentially shifts a word either left or right to output a stream of serial data.
slave device	A device that allows another device to control the timing for data exchanges between two devices. Or when devices are cascaded in width, the slave device is the one that allows another device to control the timing of data exchanges between the cascaded devices and an external interface. The controlling device is called the master device.
SRAM	An acronym for static random access memory. A memory device where you can store and retrieve data at a high rate of speed. The term static is used because, after a value is loaded into an SRAM cell, it remains unchanged until it is explicitly altered or until power is removed from the device.
SROM	An acronym for supervisory read only memory. The SROM holds code that is used to boot the device, calibrate circuitry, and perform Flash operations. The functions of the SROM may be accessed in normal user code, operating from Flash.
stop bit	A signal following a character or block that prepares the receiving device to receive the next character or block.
synchronous	1. A signal whose data is not acknowledged or acted upon until the next active edge of a clock signal. 2. A system whose operation is synchronized by a clock signal.
tri-state	A function whose output can adopt three states: 0, 1, and Z (high-impedance). The function does not drive any value in the Z state and, in many respects, may be considered to be disconnected from the rest of the circuit, allowing another output to drive the same net.
UART	A UART or universal asynchronous receiver-transmitter translates between parallel bits of data and serial bits.
user modules	Pre-build, pre-tested hardware/firmware peripheral functions that take care of managing and configuring the lower level Analog and Digital PSoC Blocks. User Modules also provide high level ***API (Application Programming Interface)*** for the peripheral function.
user space	The bank 0 space of the register map. The registers in this bank are more likely to be modified during normal program execution and not just during initialization. Registers in bank 1 are most likely to be modified only during the initialization phase of the program.
V_{DD}	A name for a power net meaning "voltage drain." The most positive power supply signal. Usually 5 V or 3.3 V.
V_{SS}	A name for a power net meaning "voltage source." The most negative power supply signal.
watchdog timer	A timer that must be serviced periodically. If it is not serviced, the CPU resets after a specified period of time.

Document History Page

Document Title: CY8C21123/CY8C21223/CY8C21323, PSoC® Programmable System-on-Chip™ Document Number: 38-12022				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	133248	NWJ	See ECN	New silicon and document (Revision **).
*A	208900	NWJ	See ECN	Add new part, new package and update all ordering codes to Pb-free.
*B	212081	NWJ	See ECN	Expand and prepare Preliminary version.
*C	227321	CMS Team	See ECN	Update specs., data, format.
*D	235973	SFV	See ECN	Updated Overview and Electrical Spec. chapters, along with 24-pin pinout. Added CMP_GO_EN register (1,64h) to mapping table.
*E	290991	HMT	See ECN	Update datasheet standards per SFV memo. Fix device table. Add part numbers to pinouts and fine tune. Change 20-pin SSOP to CY8C21323. Add Reflow Temp. table. Update diagrams and specs.
*F	301636	HMT	See ECN	DC Chip-Level Specification changes. Update links to new CY.com Portal.
*G	324073	HMT	See ECN	Obtained clearer 16 SOIC package. Update Thermal Impedances and Solder Reflow tables. Re-add pinout ISSP notation. Fix ADC type-o. Fix TMP register names. Update Electrical Specifications. Add CY logo. Update CY copyright. Make datasheet Final.
*H	2588457	KET / HMI / AESA	10/22/2008	New package information on page 9. Converted datasheet to new template. Added 16-Pin OFN package diagram.
*I	2618175	OGNE / PYRS	12/09/2008	Added Note in Ordering Information Section. Changed title from PSoC Mixed-Signal Array to PSoC Programmable System-on-Chip. Updated ‘Development Tools’ and ‘Designing with PSoC Designer’ sections on pages 5 and 6
*J	2682782	MAXK / AESA	04/03/2009	Corrected 16 COL pinout.
*K	2699713	MAXK	04/29/2009	Minor ECN to correct paragraph style of 16 COL Pinout. No change in content.
*L	2762497	JVY	09/11/2009	Updated DC GPIO, AC Chip-Level, and AC Programming Specifications as follows: Modified F_{IMO6} and T_{WRITE} specifications. Replaced T_{RAMP} time) specification with SR_{POWER_UP} (slew rate) specification. Added note [11] to Flash Endurance specification. Added I_{OH}, I_{OL}, DC_{ILO}, F_{32K_U}, $T_{POWERUP}$, $T_{ERASEALL}$, $T_{PROGRAM\_HOT}$, and $T_{PROGRAM\_COLD}$ specifications..
*M	2792630	TTO	10/26/2009	Updated ordering information for CY8C21223-24LGXI to indicate availability of XRES pin.
*N	2901653	NJF	03/30/2010	Changed 16-pin COL to 16-pin QFN in the datasheet. Added Contents. Updated links in Sales, Solutions, and Legal Information Updated Cypress website links. Added $T_{BAKETEMP}$ and $T_{BAKETIME}$ parameters in Absolute Maximum Ratings Updated 5-V and 3.3-V AC Chip-Level Specifications Updated Notes in Packaging Information and package diagrams. Updated Ordering Code Definitions
*O	2928895	YJI	05/06/2010	No technical updates. Included with EROS spec.

Document History Page (continued)

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Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*Z	4623500	DIMA	01/14/2015	Updated Pin Information: Updated 20-Pin Part Pinout: Updated Table 5: Added Note 6 and referred the same note in description of pin 5 and pin 10. Updated 24-Pin Part Pinout: Updated Table 6: Added Note 9 and referred the same note in description of pin 3, pin 9 and pin 21. Updated Packaging Information: spec 51-85066 – Changed revision from *F to *G. spec 51-85077 – Changed revision from *E to *F. Completing Sunset Review.
AA	5090662	ARVI	01/18/2016	Updated Ordering Information, Ordering Code Definitions, and Errata. Upated figure title in Figure 19. Updated Table 38. Updated Figure 15 (spec 51-85066 *G to *H) in Packaging Information. Added Figure 20 (spec 001-13937 *F) in Packaging Information.

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