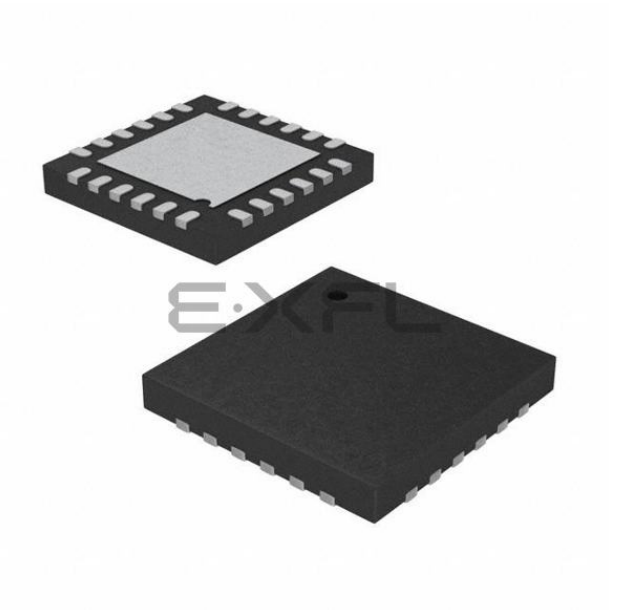

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | M8C |
| Core Size | 8-Bit |
| Speed | 24MHz |
| Connectivity | I²C, SPI, UART/USART |
| Peripherals | POR, PWM, WDT |
| Number of I/O | 16 |
| Program Memory Size | 4KB (4K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 256 x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.4V ~ 5.25V |
| Data Converters | A/D 8x8b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 24-UFQFN Exposed Pad |
| Supplier Device Package | 24-QFN (4x4) |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/cy8c21323-24lqxi |

## Contents

## Glossary (continued)

| | |
|---|---|
| shift register | A memory storage device that sequentially shifts a word either left or right to output a stream of serial data. |
| slave device | A device that allows another device to control the timing for data exchanges between two devices. Or when devices are cascaded in width, the slave device is the one that allows another device to control the timing of data exchanges between the cascaded devices and an external interface. The controlling device is called the master device. |
| SRAM | An acronym for static random access memory. A memory device where you can store and retrieve data at a high rate of speed. The term static is used because, after a value is loaded into an SRAM cell, it remains unchanged until it is explicitly altered or until power is removed from the device. |
| SROM | An acronym for supervisory read only memory. The SROM holds code that is used to boot the device, calibrate circuitry, and perform Flash operations. The functions of the SROM may be accessed in normal user code, operating from Flash. |
| stop bit | A signal following a character or block that prepares the receiving device to receive the next character or block. |
| synchronous | 1. A signal whose data is not acknowledged or acted upon until the next active edge of a clock signal.<br>2. A system whose operation is synchronized by a clock signal. |
| tri-state | A function whose output can adopt three states: 0, 1, and Z (high-impedance). The function does not drive any value in the Z state and, in many respects, may be considered to be disconnected from the rest of the circuit, allowing another output to drive the same net. |
| UART | A UART or universal asynchronous receiver-transmitter translates between parallel bits of data and serial bits. |
| user modules | Pre-build, pre-tested hardware/firmware peripheral functions that take care of managing and configuring the lower level Analog and Digital PSoC Blocks. User Modules also provide high level ***API (Application Programming Interface)*** for the peripheral function. |
| user space | The bank 0 space of the register map. The registers in this bank are more likely to be modified during normal program execution and not just during initialization. Registers in bank 1 are most likely to be modified only during the initialization phase of the program. |
| $V_{DD}$ | A name for a power net meaning "voltage drain." The most positive power supply signal. Usually 5 V or 3.3 V. |
| $V_{SS}$ | A name for a power net meaning "voltage source." The most negative power supply signal. |
| watchdog timer | A timer that must be serviced periodically. If it is not serviced, the CPU resets after a specified period of time. |