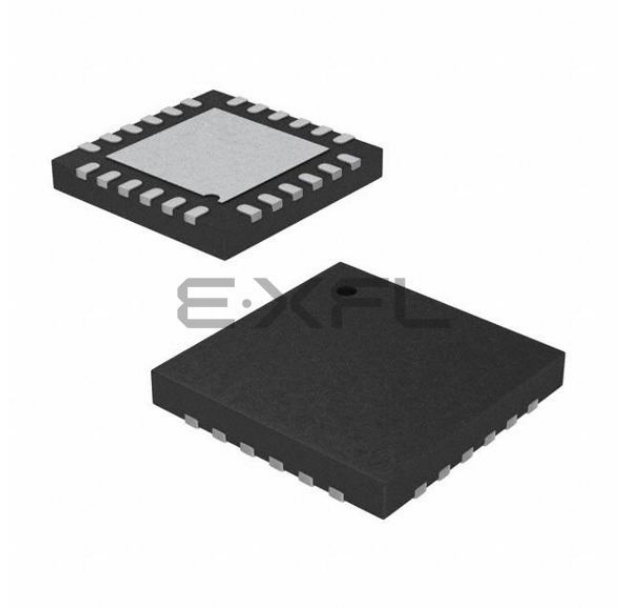

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	M8C
Core Size	8-Bit
Speed	24MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	16
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.25V
Data Converters	A/D 8x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	24-UFQFN Exposed Pad
Supplier Device Package	24-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c21323-24lqxit

Contents

PSoC Functional Overview

The PSoC family consists of many programmable system-on-chip controller devices. These devices are designed to replace multiple traditional MCU-based system components with a low cost single-chip programmable component. A PSoC device includes configurable blocks of analog and digital logic, and programmable interconnect. This architecture allows you to create customized peripheral configurations, to match the requirements of each individual application. Additionally, a fast CPU, Flash program memory, SRAM data memory, and configurable I/O are included in a range of convenient pinouts.

The PSoC architecture, as shown in Figure 1, consists of four main areas: the Core, the System Resources, the Digital System, and the Analog System. Configurable global bus resources allow the combining of all device resources into a complete custom system. Each PSoC device includes four digital blocks. Depending on the PSoC package, up to two analog comparators and up to 16 GPIO are also included. The GPIO provide access to the global digital and analog interconnects.

PSoC Core

The PSoC Core is a powerful engine that supports a rich instruction set. It encompasses SRAM for data storage, an interrupt controller, sleep and watchdog timers, and internal main oscillator (IMO), and internal low-speed oscillator (ILO). The CPU core, called the M8C, is a powerful processor with speeds up to 24 MHz. The M8C is a four MIPS 8-bit Harvard-architecture microprocessor.

System Resources provide additional capability, such as digital clocks or I^2C functionality for implementing an I^2C master, slave, MultiMaster, an internal voltage reference that provides an absolute value of 1.3 V to a number of PSoC subsystems, an SMP that generates normal operating voltages off a single battery cell, and various system resets supported by the M8C.

The digital system consists of an array of digital PSoC blocks, which can be configured into any number of digital peripherals. The digital blocks can be connected to the GPIO through a series of global bus that can route any signal to any pin. This frees designs from the constraints of a fixed peripheral controller.

The analog system consists of four analog PSoC blocks, supporting comparators and analog-to-digital conversion up to 10 bits of precision.

Digital System

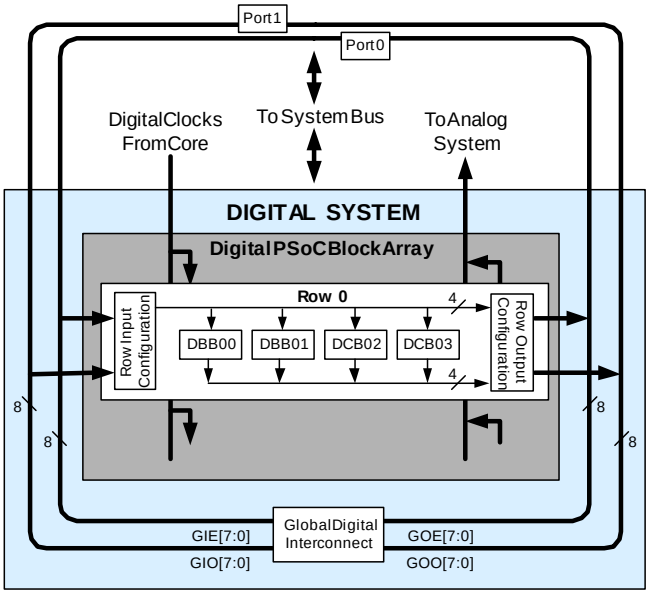
The digital system consists of four digital PSoC blocks. Each block is an 8-bit resource that can be used alone or combined with other blocks to form 8, 16, 24, and 32-bit peripherals, which are called user modules. Digital peripheral configurations include:

- PWMs (8- and 16-bit)
- PWMs with dead band (8- and 16-bit)
- Counters (8- to 32-bit)
- Timers (8- to 32-bit)
- UART 8-bit with selectable parity (up to two)
- SPI master and slave
- I^2C slave, master, multi-master (one available as a system resource)
- Cyclical redundancy checker/generator (8-bit)
- IrDA (up to two)
- Pseudo random sequence generators (8- to 32-bit)

The digital blocks can be connected to any GPIO through a series of global bus that can route any signal to any pin. The busses also allow for signal multiplexing and performing logic operations. This configurability frees your designs from the constraints of a fixed peripheral controller.

Digital blocks are provided in rows of four, where the number of blocks varies by PSoC device family. This provides an optimum choice of system resources for your application. Family resources are shown in Table 1 on page 5.

Figure 1. Digital System Block Diagram



Analog System

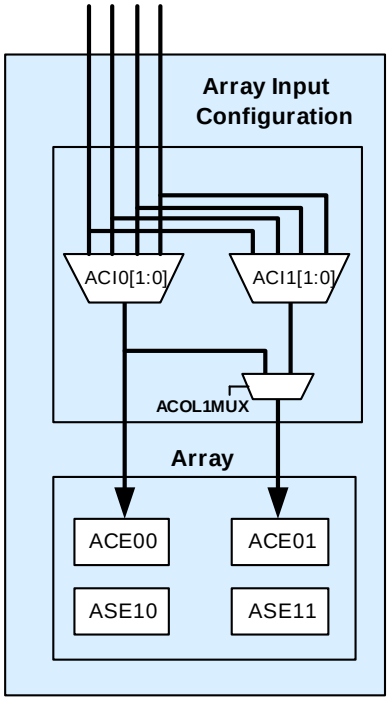
The analog system consists of four configurable blocks to allow creation of complex analog signal flows. Analog peripherals are very flexible and may be customized to support specific application requirements. Some of the more common PSoC analog functions (most available as user modules) are:

- Analog-to-digital converters (single or dual, with 8-bit or 10-bit resolution)
- Pin-to-pin comparators (one)
- Single-ended comparators (up to 2) with absolute (1.3 V) reference or 8-bit DAC reference
- 1.3 V reference (as a system resource)

In most PSoC devices, analog blocks are provided in columns of three, which includes one CT (continuous time) and two SC (switched capacitor) blocks. The CY8C21x23 devices provide limited functionality Type “E” analog blocks. Each column contains one CT block and one SC block.

The number of blocks on the device family is listed in Table 1 on page 5.

Figure 2. CY8C21x23 Analog System Block Diagram



Additional System Resources

System resources, some of which listed in the previous sections, provide additional capability useful to complete systems. Additional resources include a switch mode pump, low voltage detection, and power on reset. The merits of each system resource are.

- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks can be routed to both the digital and analog systems. Additional clocks can be generated using digital PSoC blocks as clock dividers.
- The I^2C module provides 100 and 400 kHz communication over two wires. Slave, master, and multi-master modes are all supported.
- LVD interrupts can signal the application of falling voltage levels, while the advanced POR (power on reset) circuit eliminates the need for a system supervisor.
- An internal 1.3 V voltage reference provides an absolute reference for the analog system, including ADCs and DACs.
- An integrated switch mode pump (SMP) generates normal operating voltages from a single 1.2 V battery cell, providing a low cost boost converter.

PSoC Device Characteristics

Depending on your PSoC device characteristics, the digital and analog systems can have 16, 8, or 4 digital blocks, and 12, 6, or 4 analog blocks. Table 1 lists the resources available for specific PSoC device groups. The PSoC device covered by this datasheet is highlighted.

Table 1. PSoC Device Characteristics

PSoC Part Number	Digital I/O	Digital Rows	Digital Blocks	Analog Inputs	Analog Outputs	Analog Columns	Analog Blocks	SRAM Size	Flash Size
CY8C29x66	up to 64	4	16	up to 12	4	4	12	2 K	32 K
CY8C28xxx	up to 44	up to 3	up to 12	up to 44	up to 4	up to 6	up to 12 + 4[1]	1 K	16 K
CY8C27x43	up to 44	2	8	up to 12	4	4	12	256	16 K
CY8C24x94	up to 56	1	4	up to 48	2	2	6	1 K	16 K
CY8C24x23A	up to 24	1	4	up to 12	2	2	6	256	4 K
CY8C23x33	up to 26	1	4	up to 12	2	2	4	256	8 K
CY8C22x45	up to 38	2	8	up to 38	0	4	6[1]	1 K	16 K
CY8C21x45	up to 24	1	4	up to 24	0	4	6[1]	512	8 K
CY8C21x34	up to 28	1	4	up to 28	0	2	4[1]	512	8 K
CY8C21x23	up to 16	1	4	up to 8	0	2	4[1]	256	4 K
CY8C20x34	up to 28	0	0	up to 28	0	0	3[1,2]	512	8 K
CY8C20xx6	up to 36	0	0	up to 36	0	0	3[1,2]	up to 2 K	up to 32 K

Getting Started

The quickest way to understand PSoC silicon is to read this datasheet and then use the PSoC Designer Integrated Development Environment (IDE). This datasheet is an overview of the PSoC integrated circuit and presents specific pin, register, and electrical specifications.

For in depth information, along with detailed programming details, see the Technical Reference Manual for this PSoC device.

For up to date ordering, packaging, and electrical specification information, see the latest PSoC device datasheets on the web at http://www.cypress.com.

Application Notes

Application notes are an excellent introduction to the wide variety of possible PSoC designs. They can be found at http://www.cypress.com.

Development Kits

PSoC Development Kits are available online from Cypress at http://www.cypress.com and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

Training

Free PSoC technical training (on demand, webinars, and workshops) is available online at http://www.cypress.com. The training covers a wide variety of topics and skill levels to assist you in your designs.

CYPros Consultants

Certified PSoC Consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC Consultant go to http://www.cypress.com and refer to CYPros Consultants.

Solutions Library

Visit our growing library of solution focused designs at http://www.cypress.com. Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

Technical Support

For assistance with technical issues, search KnowledgeBase articles and forums at http://www.cypress.com. If you cannot find an answer to your question, call technical support at 1-800-541-4736.

Notes
1. Limited analog functionality.
2. Two analog blocks and one CapSense®.

Development Tool Selection

Software

PSoC Designer

At the core of the PSoC development software suite is PSoC Designer. Utilized by thousands of PSoC developers, this robust software has been facilitating PSoC designs for years. PSoC Designer is available free of charge at http://www.cypress.com. PSoC Designer comes with a free C compiler.

PSoC Designer Software Subsystems

You choose a base device to work with and then select different onboard analog and digital components called user modules that use the PSoC blocks. Examples of user modules are ADCs, DACs, Amplifiers, and Filters. You configure the user modules for your chosen application and connect them to each other and to the proper pins. Then you generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The tool also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic reconfiguration allows for changing configurations at run time. Code Generation Tools PSoC Designer supports multiple third-party C compilers and assemblers. The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. The choice is yours.

Assemblers. The assemblers allow assembly code to be merged seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and linked with other software modules to get absolute addressing.

C Language Compilers. C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices. The optimizing C compilers provide all the features of C tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

Debugger

PSoC Designer has a debug environment that provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow the designer to read and program and read and write data memory, read and write I/O registers, read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows the designer to create a trace buffer of registers and memory locations of interest.

In-Circuit Emulator

A low cost, high functionality In-Circuit Emulator (ICE) is available for development support. This hardware has the capability to program single devices. The emulator consists of a base unit that connects to the PC by way of a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full speed (24MHz) operation.

Standard Cypress PSoC IDE tools are available for debugging the CY8C20x36A/66A family of parts. However, the additional trace length and a minimal ground plane in the Flex-Pod can create noise problems that make it difficult to debug the design. A custom bonded On-Chip Debug (OCD) device is available in a 48-pin QFN package. The OCD device is recommended for debugging designs that have high current and/or high analog accuracy requirements. The QFN package is compact and is connected to the ICE through a high density connector.

PSoC Programmer

Flexible enough to be used on the bench in development, yet suitable for factory programming, PSoC Programmer works either as a standalone programming application or it can operate directly from PSoC Designer. PSoC Programmer software is compatible with both PSoC ICE-Cube in-circuit emulator and PSoC MiniProg. PSoC programmer is available free of charge at http://www.cypress.com/psocprogrammer.

Pin Information

This section describes, lists, and illustrates the CY8C21x23 PSoC device pins and pinout configurations. Every port pin (labeled with a “P”) is capable of Digital I/O. However, V_{SS}, V_{DD}, SMP, and XRES are not capable of Digital I/O.

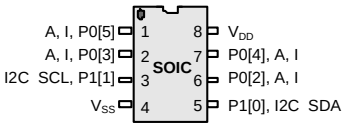
8-Pin Part Pinout

Table 2. Pin Definitions – CY8C21123 8-Pin SOIC

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O	I	P0[5]	Analog column mux input
2	I/O	I	P0[3]	Analog column mux input
3	I/O		P1[1]	I^2C serial clock (SCL), ISSP-SCLK[3]
4	Power		V_{SS}	Ground connection
5	I/O		P1[0]	I^2C serial data (SDA), ISSP-SDATA[3]
6	I/O	I	P0[2]	Analog column mux input
7	I/O	I	P0[4]	Analog column mux input
8	Power		V_{DD}	Supply voltage

LEGEND: A = Analog, I = Input, and O = Output.

Figure 3. CY8C21123 8-Pin SOIC



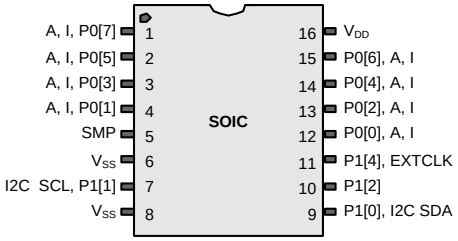
16-Pin Part Pinout

Table 3. Pin Definitions – CY8C21223 16-Pin SOIC

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O	I	P0[7]	Analog column mux input
2	I/O	I	P0[5]	Analog column mux input
3	I/O	I	P0[3]	Analog column mux input
4	I/O	I	P0[1]	Analog column mux input
5	Power		SMP	SMP connection to required external components
6	Power		V_{SS}	Ground connection
7	I/O		P1[1]	I^2C SCL, ISSP-SCLK[3]
8	Power		V_{SS}	Ground connection
9	I/O		P1[0]	I^2C SDA, ISSP-SDATA[3]
10	I/O		P1[2]	
11	I/O		P1[4]	Optional external clock input (EXTCLK)
12	I/O	I	P0[0]	Analog column mux input
13	I/O	I	P0[2]	Analog column mux input
14	I/O	I	P0[4]	Analog column mux input
15	I/O	I	P0[6]	Analog column mux input
16	Power		V_{DD}	Supply voltage

LEGEND A = Analog, I = Input, and O = Output.

Figure 4. CY8C21223 16-Pin SOIC



Note
3. These are the ISSP pins, which are not high Z at POR (power on reset). See the PSoC Technical Reference Manual for details.

Register Reference

This section lists the registers of the CY8C21x23 PSoC device. For detailed register information, refer the PSoC Technical Reference Manual.

Register Conventions

The register conventions specific to this section are listed in the following table.

Table 7. Register Conventions

Convention	Description
R	Read register or bit(s)
W	Write register or bit(s)
L	Logical register or bit(s)
C	Clearable register or bit(s)
#	Access is bit specific

Register Mapping Tables

The PSoC device has a total register address space of 512 bytes. The register space is referred to as I/O space and is divided into two banks. The XOI bit in the Flag register (CPU_F) determines the bank you are currently in. When the XOI bit is set, you are in Bank 1.

Note In the following register mapping tables, blank fields are Reserved and must not be accessed.

Table 8. Register Map Bank 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW		40		ASE10CR0	80	RW		C0	
PRT0IE	01	RW		41			81			C1	
PRT0GS	02	RW		42			82			C2	
PRT0DM2	03	RW		43			83			C3	
PRT1DR	04	RW		44		ASE11CR0	84	RW		C4	
PRT1IE	05	RW		45			85			C5	
PRT1GS	06	RW		46			86			C6	
PRT1DM2	07	RW		47			87			C7	
	08			48			88			C8	
	09			49			89			C9	
	0A			4A			8A			CA	
	0B			4B			8B			CB	
	0C			4C			8C			CC	
	0D			4D			8D			CD	
	0E			4E			8E			CE	
	0F			4F			8F			CF	
	10			50			90			D0	
	11			51			91			D1	
	12			52			92			D2	
	13			53			93			D3	
	14			54			94			D4	
	15			55			95			D5	
	16			56			96		I2C_CFG	D6	RW
	17			57			97		I2C_SCR	D7	#
	18			58			98		I2C_DR	D8	RW
	19			59			99		I2C_MSCR	D9	#
	1A			5A			9A		INT_CLR0	DA	RW
	1B			5B			9B		INT_CLR1	DB	RW
	1C			5C			9C			DC	
	1D			5D			9D		INT_CLR3	DD	RW
	1E			5E			9E		INT_MSK3	DE	RW
	1F			5F			9F			DF	
DBB00DR0	20	#	AMX_IN	60	RW		A0		INT_MSK0	E0	RW
DBB00DR1	21	W		61			A1		INT_MSK1	E1	RW
DBB00DR2	22	RW	PWM_CR	62	RW		A2		INT_VC	E2	RC
DBB00CR0	23	#		63			A3		RES_WDT	E3	W
DBB01DR0	24	#	CMP_CR0	64	#		A4			E4	
DBB01DR1	25	W		65			A5			E5	
DBB01DR2	26	RW	CMP_CR1	66	RW		A6		DEC_CR0	E6	RW
DBB01CR0	27	#		67			A7		DEC_CR1	E7	RW
DCB02DR0	28	#	ADC0_CR	68	#		A8			E8	
DCB02DR1	29	W	ADC1_CR	69	#		A9			E9	
DCB02DR2	2A	RW		6A			AA			EA	
DCB02CR0	2B	#		6B			AB			EB	
DCB03DR0	2C	#	TMP_DR0	6C	RW		AC			EC	
DCB03DR1	2D	W	TMP_DR1	6D	RW		AD			ED	
DCB03DR2	2E	RW	TMP_DR2	6E	RW		AE			EE	
DCB03CR0	2F	#	TMP_DR3	6F	RW		AF			EF	

Blank fields are Reserved and must not be accessed. # Access is bit specific.

Table 9. Register Map Bank 1 Table: Configuration Space (continued)

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
	1C			5C			9C			DC	
	1D			5D			9D		OSC_GO_EN	DD	RW
	1E			5E			9E		OSC_CR4	DE	RW
	1F			5F			9F		OSC_CR3	DF	RW
DBB00FN	20	RW	CLK_CR0	60	RW		A0		OSC_CR0	E0	RW
DBB00IN	21	RW	CLK_CR1	61	RW		A1		OSC_CR1	E1	RW
DBB00OU	22	RW	ABF_CR0	62	RW		A2		OSC_CR2	E2	RW
	23		AMD_CR0	63	RW		A3		VLT_CR	E3	RW
DBB01FN	24	RW	CMP_GO_EN	64	RW		A4		VLT_CMP	E4	R
DBB01IN	25	RW		65			A5		ADC0_TR	E5	RW
DBB01OU	26	RW	AMD_CR1	66	RW		A6		ADC1_TR	E6	RW
	27		ALT_CR0	67	RW		A7			E7	
DCB02FN	28	RW		68			A8		IMO_TR	E8	W
DCB02IN	29	RW		69			A9		ILO_TR	E9	W
DCB02OU	2A	RW		6A			AA		BDG_TR	EA	RW
	2B		CLK_CR3	6B	RW		AB		ECO_TR	EB	W
DCB03FN	2C	RW	TMP_DR0	6C	RW		AC			EC	
DCB03IN	2D	RW	TMP_DR1	6D	RW		AD			ED	
DCB03OU	2E	RW	TMP_DR2	6E	RW		AE			EE	
	2F		TMP_DR3	6F	RW		AF			EF	
	30			70		RDI0RI	B0	RW		F0	
	31			71		RDI0SYN	B1	RW		F1	
	32		ACE00CR1	72	RW	RDI0IS	B2	RW		F2	
	33		ACE00CR2	73	RW	RDI0LT0	B3	RW		F3	
	34			74		RDI0LT1	B4	RW		F4	
	35			75		RDI0RO0	B5	RW		F5	
	36		ACE01CR1	76	RW	RDI0RO1	B6	RW		F6	
	37		ACE01CR2	77	RW		B7		CPU_F	F7	RL
	38			78			B8			F8	
	39			79			B9			F9	
	3A			7A			BA		FLS_PR1	FA	RW
	3B			7B			BB			FB	
	3C			7C			BC			FC	
	3D			7D			BD			FD	
	3E			7E			BE		CPU_SCR1	FE	#
	3F			7F			BF		CPU_SCR0	FF	#

Blank fields are Reserved and must not be accessed. # Access is bit specific.

Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8C21x23 PSoC device. For up to date electrical specifications, check if you have the latest datasheet by visiting the web at http://www.cypress.com.

Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted.

Refer to Table 24 on page 25 for the electrical specifications on the IMO using SLIMO mode.

Figure 10. Voltage versus CPU Frequency

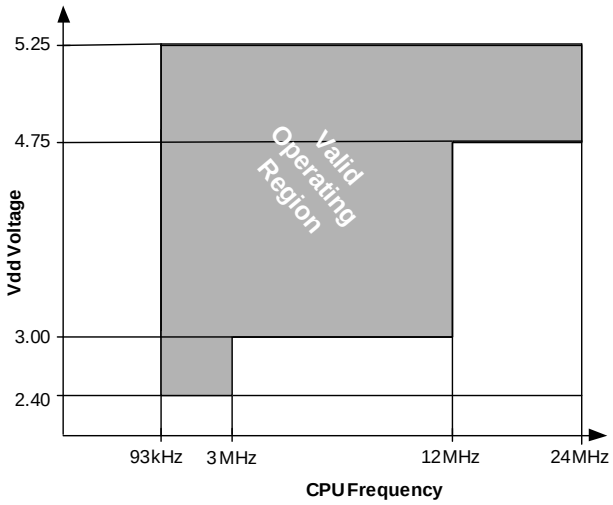
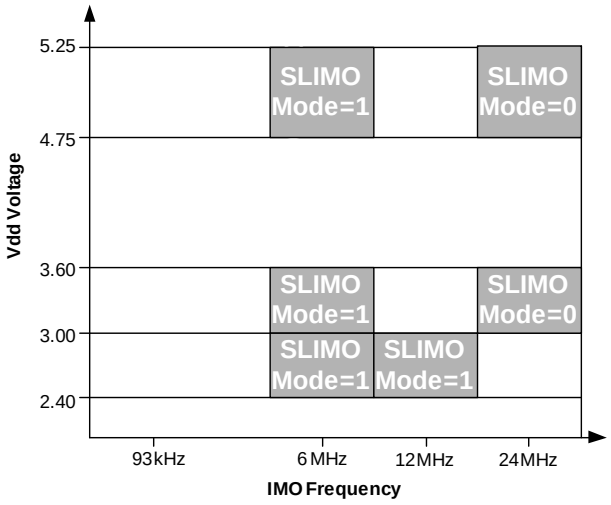


Figure 11. Voltage versus IMO Frequency



Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Table 10. Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units	Notes
T_{STG}	Storage temperature	–55	–	+100	°C	Higher storage temperatures reduce data retention time. Recommended storage temperature is +25 °C ± 25 °C. Extended duration storage temperatures higher than 65 °C degrade reliability.
$T_{BAKETEMP}$	Bake temperature	–	125	See package label	°C	
$t_{BAKETIME}$	Bake time	See package label	–	72	Hours	
T_A	Ambient temperature with power applied	–40	–	+85	°C	
V_{DD}	Supply voltage on V_{DD} relative to V_{SS}	–0.5	–	+6.0	V	
V_{IO}	DC input voltage	V_{SS} – 0.5	–	V_{DD} + 0.5	V	
V_{IOZ}	DC voltage applied to tristate	V_{SS} – 0.5	–	V_{DD} + 0.5	V	
I_{MIO}	Maximum current into any port pin	–25	–	+50	mA	
ESD	Electro static discharge voltage	2000	–	–	V	Human body model ESD
LU	Latch-up current	–	–	200	mA	

DC Switch Mode Pump Specifications

Table 18 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 18. DC Switch Mode Pump (SMP) Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{PUMP5V}	5 V output voltage from pump	4.75	5.0	5.25	V	Configuration of footnote.[11] Average, neglecting ripple. SMP trip voltage is set to 5.0 V.
V_{PUMP3V}	3.3 V output voltage from pump	3.00	3.25	3.60	V	Configuration of footnote.[11] Average, neglecting ripple. SMP trip voltage is set to 3.25 V.
V_{PUMP2V}	2.6 V output voltage from pump	2.45	2.55	2.80	V	Configuration of footnote.[11] Average, neglecting ripple. SMP trip voltage is set to 2.55 V.
I_{PUMP}	Available output current V_{BAT} = 1.8 V, V_{PUMP} = 5.0 V V_{BAT} = 1.5 V, V_{PUMP} = 3.25 V V_{BAT} = 1.3 V, V_{PUMP} = 2.55 V	 5 8 8	 – – –	 – – –	 mA mA mA	Configuration of footnote.[11] SMP trip voltage is set to 5.0 V. SMP trip voltage is set to 3.25 V. SMP trip voltage is set to 2.55 V.
V_{BAT5V}	Input voltage range from battery	1.8	–	5.0	V	Configuration of footnote.[11] SMP trip voltage is set to 5.0 V.
V_{BAT3V}	Input voltage range from battery	1.0	–	3.3	V	Configuration of footnote.[11] SMP trip voltage is set to 3.25 V.
V_{BAT2V}	Input voltage range from battery	1.0	–	2.8	V	Configuration of footnote.[11] SMP trip voltage is set to 2.55 V.
$V_{BATSTART}$	Minimum input voltage from battery to start pump	1.2	–	–	V	Configuration of footnote.[11] 0 °C ≤ T_A ≤ 100. 1.25 V at T_A = –40 °C.
ΔV_{PUMP_Line}	Line regulation (over Vi range)	–	5	–	$\%V_O$	Configuration of footnote.[11] V_O is the "V_{DD} Value for PUMP Trip" specified by the VM[2:0] setting in the DC POR and LVD Specification, Table 19 on page 21.
ΔV_{PUMP_Load}	Load regulation	–	5	–	$\%V_O$	Configuration of footnote.[11] V_O is the "V_{DD} Value for PUMP Trip" specified by the VM[2:0] setting in the DC POR and LVD Specification, Table 19 on page 21.
ΔV_{PUMP_Ripple}	Output voltage ripple (depends on cap/load)	–	100	–	mVpp	Configuration of footnote.[11] Load is 5 mA.
E_3	Efficiency	35	50	–	%	Configuration of footnote.[11] Load is 5 mA. SMP trip voltage is set to 3.25 V.
E_2	Efficiency	35	80	–	%	For I load = 1 mA, V_{PUMP} = 2.55 V, V_{BAT} = 1.3 V, 10 uH inductor, 1 uF capacitor, and Schottky diode.
F_{PUMP}	Switching frequency	–	1.3	–	MHz	
DC_{PUMP}	Switching duty cycle	–	50	–	%	

Note
11. L_1 = 2 mH inductor, C_1 = 10 mF capacitor, D_1 = Schottky diode. Refer to Figure 12 on page 21.

DC Programming Specifications

Table 20 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 20. DC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{DDP}	V_{DD} for programming and erase	4.5	5.0	5.5	V	This specification applies to the functional requirements of external programmer tools
V_{DDLV}	Low V_{DD} for verify	2.4	2.5	2.6	V	This specification applies to the functional requirements of external programmer tools
V_{DDHV}	High V_{DD} for verify	5.1	5.2	5.3	V	This specification applies to the functional requirements of external programmer tools
$V_{DDIWRITE}$	Supply voltage for flash write operations	2.70	–	5.25	V	This specification applies to this device when it is executing internal flash writes
I_{DDP}	Supply current during programming or verify	–	5	25	mA	
V_{ILP}	Input low voltage during programming or verify	–	–	0.8	V	
V_{IHP}	Input high voltage during programming or verify	2.2	–	–	V	
I_{ILP}	Input current when applying V_{ILP} to P1[0] or P1[1] during programming or verify	–	–	0.2	mA	Driving internal pull-down resistor
I_{IHP}	Input current when applying V_{IHP} to P1[0] or P1[1] during programming or verify	–	–	1.5	mA	Driving internal pull-down resistor
V_{OLV}	Output low voltage during programming or verify	–	–	V_{SS} + 0.75	V	
V_{OHV}	Output high voltage during programming or verify	V_{DD} – 1.0	–	V_{DD}	V	
$Flash_{ENPB}$	Flash endurance (per block)	50,000[16]	–	–	–	Erase/write cycles per block
$Flash_{ENT}$	Flash endurance (total)[17]	1,800,000	–	–	–	Erase/write cycles
$Flash_{DR}$	Flash data retention	10	–	–	Years	

DC I^2C Specifications

Table 20 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 21. DC I^2C Specifications[18]

Symbol	Description	Min	Typ	Max	Units	Notes
V_{ILI2C}	Input low level	–	–	0.3 × V_{DD}	V	2.4 V ≤ V_{DD} ≤ 3.6 V
		–	–	0.25 × V_{DD}	V	4.75 V ≤ V_{DD} ≤ 5.25 V
V_{IHI2C}	Input high level	0.7 × V_{DD}	–	–	V	2.4 V ≤ V_{DD} ≤ 5.25 V

Notes

16. The 50,000 cycle flash endurance per block is guaranteed if the flash is operating within one voltage range. Voltage ranges are 2.4 V to 3.0 V, 3.0 V to 3.6 V, and 4.75 V to 5.25 V.
17. A maximum of 36 × 50,000 block endurance cycles is allowed. This may be balanced between operations on 36 × 1 blocks of 50,000 maximum cycles each, 36 × 2 blocks of 25,000 maximum cycles each, or 36 × 4 blocks of 12,500 maximum cycles each (and so forth to limit the total number of cycles to 36 × 50,000 and that no single block ever sees more than 50,000 cycles).For the full industrial range, you must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the application note, Design Aids — Reading and Writing PSoC® Flash – AN2015 for more information on Flash APIs.
18. All GPIO meet the DC GPIO V_{IL} and V_{IH} specifications mentioned in section DC GPIO Specifications on page 18. The I^2C GPIO pins also meet the mentioned specs.

AC Programming Specifications

Table 33 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 33. AC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
t_{RSCLK}	Rise time of SCLK	1	–	20	ns	
t_{FSCLK}	Fall time of SCLK	1	–	20	ns	
t_{SSCLK}	Data set up time to falling edge of SCLK	40	–	–	ns	
t_{HSCLK}	Data hold time from falling edge of SCLK	40	–	–	ns	
F_{SCLK}	Frequency of SCLK	0	–	8	MHz	
t_{ERASEB}	Flash erase time (block)	–	10	–	ms	
t_{WRITE}	Flash block write time	–	80	–	ms	
t_{DSCLK3}	Data out delay from falling edge of SCLK	–	–	50	ns	3.0 ≤ V_{DD} ≤ 3.6.
t_{DSCLK2}	Data out delay from falling edge of SCLK	–	–	70	ns	2.4 ≤ V_{DD} ≤ 3.0.
$t_{ERASEALL}$	Flash erase time (bulk)	–	20	–	ms	Erase all blocks and protection fields at once.
$t_{PROGRAM\_HOT}$	Flash block erase + flash block write time	–	–	180[30]	ms	0 °C ≤ Tj ≤ 100 °C.
$t_{PROGRAM\_COLD}$	Flash block erase + flash block write time	–	–	360[30]	ms	–40 °C ≤ Tj ≤ 0 °C.

AC I^2C Specifications

Table 34 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 34. AC Characteristics of the I^2C SDA and SCL Pins for V_{CC} ≥ 3.0 V

Symbol	Description	Standard Mode		Fast Mode		Units
		Min	Max	Min	Max	
F_{SCLI2C}	SCL clock frequency	0	100	0	400	kHz
$t_{HDSTAI2C}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	4.0	–	0.6	–	µs
t_{LOWI2C}	Low period of the SCL clock	4.7	–	1.3	–	µs
$t_{HIGHI2C}$	High period of the SCL clock	4.0	–	0.6	–	µs
$t_{SUSTAI2C}$	Setup time for a repeated START condition	4.7	–	0.6	–	µs
$t_{HDDATI2C}$	Data hold time	0	–	0	–	µs
$t_{SUDATI2C}$	Data setup time	250	–	100[29]	–	ns
$t_{SUSTOI2C}$	Setup time for STOP condition	4.0	–	0.6	–	µs
t_{BUFI2C}	Bus free time between a STOP and START condition	4.7	–	1.3	–	µs
t_{SPI2C}	Pulse width of spikes are suppressed by the input filter	–	–	0	50	ns

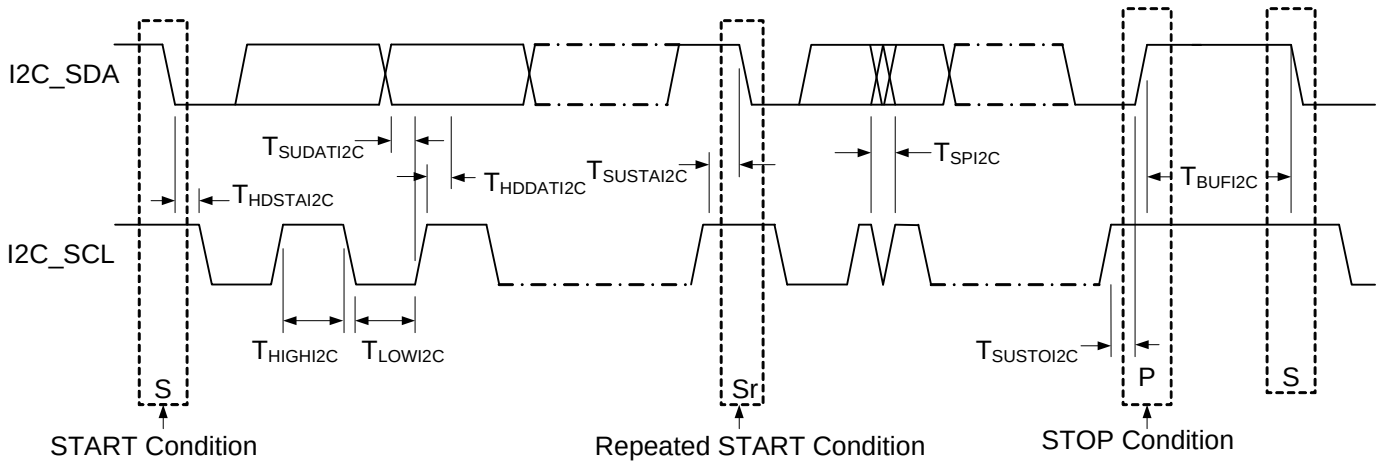
Notes

29. A fast-mode I^2C-bus device can be used in a standard-mode I^2C-bus system, but the requirement t_{SUDAT} ≥ 250 ns must then be met. This automatically becomes the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t_{rmax} + t_{SUDAT} = 1000 + 250 = 1250 ns (according to the standard-mode I^2C-bus specification) before the SCL line is released.
30. For the full industrial range, you must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the application note, Design Aids — Reading and Writing PSoC® Flash – AN2015 for more information on Flash APIs.

Table 35. 2.7-V AC Characteristics of the I²C SDA and SCL Pins (Fast Mode Not Supported)

Symbol	Description	Standard Mode		Fast Mode		Units
		Min	Max	Min	Max	
F_{SCLI2C}	SCL clock frequency	0	100	–	–	kHz
$t_{HDSTAI2C}$	Hold time (repeated) START Condition. After this period, the first clock pulse is generated.	4.0	–	–	–	µs
t_{LOWI2C}	Low period of the SCL clock	4.7	–	–	–	µs
$t_{HIGHI2C}$	High period of the SCL clock	4.0	–	–	–	µs
$t_{SUSTAI2C}$	Setup time for a repeated START condition	4.7	–	–	–	µs
$t_{HDDATI2C}$	Data hold time	0	–	–	–	µs
$t_{SUDATI2C}$	Data setup time	250	–	–	–	ns
$t_{SUSTOI2C}$	Setup time for STOP condition	4.0	–	–	–	µs
t_{BUFI2C}	Bus free time between a STOP and START condition	4.7	–	–	–	µs
t_{SPI2C}	Pulse width of spikes are suppressed by the input filter.	–	–	–	–	ns

Figure 14. Definition for Timing for Fast/Standard Mode on the I²C Bus



Document Conventions

Units of Measure

Table 40 lists the units of measures.

Table 40. Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure
dB	decibels	mH	millihenry
°C	degree Celsius	µH	microhenry
µF	microfarad	µs	microsecond
pF	picofarad	ms	millisecond
kHz	kilohertz	ns	nanosecond
MHz	megahertz	ps	picosecond
rt-Hz	root hertz	µV	microvolt
kΩ	kilohm	mV	millivolt
Ω	ohm	mVpp	millivolts peak-to-peak
µA	microampere	V	volt
mA	milliampere	W	watt
nA	nanoampere	mm	millimeter
pA	pikoampere	%	percent

Numeric Conventions

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase ‘h’ (for example, ‘14h’ or ‘3Ah’). Hexadecimal numbers may also be represented by a ‘0x’ prefix, the C coding convention. Binary numbers have an appended lowercase ‘b’ (for example, 01010100b’ or ‘01000011b’). Numbers not indicated by an ‘h’ or ‘b’ are decimals.

Glossary

active high	1. A logic signal having its asserted state as the logic 1 state. 2. A logic signal having the logic 1 state as the higher voltage of the two states.
analog blocks	The basic programmable opamp circuits. These are SC (switched capacitor) and CT (continuous time) blocks. These blocks can be interconnected to provide ADCs, DACs, multi-pole filters, gain stages, and much more.
analog-to-digital (ADC)	A device that changes an analog signal to a digital signal of corresponding magnitude. Typically, an ADC converts a voltage to a digital number. The digital-to-analog (DAC) converter performs the reverse operation.
Application programming interface (API)	A series of software routines that comprise an interface between a computer application and lower level services and functions (for example, user modules and libraries). APIs serve as building blocks for programmers that create software applications.
asynchronous	A signal whose data is acknowledged or acted upon immediately, irrespective of any clock signal.
bandgap reference	A stable voltage reference design that matches the positive temperature coefficient of VT with the negative temperature coefficient of VBE, to produce a zero temperature coefficient (ideally) reference.
bandwidth	1. The frequency range of a message or information processing system measured in hertz. 2. The width of the spectral region over which an amplifier (or absorber) has substantial gain (or loss); it is sometimes represented more specifically as, for example, full width at half maximum.

Glossary (continued)

bias	1. A systematic deviation of a value from a reference value. 2. The amount by which the average of a set of values departs from a reference value. 3. The electrical, mechanical, magnetic, or other force (field) applied to a device to establish a reference level to operate the device.
block	1. A functional unit that performs a single function, such as an oscillator. 2. A functional unit that may be configured to perform one of several functions, such as a digital PSoC block or an analog PSoC block.
buffer	1. A storage area for data that is used to compensate for a speed difference, when transferring data from one device to another. Usually refers to an area reserved for IO operations, into which data is read, or from which data is written. 2. A portion of memory set aside to store data, often before it is sent to an external device or as it is received from an external device. 3. An amplifier used to lower the output impedance of a system.
bus	1. A named connection of nets. Bundling nets together in a bus makes it easier to route nets with similar routing patterns. 2. A set of signals performing a common function and carrying similar data. Typically represented using vector notation; for example, address[7:0]. 3. One or more conductors that serve as a common connection for a group of related devices.
clock	The device that generates a periodic signal with a fixed frequency and duty cycle. A clock is sometimes used to synchronize different logic blocks.
comparator	An electronic circuit that produces an output voltage or current whenever two input levels simultaneously satisfy predetermined amplitude requirements.
compiler	A program that translates a high level language, such as C, into machine language.
configuration space	In PSoC devices, the register space accessed when the XIO bit, in the CPU_F register, is set to ‘1’.
crystal oscillator	An oscillator in which the frequency is controlled by a piezoelectric crystal. Typically a piezoelectric crystal is less sensitive to ambient temperature than other circuit components.
cyclic redundancy check (CRC)	A calculation used to detect errors in data communications, typically performed using a linear feedback shift register. Similar calculations may be used for a variety of other purposes such as data compression.
data bus	A bi-directional set of signals used by a computer to convey information from a memory location to the central processing unit and vice versa. More generally, a set of signals used to convey data between digital functions.
debugger	A hardware and software system that allows you to analyze the operation of the system under development. A debugger usually allows the developer to step through the firmware one step at a time, set break points, and analyze memory.
dead band	A period of time when neither of two or more signals are in their active state or in transition.
digital blocks	The 8-bit logic blocks that can act as a counter, timer, serial receiver, serial transmitter, CRC generator, pseudo-random number generator, or SPI.
digital-to-analog (DAC)	A device that changes a digital signal to an analog signal of corresponding magnitude. The analog-to-digital (ADC) converter performs the reverse operation.

Glossary (continued)

duty cycle	The relationship of a clock period high time to its low time, expressed as a percent.
emulator	Duplicates (provides an emulation of) the functions of one system with a different system, so that the second system appears to behave like the first system.
External Reset (XRES)	An active high signal that is driven into the PSoC device. It causes all operation of the CPU and blocks to stop and return to a pre-defined state.
Flash	An electrically programmable and erasable, non-volatile technology that provides you the programmability and data storage of EPROMs, plus in-system erasability. Non-volatile means that the data is retained when power is OFF.
Flash block	The smallest amount of Flash ROM space that may be programmed at one time and the smallest amount of Flash space that may be protected. A Flash block holds 64 bytes.
frequency	The number of cycles or events per unit of time, for a periodic function.
gain	The ratio of output current, voltage, or power to input current, voltage, or power, respectively. Gain is usually expressed in dB.
I^2C	A two-wire serial computer bus by Philips Semiconductors (now NXP Semiconductors). I2C is an Inter-Integrated Circuit. It is used to connect low-speed peripherals in an embedded system. The original system was created in the early 1980s as a battery control interface, but it was later used as a simple internal bus system for building control electronics. I2C uses only two bi-directional pins, clock and data, both running at +5 V and pulled high with resistors. The bus operates at 100 kbits/second in standard mode and 400 kbits/second in fast mode.
ICE	The in-circuit emulator that allows you to test the project in a hardware environment, while viewing the debugging device activity in a software environment (PSoC Designer).
input/output (I/O)	A device that introduces data into or extracts data from a system.
interrupt	A suspension of a process, such as the execution of a computer program, caused by an event external to that process, and performed in such a way that the process can be resumed.
interrupt service routine (ISR)	A block of code that normal code execution is diverted to when the M8C receives a hardware interrupt. Many interrupt sources may each exist with its own priority and individual ISR code block. Each ISR code block ends with the RETI instruction, returning the device to the point in the program where it left normal program execution.
jitter	1. A misplacement of the timing of a transition from its ideal position. A typical form of corruption that occurs on serial data streams. 2. The abrupt and unwanted variations of one or more signal characteristics, such as the interval between successive pulses, the amplitude of successive cycles, or the frequency or phase of successive cycles.
low-voltage detect (LVD)	A circuit that senses V_{DD} and provides an interrupt to the system when V_{DD} falls lower than a selected threshold.
M8C	An 8-bit Harvard-architecture microprocessor. The microprocessor coordinates all activity inside a PSoC by interfacing to the Flash, SRAM, and register space.
master device	A device that controls the timing for data exchanges between two devices. Or when devices are cascaded in width, the master device is the one that controls the timing for data exchanges between the cascaded devices and an external interface. The controlled device is called the ***slave device.***

Errata

This section describes the errata for the CY8C21x23 PSoC® programmable system-on-chip family. Details include errata trigger conditions, scope of impact, available workarounds, and silicon revision applicability.

Contact your local Cypress Sales Representative if you have questions.

Part Numbers Affected

Part Number	Ordering Information
CY8C21123	CY8C21123-24SXI
	CY8C21123-24SXIT
	CY8C21223-24SXI
	CY8C21223-24SXIT
	CY8C21323-24PVXI
	CY8C21323-24PVXIT
	CY8C21323-24LFXI
	CY8C21323-24LFXIT
	CY8C21323-24LQXI
	CY8C21323-24LQXIT

CY8C21123 Qualification Status

Product Status: Production

CY8C21123 Errata Summary

The following table defines the errata applicability to available CY8C21123 family devices. An "X" indicates that the errata pertains to the selected device.

Note Errata items, in the table below, are hyperlinked. Click on any item entry to jump to its description.

Items	Part Number	Silicon Revision	Fix Status
[1.] Internal Main Oscillator (IMO) Tolerance Deviation at Temperature Extremes	CY8C21123	A	No silicon fix is planned. Workaround is required.

1. Internal Main Oscillator (IMO) Tolerance Deviation at Temperature Extremes

- **Problem Definition**
  Asynchronous Digital Communications Interfaces may fail framing beyond 0 to 70 °C. This problem does not affect end-product usage between 0 and 70 °C.
- **Parameters Affected**
  The IMO frequency tolerance. The worst case deviation when operated below 0 °C and above +70 °C and within the upper and lower datasheet temperature range is ±5%.
- **Trigger Condition(S)**
  The asynchronous Rx/Tx clock source IMO frequency tolerance may deviate beyond the data sheet limit of ±2.5% when operated beyond the temperature range of 0 to +70 °C.
- **Scope of Impact**
  This problem may affect UART, IrDA, and FSK implementations.
- **Workaround**
  Implement a quartz crystal stabilized clock source on at least one end of the asynchronous digital communications interface.
- **Fix Status**
  No silicon fix is planned. The workaround mentioned above should be used.

Document History Page

Document Title: CY8C21123/CY8C21223/CY8C21323, PSoC® Programmable System-on-Chip™ Document Number: 38-12022				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	133248	NWJ	See ECN	New silicon and document (Revision **).
*A	208900	NWJ	See ECN	Add new part, new package and update all ordering codes to Pb-free.
*B	212081	NWJ	See ECN	Expand and prepare Preliminary version.
*C	227321	CMS Team	See ECN	Update specs., data, format.
*D	235973	SFV	See ECN	Updated Overview and Electrical Spec. chapters, along with 24-pin pinout. Added CMP_GO_EN register (1,64h) to mapping table.
*E	290991	HMT	See ECN	Update datasheet standards per SFV memo. Fix device table. Add part numbers to pinouts and fine tune. Change 20-pin SSOP to CY8C21323. Add Reflow Temp. table. Update diagrams and specs.
*F	301636	HMT	See ECN	DC Chip-Level Specification changes. Update links to new CY.com Portal.
*G	324073	HMT	See ECN	Obtained clearer 16 SOIC package. Update Thermal Impedances and Solder Reflow tables. Re-add pinout ISSP notation. Fix ADC type-o. Fix TMP register names. Update Electrical Specifications. Add CY logo. Update CY copyright. Make datasheet Final.
*H	2588457	KET / HMI / AESA	10/22/2008	New package information on page 9. Converted datasheet to new template. Added 16-Pin OFN package diagram.
*I	2618175	OGNE / PYRS	12/09/2008	Added Note in Ordering Information Section. Changed title from PSoC Mixed-Signal Array to PSoC Programmable System-on-Chip. Updated ‘Development Tools’ and ‘Designing with PSoC Designer’ sections on pages 5 and 6
*J	2682782	MAXK / AESA	04/03/2009	Corrected 16 COL pinout.
*K	2699713	MAXK	04/29/2009	Minor ECN to correct paragraph style of 16 COL Pinout. No change in content.
*L	2762497	JVY	09/11/2009	Updated DC GPIO, AC Chip-Level, and AC Programming Specifications as follows: Modified F_{IMO6} and T_{WRITE} specifications. Replaced T_{RAMP} time) specification with SR_{POWER_UP} (slew rate) specification. Added note [11] to Flash Endurance specification. Added I_{OH}, I_{OL}, DC_{ILO}, F_{32K_U}, $T_{POWERUP}$, $T_{ERASEALL}$, $T_{PROGRAM\_HOT}$, and $T_{PROGRAM\_COLD}$ specifications..
*M	2792630	TTO	10/26/2009	Updated ordering information for CY8C21223-24LGXI to indicate availability of XRES pin.
*N	2901653	NJF	03/30/2010	Changed 16-pin COL to 16-pin QFN in the datasheet. Added Contents. Updated links in Sales, Solutions, and Legal Information Updated Cypress website links. Added $T_{BAKETEMP}$ and $T_{BAKETIME}$ parameters in Absolute Maximum Ratings Updated 5-V and 3.3-V AC Chip-Level Specifications Updated Notes in Packaging Information and package diagrams. Updated Ordering Code Definitions
*O	2928895	YJI	05/06/2010	No technical updates. Included with EROS spec.

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