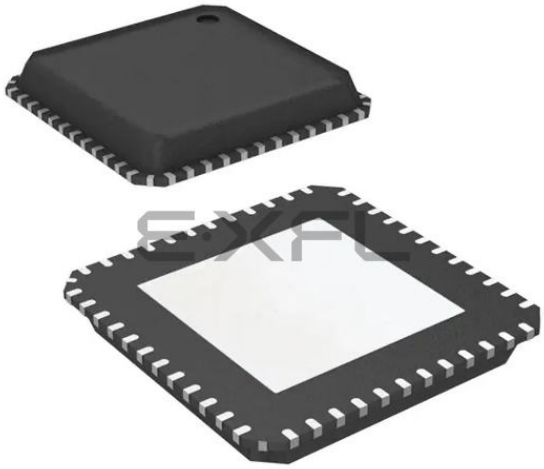

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Product Status	Not For New Designs
Applications	Automotive
Core Processor	ARM® Cortex®-M3
Program Memory Type	FLASH (36kB)
Controller Series	-
RAM Size	3K x 8
Interface	SSI, UART
Number of I/O	10
Voltage - Supply	5.5V ~ 28V
Operating Temperature	-40°C ~ 150°C
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	PG-VQFN-48-29
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/tle9861qxa20xuma1

2 Block Diagram

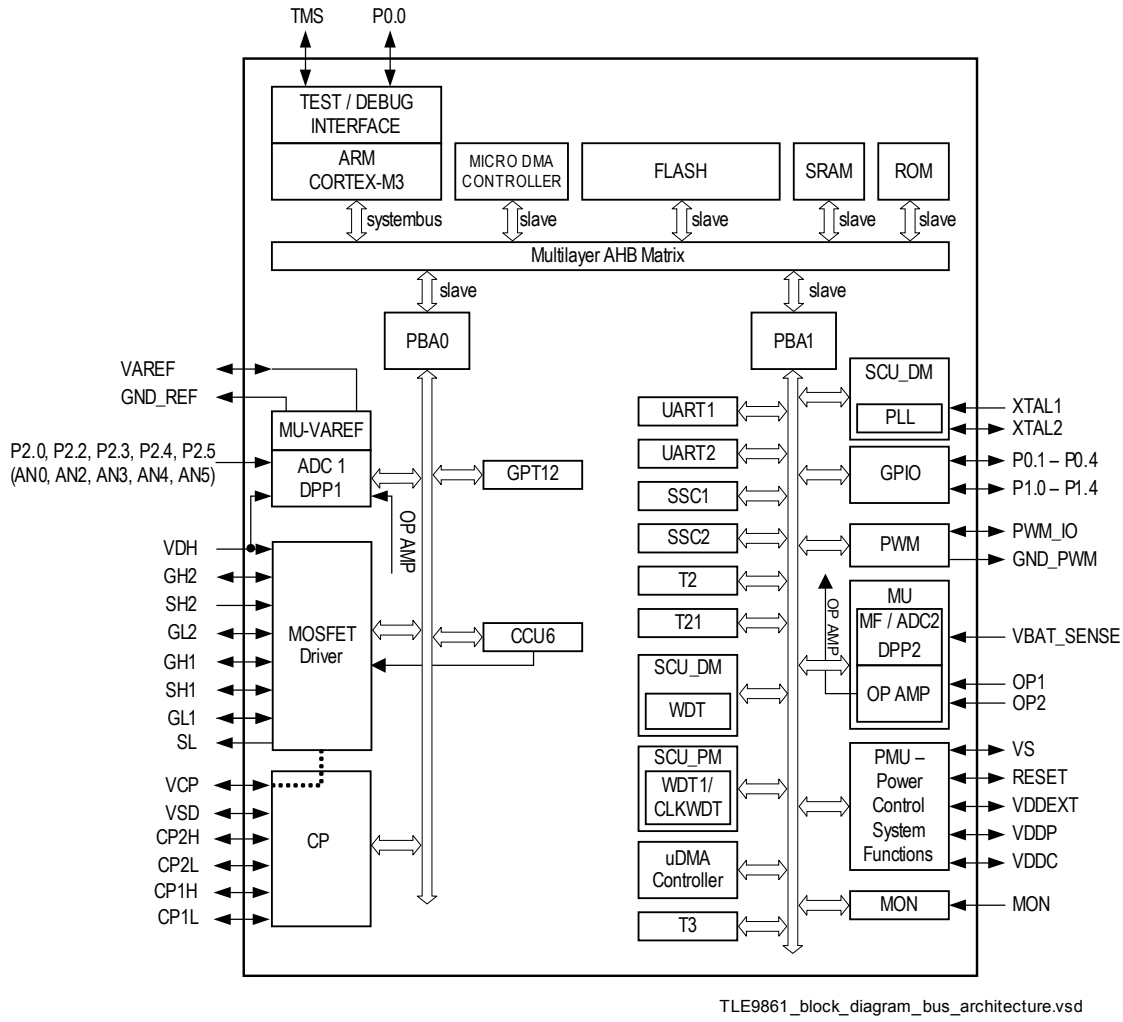

Figure 1 Block Diagram

5.2.1 Block Diagram

The following figure shows the structure of the Power Management Unit. **Table 4** describes the submodules in more detail.

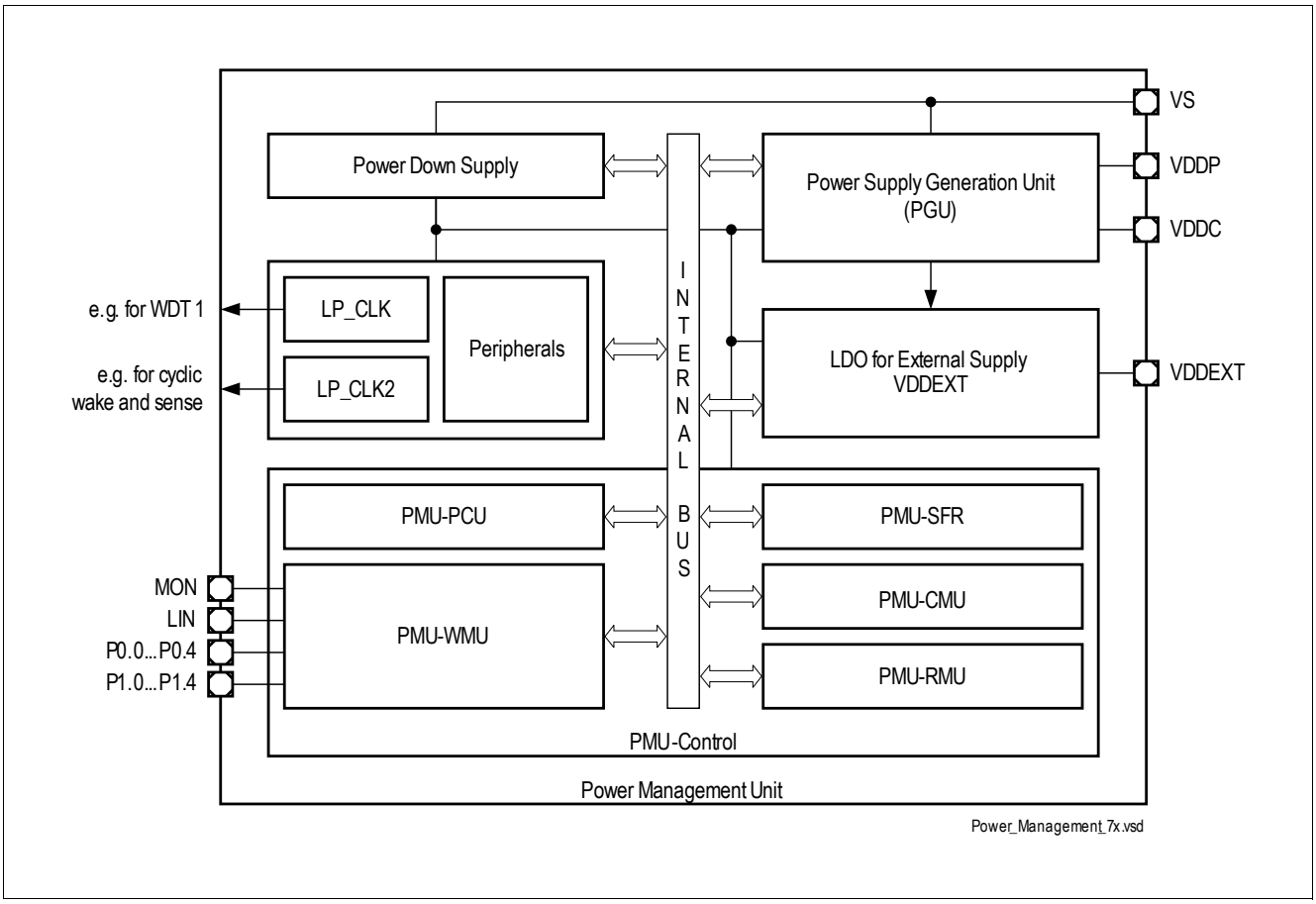

Figure 3 Power Management Unit Block Diagram

Table 4 Description of PMU Submodules

Mod. Name	Modules	Functions
Power Down Supply	Independent supply voltage generation for PMU	This supply is dedicated to the PMU to ensure an independent operation from generated power supplies (VDDP, VDDC).
LP_CLK (= 18 MHz)	- Clock source for all PMU submodules - Backup clock source for System - Clock source for WDT1	This ultra low power oscillator generates the clock for the PMU. This clock is also used as backup clock for the system in case of PLL Clock failure and as an independent clock source for WDT1.
LP_CLK2 (= 100 kHz)	Clock source for PMU	This ultra low power oscillator generates the clock for the PMU in Stop Mode and in the cyclic modes.
Peripherals	Peripheral blocks of PMU	These blocks include the analog peripherals to ensure a stable and fail-safe PMU startup and operation (bandgap, bias).

5.2.2 PMU Modes Overview

The following state diagram shows the available modes of the device.

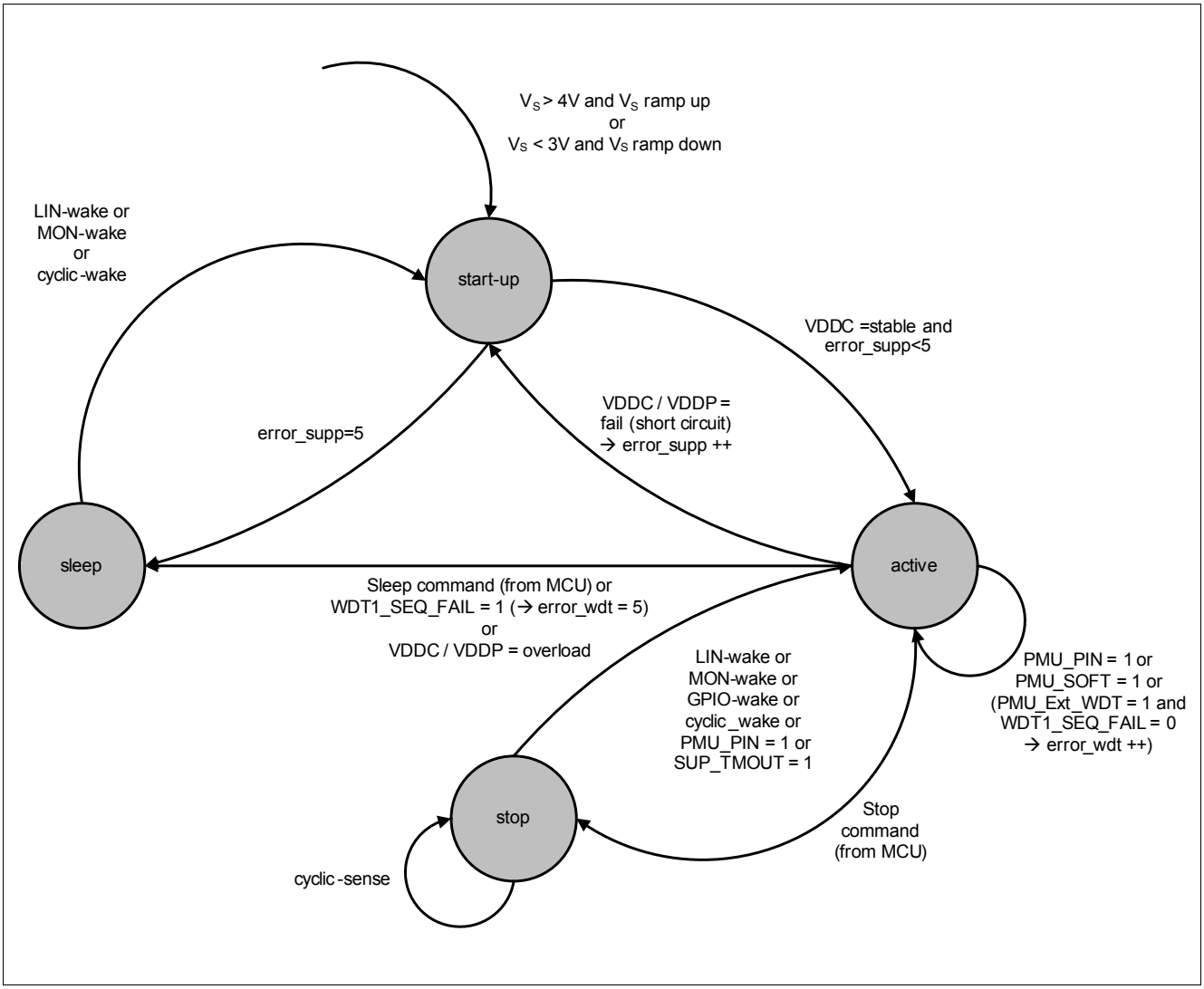

Figure 4 Power Management Unit System Modes

5.3 Power Supply Generation Unit (PGU)

5.3.1 Voltage Regulator 5.0V (VDDP)

This module represents the 5 V voltage regulator, which provides the pad supply for the parallel port pins and other 5 V analog functions (e.g. PWM Interface).

Features

- 5 V low-drop voltage regulator
- Overcurrent monitoring and shutdown with MCU signaling (interrupt)
- Overvoltage monitoring with MCU signaling (interrupt)
- Undervoltage monitoring with MCU signaling (interrupt)
- Undervoltage monitoring with reset (Undervoltage Reset, V_{DDPUV})
- Pre-Regulator for VDDC Regulator
- GPIO Supply
- Pull Down Current Source at the output for Sleep Mode only (typ. 5 mA)

The output capacitor C_{VDDP} is mandatory to ensure proper regulator functionality.

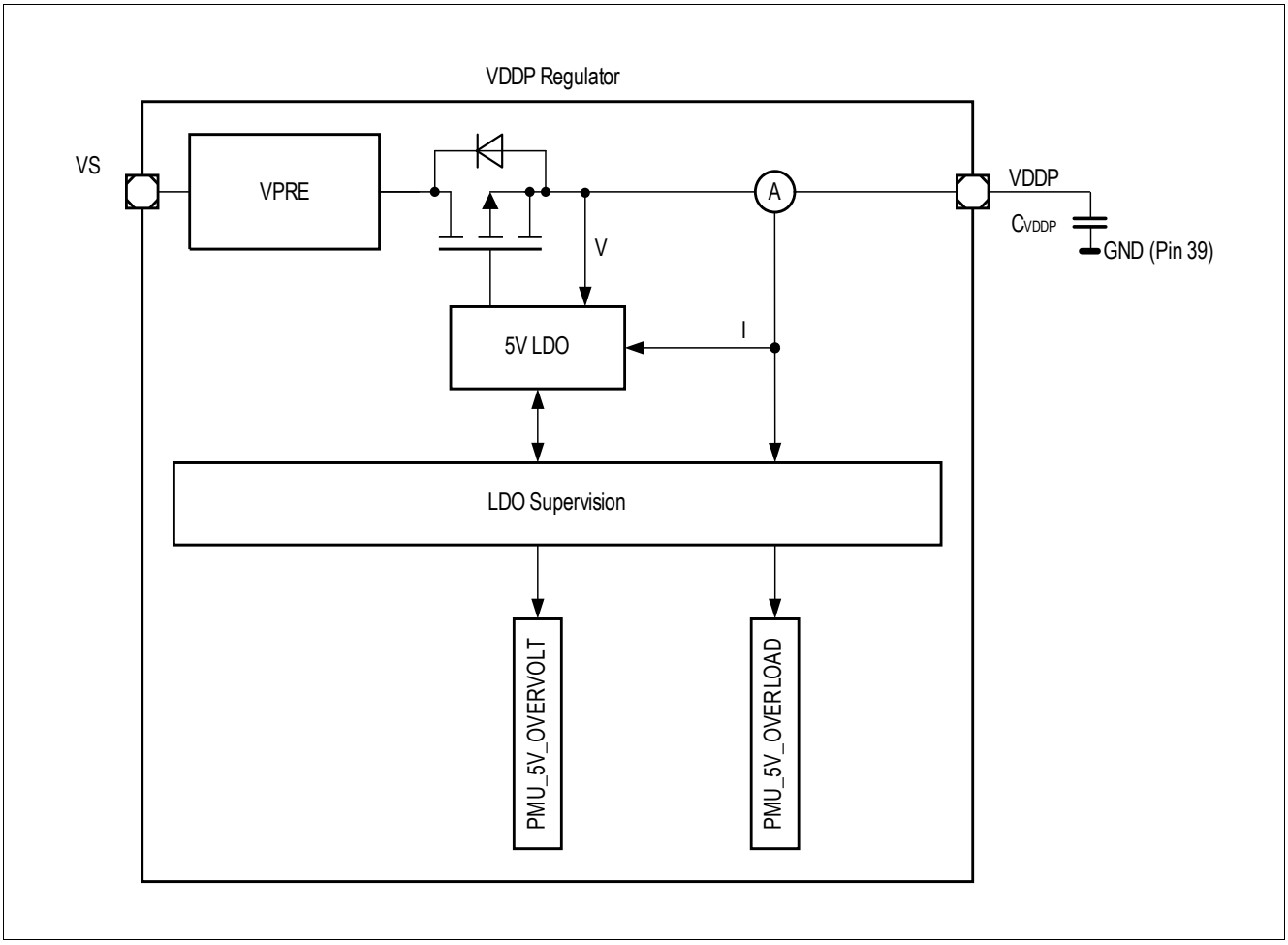

Figure 5 Module Block Diagram of VDDP Voltage Regulator

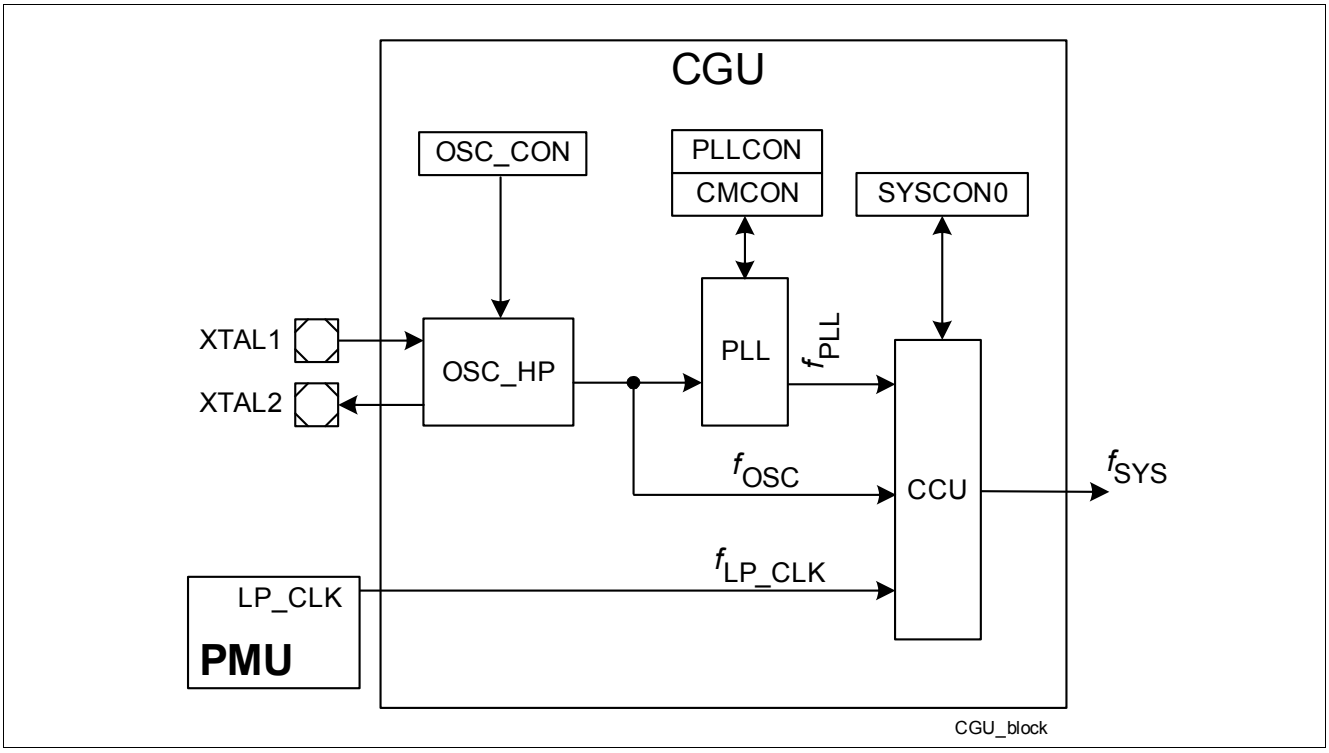

Figure 9 Clock Generation Unit Block Diagram

The following sections describe the different parts of the CGU.

6.3.1 Low Precision Clock

The clock source LP_CLK is a low-precision RC oscillator (LP-OSC) with a nominal frequency of 18 MHz that is enabled by hardware as an independent clock source for the TLE9861QXA20 startup after reset and during the power-down wake-up sequence. f_{LP_CLK} is not user configurable.

6.3.2 High Precision Oscillator Circuit (OSC_HP)

The high precision oscillator circuit, designed to work with both an external crystal oscillator or an external stable clock source, consists of an inverting amplifier with XTAL1 as the input, and XTAL2 as the output.

Figure 10 shows the recommended external circuitry for both operating modes, External Crystal Mode and External Input Clock Mode.

6.3.2.1 External Input Clock Mode

When supplying the clock signal directly, not using an external crystal and bypassing the oscillator, the input frequency needs to be equal or greater than 4 MHz if the PLL VCO part is used.

When using an external clock signal it must be connected to XTAL1. XTAL2 is left open (unconnected).

6.3.2.2 External Crystal Mode

When using an external crystal, its frequency can be within the range of 4 MHz to 25 MHz. An external oscillator load circuitry must be used, connected to both pins, XTAL1 and XTAL2. It normally consists of the two load capacitances C1 and C2. A series damping resistor could be required for some crystals. The exact values and the corresponding operating ranges depend on the crystal and have to be determined and optimized in cooperation with the crystal vendor using the negative resistance method. The following load cap values can be used as starting point for the evaluation:

8 ARM Cortex-M3 Core

8.1 Features

The key features of the Cortex-M3 implemented are listed below.

Processor Core; a low gate count core, with low latency interrupt processing:

- A subset of the Thumb®-2 Instruction Set
- Banked stack pointer (SP) only
- 32-bit hardware divide instructions, SDIV and UDIV (Thumb-2 instructions)
- Handler and Thread Modes
- Thumb and debug states
- Interruptible-continued instructions LDM/STM, Push/Pop for low interrupt latency
- Automatic processor state saving and restoration for low latency Interrupt Service Routine (ISR) entry and exit
- ARM architecture v7-M Style BE8/LE support
- ARMv6 unaligned accesses

Nested Vectored Interrupt Controller (NVIC) closely integrated with the processor core to achieve low latency interrupt processing:

- Interrupts, configurable from 1 to 16
- Bits of priority (4)
- Dynamic reprioritization of interrupts
- Priority grouping. This enables selection of preemptive interrupt levels and non-preemptive interrupt levels
- Support for tail-chaining and late arrival of interrupts. This enables back-to-back interrupt processing without the overhead of state saving and restoration between interrupts.
- Processor state automatically saved on interrupt entry, and restored on interrupt exit, with no instruction overhead

Bus interfaces

- Advanced High-performance Bus-Lite (AHB-Lite) interfaces: ICode, DCode, and System bus interface
- Memory access alignment
- Write buffer for buffering of write data

11.3 NVM Module (Flash Memory)

The Flash Memory provides an embedded user-programmable non-volatile memory, allowing fast and reliable storage of user code and data.

Features

- In-system programming via PWM Interface (Flash Mode) and SWD
- Error Correction Code (ECC) for detection of single-bit and double-bit errors and dynamic correction of single Bit errors.
- Interrupts and signals double-bit error by NMI
- Program width of 128 byte (page)
- Minimum erase width of 128 bytes (page)
- Integrated hardware support for EEPROM emulation
- 8 byte read access
- Physical read access time: 75 ns
- Code read access acceleration integrated; read buffer and automatic pre-fetch
- Page program time: 3 ms
- Page erase (128 bytes) and sector erase (4K bytes) time: 4ms

Note: The user has to ensure that no flash operations which change the content of the flash get interrupted at any time.

The clock for the NVM is supplied with the system frequency fsys. Integrated firmware routines are provided to erase NVM, and other operations including EEPROM emulation are provided as well.

14.3.2 Port 1

14.3.2.1 Port 1 Functions

Table 9 Port 1 Input / Output Functions

Port Pin	Input/Output	Select	Connected Signal(s)	From/to Module
P1.0	Input	GPI	P1_DATA.P0	
		INP1	T3INC	GPT12T3
		INP2	T4EUDB	GPT12T4
		INP3	CC61_0	CCU6
		INP4	SCK_2	SSC2
		INP5	EXINT1_2	SCU
	Output	GPO	P1_DATA.P0	
		ALT1	SCK_2	SSC2
		ALT2	CC61_0	CCU6
		ALT3	EXF21_3	Timer 21
P1.1	Input	GPI	P1_DATA.P1	
		INP1	–	–
		INP2	T6EUDA	GPT12T6
		INP3	–	-
		INP4	MTSR_2	SSC2
		INP5	T21_1	Timer 21
		INP6	EXINT1_0	SCU
	Output	GPO	P1_DATA.P1	–
		ALT1	MTSR_2	SSC2
		ALT2	COUT61_0	CCU6
		ALT3	TXD2_0	UART2
P1.2	Input	GPI	P1_DATA.P2	
		INP1	T2INA	GPT12T2
		INP2	T2EX_1	Timer 2
		INP3	T21EX_3	Timer 21
		INP4	MRST_2_0	SSC2
		INP5	RXD2_0	UART2
		INP6	CCPOS2_2	CCU6
		INP7	EXINT0_1	SCU
	Output	GPO	P1_DATA.P2	
		ALT1	MRST_2_0	SSC2
		ALT2	COUT63_0	CCU6
		ALT3	T3OUT	GPT12T3

15.2.1 Block Diagram GPT1

Block GPT1 contains three timers/counters: The core timer T3 and the two auxiliary timers T2 and T4. The maximum resolution is $f_{GPT}/4$. The auxiliary timers of GPT1 may optionally be configured as reload or capture registers for the core timer.

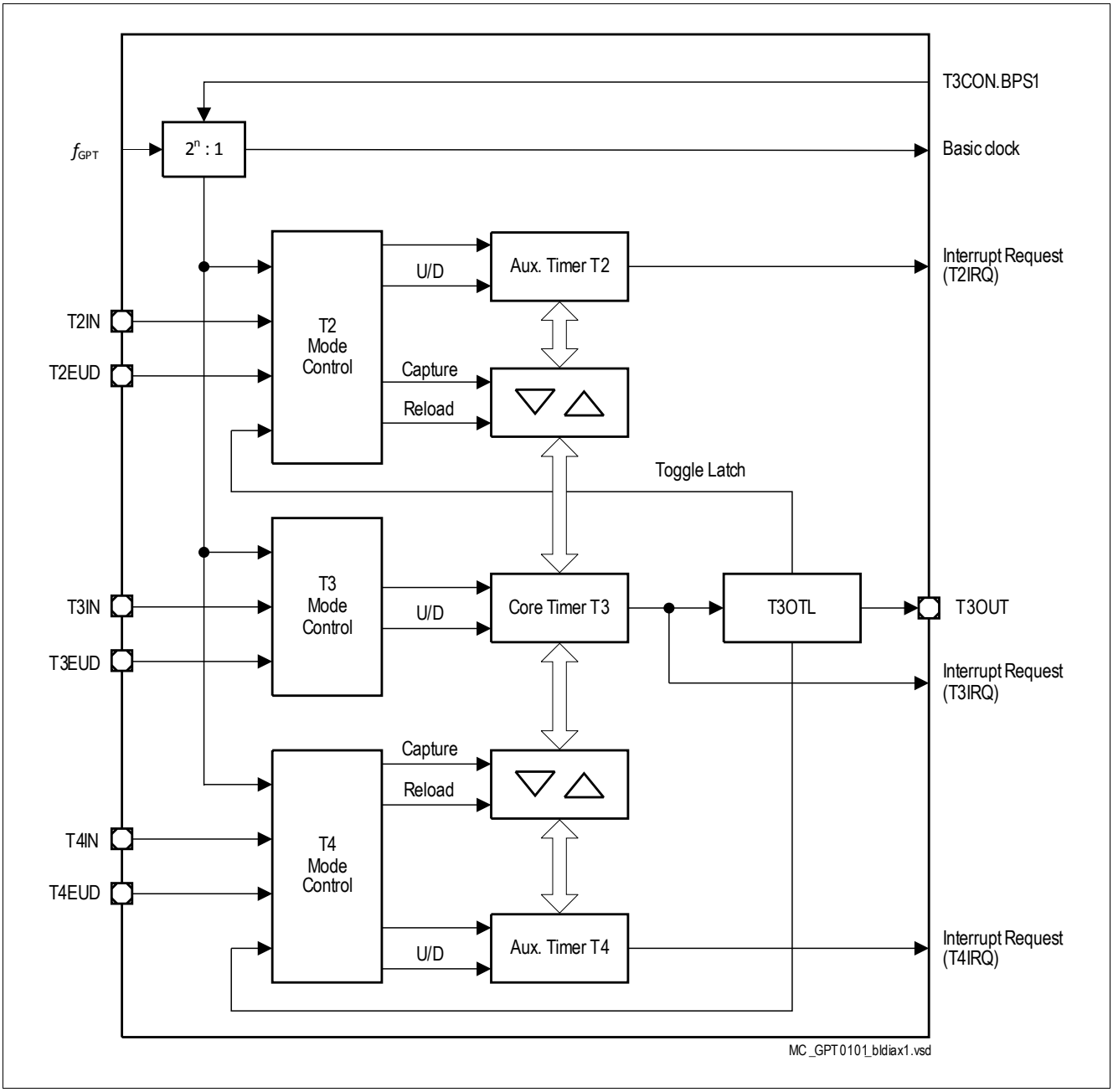

Figure 19 GPT1 Block Diagram (n = 2 … 5)

26.2.1 Block Diagram

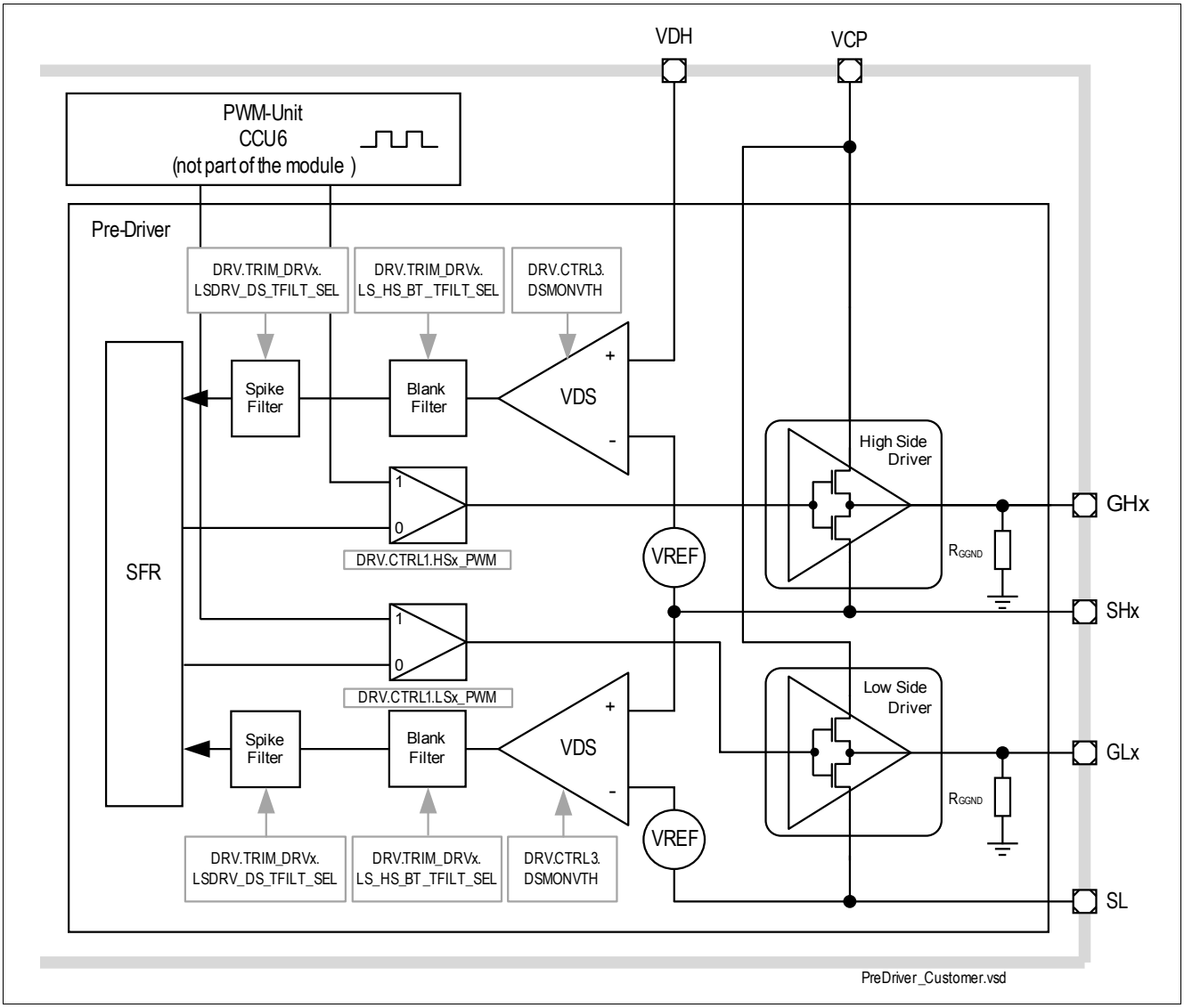

Figure 29 Driver Module Block Diagram (incl. system connections)

26.2.2 General

The Driver can be controlled in two different ways:

- In Normal Mode the output stage is fully controllable through the SFR registers CTRLx (x = 1,2,3). Protection functions such as overcurrent and open-load detection are available.
- The PWM Mode can also be enabled by the corresponding bit in CTRL1 and CTRL2. The PWM must be configured in the System PWM Module (CCU6). All protection functions are available in PWM mode as well.

Protection Functions

- Overcurrent detection and shutdown feature for external MOSFET by Drain Source measurement
- Programmable minimum cross current protection time
- Open-load detection feature in Off-state for external MOSFET.

Table 17 Absolute Maximum Ratings[1)] (cont'd)

T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Voltage range at charge pump pins CP1H, CP1L, CP2H, CP2L, VCP	V_{CPx}	-0.3	–	48	V	[8)]	P_1.1.15
Voltages – GPIOs							
Voltage on any port pin[9)]	V_{in}	-0.3	–	V_{DDP} +0.3	V	$V_{IN} < V_{DDPmax}$ [10)]	P_1.1.16
Current at VCP Pin							
Max. current at VCP pin	I_{VCP}	-15	–	–	mA	–	P_1.1.35
Injection Current at GPIOs							
Injection current on any port pin	I_{GPIONM}	-5	–	5	mA	[11)]	P_1.1.34
Sum of all injected currents in Normal Mode	I_{GPIOAM_sum}	-50	–	50	mA	[11)]	P_1.1.30
Sum of all injected currents in Power Down Mode (Stop Mode)	I_{GPIOPD_sum}	-5000	–	50	µA	[11)]	P_1.1.36
Sum of all injected currents in Sleep Mode	$I_{GPIOSleep\_sum}$	-5	–	5	mA	[11)]	P_1.1.37
Other Voltages							
Input voltage VAREF	V_{AREF}	-0.3	–	V_{DDP} +0.3	V	–	P_1.1.17
Input voltage OP1, OP2	V_{OAI}	-7	–	7	V	–	P_1.1.23
Temperatures							
Junction temperature	T_j	-40	–	150	°C	–	P_1.1.18
Storage temperature	T_{stg}	-55	–	150	°C	–	P_1.1.19
ESD Susceptibility							
ESD susceptibility all pins	V_{ESD1}	-2	–	2	kV	HBM [12)]	P_1.1.20
ESD susceptibility pins MON, VS, VSD, VBAT_SENSE vs.GND	V_{ESD2}	-4	–	4	kV	HBM [13)]	P_1.1.21
ESD susceptibility pins PWM_IO vs. GND_PWM	V_{ESD3}	-6	–	6	kV	HBM [12)]	P_1.1.22
ESD susceptibility **CDM** all pins vs. GND	V_{ESD_CDM1}	-500	–	500	V	[14)]	P_1.1.28
ESD susceptibility **CDM** pins 1, 12, 13, 24, 25, 36, 37, 48 (corner pins) vs. GND	V_{ESD_CDM2}	-750	–	750	V	[14)]	P_1.1.43

1) Not subject to production test, specified by design.

2) Conditions and min. value is derived from application condition for reverse polarity event.

29.1.3 Current Consumption

Table 19 Electrical Characteristics

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Current Consumption @VS pin							
Current consumption in Active Mode at pin VS	I_{Vs}	–	30	35	mA	f_{sys} = 20 MHz no loads on pins, PWM interface in recessive state[1)]	P_1.3.1
Current consumption in Active Mode at pin VSD	I_{VSD}	–	–	40	mA	20 kHz PWM on Bridge Driver	P_1.3.8
Current consumption in Slow Down Mode	I_{SDM}	–	–	30	mA	f_{sys} = 5 MHz; PWM communication running; charge pump on (reverse polarity FET on), external Low Side FET static on (motor break mode); VDDEXT on; all other module set to power down; V_S = 13.5V	P_1.3.6
Current consumption in Sleep Mode	I_{Sleep}	–	30	35	µA	System in Sleep Mode, microcontroller not powered, Wake capable via PWM interface and MON; MON connected to VS or GND; GPIOs open (no loads) or connected to GND: T_J = -40°C to 85°C; V_S = 5.5 V to 18V;[2)]	P_1.3.3
Current consumption in Sleep Mode extended range	I_{Sleep_extend}	–	90	200	µA	System in Sleep Mode, microcontroller not powered, Wake capable via PWM interface and MON; MON connected to VS or GND; GPIOs open (no loads) or connected to GND: T_J = -40°C to 150°C; V_S = 5.5 V to 18V;[2)]	P_1.3.15
Current consumption in Sleep Mode	I_{Sleep}	–	–	33	µA	System in Sleep Mode, microcontroller not powered, Wake capable via PWM interface and MON; MON connected to VS or GND; GPIOs open (no loads) or connected to GND: T_J = -40°C to 40°C; V_S = 5.5 V to 18V;[2)]	P_1.3.9

29.2.3 VDDEXT Voltage Regulator (5.0V) Parameters

Table 24 Electrical Characteristics

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Specified output current	I_{VDDEXT}	0	–	20	mA	–	P_2.3.1
Specified output current	I_{VDDEXT}	0	–	40	mA	1)	P_2.3.21
Required decoupling capacitance	$C_{VDDEXT1}$	0.1	–	2.2	µF	3) 2)ESR < 1 Ω; the specified capacitor value is a typical value.	P_2.3.22
Required buffer capacitance for stability (load jumps)	$C_{VDDEXT2}$	1	–	2.2	µF	3)2)the specified capacitor value is a typical value.	P_2.3.20
Output voltage including line and load regulation	V_{DDEXT}	4.9	5.0	5.1	V	3) I_{load}<20mA; V_S > 5.5V	P_2.3.3
Output voltage including line and load regulation	V_{DDEXT}	4.8	5.0	5.2	V	I_{load}<40mA; V_S > 5.5V	P_2.3.23
Output drop @ Active Mode	V_S-V_{DDEXT}		50	+300	mV	3) I_{load} < 20mA; 3V < V_S < 5.0V	P_2.3.4
Output drop @ Active Mode	V_S-V_{DDEXT}		–	+400	mV	I_{load} < 40mA; 3V < V_S < 5.0V	P_2.3.14
Load regulation @ Active Mode	$V_{DDEXTLOR}$	-50	–	50	mV	2 ... 40mA; C =200nF	P_2.3.5
Line regulation @ Active Mode	$V_{VDDEXTLIR}$	-50	–	50	mV	V_S = 5.5 ... 28V	P_2.3.6
Power supply ripple rejection @ Active Mode	$P_{SSRVDDEXT}$	50	–	–	dB	3) V_S = 13.5V; f =0 ... 1KHz; Vr=2Vpp	P_2.3.7
Overvoltage detection	$V_{VDDEXTOV}$	5.18	–	5.4	V	V_S > 5.5V	P_2.3.8
Overvoltage detection filter time	$t_{FILT\_VDDEXTOV}$	–	735	–	µs	3)4)	P_2.3.24
Voltage OK detection range	$V_{VDDEXTOK}$	–	3	–	V	3)	P_2.3.25
Voltage stable detection range[5)]	$\Delta V_{VDDEXTSTB}$	- 220	–	+ 220	mV	3)	P_2.3.26
Undervoltage trigger	$V_{VDDEXTUV}$	2.6	2.8	3.0	V	6)	P_2.3.9
Overcurrent diagnostic	$I_{VDDEXTOC}$	50	–	160	mA	–	P_2.3.10
Overcurrent diagnostic filter time	t_{FILT_VDDCOC}	–	27	–	µs	3)4)	P_2.3.27
Overcurrent diagnostic shutdown time	$t_{FILT\_VDDCOC\_SD}$	–	290	–	µs	3)4)	P_2.3.28

1) This use case requires the reduced utilization of VDDP output current by 20 mA, see P_2.1.22.
2) Ceramic capacitor.
3) Not subject to production test, specified by design.
4) This filter time and its variation is derived from the time base t_{LP_CLK} = 1 / f_{LP_CLK}.

29.2.4 VPRE Voltage Regulator (PMU Subblock) Parameters

The PMU VPRE Regulator acts as a supply of VDDP and VDDEXT voltage regulators.

Table 25 Functional Range

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Specified output current	I_{VPRE}	–	–	110	mA	1)	P_2.4.1

1) Not subject to production test, specified by design.

29.2.4.1 Load Sharing Scenarios of VPRE Regulator

The figure below shows the possible load sharing scenarios of VPRE regulator.

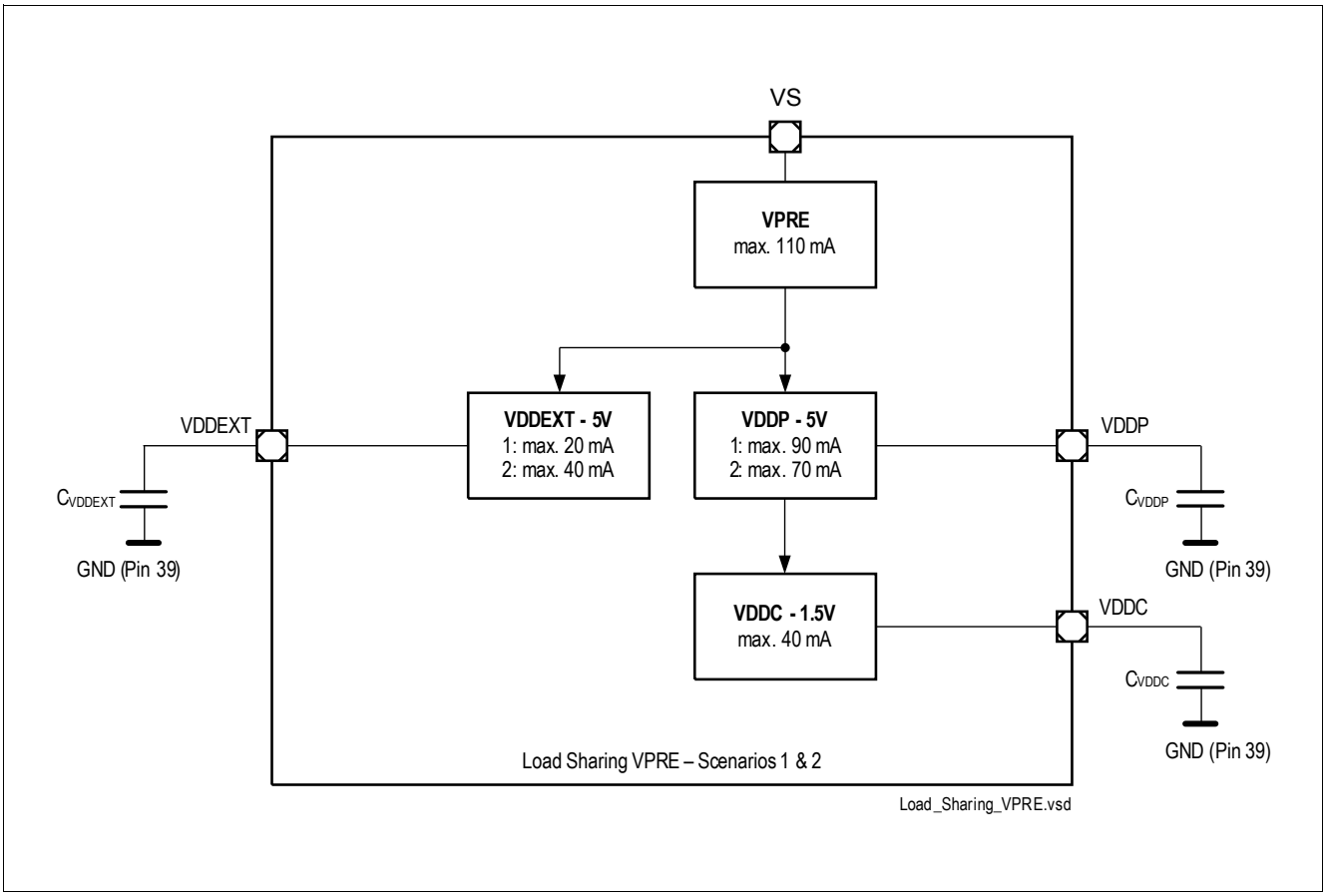

Figure 32 Load Sharing Scenarios of VPRE Regulator

29.2.5 Power Down Voltage Regulator (PMU Subblock) Parameters

The PMU Power Down voltage regulator consists of two subblocks:

- Power Down Pre regulator: VDD5VPD
- Power Down Core regulator: VDD1V5_PD (Supply used for GPUDATAxy registers)

Both regulators are used as purely internal supplies. The following table contains all relevant parameters:

Table 26 Functional Range

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
VDD1V5_PD							
Power-On Reset Threshold	$V_{DD1V5\_PD\_RSTTH}$	1.2	–	1.5	V	1)	P_2.5.1

1) Not subject to production test, specified by design

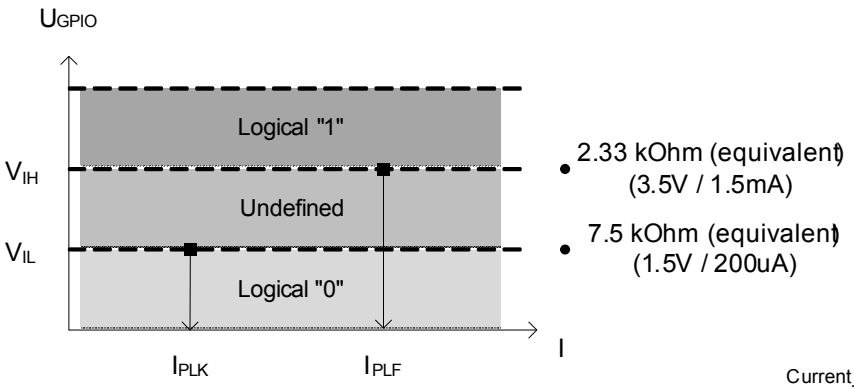

Figure 35 Pull-Down Keep and Force Current

29.5.2 DC Parameters of Port 0, Port 1, TMS and Reset

Note: Operating Conditions apply.
Keeping signal levels within the limits specified in this table ensures operation without overload conditions. For signal levels outside these specifications, also refer to the specification of the maximum allowed ocurrent which can be taken out of VDDP.

Table 30 Current Limits for Port Output Drivers[1)]

Port Output Driver Mode	Maximum Output Current (I_{OLmax} , - I_{OHmax})		Maximum Output Current (I_{OLnom} , - I_{OHnom})		Number
	V_{DDP} ≥ 4.5V	2.6V < V_{DDP} < 4.5V	V_{DDP} ≥ 4.5V	2.6V < V_{DDP} < 4.5V	
Strong driver[2)]	5 mA	3 mA	1.6 mA	1.0 mA	P_5.1.15
Medium driver[3)]	3 mA	1.8 mA	1.0 mA	0.8 mA	P_5.1.1
Weak driver[3)]	0.5 mA	0.3 mA	0.25 mA	0.15 mA	P_5.1.2

1) Not subject to production test, specified by design.
2) Not available for port pins P0.4, P1.0, P1.1 and P1.2
3) All P0.x and P1.x

Table 31 DC Characteristics Port0, Port1

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Input hysteresis	HYS_{P0_P1}	0.11 x V_{DDP}	–	–	V	[1)] Series resistance = 0 Ω; 4.5V ≤ V_{DDP} ≤ 5.5V	P_5.1.5
Input hysteresis	$HYS_{P0\_P1\_exend}$	–	0.09 x V_{DDP}	–	V	[1)] Series resistance = 0 Ω; 2.6V ≤ V_{DDP} ≤ 4.5V	P_5.1.16

29.6 PWM Interface

29.6.1 Electrical Characteristics

Table 33 Electrical Characteristics PWM Interface

V_s = 5.5V to 18V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Bus Receiver Interface							
Receiver threshold voltage, recessive to dominant edge	V_{th_dom}	0.4 × V_S	0.45 × V_S	0.53 x V_S	V	SAE J2602	P_6.1.1
Receiver dominant state	V_{BUSdom}	-27	–	0.4 × V_S	V	–	P_6.1.2
Receiver threshold voltage, dominant to recessive edge	V_{th_rec}	0.47 x V_S	0.55 × V_S	0.6 × V_S	V	SAE J2602	P_6.1.3
Receiver recessive state	V_{BUSrec}	0.6 × V_S	–	1.15 × V_S	V	1)	P_6.1.4
Receiver center voltage	V_{BUS_CNT}	0.475 × V_S	0.5 × V_S	0.525 × V_S	V	2)	P_6.1.5
Receiver hysteresis	V_{HYS}	0.07 V_S	0.12 × V_S	0.175 × V_S	V	3)	P_6.1.6
Wake-up threshold voltage	$V_{BUS,wk}$	0.4 × V_S	0.5 × V_S	0.6 × V_S	V	–	P_6.1.7
Dominant time for bus wake-up (internal analog filter delay)	$t_{WK,bus}$	3	–	15	µs	The overall dominant time for bus wake-up is a sum of $t_{WK,bus}$ + adjustable digital filter time.	P_6.1.8
Bus Transmitter Interface							
Bus recessive output voltage	$V_{BUS,ro}$	0.8 × V_S	–	V_S	V	V_{TxD} = high Level	P_6.1.9
Bus short circuit current	$I_{BUS,sc}$	40	100	150	mA	Current Limitation for driver dominant state driver on V_{BUS} = 18 V;	P_6.1.10
Bus short circuit filter time	$t_{BUS,sc}$	–	5	–	µs	9)The overall bus short circuit filter time is a sum of tBUS,sc + digital filter time. The digital filter time is 4 µs (typ.)	P_6.1.71
Leakage current (loss of ground)	$I_{BUS\_NO\_GND}$	-1000	-450	1000	µA	V_S = 12 V; 0 < V_{BUS} < 18 V;	P_6.1.11
Leakage current	$I_{BUS\_NO\_BAT}$	–	10	20	µA	V_S = 0 V; V_{BUS} = 18 V;	P_6.1.12

Table 33 Electrical Characteristics PWM Interface (cont'd)

V_s = 5.5V to 18V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
TxD dominant time out	$t_{timeout}$	6	12	20	ms	V_{TxD} = 0 V	P_6.1.36
Thermal Shutdown (Junction Temperature)							
Thermal shutdown temp.	T_{jSD}	190	200	215	°C	7)	P_6.1.65
Thermal shutdown hyst.	ΔT	–	10	–	K	7)	P_6.1.66

1) Maximum limit specified by design.
2) $V_{BUS\_CNT} = (V_{th\_dom} + V_{th\ rec})/2$
3) $V_{HYS} = V_{BUSrec} - V_{BUSdom}$
4) Bus load :
   Load 1 = 1 nF / 1 kΩ = C_{BUS} / R_{BUS}
   Load 2 = 6.8 nF / 660 Ω = C_{BUS} / R_{BUS}
   Load 3 = 10 nF / 500 Ω = C_{BUS} / R_{BUS}
5) Bus load
   Load 1 = 1 nF / 500 Ω = C_{BUS} / R_{BUS}
6) Not subject to production test, specified by design.

29.11 High-Voltage Monitoring Input

29.11.1 Electrical Characteristics

Table 41 Electrical Characteristics Monitoring Input

T_j = -40 °C to +150 °C; V_S = 5.5 V to 28 V, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
MON Input Pin characteristics							
Wake-up/monitoring threshold voltage	V_{MONth}	0.4*V_S	0.5*V_S	0.6*V_S	V	Without external serial resistor R_s (with R_s:DV = $I_{PD/PU}$ * R_s); V_S = 5.5V to 18V	P_11.1.1
Wake-up/monitoring threshold voltage extended range	V_{MONth_extend}	0.44*V_S	0.53*V_S	0.64*V_S	V	Without external serial resistor R_s (with R_s:DV = $I_{PD/PU}$ * R_s)	P_11.1.11
Threshold hysteresis	$V_{MONth,hys}$	0.015*V_S	0.05*V_S	0.1*V_S	V	In all modes; without external serial resistor R_s (with R_s:dV = $I_{PD/PU}$ * R_s); V_S = 5.5V to 18V;	P_11.1.12
Threshold hysteresis	$V_{MONth,hys}$	0.02*V_S	0.06*V_S	0.12*V_S	V	In all modes; without external serial resistor R_s (with R_s:dV = $I_{PD/PU}$ * R_s); V_S = 18V to 28V;	P_11.1.2
Pull-up current	$I_{PU, MON}$	-20	-10	-1	µA	0.6*V_S	P_11.1.3
Pull-down current	$I_{PD, MON}$	3	10	20	µA	0.4*V_S	P_11.1.4
Input leakage current	$I_{LK,MON}$	-2.5	–	2.5	µA	[1] 0 V < V_{MON_IN} < 28 V	P_11.1.5
Timing							
Wake-up filter time (internal analog filter delay)	$t_{FT,MON}$	–	500	–	ns	[2] The overall filter time for MON wake-up is a sum of $t_{FT,MON}$ + adjustable digital filter time. The digital filter time can be adjusted by PMU.CNF_WAKE_FILTER.CNF_MON_FT;	P_11.1.6

1) Input leakage is valid for disabled state.

2) With pull-up, pull down current disabled.