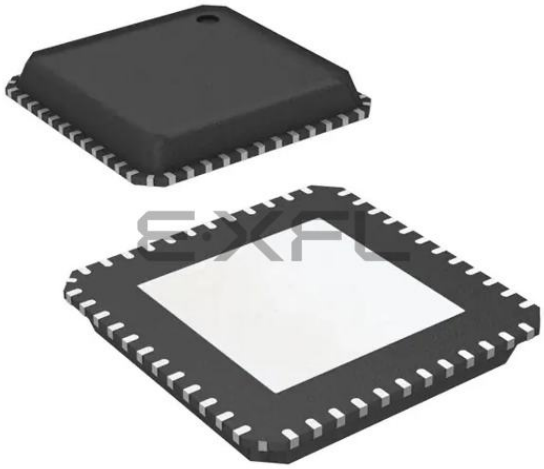

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Application-specific microcontrollers are engineered to

Details	
Product Status	Active
Applications	Automotive
Core Processor	ARM® Cortex®-M3
Program Memory Type	FLASH (36kB)
Controller Series	-
RAM Size	3K x 8
Interface	SSI, UART
Number of I/O	10
Voltage - Supply	5.5V ~ 28V
Operating Temperature	-40°C ~ 150°C
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	PG-VQFN-48-29
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/tle9861qxa20xuma2

Table 1 Acronyms

Acronyms	Name
PD	Pull Down
PGU	Power supply Generation Unit
PLL	Phase Locked Loop
PPB	Private Peripheral Bus
PU	Pull Up
PWM	Pulse Width Modulation
RAM	Random Access Memory
RCU	Reset Control Unit
RMU	Reset Management Unit
ROM	Read Only Memory
SCU-DM	System Control Unit - Digital Modules
SCU-PM	System Control Unit - Power Modules
SFR	Special Function Register
SOW	Short Open Window (for WDT)
SPI	Serial Peripheral Interface
SSC	Synchronous Serial Channel
STM	Store Instruction
SWD	ARM Serial Wire Debug
TCCR	Temperature Compensation Control Register
TMS	Test Mode Select
TSD	Thermal Shut Down
UART	Universal Asynchronous Receiver Transmitter
VBG	Voltage reference Band Gap
VCO	Voltage Controlled Oscillator
VPRE	Pre Regulator
WDT	Watchdog Timer in SCU-DM
WDT1	Watchdog Timer in SCU-PM
WMU	Wake-up Management Unit
100TP	100 Time Programmable

4 Modes of Operation

This highly integrated circuit contains analog and digital functional blocks. An embedded 32-bit microcontroller is available for system and interface control. On-chip, low-dropout regulators are provided for internal and external power supply. An internal oscillator provides a cost effective clock that is particularly well suited for PWM communications. A PWM interface is available as a communication interface. Driver stages for an H-Bridge with external MOSFET are integrated, featuring PWM capability, protection features and a charge pump for operation at low supply voltage. A 10-bit SAR ADC is implemented for high precision sensor measurement. An 8-bit ADC is used for diagnostic measurements.

The Micro Controller Unit supervision and system protection (including a reset feature) is complemented by a programmable window watchdog. A cyclic wake-up circuit, supply voltage supervision and integrated temperature sensors are available on-chip.

All relevant modules offer power saving modes in order to support automotive applications connected to terminal 30. A wake-up from power-save mode is possible via a PWM interface, via the monitoring input or using a programmable time period (cyclic wake-up).

Featuring LTI, the integrated circuit is available in a VQFN-48-31 package with 0.5 mm pitch, and is designed to withstand the severe conditions of automotive applications.

The TLE9861QXA20 has several operation modes mainly to support low power consumption requirements.

Reset Mode

The Reset Mode is a transition mode used e.g. during power-up of the device after a power-on reset, or after wake-up from Sleep Mode. In this mode, the on-chip power supplies are enabled and all other modules are initialized. Once the core supply VDDC is stable, the device enters Active Mode. If the watchdog timer WDT1 fails more than four times, the device performs a fail-safe transition to Sleep Mode.

Active Mode

In Active Mode, all modules are activated and the TLE9861QXA20 is fully operational.

Stop Mode

Stop Mode is one of two major low power modes. The transition to the low power modes is performed by setting the corresponding bits in the mode control register. In Stop Mode the embedded microcontroller is still powered, allowing faster wake-up response times. Wake-up from this mode is possible through LIN bus activity, by using the high-voltage monitoring pin or the corresponding 5V GPIOs.

Stop Mode with Cyclic Wake-Up

The Cyclic Wake-Up Mode is a special operating mode of the Stop Mode. The transition to the Cyclic Wake-Up Mode is done by first setting the corresponding bits in the mode control register followed by the Stop Mode command. In addition to the cyclic wake-up behavior (wake-up after a programmable time period), asynchronous wake events via the activated sources (LIN and/or MON) are available, as in normal Stop Mode.

Sleep Mode

The Sleep Mode is a low-power mode. The transition to the low-power mode is done by setting the corresponding bits in the MCU mode control register or in case of failure, see below. In Sleep Mode the embedded microcontroller power supply is deactivated allowing the lowest system power consumption. A wake-up from this mode is possible by PWM Interface activity, the High Voltage Monitor Input pin or Cyclic Wake-up.

Sleep Mode in Case of Failure

5.2.1 Block Diagram

The following figure shows the structure of the Power Management Unit. **Table 4** describes the submodules in more detail.

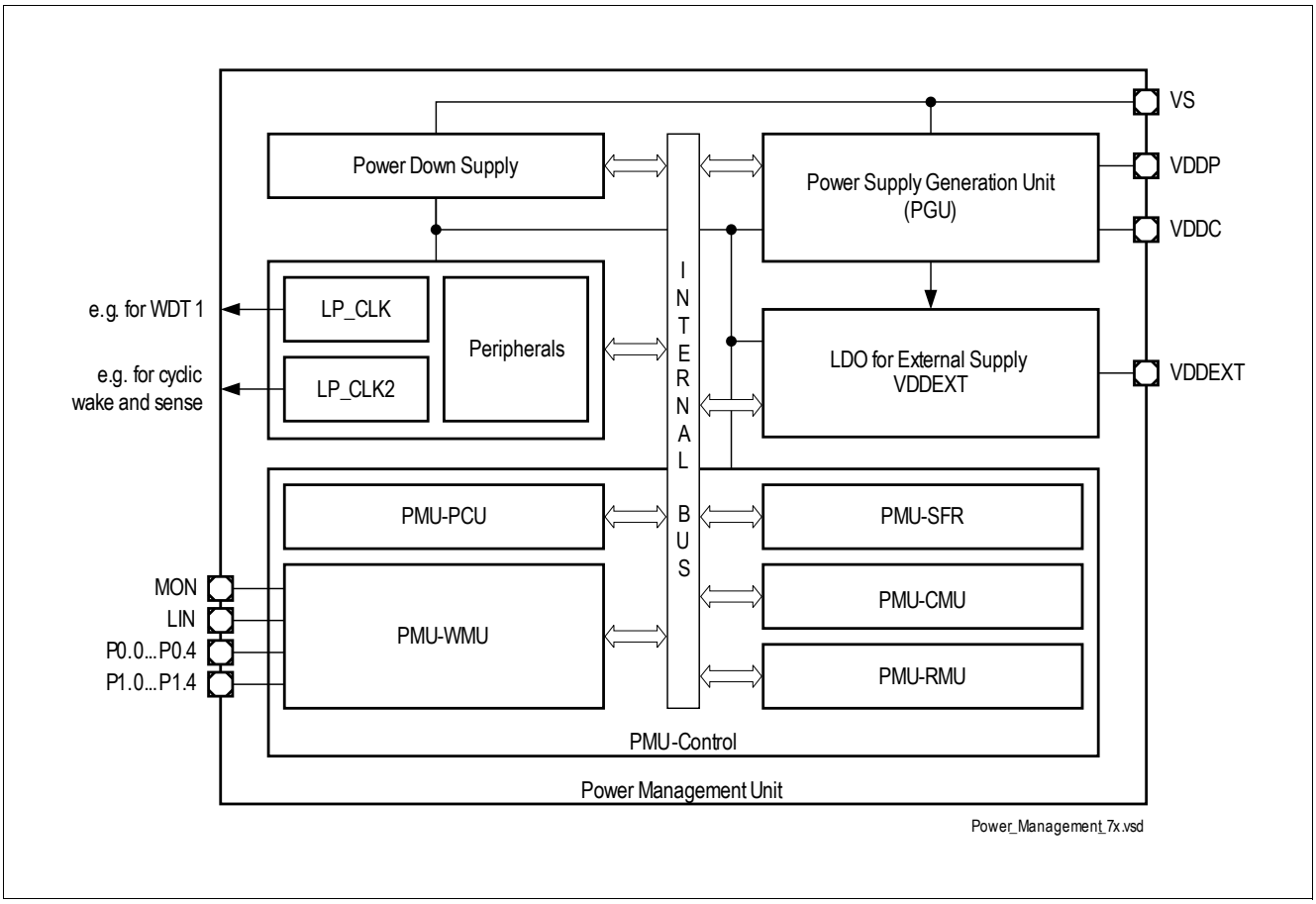

Figure 3 Power Management Unit Block Diagram

Table 4 Description of PMU Submodules

Mod. Name	Modules	Functions
Power Down Supply	Independent supply voltage generation for PMU	This supply is dedicated to the PMU to ensure an independent operation from generated power supplies (VDDP, VDDC).
LP_CLK (= 18 MHz)	- Clock source for all PMU submodules - Backup clock source for System - Clock source for WDT1	This ultra low power oscillator generates the clock for the PMU. This clock is also used as backup clock for the system in case of PLL Clock failure and as an independent clock source for WDT1.
LP_CLK2 (= 100 kHz)	Clock source for PMU	This ultra low power oscillator generates the clock for the PMU in Stop Mode and in the cyclic modes.
Peripherals	Peripheral blocks of PMU	These blocks include the analog peripherals to ensure a stable and fail-safe PMU startup and operation (bandgap, bias).

Table 4 Description of PMU Submodules (cont'd)

Mod. Name	Modules	Functions
Power Supply Generation Unit (PGU)	Voltage regulators for VDDP and VDDC	This block includes the voltage regulators for the pad supply (VDDP) and the core supply (VDDC).
VDDEXT	Voltage regulator for VDDEXT to supply external modules (e.g. sensors)	This voltage regulator is a dedicated supply for external modules and can also be used for cyclic sense operations (e.g. with hall sensor).
PMU-SFR	All Extended Special Function registers that are relevant to the PMU.	This module contains all registers needed to control and monitor the PMU.
PMU-PCU	Power Control Unit of the PMU	This block is responsible for controlling all power related actions within the PGU Module. It also contains all regulator related diagnostics such as undervoltage and overvoltage detection as well as overcurrent and short circuit diagnostics.
PMU-WMU	Wake-Up Management Unit of the PMU	This block is responsible for controlling all wake-up related actions within the PMU Module.
PMU-CMU	Cyclic Management Unit of the PMU	This block is responsible for controlling all actions in cyclic mode.
PMU-RMU	Reset Management Unit of the PMU	This block generates resets triggered by the PMU such as undervoltage or short circuit reset, and passes all resets to the relevant modules and their register.

5.2.2 PMU Modes Overview

The following state diagram shows the available modes of the device.

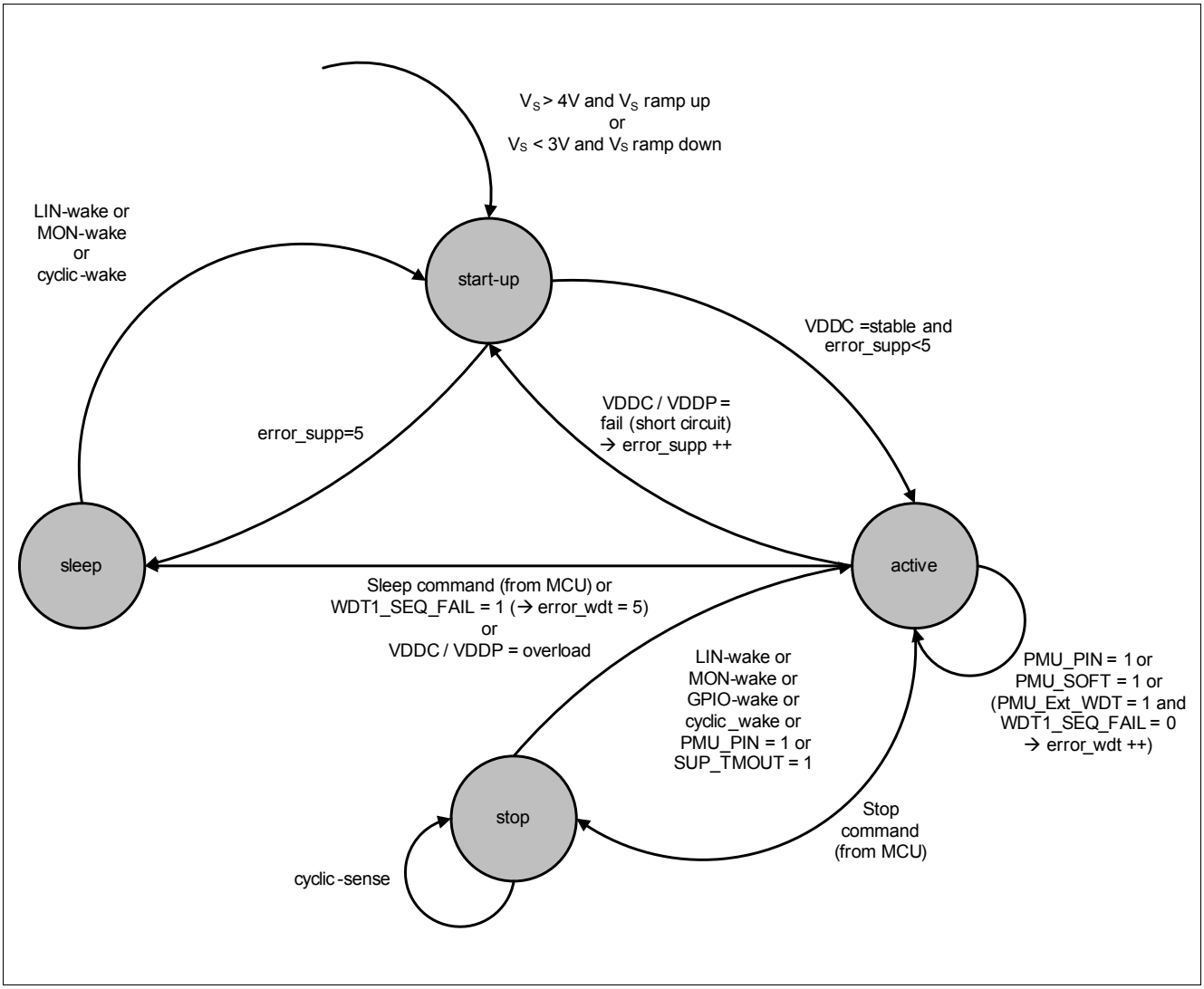

Figure 4 Power Management Unit System Modes

9.2 Introduction

Please also refer to **Chapter 9.3**, **Functional Description**.

9.2.1 Block Diagram

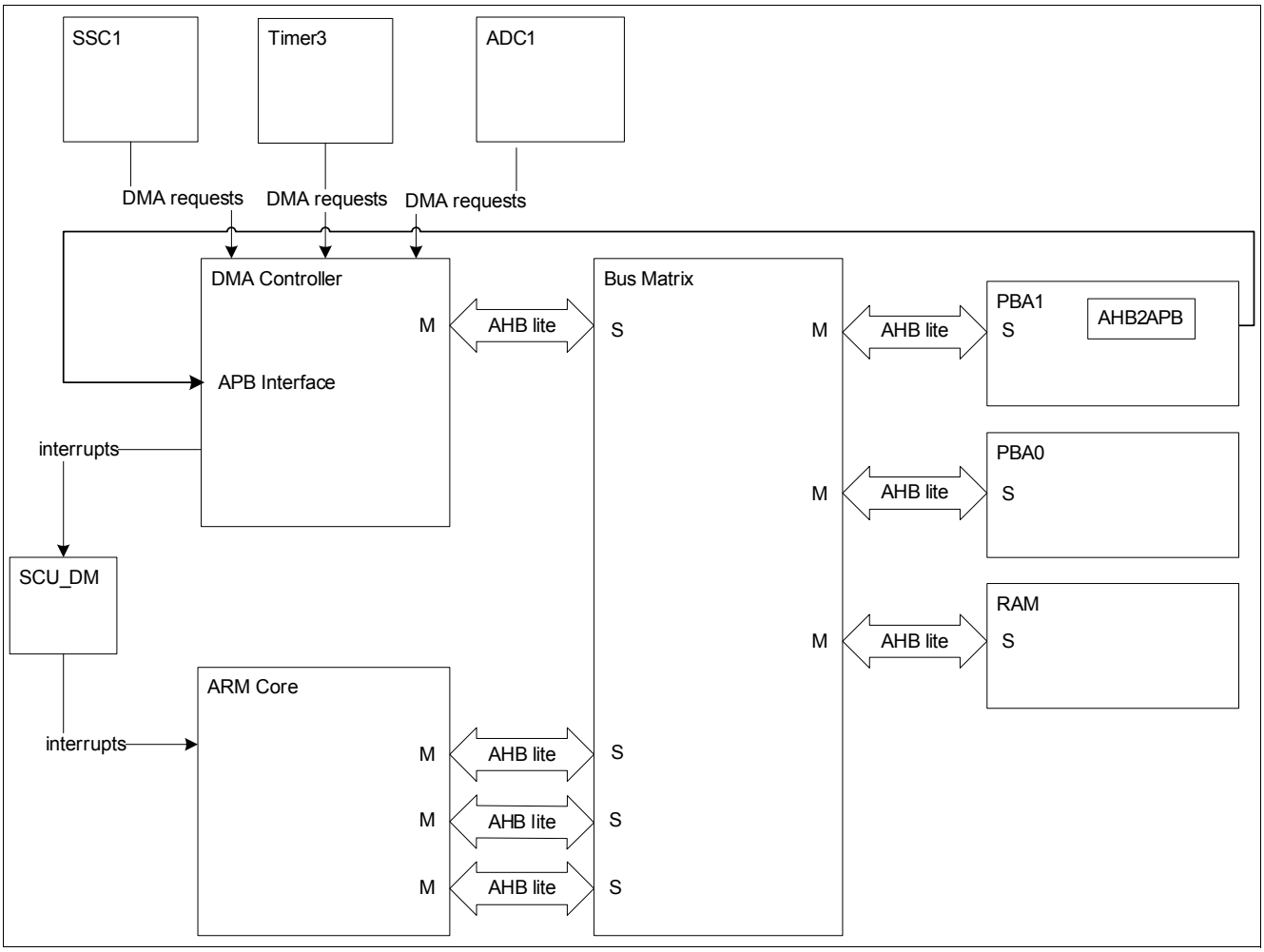

Figure 13 DMA Controller Top Level Block Diagram

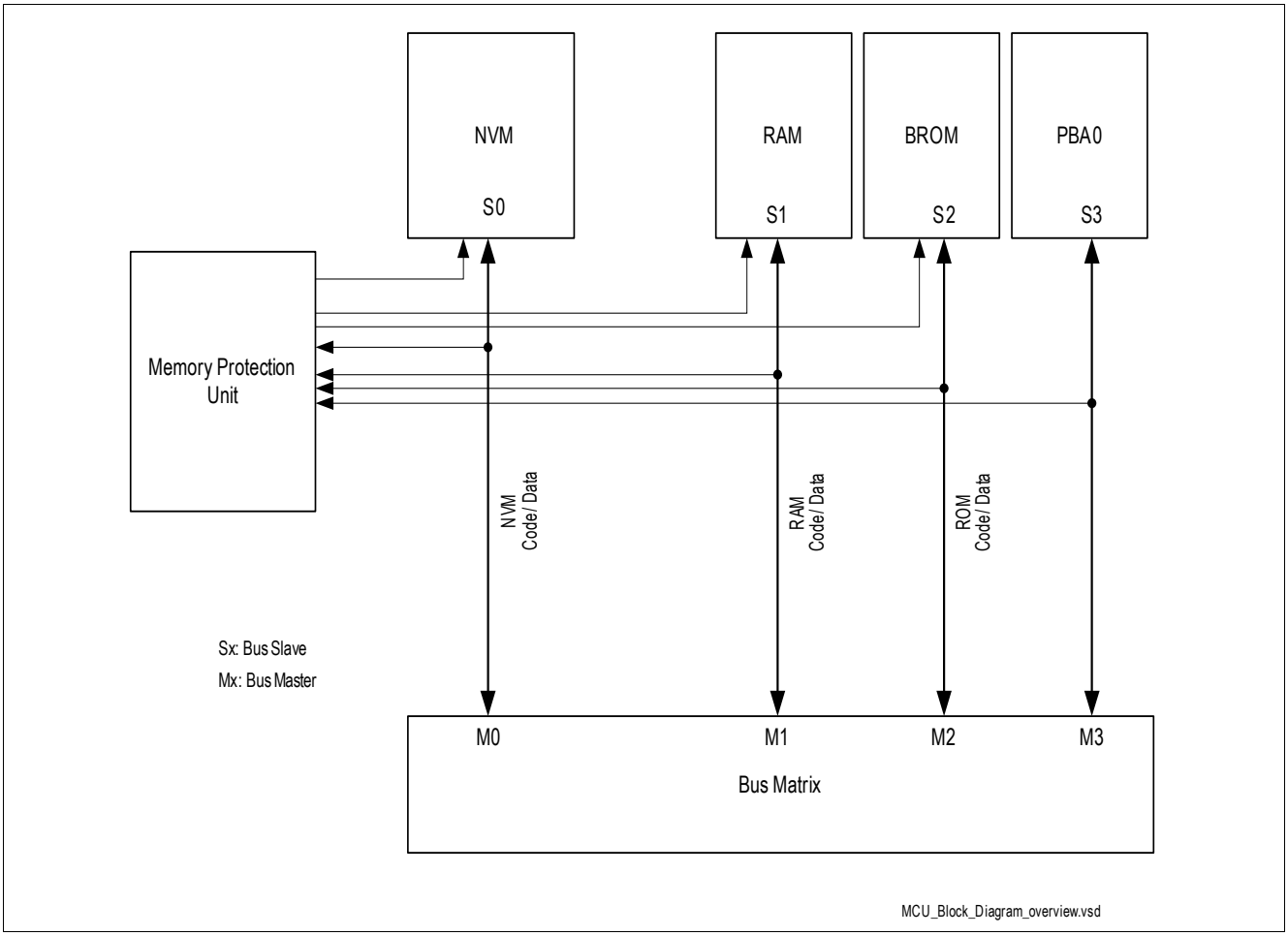

Figure 15 MCU Block View

11.3 NVM Module (Flash Memory)

The Flash Memory provides an embedded user-programmable non-volatile memory, allowing fast and reliable storage of user code and data.

Features

- In-system programming via PWM Interface (Flash Mode) and SWD
- Error Correction Code (ECC) for detection of single-bit and double-bit errors and dynamic correction of single Bit errors.
- Interrupts and signals double-bit error by NMI
- Program width of 128 byte (page)
- Minimum erase width of 128 bytes (page)
- Integrated hardware support for EEPROM emulation
- 8 byte read access
- Physical read access time: 75 ns
- Code read access acceleration integrated; read buffer and automatic pre-fetch
- Page program time: 3 ms
- Page erase (128 bytes) and sector erase (4K bytes) time: 4ms

Note: The user has to ensure that no flash operations which change the content of the flash get interrupted at any time.

The clock for the NVM is supplied with the system frequency fsys. Integrated firmware routines are provided to erase NVM, and other operations including EEPROM emulation are provided as well.

12 Interrupt System

12.1 Features

- Up to 16 interrupt nodes for on-chip peripherals
- Up to 8 NMI nodes for critical system events
- Maximum flexibility for all 16 interrupt nodes

12.2 Introduction

Before enabling an interrupt, all corresponding interrupt status flags should be cleared.

12.2.1 Overview

The TLE9861QXA20 supports 16 interrupt vectors with 16 priority levels. Fifteen of these interrupt vectors are assigned to the on-chip peripherals: GPT12, SSC, CCU6, DMA, Bridge Driver and A/D Converter are each assigned to one dedicated interrupt vector; while UART1 and Timer2 or UART2, External Interrupt 2 and Timer21 share interrupt vectors. Two vectors are dedicated for External Interrupt 0 and 1.

Table 6 Interrupt Vector Table

Service Request	Node ID	Description
GPT12	0/1	GPT interrupt (T2-T6, CAPIN)
MU- ADC8/T3	2	Measurement Unit, VBG, Timer3
ADC1	3	ADC1 interrupt / VREF5V Overload / VREF5V OV/UV, 10-bit ADC
CCU0	4	CCU6 node 0 interrupt
CCU1	5	CCU6 node 1 interrupt
CCU2	6	CCU6 node 2 interrupt
CCU3	7	CCU6 node 3 interrupt
SSC1	8	SSC1 interrupt (receive, transmit, error)
SSC2	9	SSC2 interrupt (receive, transmit, error)
UART1	10	UART1 interrupt (receive, transmit), Timer2, PWM-Interface
UART2	11	UART2 interrupt (receive, transmit), Timer21, External interrupt (EINT2)
EXINT0	12	External interrupt (EINT0), MON
EXINT1	13	External interrupt (EINT1)
BDRV/CP	14	Bridge Driver / Charge Pump
DMA	15	DMA Controller

Table 7 NMI Interrupt Table

Service Request	Node	Description
Watchdog Timer NMI	NMI	Watchdog Timer overflow
PLL NMI	NMI	PLL Loss-of-Lock
NVM Operation Complete NMI	NMI	NVM Operation Complete
Overtemperature NMI	NMI	System Overtemperature

Each pin can also be programmed to activate an internal weak pull-up or pull-down device. Register Px_PUDSEL selects whether a pull-up or the pull-down device is activated while register Px_PUDEN enables or disables the pull device.

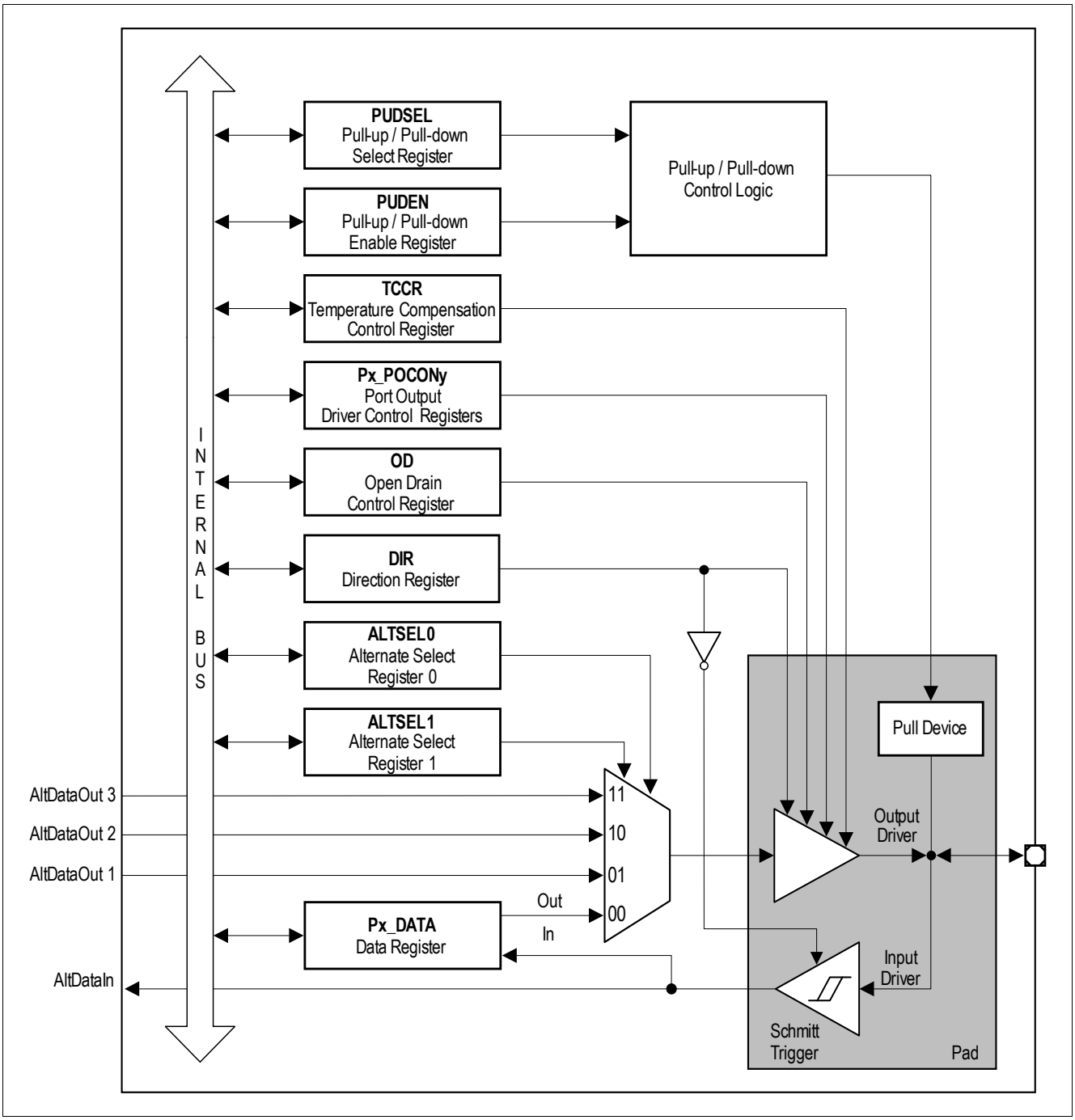

Figure 17 General Structure of Bidirectional Port (P0, P1)

14.3 TLE9861QXA20 Port Module

14.3.1 Port 0

14.3.1.1 Port 0 Functions

Table 8 Port 0 Input/Output Functions

Port Pin	Input/Output	Select	Connected Signal(s)	From/to Module
P0.0	Input	GPI	P0_DATA.P0	
		INP1	SWCLK / TCK_0	SW
		INP2	T12HR_0	CCU6
		INP3	T4INA	GPT12T4
		INP4	T2_0	Timer 2
		INP5	–	–
		INP6	EXINT2_3	SCU
	Output	GPO	P0_DATA.P0	
		ALT1	T3OUT	GPT12T3
		ALT2	EXF21_0	Timer 21
		ALT3	RXDO_2	UART2
P0.1	Input	GPI	P0_DATA.P1	
		INP2	T13HR_0	CCU6
		INP3	TxD1	PWM_TxD
		INP4	CAPINA	GPT12CAP
		INP5	T21_0	Timer 21
		INP6	T4INC	GPT12T4
		INP7	MRST_1_2	SSC1
		INP8	EXINT0_2	SCU
	Output	GPO	P0_DATA.P1	
		ALT1	TxD1	UART1 / PWM_TxD
		ALT2	–	–
		ALT3	T6OUT	GPT12T6

14.3.3 Port 2

14.3.3.1 Port 2 Functions

Table 10 Port 2 Input Functions

Port Pin	Input/Output	Select	Connected Signal(s)	From/to Module
P2.0	Input	GPI	P2_DATA.P0	
		INP1	CCPOS0_3	CCU6
		INP2	-	-
		INP3	T12HR_2	CCU6
		INP4	EXINT0_0	SCU
		INP5	CC61_2	CCU6
		ANALOG	AN0	ADC
			XTAL (in)	XTAL
P2.2	Input	GPI	P2_DATA.P2	
		INP1	CCPOS2_3	CCU6
		INP2	T13HR_2	CCU6
		INP3	–	
		INP4	CC62_2	CCU6
		ANALOG	AN2	ADC
		OUT	XTAL (out)	XTAL
P2.3	Input	GPI	P2_DATA.P3	
		INP1	CCPOS1_0	CCU6
		INP2	CTRAP#_1	CCU6
		INP3	T21EX_2	Timer 21
		INP4	CC60_1	CCU6
		INP5	EXINT0_3	SCU
		ANALOG	AN3	ADC
P2.4	Input	GPI	P2_DATA.P4	
		INP1	$\overline{\text{CTRAP\#\_0}}$	CCU6
		INP2	T2EUDB	GPT12T2
		INP3	MRST_1_1	SSC1
		INP4	EXINT1_3	SCU
		ANALOG	AN4	ADC
P2.5	Input	GPI	P2_DATA.P5	
		INP1	RXD2_1	UART2
		INP2	T3EUDB	GPT12T3
		INP3	MRST_2_1	SSC2
		INP4	T2_1	Timer 2
		ANALOG	AN5	ADC

15.2.2 Block Diagram GPT2

Block GPT2 contains two timers/counters: The core timer T6 and the auxiliary timer T5. The maximum resolution is $f_{GPT}/2$. An additional Capture/Reload register (CAPREL) supports capture and reload operation with extended functionality.

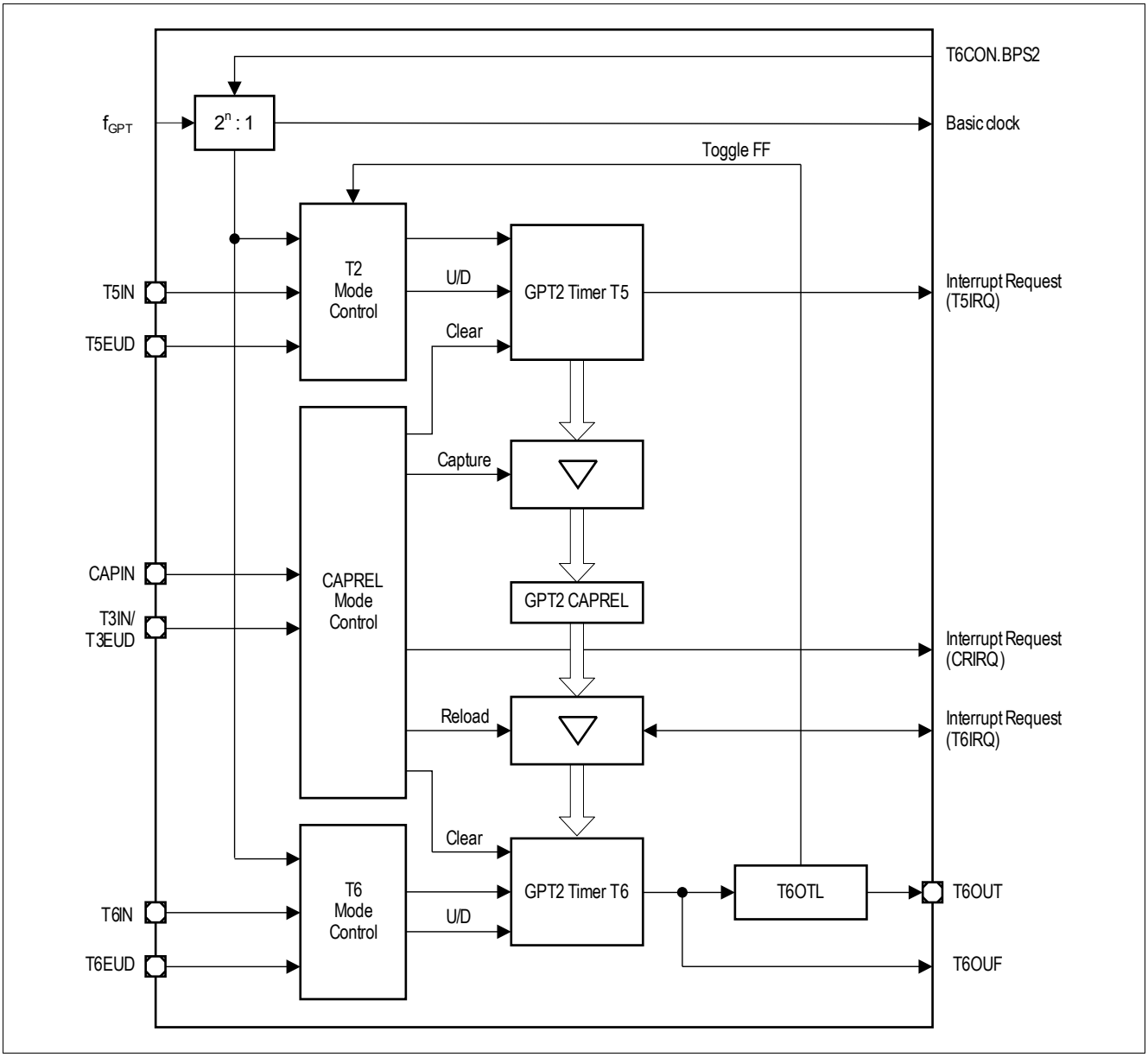

Figure 20 GPT2 Block Diagram (n = 1 … 4)

Note: The capture/compare module itself is referred to as CCU6 (capture/compare unit 6). A capture/compare channel inside this module is referred to as CC6x.

The timer T12 can work in capture and/or compare mode for its three channels. The modes can also be combined (e.g. a channel works in compare mode, whereas another channel works in capture mode). The timer T13 can work in compare mode only. The multi-channel control unit generates output patterns which can be modulated by T12 and/or T13. The modulation sources can be selected and combined for the signal modulation.

18.2.1 Block Diagram

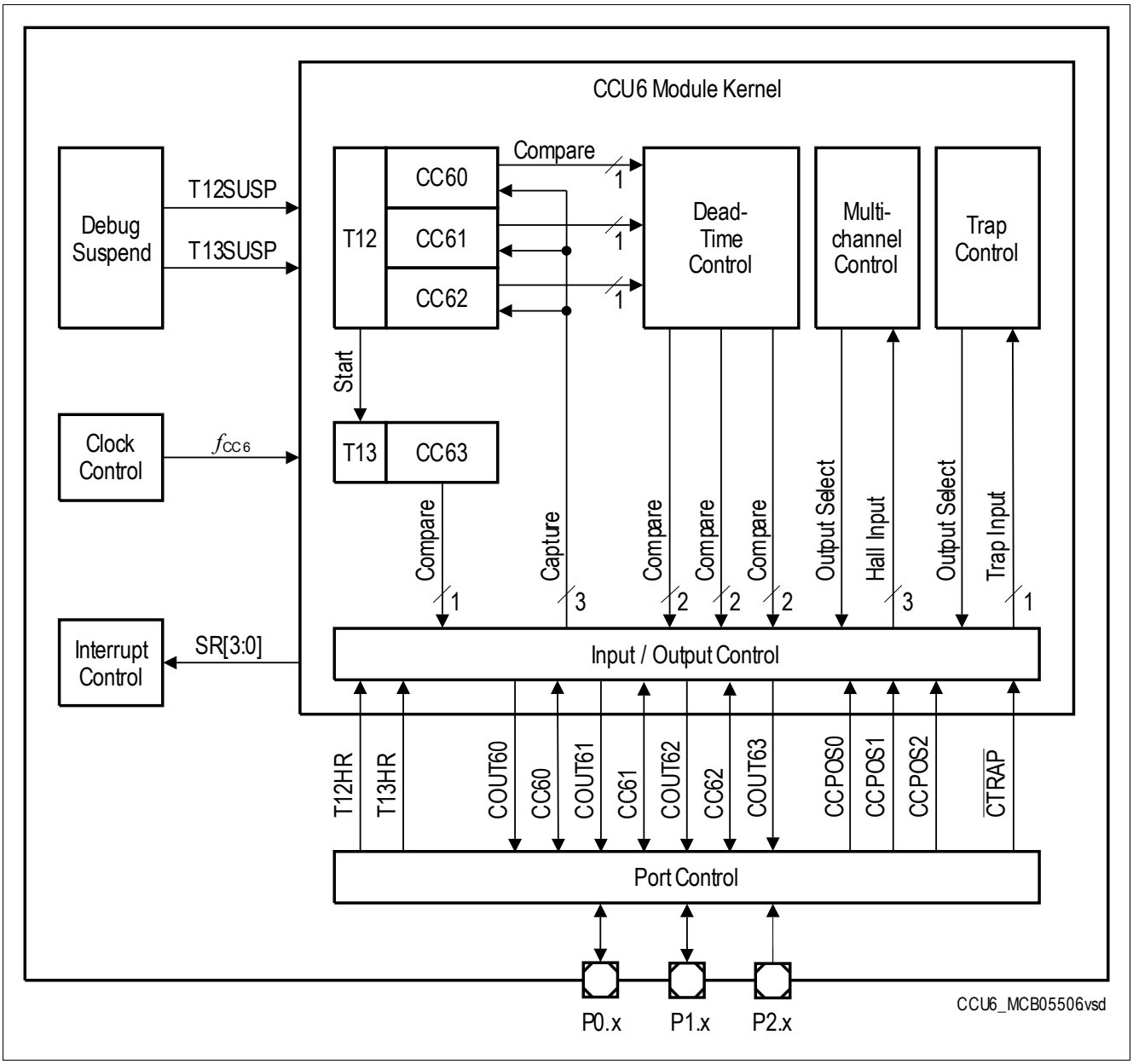

Figure 21 CCU6 Block Diagram

29.1.4 Thermal Resistance

Table 20 Thermal Resistance

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Junction to Soldering Point	R_{thJSP}	–	6	–	K/W	1) measured to Exposed Pad	P_1.4.1
Junction to Ambient	R_{thJA}	–	33	–	K/W	2)	P_1.4.2

1) Not subject to production test, specified by design.

2) According to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board. Board: 76.2x114.3x1.5mm³ with 2 inner copper layers (35µm thick), with thermal via array under the exposed pad contacting the first inner copper layer and 300mm^2 cooling area on the bottom layer (70µm).

29.1.5 Timing Characteristics

The transition times between the system modes are specified here. Generally the timings are defined from the time when the corresponding bits in register PMCON0 are set until the sequence is terminated.

Table 21 System Timing1)

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Wake-up over battery	t_{start}	–	–	3	ms	Battery ramp-up time to code execution	P_1.5.6
Wake-up over battery	$t_{startSW}$	–	–	1.5	ms	Battery ramp-up time to till MCU reset is released; V_S > 3 V and RESET = 1	P_1.5.1
Sleep-Exit	$t_{sleep\ -\ exit}$	–	–	1.5	ms	Rising/falling edge of any wake-up signal (PWM interface, MON) till MCU reset is released;	P_1.5.2
Sleep-Entry	$t_{sleep\ -\ entry}$	–	–	330	µs	2)	P_1.5.3

1) Not subject to production test, specified by design.

2) Wake events during Sleep-Entry are stored and lead to wake-up after Sleep Mode is reached.

5) The absolute voltage value is the sum of parameters V_{DDEXT} + $\Delta V_{DDEXTSTB}$.
6) When the condition is met, the Bit VDDEXT_CTRL.bit.SHORT will be set.

29.2.4 VPRE Voltage Regulator (PMU Subblock) Parameters

The PMU VPRE Regulator acts as a supply of VDDP and VDDEXT voltage regulators.

Table 25 Functional Range

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Specified output current	I_{VPRE}	–	–	110	mA	1)	P_2.4.1

1) Not subject to production test, specified by design.

29.2.4.1 Load Sharing Scenarios of VPRE Regulator

The figure below shows the possible load sharing scenarios of VPRE regulator.

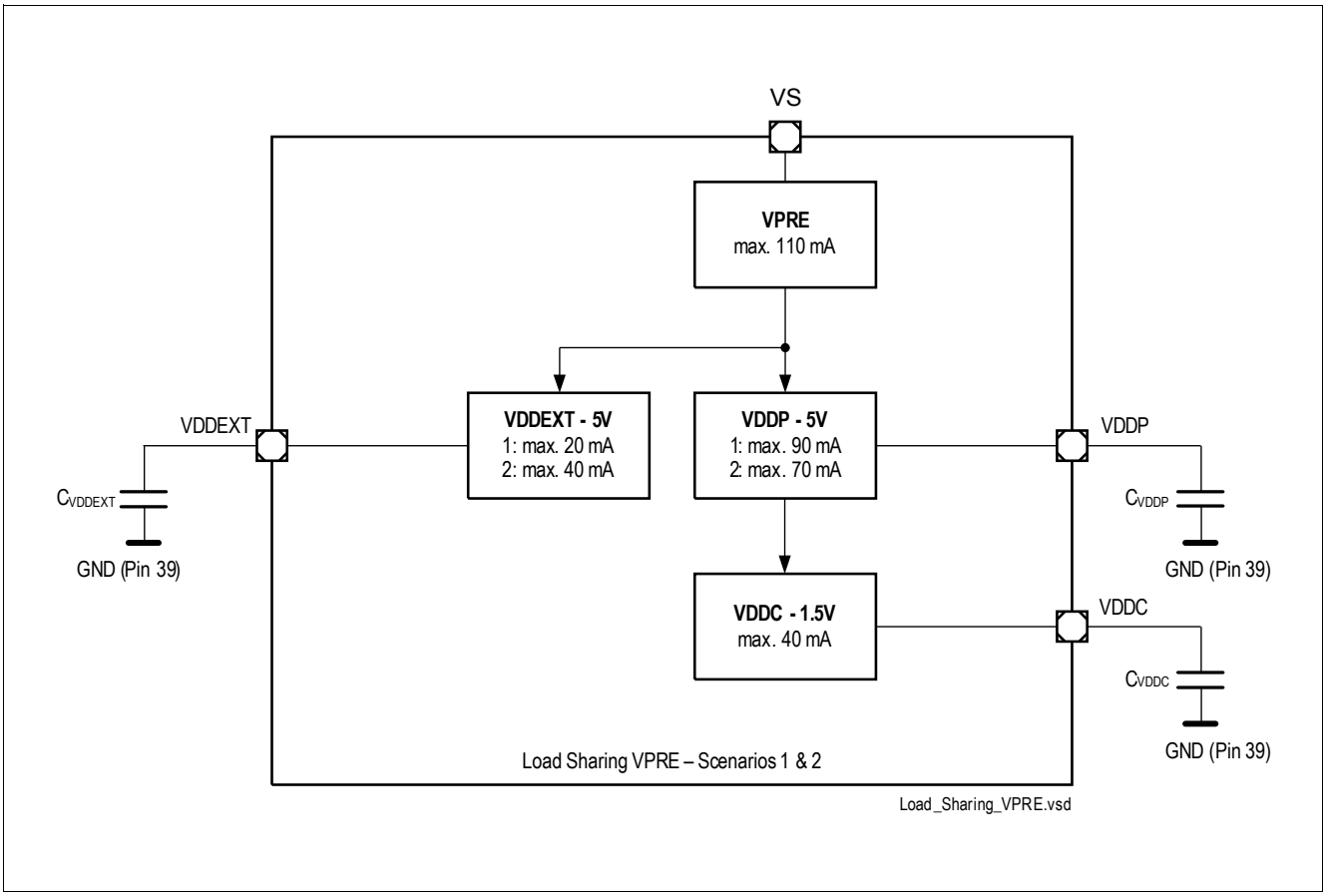

Figure 32 Load Sharing Scenarios of VPRE Regulator

29.2.5 Power Down Voltage Regulator (PMU Subblock) Parameters

The PMU Power Down voltage regulator consists of two subblocks:

- Power Down Pre regulator: VDD5VPD
- Power Down Core regulator: VDD1V5_PD (Supply used for GPUDATAxy registers)

Both regulators are used as purely internal supplies. The following table contains all relevant parameters:

Table 26 Functional Range

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
VDD1V5_PD							
Power-On Reset Threshold	$V_{DD1V5\_PD\_RSTTH}$	1.2	–	1.5	V	1)	P_2.5.1

1) Not subject to production test, specified by design

29.3 System Clocks

29.3.1 Oscillators and PLL Parameters

Table 27 Electrical Characteristics System Clocks

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
PMU Oscillators (Power Management Unit)							
Frequency of LP_CLK	f_{LP_CLK}	14	18	22	MHz	This clock is used at startup and can be used in case the PLL fails	P_3.1.1
Frequency of LP_CLK2	f_{LP_CLK2}	70	100	130	kHz	This clock is used for cyclic wake	P_3.1.2
CGU Oscillator (Clock Generation Unit Microcontroller)							
Short term frequency deviation[1)]	f_{TRIMST}	-0.4	–	+0.4	%	[2)3)] Within any 10 ms, e.g. after synchronization to a PWM signal (PLL settings untouched within 10 ms)	P_3.1.3
Absolute accuracy	$f_{TRIMABSA}$	-1.5	–	+1.5	%	Including temperature and lifetime deviation	P_3.1.4
CGU-OSC Start-up time	t_{OSC}	–	–	10	µs	[3)] Startup time OSC from Sleep Mode, power supply stable	P_3.1.5
PLL (Clock Generation Unit Microcontroller) [3)]							
VCO frequency range Mode 0	f_{VCO-0}	48	–	112	MHz	VCOSEL =”0”	P_3.1.6
VCO frequency range Mode 1	f_{VCO-1}	96	–	160	MHz	VCOSEL =”1”	P_3.1.7
Input frequency range	f_{OSC}	4	–	16	MHz	–	P_3.1.8
XTAL1 input freq. range	f_{OSC}	4	–	16	MHz	–	P_3.1.9
Output freq. range	f_{PLL}	0.04687	–	80	MHz	–	P_3.1.10
Free-running frequency Mode 0	$f_{VCOfree\_0}$	–	–	38	MHz	VCOSEL =”0”	P_3.1.11
Free-running frequency Mode 1	$f_{VCOfree\_1}$	–	–	76	MHz	VCOSEL =”1”	P_3.1.12
Input clock high/low time	$t_{high/low}$	10	–	–	ns	–	P_3.1.13
Peak period jitter	t_{jp}	-500	–	500	ps	[4)] for K=1	P_3.1.14
Accumulated jitter	jacc	–	–	5	ns	[4)] for K=1	P_3.1.15
Lock-in time	t_L	–	–	200	µs	–	P_3.1.16

Table 32 DC Characteristics Port 2 (cont'd)

V_S = 5.5 V to 28 V, T_j = -40 °C to +150 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Pull level force current	I_{PLF}	-750	–	+750	µA	3) $V_{PIN} \le V_{IL}$ (up) $V_{PIN} \ge V_{IH}$ (dn)	P_5.2.6
Pin capacitance (digital inputs/outputs)	C_{IO}	–	–	10	pF	2)	P_5.2.7

1) Tested at V_{DDP} = 5V, specified for 4.5V < V_{DDP} < 5.5V.

2) Not subject to production test, specified by design.

3) Keep current: Limit the current through this pin to the indicated value so that the enabled pull device can keep the default pin level: $V_{PIN} \ge V_{IH}$ for a pull-up; $V_{PIN} \le V_{IL}$ for a pull-down.
Force current: Drive the indicated minimum current through this pin to change the default pin level driven by the enabled pull device: $V_{PIN} \le V_{IL}$ for a pull-up; $V_{PIN} \ge V_{IH}$ for a pull-down.