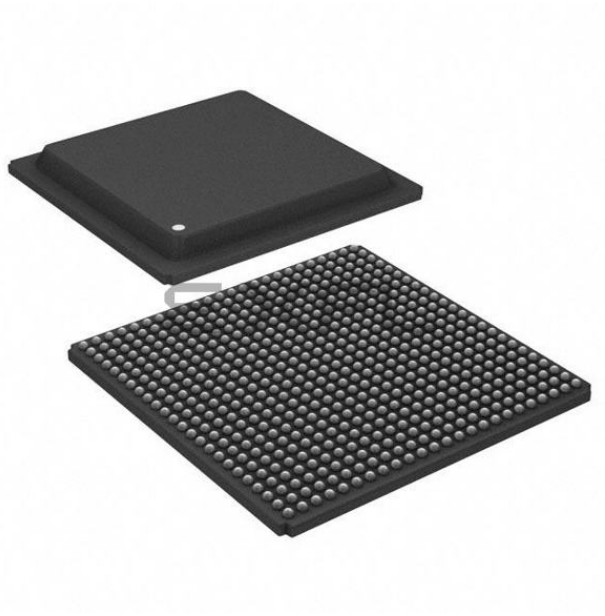

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed/Floating Point
Interface	Host Interface, Link Port, Multi-Processor
Clock Rate	500MHz
Non-Volatile Memory	External
On-Chip RAM	512kB
Voltage - I/O	2.50V
Voltage - Core	1.05V
Operating Temperature	-40°C ~ 85°C (TC)
Mounting Type	Surface Mount
Package / Case	576-BBGA
Supplier Device Package	576-BGA-ED (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-ts203sabp-050

- EE-217: Updating the ADSP-TS101S TigerSHARC® EZ-KIT Lite™ Firmware
- EE-218: Writing Efficient Floating-Point FFTs for ADSP-TS201 TigerSHARC® Processors
- EE-261: Understanding Jitter Requirements of PLL-Based Processors
- EE-263: Parallel Implementation of Fixed-Point FFTs on TigerSHARC® Processors
- EE-283: External Bus Arbitration with ADSP-TS20x TigerSHARC® Processors
- EE-330: Windows Vista Compatibility in VisualDSP++ 5.0 Development Tools
- EE-332: Cycle Counting and Profiling
- EE-356: Emulator and Evaluation Hardware Troubleshooting Guide for CCES Users
- EE-68: Analog Devices JTAG Emulation Technical Reference

Data Sheet

- ADSP-TS203S: TigerSHARC Embedded Processor Data Sheet
- TigerSHARC Embedded Processor ADSP-TS203S

Integrated Circuit Anomalies

- ADSP-TS203S TigerSHARC Anomaly List for Revision(s) 1.1, 1.2, 2.0

Processor Manuals

- ADSP-TS201 TigerSHARC Processor Hardware Reference
- ADSP-TS201 TigerSHARC Processor Programming Reference

Product Highlight

- 600 MHz TigerSHARC Processor: The Performance Density Leader

Software Manuals

- VisualDSP++® 5.0 Assembler and Preprocessor Manual
- VisualDSP++® 5.0 C/C++ Compiler and Library Manual for TigerSHARC Processors
- VisualDSP++® 5.0 Kernel (VDK) Users Guide
- VisualDSP++® 5.0 Licensing Guide
- VisualDSP++® 5.0 Linker and Utilities Manual
- VisualDSP++® 5.0 Loader and Utilities Manual
- VisualDSP++® 5.0 Product Release Bulletin
- VisualDSP++® 5.0 Quick Installation Reference Card
- VisualDSP++® 5.0 Users Guide

SOFTWARE AND SYSTEMS REQUIREMENTS

- TigerSHARC Evaluation Kits

TOOLS AND SIMULATIONS

- ADSP-TS20x TigerSHARC BSDL File 25x25mm PBGA Package for Revision 1.1, (03/2005)
- ADSP-TS20x TigerSHARC BSDL File 25x25mm PBGA Package for Revision 1.2, (03/2005)
- ADSP-TS20x TigerSHARC BSDL File 25x25mm PBGA Package for Revision 2.0, (01/2006)

REFERENCE MATERIALS

Informational

- TigerSHARC Processor Architectural Features

Product Selection Guide

- ADI Complementary Parts Guide - Supervisory Devices and DSP Processors

Technical Articles

- A Software Solution for Chip Rate Processing in CDMA Wireless Infrastructure
- Continuous Real-Time Signal Processing -- Comparing TigerSHARC and PowerPC Via Continuous cFFTs
- DSPs Step Forward in 3G Stations
- SHARC Bites Back - The Memory Inside: TigerSHARC Swallows Its DRAM

DESIGN RESOURCES

- ADSP-TS203S Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

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GENERAL DESCRIPTION

The ADSP-TS203S TigerSHARC processor is an ultrahigh performance, static superscalar processor optimized for large signal processing tasks and communications infrastructure. The processor combines very wide memory widths with dual computation blocks—supporting floating-point (IEEE 32-bit and extended precision 40-bit) and fixed-point (8-, 16-, 32-, and 64-bit) processing—to set a new standard of performance for digital signal processors. The TigerSHARC static superscalar architecture lets the processor execute up to four instructions each cycle, performing 24 fixed-point (16-bit) operations or six floating-point operations.

Four independent 128-bit wide internal data buses, each connecting to the four 1M bit memory banks, enable quad-word data, instruction, and I/O access and provide 28G bytes per second of internal memory bandwidth. Operating at 500 MHz, the ADSP-TS203S processor's core has a 2.0 ns instruction cycle time. Using its single-instruction, multiple-data (SIMD) features, the processor can perform four billion 40-bit MACS or one billion 80-bit MACS per second. Table 1 shows the processor's performance benchmarks.

Table 1. General-Purpose Algorithm Benchmarks at 500 MHz

Benchmark	Speed	Clock Cycles
32-bit algorithm, 1 billion MACS/s peak performance		
1K point complex FFT[1] (Radix 2)	18.8 µs	9419
		13975
64K point complex FFT[1] (Radix 2)	2.8 ms	44
FIR filter (per real tap)	1 ns	0.5
[8 × 8][8 × 8] matrix multiply (complex, floating-point)	2.8 µs	1399
16-bit algorithm, 4 billion MACS/s peak performance		
256 point complex FFT[1] (Radix 2)	1.9 µs	928
I/O DMA transfer rate		
External port	500M bytes/s	n/a
Link ports (each)	500M bytes/s	n/a

[1] Cache preloaded.

The ADSP-TS203S processor is code compatible with the other TigerSHARC processors.

The Functional Block Diagram on Page 1 shows the processor's architectural blocks. These blocks include

- Dual compute blocks, each consisting of an ALU, multiplier, 64-bit shifter, and 32-word register file and associated data alignment buffers (DABs)
- Dual integer ALUs (IALUs), each with its own 31-word register file for data addressing and a status register
- A program sequencer with instruction alignment buffer (IAB) and branch target buffer (BTB)
- An interrupt controller that supports hardware and software interrupts, supports level- or edge-triggers, and supports prioritized, nested interrupts
- Four 128-bit internal data buses, each connecting to the four 1M-bit memory banks
- On-chip DRAM (4M-bit)
- An external port that provides the interface to host processors, multiprocessing space (DSPs), off-chip memory-mapped peripherals, and external SRAM and SDRAM
- A 10-channel DMA controller
- Two full-duplex LVDS link ports
- Two 64-bit interval timers and timer expired pin
- An 1149.1 IEEE-compliant JTAG test access port for on-chip emulation

The TigerSHARC uses a Static Superscalar™* architecture. This architecture is superscalar in that the ADSP-TS203S processor's core can execute simultaneously from one to four 32-bit instructions encoded in a very large instruction word (VLIW) instruction line using the processor's dual compute blocks. Because the processor does not perform instruction reordering at runtime—the programmer selects which operations will execute in parallel prior to runtime—the order of instructions is static.

With few exceptions, an instruction line, whether it contains one, two, three, or four 32-bit instructions, executes with a throughput of one cycle in a 10-deep processor pipeline.

For optimal processor program execution, programmers must follow the processor's set of instruction parallelism rules when encoding an instruction line. In general, the selection of instructions that the processor can execute in parallel each cycle depends both on the instruction line resources each instruction requires and on the source and destination registers used in the instructions. The programmer has direct control of three core components—the IALUs, the compute blocks, and the program sequencer.

The ADSP-TS203S processor, in most cases, has a two-cycle execution pipeline that is fully interlocked, so—whenever a computation result is unavailable for another operation dependent on it—the processor automatically inserts one or more stall cycles as needed. Efficient programming with dependency-free instructions can eliminate most computational and memory transfer data dependencies.

In addition, the processor supports SIMD operations two ways—SIMD compute blocks and SIMD computations. The programmer can load both compute blocks with the same data (broadcast distribution) or different data (merged distribution).

* Static Superscalar is a trademark of Analog Devices, Inc.

Interrupt Controller

The processor supports nested and nonnested interrupts. Each interrupt type has a register in the interrupt vector table. Also, each has a bit in both the interrupt latch register and the interrupt mask register. All interrupts are fixed as either level-sensitive or edge-sensitive, except the $\overline{\text{IRQ3–0}}$ hardware interrupts, which are programmable.

The processor distinguishes between hardware interrupts and software exceptions, handling them differently. When a software exception occurs, the processor aborts all other instructions in the instruction pipe. When a hardware interrupt occurs, the processor continues to execute instructions already in the instruction pipe.

Flexible Instruction Set

The 128-bit instruction line, which can contain up to four 32-bit instructions, accommodates a variety of parallel operations for concise programming. For example, one instruction line can direct the processor to conditionally execute a multiply, an add, and a subtract in both computation blocks while it also branches to another location in the program. Some key features of the instruction set include:

- Algebraic assembly language syntax
- Direct support for all DSP, imaging, and video arithmetic types
- Eliminates toggling hardware modes because modes are supported as options (for example, rounding, saturation, and others) within instructions
- Branch prediction encoded in instruction; enables zero-overhead loops
- Parallelism encoded in instruction line
- Conditional execution optional for all instructions
- User-defined partitioning between program and data memory

MEMORY

The processor's internal and external memory is organized into a unified memory map, which defines the location (address) of all elements in the system, as shown in Figure 2.

The memory map is divided into four memory areas—host space, external memory, multiprocessor space, and internal memory—and each memory space, except host memory, is subdivided into smaller memory spaces.

The ADSP-TS203S processor internal memory has 4M bits of on-chip DRAM memory, divided into four blocks of 1M bits (32K words × 32 bits). Each block—M0, M2, M4, and M6—can store program instructions, data, or both, so applications can configure memory to suit specific needs. Placing program instructions and data in different memory blocks, however, enables the processor to access data while performing an instruction fetch. Each memory segment contains a 128K bit cache to enable single-cycle accesses to internal DRAM.

The four internal memory blocks connect to the four 128-bit wide internal buses through a crossbar connection, enabling the processor to perform four memory transfers in the same cycle. The processor's internal bus architecture provides a total memory bandwidth of 28G bytes per second, allowing the core and I/O to access eight 32-bit data-words and four 32-bit instructions each cycle. Additional features are:

- Processor core and I/O access to different memory blocks in the same cycle
- Processor core access to three memory blocks in parallel—one instruction and two data accesses
- Programmable partitioning of program and data memory
- Program access of all memory as 32-, 64-, or 128-bit words—16-bit words with the DAB

EXTERNAL PORT (OFF-CHIP MEMORY/PERIPHERALS INTERFACE)

The ADSP-TS203S processor's external port provides the processor's interface to off-chip memory and peripherals. The 4G word address space is included in the processor's unified address space. The separate on-chip buses—four 128-bit data buses and four 32-bit address buses—are multiplexed at the SOC interface and transferred to the external port over the SOC bus to create an external system bus transaction. The external system bus provides a single 32-bit data bus and a single 32-bit address bus. The external port supports data transfer rates of 500M bytes per second over the external bus.

The external bus is configured for 32-bit, little-endian operations. Unlike the ADSP-TS201, the ADSP-TS203S processor's external port cannot support 64-bit operations; the external bus width control bits (Bits 21-19) must = 0 in the SYSCON register—all other values are illegal for the ADSP-TS203S. Because the external port is restricted to 32 bits on the ADSP-TS203S processor, there are a number of pinout differences between the ADSP-TS203S and the ADSP-TS201 processors.

The external port supports pipelined, slow, and SDRAM protocols. Addressing of external memory devices and memory-mapped peripherals is facilitated by on-chip decoding of high order address lines to generate memory bank select signals.

The ADSP-TS203S processor provides programmable memory, pipeline depth, and idle cycle for synchronous accesses, and external acknowledge controls to interface to pipelined or slow devices, host processors, and other memory-mapped peripherals with variable access, hold, and disable time requirements.

Host Interface

The ADSP-TS203S processor provides an easy and configurable interface between its external bus and host processors through the external port. To accommodate a variety of host processors, the host interface supports pipelined or slow protocols for processor access of the host as slave or pipelined for host access of the ADSP-TS203S processor as slave. Each protocol has programmable transmission parameters, such as idle cycles, pipe depth, and internal wait cycles.

The host interface supports burst transactions initiated by a host processor. After the host issues the starting address of the burst and asserts the $\overline{\text{BRST}}$ signal, the processor increments the address internally while the host continues to assert $\overline{\text{BRST}}$.

The host interface provides a deadlock recovery mechanism that enables a host to recover from deadlock situations involving the processor. The $\overline{\text{BOFF}}$ signal provides the deadlock recovery mechanism. When the host asserts $\overline{\text{BOFF}}$, the processor backs off the current transaction and asserts $\overline{\text{HBG}}$ and relinquishes the external bus.

The host can directly read or write the internal memory of the ADSP-TS203S processor, and it can access most of the processor registers, including DMA control (TCB) registers. Vector interrupts support efficient execution of host commands.

Multiprocessor Interface

The processor offers powerful features tailored to multiprocessing processor systems through the external port and link ports. This multiprocessing capability provides the highest bandwidth for interprocessor communication, including

- Up to eight DSPs on a common bus
- On-chip arbitration for glueless multiprocessing
- Link ports for point-to-point communication

The external port and link ports provide integrated, glueless multiprocessing support.

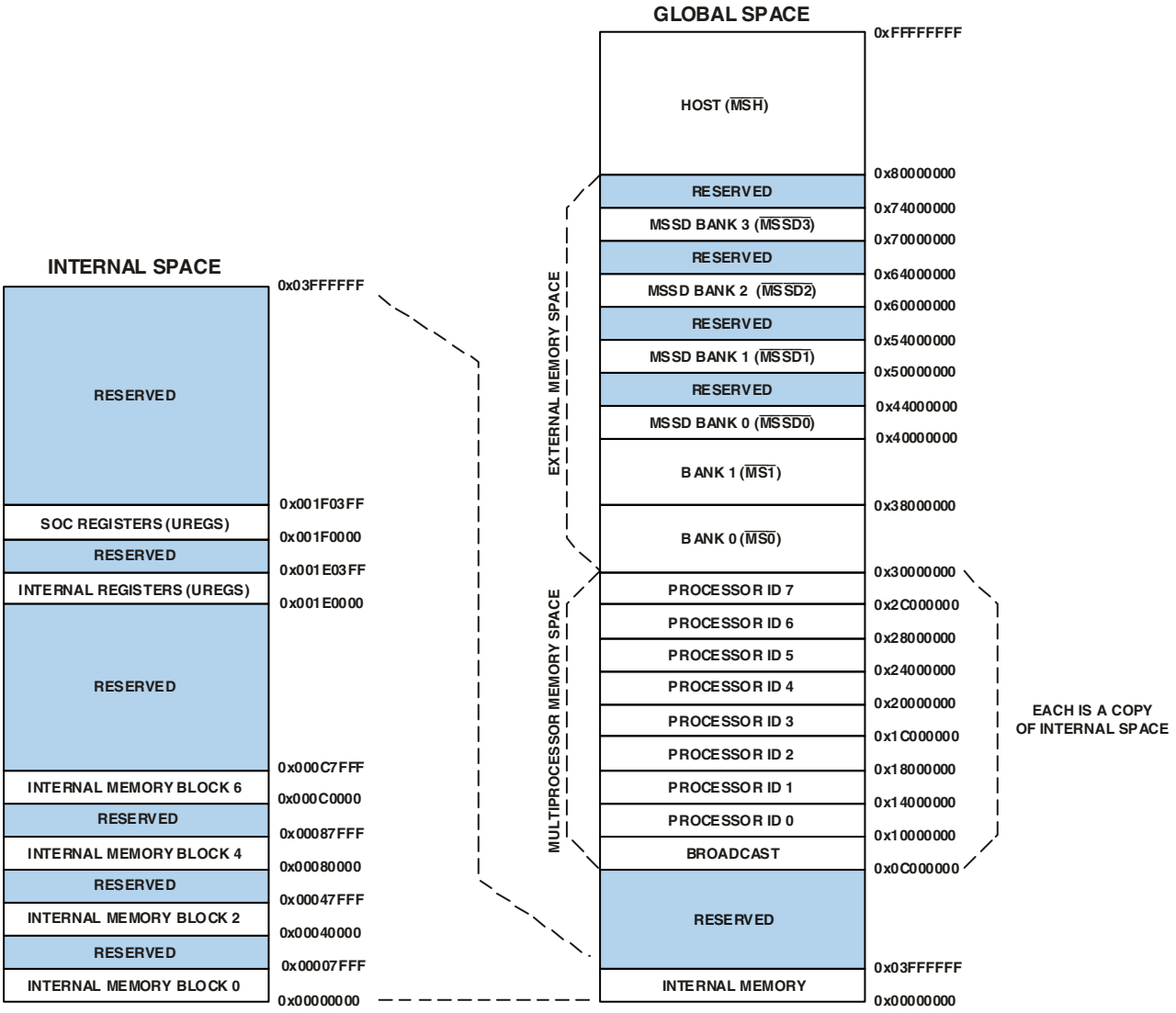

Figure 2. ADSP-TS203S Memory Map

The external port supports a unified address space (see Figure 2) that enables direct interprocessor accesses of each ADSP-TS203S processor's internal memory and registers. The processor's on-chip distributed bus arbitration logic provides simple, glueless connection for systems containing up to eight ADSP-TS203S processors and a host processor. Bus arbitration has a rotating priority. Bus lock supports indivisible read-modify-write sequences for semaphores. A bus fairness feature prevents one processor from holding the external bus too long.

The processor's two link ports provide a second path for interprocessor communications with throughput of 1G byte per second. The cluster bus provides 500M bytes per second throughput—with a total of 1.5G bytes per second interprocessor bandwidth.

SDRAM Controller

The SDRAM controller controls the processor's transfers of data to and from external synchronous DRAM (SDRAM) at a throughput of 32 bits per SCLK cycle using the external port and SDRAM control pins.

The SDRAM interface provides a glueless interface with standard SDRAMs—16M bits, 64M bits, 128M bits, 256M bits and 512M bits. The processor supports directly a maximum of four banks of 64M words × 32 bits of SDRAM. The SDRAM interface is mapped in external memory in each processor's unified memory map.

EPROM Interface

The processor can be configured to boot from an external 8-bit EPROM at reset through the external port. An automatic process (which follows reset) loads a program from the EPROM into internal memory. This process uses 16 wait cycles for each read access. During booting, the $\overline{\text{BMS}}$ pin functions as the EPROM chip select signal. The EPROM boot procedure uses DMA Channel 0, which packs the bytes into 32-bit instructions. Applications can also access the EPROM (write flash memories) during normal operation through DMA.

The EPROM or flash memory interface is not mapped in the processor's unified memory map. It is a byte address space limited to a maximum of 16M bytes (24 address bits). The EPROM or flash memory interface can be used after boot via a DMA.

DMA CONTROLLER

The ADSP-TS203S processor's on-chip DMA controller, with 10 DMA channels, provides zero-overhead data transfers without processor intervention. The DMA controller operates independently and invisibly to the processor's core, enabling DMA operations to occur while the processor's core continues to execute program instructions.

The DMA controller performs DMA transfers between internal memory, external memory, and memory-mapped peripherals; the internal memory of other DSPs on a common bus, a host processor, or link port I/O; between external memory and external peripherals or link port I/O; and between an external bus master and internal memory or link port I/O. The DMA controller performs the following DMA operations:

- External port block transfers. Four dedicated bidirectional DMA channels transfer blocks of data between the processor's internal memory and any external memory or memory-mapped peripheral on the external bus. Master mode and handshake mode protocols are supported.
- Link port transfers. Four dedicated DMA channels (two transmit and two receive) transfer quad-word data only between link ports and between a link port and internal or external memory. These transfers only use handshake mode protocol. DMA priority rotates between the two receive channels.
- AutoDMA transfers. Two dedicated unidirectional DMA channels transfer data received from an external bus master to internal memory or to link port I/O. These transfers only use slave mode protocol, and an external bus master must initiate the transfer.

The DMA controller provides these additional features:

- Flyby transfers. Flyby operations only occur through the external port (DMA channel 0) and do not involve the processor's core. The DMA controller acts as a conduit to transfer data from an external I/O device to external SDRAM memory. During a transaction, the processor relinquishes the external data bus; outputs addresses and memory selects ($\overline{\text{MSSD3–0}}$); outputs the $\overline{\text{IORD}}$, $\overline{\text{IOWR}}$, $\overline{\text{IOEN}}$, and $\overline{\text{RD}}$/$\overline{\text{WR}}$ strobes; and responds to ACK.
- DMA chaining. DMA chaining operations enable applications to automatically link one DMA transfer sequence to another for continuous transmission. The sequences can occur over different DMA channels and have different transmission attributes.
- Two-dimensional transfers. The DMA controller can access and transfer two-dimensional memory arrays on any DMA transmit or receive channel. These transfers are implemented with index, count, and modify registers for both the X and Y dimensions.

LINK PORTS (LVDS)

The processor's two full-duplex link ports each provide additional four-bit receive and four-bit transmit I/O capability, using low-voltage, differential-signal (LVDS) technology. With the ability to operate at a double data rate—latching data on both the rising and falling edges of the clock—running at 250 MHz, each link port can support up to 250M bytes per second per direction, for a combined maximum throughput of 1G byte per second.

The link ports provide an optional communications channel that is useful in multiprocessor systems for implementing point-to-point interprocessor communications. Applications can also use the link ports for booting.

Each link port has its own triple-buffered quad-word input and double-buffered quad-word output registers. The processor's core can write directly to a link port's transmit register and read

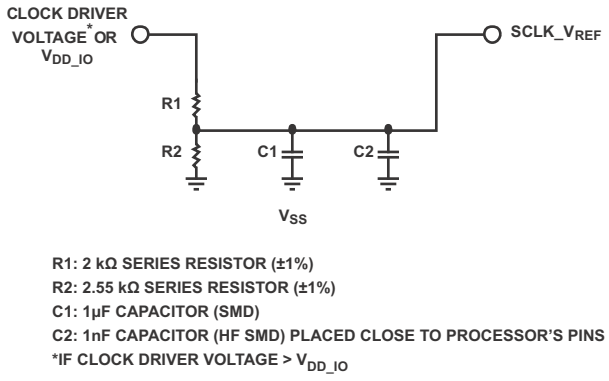

Figure 5. SCLK_V_{REF} Filtering Scheme

POWER DOMAINS

The ADSP-TS203S processor has separate power supply connections for internal logic (V_{DD}), analog circuits (V_{DD_A}), I/O buffer (V_{DD_IO}), and internal DRAM (V_{DD_DRAM}) power supply.

Note that the analog (V_{DD_A}) supply powers the clock generator PLLs. To produce a stable clock, systems must provide a clean power supply to power input V_{DD_A}. Designs must pay critical attention to bypassing the V_{DD_A} supply.

DEVELOPMENT TOOLS

The ADSP-TS203S processor is supported with a complete set of CROSSCORE® software and hardware development tools, including Analog Devices emulators and VisualDSP++® development environment. The same emulator hardware that supports other TigerSHARC processors also fully emulates the ADSP-TS203S processor.

The VisualDSP++ project management environment lets programmers develop and debug an application. This environment includes an easy to use assembler (which is based on an algebraic syntax), an archiver (librarian/library builder), a linker, a loader, a cycle-accurate instruction-level simulator, a C/C++ compiler, and a C/C++ run-time library that includes DSP and mathematical functions. A key point for theses tools is C/C++ code efficiency. The compiler has been developed for efficient translation of C/C++ code to DSP assembly. The processor has architectural features that improve the efficiency of compiled C/C++ code.

The VisualDSP++ debugger has a number of important features. Data visualization is enhanced by a plotting package that offers a significant level of flexibility. This graphical representation of user data enables the programmer to quickly determine the performance of an algorithm. As algorithms grow in complexity, this capability can have increasing significance on the designer's development schedule, increasing productivity. Statistical profiling enables the programmer to nonintrusively poll the processor as it is running the program. This feature, unique to VisualDSP++, enables the software developer to passively gather important code execution metrics without interrupting the real-time characteristics of the program. Essentially, the developer can identify bottlenecks in software quickly and efficiently. By using the profiler, the programmer can focus on those areas in the program that impact performance and take corrective action.

Debugging both C/C++ and assembly programs with the VisualDSP++ debugger, programmers can:

- View mixed C/C++ and assembly code (interleaved source and object information)
- Insert breakpoints
- Set conditional breakpoints on registers, memory, and stacks
- Trace instruction execution
- Perform linear or statistical profiling of program execution
- Fill, dump, and graphically plot the contents of memory
- Perform source level debugging
- Create custom debugger windows

The VisualDSP++ IDE lets programmers define and manage DSP software development. Its dialog boxes and property pages let programmers configure and manage all of the TigerSHARC processor development tools, including the color syntax highlighting in the VisualDSP++ editor. This capability permits programmers to:

- Control how the development tools process inputs and generate outputs
- Maintain a one-to-one correspondence with the tool's command line switches

The VisualDSP++ Kernel (VDK) incorporates scheduling and resource management tailored specifically to address the memory and timing constraints of DSP programming. These capabilities enable engineers to develop code more effectively, eliminating the need to start from the very beginning when developing new application code. The VDK features include threads, critical and unscheduled regions, semaphores, events, and device flags. The VDK also supports priority-based, preemptive, cooperative, and time-sliced scheduling approaches. In addition, the VDK was designed to be scalable. If the application does not use a specific feature, the support code for that feature is excluded from the target system.

Because the VDK is a library, a developer can decide whether to use it or not. The VDK is integrated into the VisualDSP++ development environment, but can also be used via standard command line tools. When the VDK is used, the development environment assists the developer with many error-prone tasks and assists in managing system resources, automating the generation of various VDK-based objects, and visualizing the system state, when debugging an application that uses the VDK.

VCSE is Analog Devices' technology for creating, using, and reusing software components (independent modules of substantial functionality) to quickly and reliably assemble software applications. It is also used for downloading components from the Web, dropping them into the application, and publish component archives from within VisualDSP++. VCSE supports component implementation in C/C++ or assembly language.

Table 12. Pin Definitions—Impedance Control, Drive Strength Control, and Regulator Enable

Signal	Type	Term	Description
CONTROLIMP0 CONTROLIMP1	I (pd) I (pu)	na na	Impedance Control. As shown in Table 13, the CONTROLIMP1–0 pins select between normal driver mode and A/D driver mode. When using normal mode (recommended), the output drive strength is set relative to maximum drive strength according to Table 14. When using A/D mode, the resistance control operates in the analog mode, where drive strength is continuously controlled to match a specific line impedance as shown in Table 14.
DS2, 0 DS1	I (pu) I (pd)	na	Digital Drive Strength Selection. Selected as shown in Table 14. For drive strength calculation, see Output Drive Currents on Page 34. The drive strength for some pins is preset, not controlled by the DS2–0 pins. The pins that are always at drive strength 7 (100%) include: $\overline{\text{CPA}}$, $\overline{\text{DPA}}$, TDO, $\overline{\text{EMU}}$, and $\overline{\text{RST\_OUT}}$. The drive strength for the ACK pin is always ×2 drive strength 7 (100%).
ENEDREG	I (pu)	V_{SS}	Connect the ENEDREG pin to V_{SS}. Connect the V_{DD_DRAM} pins to a properly decoupled DRAM power supply.

I = input; **A** = asynchronous; **O** = output; **OD** = open-drain output; **T** = three-state; **P** = power supply; **G** = ground; **pd** = internal pull-down 5 kΩ; **pu** = internal pull-up 5 kΩ; **pd_0** = internal pull-down 5 kΩ on processor ID = 0; **pu_0** = internal pull-up 5 kΩ on processor ID = 0; **pu_od_0** = internal pull-up 500 Ω on processor ID = 0; **pd_m** = internal pull-down 5 kΩ on processor bus master; **pu_m** = internal pull-up 5 kΩ on processor bus master; **pu_ad** = internal pull-up 40 kΩ. For more pull-down and pull-up information, see Electrical Characteristics on Page 21.

Term (termination of unused pins) column symbols: epd = external pull-down approximately 5 kΩ to V_{SS}; epu = external pull-up approximately 5 kΩ to V_{DD_IO}, nc = not connected; na = not applicable (always used); V_{DD_IO} = connect directly to V_{DD_IO}; V_{SS} = connect directly to V_{SS}

Table 13. Impedance Control Selection

CONTROLIMP1-0	Driver Mode
00 (recommended)	Normal
01	Reserved
10 (default)	A/D Mode
11	Reserved

Table 14. Drive Strength/Output Impedance Selection

DS2–0 Pins	Drive Strength[1]	Output Impedance[2]
000	Strength 0 (11.1%)	26 Ω
001	Strength 1 (23.8%)	32 Ω
010	Strength 2 (36.5%)	40 Ω
011	Strength 3 (49.2%)	50 Ω
100	Strength 4 (61.9%)	62 Ω
101 (default)	Strength 5 (74.6%)	70 Ω
110	Strength 6 (87.3%)	96 Ω
111	Strength 7 (100%)	120 Ω

[1] CONTROLIMP1 = 0, A/D mode disabled.
[2] CONTROLIMP1 = 1, A/D mode enabled.

Table 15. Pin Definitions—Power, Ground, and Reference

Signal	Type	Term	Description
V_{DD}	P	na	V_{DD} pins for internal logic.
V_{DD_A}	P	na	V_{DD} pins for analog circuits. Pay critical attention to bypassing this supply.
V_{DD_IO}	P	na	V_{DD} pins for I/O buffers.
V_{DD_DRAM}	P	na	V_{DD} pins for internal DRAM.
V_{REF}	I	na	Reference voltage defines the trip point for all input buffers, except SCLK, $\overline{RST\_IN}$, $\overline{POR\_IN}$, $\overline{IRQ3–0}$, FLAG3–0, $\overline{DMAR3–0}$, ID2–0, CONTROLIMP1–0, LxDATO3–0P/N, LxCLKOUTP/N, LxDATI3–0P/N, LxCLKINP/N, TCK, TDI, TMS, and $\overline{TRST}$. V_{REF} can be connected to a power supply or set by a voltage divider circuit as shown in Figure 4. For more information, see Filtering Reference Voltage and Clocks on Page 8.
SCLK_V_{REF}	I	na	System Clock Reference. Connect this pin to a reference voltage as shown in Figure 5. For more information, see Filtering Reference Voltage and Clocks on Page 8.
V_{SS}	G	na	Ground pins.
NC	—	nc	No Connect. Do not connect these pins to anything (not to any supply, signal, or each other). These pins are reserved and must be left unconnected.

I = input; **A** = asynchronous; **O** = output; **OD** = open-drain output; **T** = three-state; **P** = power supply; **G** = ground; **pd** = internal pull-down 5 kΩ; **pu** = internal pull-up 5 kΩ; **pd_0** = internal pull-down 5 kΩ on processor ID = 0; **pu_0** = internal pull-up 5 kΩ on processor ID = 0; **pu_od_0** = internal pull-up 500 Ω on processor ID = 0; **pd_m** = internal pull-down 5 kΩ on processor bus master; **pu_m** = internal pull-up 5 kΩ on processor bus master; **pu_ad** = internal pull-up 40 kΩ. For more pull-down and pull-up information, see Electrical Characteristics on Page 21.

Term (termination of unused pins) column symbols: epd = external pull-down approximately 5 kΩ to V_{SS}; epu = external pull-up approximately 5 kΩ to V_{DD_IO}, nc = not connected; na = not applicable (always used); V_{DD_IO} = connect directly to V_{DD_IO}; V_{SS} = connect directly to V_{SS}

STRAP PIN FUNCTION DESCRIPTIONS

Some pins have alternate functions at reset. Strap options set processor operating modes. During reset, the processor samples the strap option pins. Strap pins have an internal pull-up or pull-down for the default value. If a strap pin is not connected to an overdriving external pull-up, pull-down, or logic load, the processor samples the default value during reset. If strap pins are connected to logic inputs, a stronger external pull-up or pull-down may be required to ensure default value depending on leakage and/or low level input current of the logic load. To set a mode other than the default mode, connect the strap pin to a sufficiently stronger external pull-up or pull-down. Table 16 lists and describes each of the processor's strap pins.

Table 16. Pin Definitions—I/O Strap Pins

Signal	Type (at Reset)	On Pin …	Description
EBOOT	I (pd_0)	$\overline{BMS}$	EPROM Boot. 0 = boot from EPROM immediately after reset (default) 1 = idle after reset and wait for an external device to boot processor through the external port or a link port
IRQEN	I (pd)	$\overline{BM}$	Interrupt Enable. 0 = disable and set $\overline{IRQ3–0}$ interrupts to edge-sensitive after reset (default) 1 = enable and set $\overline{IRQ3–0}$ interrupts to level-sensitive immediately after reset
LINK_DWIDTH	I (pd)	TMR0E	Link Port Input Default Data Width. 0 = 1-bit (default) 1 = 4-bit

I = input; **A** = asynchronous; **O** = output; **OD** = open-drain output; **T** = three-state; **P** = power supply; **G** = ground; **pd** = internal pull-down 5 kΩ; **pu** = internal pull-up 5 kΩ; **pd_0** = internal pull-down 5 kΩ on processor ID = 0; **pu_0** = internal pull-up 5 kΩ on processor ID = 0; **pu_od_0** = internal pull-up 500 Ω on processor ID = 0; **pd_m** = internal pull-down 5 kΩ on processor bus master; **pu_m** = internal pull-up 5 kΩ on processor bus master; **pu_ad** = internal pull-up 40 kΩ. For more pull-down and pull-up information, see Electrical Characteristics on Page 21.

SPECIFICATIONS

Note that component specifications are subject to change with out notice. For information on link port electrical characteristics, see Link Port Low Voltage, Differential-Signal (LVDS) Electrical Characteristics, and Timing on Page 29.

OPERATING CONDITIONS

Parameter	Description	Test Conditions	Grade[1]	Min	Typ	Max	Unit
V_{DD}	Internal Supply Voltage	@ CCLK = 500 MHz	050	1.00	1.05	1.10	V
V_{DD_A}	Analog Supply Voltage	@ CCLK = 500 MHz	050	1.00	1.05	1.10	V
V_{DD_IO}	I/O Supply Voltage		(all)	2.38	2.50	2.63	V
V_{DD_DRAM}	Internal DRAM Supply Voltage	@ CCLK = 500 MHz	050	1.425	1.500	1.575	V
T_{CASE}	Case Operating Temperature		A	–40		+85	°C
T_{CASE}	Case Operating Temperature		B	0		+85	°C
V_{IH1}	High Level Input Voltage[2, 3]	@ V_{DD}, V_{DD_IO} = Max	(all)	1.7		3.63	V
V_{IH2}	High Level Input Voltage[3, 4]	@ V_{DD}, V_{DD_IO} = Max	(all)	1.9		3.63	V
V_{IL}	Low Level Input Voltage[3, 5]	@ V_{DD}, V_{DD_IO} = Min	(all)	–0.33		+0.8	V
I_{DD}	V_{DD} Supply Current, Typical Activity[6]	@ CCLK = 500 MHz, V_{DD} = 1.05 V, T_{CASE} = 25°C	050		2.06		A
I_{DD_A}	V_{DD_A} Supply Current, Typical Activity	@ CCLK = 500 MHz, V_{DD} = 1.05 V, T_{CASE} = 25°C	050		20	50	mA
I_{DD_IO}	V_{DD_IO} Supply Current, Typical Activity[6]	@ SCLK = 62.5 MHz, V_{DD_IO} = 2.5 V, T_{CASE} = 25°C	(all)		0.15		A
I_{DD_DRAM}	V_{DD_DRAM} Supply Current, Typical Activity[6]	@ CCLK = 500 MHz, V_{DD_DRAM} = 1.5 V, T_{CASE} = 25°C	050		0.25	0.40	A
V_{REF}	Voltage Reference		(all)	(V_{DD_IO} × 0.56) ±5%			V
SCLK_V_{REF}	Voltage Reference		(all)	(V_{CLOCK_DRIVE} × 0.56) ±5%			V

[1] Specifications vary for different grades (for example, SABP–060, SABP–050, SWBP–050). For more information on part grades, see Ordering Guide on Page 47.

[2] V_{IH1} specification applies to input and bidirectional pins: SCLKRAT2–0, SCLK, ADDR31–0, DATA63–0, $\overline{RD}$, $\overline{WRL}$, ACK, $\overline{BRST}$, $\overline{BR7–0}$, $\overline{BOFF}$, $\overline{HBR}$, $\overline{HBG}$, $\overline{MSSD3–0}$, $\overline{RAS}$, $\overline{CAS}$, SDCKE, $\overline{SDWE}$, TCK, FLAG3–0, DS2–0, ENEDREG.

[3] Values represent dc case. During transitions, the inputs may overshoot or undershoot to the voltage shown in Table 18, based on the transient duty cycle. The dc case is equivalent to 100% duty cycle.

[4] V_{IH2} specification applies to input and bidirectional pins: TDI, TMS, $\overline{TRST}$, CIMP1–0, ID2–0, $\overline{LxBCMPI}$, LxACKI, $\overline{POR\_IN}$, $\overline{RST\_IN}$, $\overline{IRQ3–0}$, $\overline{CPA}$, $\overline{DPA}$, $\overline{DMAR3–0}$.

[5] Applies to input and bidirectional pins.

[6] For details on internal and external power calculation issues, including other operating conditions, see *EE-170, Estimating Power for the ADSP-TS203S*.

Table 18. Maximum Duty Cycle for Input Transient Voltage

V_{IN} Max (V)[1]	V_{IN} Min (V)[1]	Maximum Duty Cycle[2]
+3.63	–0.33	100%
+3.64	–0.34	90%
+3.70	–0.40	50%
+3.78	–0.48	30%
+3.86	–0.56	17%
+3.93	–0.63	10%

[1] The individual values cannot be combined for analysis of a single instance of overshoot or undershoot. The worst case observed value must fall within one of the voltages specified and the total duration of the overshoot or undershoot (exceeding the 100% case) must be less than or equal to the corresponding duty cycle.

[2] Duty cycle refers to the percentage of time the signal exceeds the value for the 100% case. This is equivalent to the measured duration of a single instance of overshoot or undershoot as a percentage of the period of occurrence. The practical worst case for period of occurrence for either overshoot or undershoot is 2 × t_{SCLK}.

PACKAGE INFORMATION

The information presented in Figure 6 provide details about the package branding for the ADSP-TS203S processors. For a complete listing of product availability, see Ordering Guide on Page 47.

Figure 6. Typical Package Brand

Table 19. Package Brand Information

Brand Key	Field Description
t	Temperature Range
pp	Package Type
Z	Lead Free Option (optional)
ccc	See Ordering Guide
tppzccc	Silicon Lot Number
2.0	Silicon Revision
yyww	Date Code
vvvvvv	Assembly Lot Code

ABSOLUTE MAXIMUM RATINGS

Stresses greater than those listed in Table 20 may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 20. Absolute Maximum Ratings

Parameter	Rating
Internal (Core) Supply Voltage (V_{DD})	–0.3 V to +1.4 V
Analog (PLL) Supply Voltage (V_{DD_A})	–0.3 V to +1.4 V
External (I/O) Supply Voltage (V_{DD_IO})	–0.3 V to +3.5 V
External (DRAM) Supply Voltage (V_{DD_DRAM})	–0.3 V to +2.1 V
Input Voltage[1]	–0.63 V to +3.93 V
Output Voltage Swing	–0.5 V to V_{DD_IO} + 0.5 V
Storage Temperature Range	–65°C to +150°C

[1] Applies to 10% transient duty cycle. For other duty cycles see Table 18.

ESD SENSITIVITY

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Table 25. Power-Up Timing[1]

Parameter		Min	Max	Unit
Timing Requirement				
t_{VDD_DRAM}	V_{DD_DRAM} Stable After V_{DD}, V_{DD_A}, V_{DD_IO} Stable	>0		ms

[1] For information about power supply sequencing and monitoring solutions, please visit www.analog.com/sequencing.

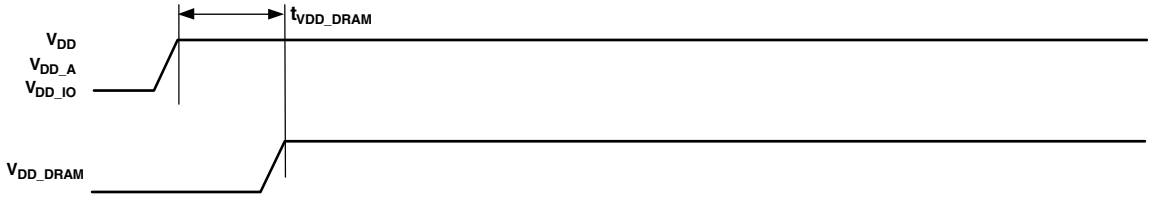

Figure 10. Power-Up Timing

Table 26. Power-Up Reset Timing

Parameter		Min	Max	Unit
Timing Requirements				
$t_{RST\_IN\_PWR}$	$\overline{RST\_IN}$ Deasserted After V_{DD}, V_{DD_A}, V_{DD_IO}, V_{DD_DRAM}, SCLK, and Static/ Strap Pins Stable	2		ms
$t_{TRST\_IN\_PWR}$[1]	$\overline{TRST}$ Asserted During Power-Up Reset	$100 \times t_{SCLK}$		ns
Switching Characteristic				
$t_{RST\_OUT\_PWR}$	$\overline{RST\_OUT}$ Deasserted After $\overline{RST\_IN}$ Deasserted	1.5		ms

[1] Applies after V_{DD}, V_{DD_A}, V_{DD_IO}, V_{DD_DRAM}, and SCLK are stable and before $\overline{RST\_IN}$ deasserted.

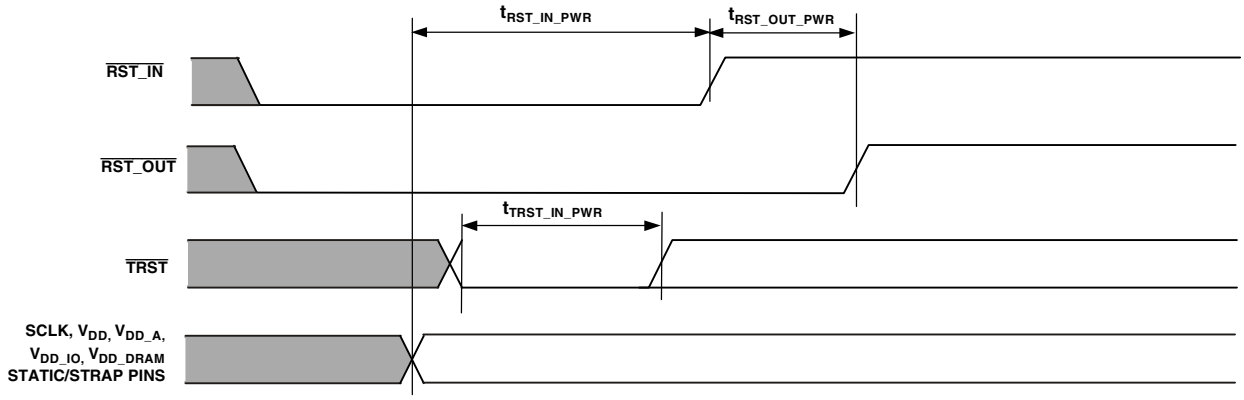

Figure 11. Power-Up Reset Timing

Table 27. Normal Reset Timing

Parameter		Min	Max	Unit
Timing Requirements				
t_{RST_IN}	$\overline{RST\_IN}$ Asserted	2		ms
t_{STRAP}	$\overline{RST\_IN}$ Deasserted After Strap Pins Stable	1.5		ms
Switching Characteristic				
t_{RST_OUT}	$\overline{RST\_OUT}$ Deasserted After $\overline{RST\_IN}$ Deasserted	1.5		ms

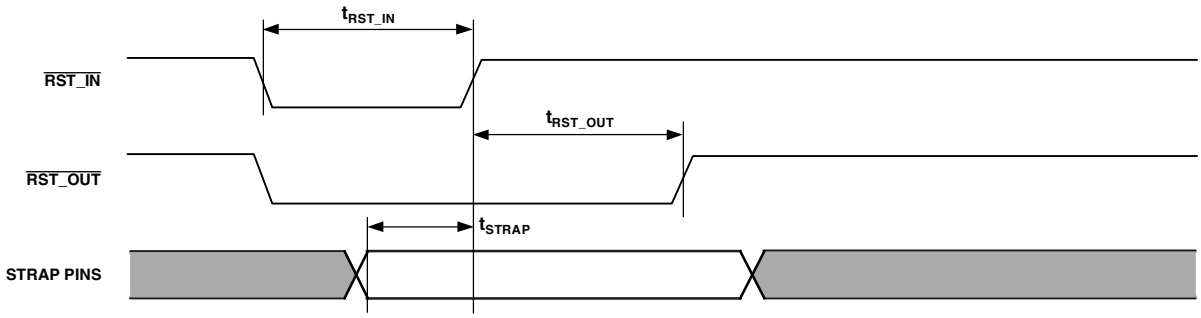

Figure 12. Normal Reset Timing

Table 28. On-Chip DRAM Refresh[1]

Parameter		Min	Max	Unit
Timing Requirement				
t_{REF}	On-chip DRAM Refresh Period		1.56	µs

[1] For more information on setting the refresh rate for the on-chip DRAM, refer to the *ADSP-TS201 TigerSHARC Processor Programming Reference*.

Table 29. AC Signal Specifications

(All values in this table are in nanoseconds.)

Name	Description	Input Setup (Min)	Input Hold (Min)	Output Valid (Max)	Output Hold (Min)	Output Enable (Min)[1]	Output Disable (Max)[1]	Reference Clock
ADDR31–0	External Address Bus	1.5	0.5	4.0	1.0	1.15	2.0	SCLK
DATA31–0	External Data Bus	1.5	0.5	4.0	1.0	1.15	2.0	SCLK
$\overline{\text{MSH}}$	Memory Select HOST Line	—	—	4.0	1.0	1.15	2.0	SCLK
$\overline{\text{MSSD3–0}}$	Memory Select SDRAM Lines	1.5	0.5	4.0	1.0	1.0	2.0	SCLK
$\overline{\text{MS1–0}}$	Memory Select for Static Blocks	—	—	4.0	1.0	1.15	2.0	SCLK
$\overline{\text{RD}}$	Memory Read	1.5	0.5	4.0	1.0	1.15	2.0	SCLK
$\overline{\text{WRL}}$	Write Low Word	1.5	0.5	4.0	1.0	1.15	2.0	SCLK
ACK	Acknowledge for Data High to Low	1.5	0.5	3.6	1.0	1.15	2.0	SCLK
	Acknowledge for Data Low to High	1.5	0.5	4.2	0.9	1.15	2.0	SCLK
SDCKE	SDRAM Clock Enable	1.5	0.5	4.0	1.0	1.15	2.0	SCLK
$\overline{\text{RAS}}$	Row Address Select	1.5	0.5	4.0	1.0	1.15	2.0	SCLK
$\overline{\text{CAS}}$	Column Address Select	1.5	0.5	4.0	1.0	1.15	2.0	SCLK
$\overline{\text{SDWE}}$	SDRAM Write Enable	1.5	0.5	4.0	1.0	1.15	2.0	SCLK
LDQM	Low Word SDRAM Data Mask	—	—	4.0	1.0	1.15	2.0	SCLK
SDA10	SDRAM ADDR10	—	—	4.0	1.0	1.15	2.0	SCLK
$\overline{\text{HBR}}$	Host Bus Request	1.5	0.5	—	—	—	—	SCLK
$\overline{\text{HBG}}$	Host Bus Grant	1.5	0.5	4.0	1.0	1.15	2.0	SCLK
$\overline{\text{BOFF}}$	Back Off Request	1.5	0.5	—	—	—	—	SCLK
$\overline{\text{BUSLOCK}}$	Bus Lock	—	—	4.0	1.0	1.15	2.0	SCLK
$\overline{\text{BRST}}$	Burst Pin	1.5	0.5	4.0	1.0	1.15	2.0	SCLK
$\overline{\text{BR7–0}}$	Multiprocessing Bus Request Pins	1.5	0.5	4.0	1.0	—	—	SCLK
$\overline{\text{BM}}$	Bus Master Debug Aid Only	—	—	4.0	1.0	—	—	SCLK
$\overline{\text{IORD}}$	I/O Read Pin	—	—	4.0	1.0	1.0	2.0	SCLK
$\overline{\text{IOWR}}$	I/O Write Pin	—	—	4.0	1.0	1.15	2.0	SCLK
$\overline{\text{IOEN}}$	I/O Enable Pin	—	—	4.0	1.0	1.15	2.0	SCLK
$\overline{\text{CPA}}$	Core Priority Access High to Low	1.5	0.5	4.0	1.0	0.75	2.0	SCLK
	Core Priority Access Low to High	1.5	0.5	29.5	2.0	0.75	2.0	SCLK
$\overline{\text{DPA}}$	DMA Priority Access High to Low	1.5	0.5	4.0	1.0	0.75	2.0	SCLK
	DMA Priority Access Low to High	1.5	0.5	29.5	2.0	0.75	2.0	SCLK
$\overline{\text{BMS}}$	Boot Memory Select	—	—	4.0	1.0	1.15	2.0	SCLK
FLAG3–0[2]	FLAG Pins	—	—	4.0	1.0	1.15	2.0	SCLK
$\overline{\text{RST\_IN}}$[3, 4]	Global Reset Pin	1.5	2.5	—	—	—	—	SCLK[5]
TMS	Test Mode Select (JTAG)	1.5	0.5	—	—	—	—	TCK
TDI	Test Data Input (JTAG)	1.5	0.5	—	—	—	—	TCK
TDO	Test Data Output (JTAG)	—	—	4.0	1.0	0.75	2.0	TCK[6]
$\overline{\text{TRST}}$[3, 4]	Test Reset (JTAG)	1.5	0.5	—	—	—	—	TCK
$\overline{\text{EMU}}$[7]	Emulation High to Low	—	—	5.5	2.0	1.15	4.0	TCK or SCLK
ID2–0[8]	Static Pins—Must Be Constant	—	—	—	—	—	—	—
CONTROLIMP1–0[8]	Static Pins—Must Be Constant	—	—	—	—	—	—	—
DS2–0[8]	Static Pins—Must Be Constant	—	—	—	—	—	—	—
SCLKRAT2–0[8]	Static Pins—Must Be Constant	—	—	—	—	—	—	—

Table 29. AC Signal Specifications (Continued)

(All values in this table are in nanoseconds.)

Name	Description	Input Setup (Min)	Input Hold (Min)	Output Valid (Max)	Output Hold (Min)	Output Enable (Min)[1]	Output Disable (Max)[1]	Reference Clock
ENEDREG	Static Pins—Must Be Connected to V_{SS}	—	—	—	—	—	—	—
STRAP SYS[9, 10]	Strap Pins	1.5	0.5	—	—	—	—	SCLK
JTAG SYS[11, 12]	JTAG System Pins	+2.5	+10.0	+12.0	–1.0	—	—	TCK

[1] The external port protocols employ bus IDLE cycles for bus mastership transitions as well as slave address boundary crossings to avoid any potential bus contention. The apparent driver overlap, due to output disables being larger than output enables, is not actual.
[2] For input specifications on FLAG3–0 pins, see Table 21.
[3] These input pins are asynchronous and therefore do not need to be synchronized to a clock reference.
[4] For additional requirement details, see Reset and Booting on Page 8.
[5] $\overline{RST\_IN}$ clock reference is the falling edge of SCLK.
[6] TDO output clock reference is the falling edge of TCK.
[7] Reference clock depends on function.
[8] These pins may change only during reset; recommend connecting it to V_{DD_IO}/V_{SS}.
[9] STRAP pins include: $\overline{BMS}$, $\overline{BM}$, $\overline{BUSLOCK}$, TMR0E, $\overline{L1BCMPO}$, TM2, and TM3.
[10] Specifications applicable during reset only.
[11] JTAG system pins include: $\overline{RST\_IN}$, $\overline{RST\_OUT}$, $\overline{POR\_IN}$, $\overline{IRQ3–0}$, $\overline{DMAR3–0}$, $\overline{HBR}$, $\overline{BOFF}$, $\overline{MS1–0}$, $\overline{MSH}$, SDCKE, LDQM, $\overline{BMS}$, $\overline{IOWR}$, $\overline{IORD}$, $\overline{BM}$, $\overline{EMU}$, SDA10, $\overline{IOEN}$, $\overline{BUSLOCK}$, TMR0E, DATA31–0, ADDR31–0, $\overline{RD}$, $\overline{WRL}$, $\overline{BRST}$, $\overline{MSSD3–0}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{SDWE}$, $\overline{HBG}$, $\overline{BR7–0}$, FLAG3–0, L0DATOP3–0, L0DATON3–0, L1DATOP3–0, L1DATON3–0, L0CLKOUTP, L0CLKOUTN, L1CLKOUTP, L1CLKOUTN, L0ACKI, L1ACKI, L0DATIP3–0, L0DATIN3–0, L1DATIP3–0, L1DATIN3–0, L0CLKINP, L0CLKINN, L1CLKINP, L1CLKINN, L0ACKO, L1ACKO, ACK, $\overline{CPA}$, $\overline{DPA}$, $\overline{L0BCMPO}$, $\overline{L1BCMPO}$, $\overline{L0BCMPI}$, $\overline{L1BCMPI}$, ID2–0, CTRL_IMPD1–0, SCLKRAT2–0, DS2–0, ENEDREG, TM2, TM3, TM4.
[12] JTAG system output timing clock reference is the falling edge of TCK.

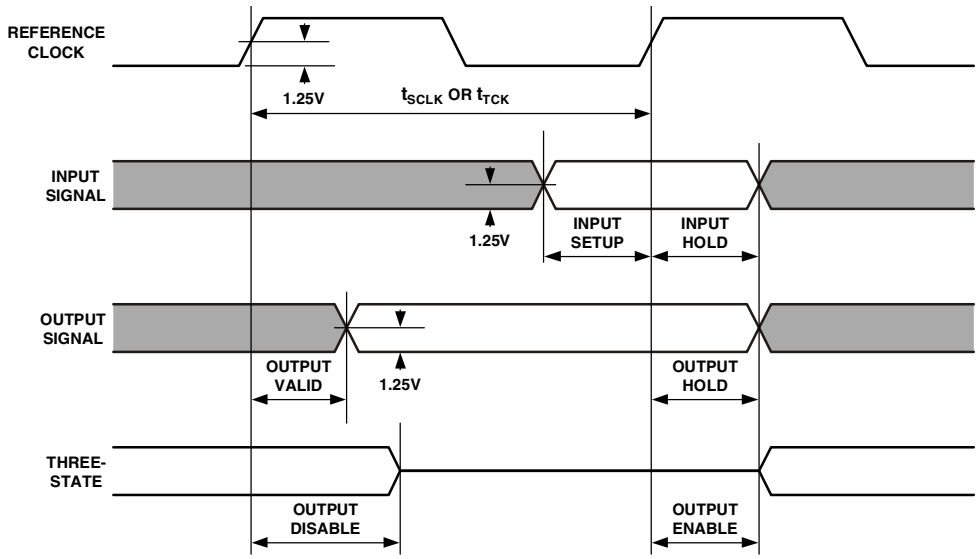

Figure 13. General AC Parameters Timing

Link Port—Data Out Timing

Table 32 with Figure 16, Figure 17, Figure 18, Figure 19, Figure 20, and Figure 21 provide the data out timing for the LVDS link ports.

Table 32. Link Port—Data Out Timing

Parameter	Description	Min	Max	Unit
Outputs				
t_{REO}	Rising Edge (Figure 17)		350	ps
t_{FEO}	Falling Edge (Figure 17)		350	ps
t_{LCLKOP}	LxCLKOUT Period (Figure 16)	Greater of 4.0 or $0.9 \times LCR \times t_{CCLK}$[1, 2, 3]	Smaller of 12.5 or $1.1 \times LCR \times t_{CCLK}$[1, 2, 3]	ns
t_{LCLKOH}	LxCLKOUT High (Figure 16)	$0.4 \times t_{LCLKOP}$[1]	$0.6 \times t_{LCLKOP}$[1]	ns
t_{LCLKOL}	LxCLKOUT Low (Figure 16)	$0.4 \times t_{LCLKOP}$[1]	$0.6 \times t_{LCLKOP}$[1]	ns
t_{COJT}	LxCLKOUT Jitter (Figure 16)		±150[4, 5, 6]	ps
			±250[7]	ps
t_{LDOS}	LxDATO Output Setup (Figure 18)	$0.25 \times LCR \times t_{CCLK} - 0.10 \times t_{CCLK}$[1, 4, 8]		ns
		$0.25 \times LCR \times t_{CCLK} - 0.15 \times t_{CCLK}$[1, 5, 6, 8]		ns
		$0.25 \times LCR \times t_{CCLK} - 0.30 \times t_{CCLK}$[1, 7, 8]		ns
t_{LDOH}	LxDATO Output Hold (Figure 18)	$0.25 \times LCR \times t_{CCLK} - 0.10 \times t_{CCLK}$[1, 4, 8]		ns
		$0.25 \times LCR \times t_{CCLK} - 0.15 \times t_{CCLK}$[1, 5, 6, 8]		ns
		$0.25 \times LCR \times t_{CCLK} - 0.30 \times t_{CCLK}$[1, 7, 8]		ns
t_{LACKID}	Delay from LxACKI rising edge to first transmission clock edge (Figure 19)		$16 \times LCR \times t_{CCLK}$[1, 2]	ns
t_{BCMPOV}	$\overline{\text{LxBCMPO}}$ Valid (Figure 19)		$2 \times LCR \times t_{CCLK}$[1, 2]	ns
t_{BCMPOH}	$\overline{\text{LxBCMPO}}$ Hold (Figure 20)	$3 \times TSW - 0.5$[1, 9]		ns
Inputs				
t_{LACKIS}	LxACKI low setup to guarantee that the transmitter stops transmitting (Figure 20)			
	LxACKI high setup to guarantee that the transmitter continues its transmission without any interruption (Figure 21)	$16 \times LCR \times t_{CCLK}$[1, 2]		ns
t_{LACKIH}	LxACKI High Hold Time (Figure 21)	0.51		ns

[1] Timing is relative to the 0 differential voltage (V_{OD} = 0).
[2] LCR (link port clock ratio) = 1, 1.5, 2, or 4. t_{CCLK} is the core period.
[3] For the cases of t_{LCLKOP} = 4.0 ns and t_{LCLKOP} = 12.5 ns, the effect of t_{COJT} specification on output period must be considered.
[4] LCR = 1.
[5] LCR = 1.5.
[6] LCR = 2.
[7] LCR = 4.
[8] The t_{LDOS} and t_{LDOH} values include LCLKOUT jitter.
[9] TSW is a short-word transmission period. For a 4-bit link, it is 2 × LCR × t_{CCLK}. For a 1-bit link, it is 8 × LCR × t_{CCLK} ns.

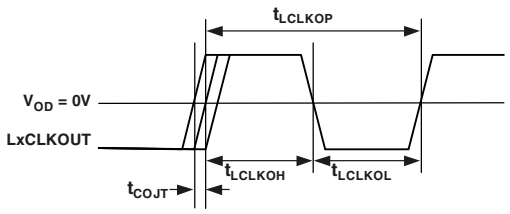

Figure 16. Link Ports—Output Clock

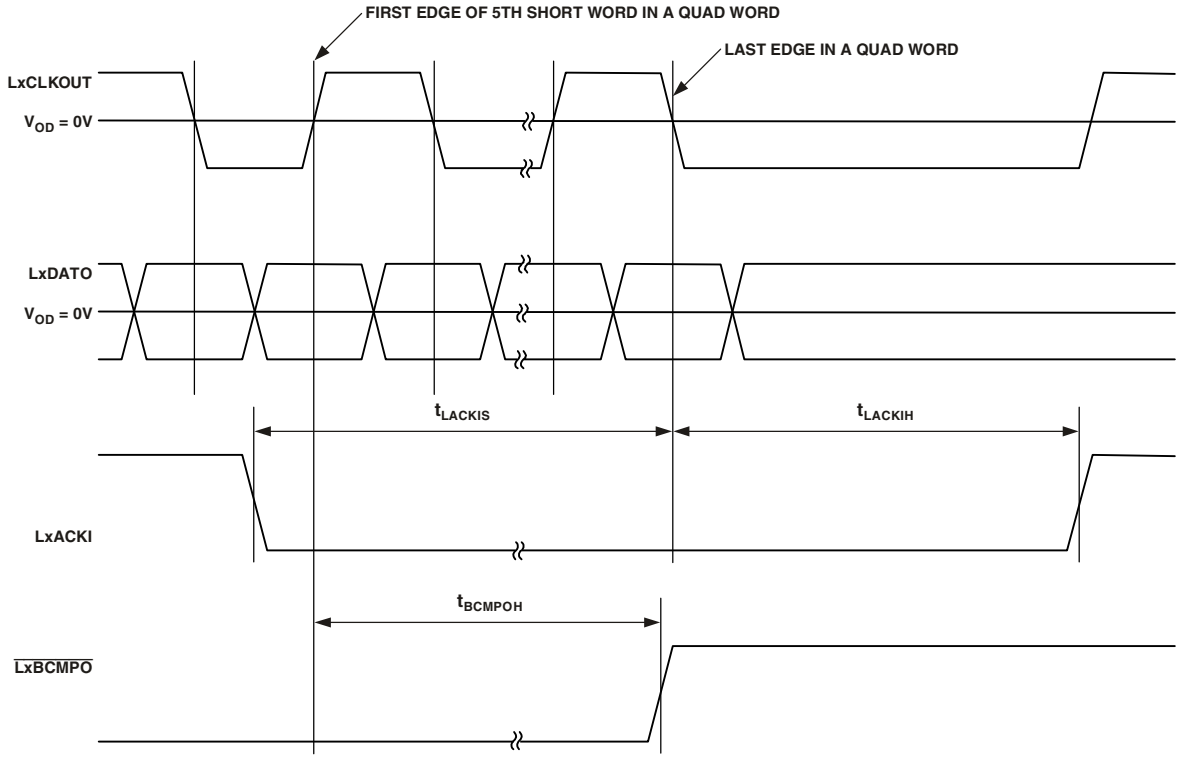

Figure 20. Link Ports—Transmission End and Stops

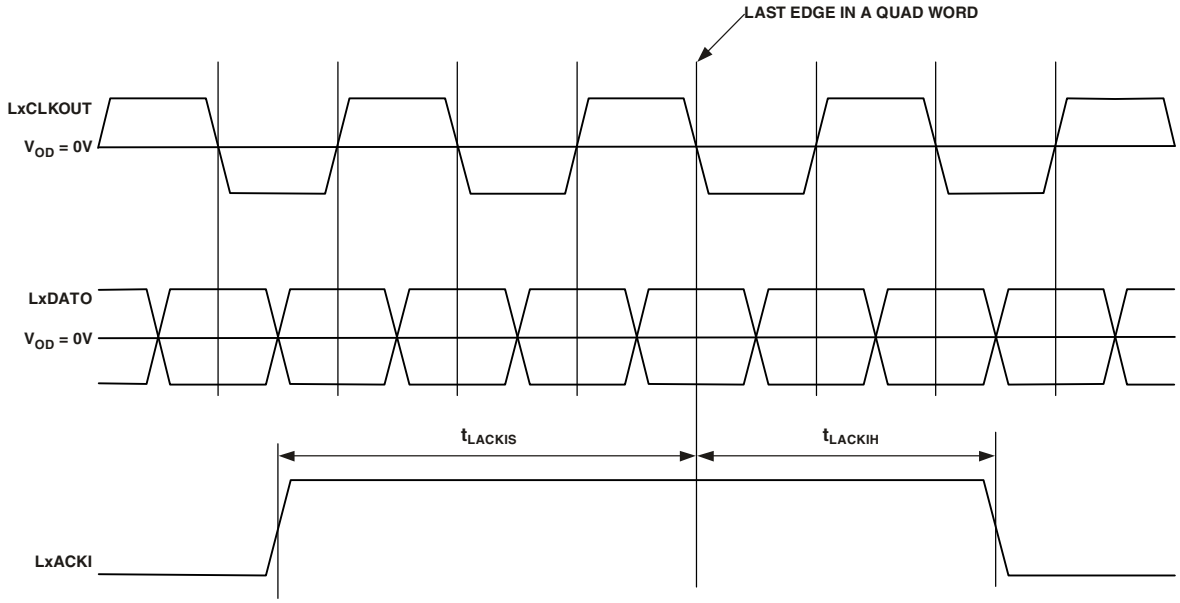

Figure 21. Link Ports—Back to Back Transmission

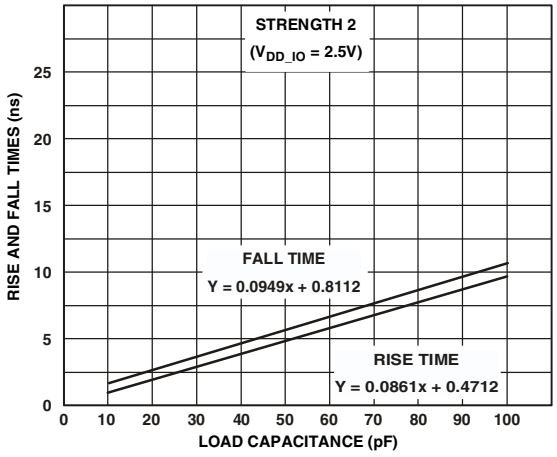

Figure 37. Typical Output Rise and Fall Time (10% to 90%, V_{DD_IO} = 2.5 V) vs. Load Capacitance at Strength 2

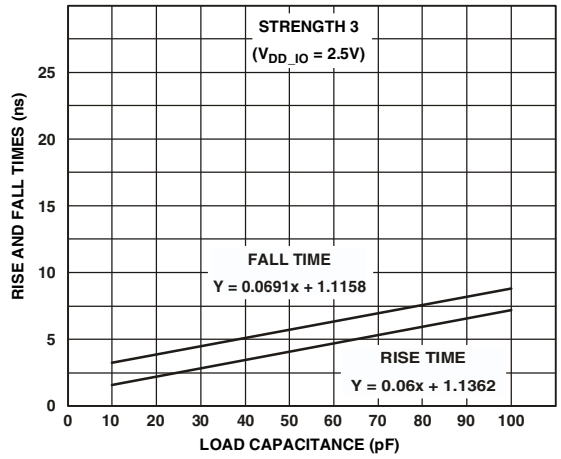

Figure 38. Typical Output Rise and Fall Time (10% to 90%, V_{DD_IO} = 2.5 V) vs. Load Capacitance at Strength 3

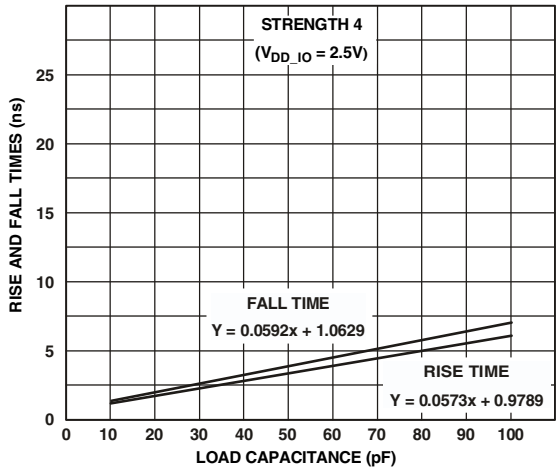

Figure 39. Typical Output Rise and Fall Time (10% to 90%, V_{DD_IO} = 2.5 V) vs. Load Capacitance at Strength 4

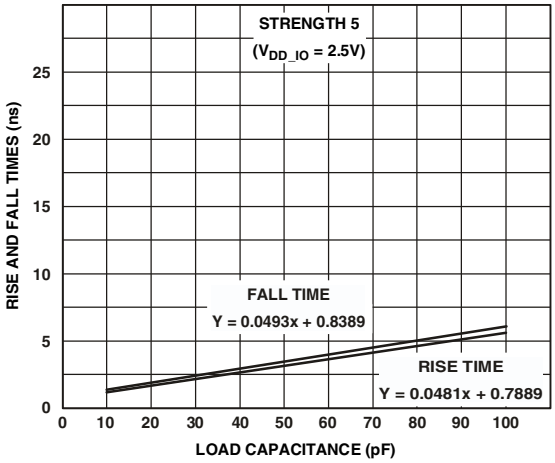

Figure 40. Typical Output Rise and Fall Time (10% to 90%, V_{DD_IO} = 2.5 V) vs. Load Capacitance at Strength 5

Table 35. 576-Ball (25 mm × 25 mm) BGA_ED Ball Assignments (Continued)

Ball No.	Signal Name	Ball No.	Signal Name	Ball No.	Signal Name	Ball No.	Signal Name
N1	ID0	P1	SCLK	R1	V_{SS}	T1	$\overline{RST\_IN}$
N2	V_{SS}	P2	SCLK_VREF	R2	NC (SCLK)[1]	T2	SCLKRAT2
N3	V_{DD_A}	P3	V_{SS}	R3	NC (SCLK_VREF)[1]	T3	$\overline{BR4}$
N4	V_{DD_A}	P4	$\overline{BM}$	R4	$\overline{BR7}$	T4	DS0
N5	V_{DD_IO}	P5	V_{DD_IO}	R5	V_{DD_IO}	T5	V_{SS}
N6	V_{DD}	P6	V_{DD}	R6	V_{DD}	T6	V_{DD}
N7	V_{DD}	P7	V_{DD}	R7	V_{DD}	T7	V_{DD}
N8	V_{SS}	P8	V_{SS}	R8	V_{SS}	T8	V_{SS}
N9	V_{SS}	P9	V_{SS}	R9	V_{SS}	T9	V_{SS}
N10	V_{SS}	P10	V_{SS}	R10	V_{SS}	T10	V_{SS}
N11	V_{SS}	P11	V_{SS}	R11	V_{SS}	T11	V_{SS}
N12	V_{SS}	P12	V_{SS}	R12	V_{SS}	T12	V_{SS}
N13	V_{SS}	P13	V_{SS}	R13	V_{SS}	T13	V_{SS}
N14	V_{SS}	P14	V_{SS}	R14	V_{SS}	T14	V_{SS}
N15	V_{SS}	P15	V_{SS}	R15	V_{SS}	T15	V_{SS}
N16	V_{SS}	P16	V_{SS}	R16	V_{SS}	T16	V_{SS}
N17	V_{SS}	P17	V_{SS}	R17	V_{SS}	T17	V_{SS}
N18	V_{DD}	P18	V_{DD_DRAM}	R18	V_{DD_DRAM}	T18	V_{DD}
N19	V_{DD}	P19	V_{DD_DRAM}	R19	V_{DD_DRAM}	T19	V_{DD}
N20	V_{DD_IO}	P20	V_{DD_IO}	R20	V_{DD_IO}	T20	V_{SS}
N21	L0DATO2_N	P21	L0DATO1_N	R21	NC	T21	L1DATI0_N
N22	L0DATO2_P	P22	L0DATO1_P	R22	V_{SS}	T22	L1DATI0_P
N23	L0CLKON	P23	L0DATO0_N	R23	$\overline{L0BCMPO}$	T23	L1ACKO
N24	L0CLKOP	P24	L0DATO0_P	R24	L0ACKI	T24	$\overline{L1BCMPI}$

Table 35. 576-Ball (25 mm × 25 mm) BGA_ED Ball Assignments (Continued)

Ball No.	Signal Name	Ball No.	Signal Name	Ball No.	Signal Name	Ball No.	Signal Name
U1	$\overline{\text{MSSD0}}$	V1	$\overline{\text{MSSD2}}$	W1	CONTROLIMP0	Y1	$\overline{\text{EMU}}$
U2	$\overline{\text{RST\_OUT}}$	V2	DS2	W2	ENEDREG	Y2	TCK
U3	ID2	V3	$\overline{\text{POR\_IN}}$	W3	TDI	Y3	TMR0E
U4	DS1	V4	CONTROLIMP1	W4	TDO	Y4	FLAG3
U5	V_{DD_IO}	V5	V_{SS}	W5	V_{DD_IO}	Y5	V_{SS}
U6	V_{DD}	V6	V_{DD}	W6	V_{DD}	Y6	V_{DD_IO}
U7	V_{DD}	V7	V_{DD}	W7	V_{DD}	Y7	V_{SS}
U8	V_{SS}	V8	V_{DD}	W8	V_{DD}	Y8	V_{DD_IO}
U9	V_{SS}	V9	V_{DD}	W9	V_{DD}	Y9	V_{SS}
U10	V_{DD}	V10	V_{DD}	W10	V_{DD}	Y10	V_{DD_IO}
U11	V_{DD_DRAM}	V11	V_{DD_DRAM}	W11	V_{DD_DRAM}	Y11	V_{DD_IO}
U12	V_{SS}	V12	V_{DD_DRAM}	W12	V_{DD_DRAM}	Y12	V_{DD_IO}
U13	V_{SS}	V13	V_{DD}	W13	V_{DD}	Y13	V_{DD_IO}
U14	V_{SS}	V14	V_{DD}	W14	V_{DD}	Y14	V_{DD_IO}
U15	V_{SS}	V15	V_{DD_DRAM}	W15	V_{DD_DRAM}	Y15	V_{DD_IO}
U16	V_{SS}	V16	V_{DD_DRAM}	W16	V_{DD_DRAM}	Y16	V_{SS}
U17	V_{SS}	V17	V_{DD}	W17	V_{DD}	Y17	V_{DD_IO}
U18	V_{DD}	V18	V_{DD}	W18	V_{DD}	Y18	V_{SS}
U19	V_{DD}	V19	V_{DD}	W19	V_{DD}	Y19	V_{DD_IO}
U20	V_{DD_IO}	V20	V_{DD_IO}	W20	V_{DD_IO}	Y20	V_{SS}
U21	L1CLKINN	V21	L1DATI3_N	W21	L1CLKON	Y21	L1DATO1_N
U22	L1CLKINP	V22	L1DATI3_P	W22	L1CLKOP	Y22	L1DATO1_P
U23	L1DATI1_N	V23	L1DATI2_N	W23	L1DATO3_N	Y23	L1DATO2_N
U24	L1DATI1_P	V24	L1DATI2_P	W24	L1DATO3_P	Y24	L1DATO2_P

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