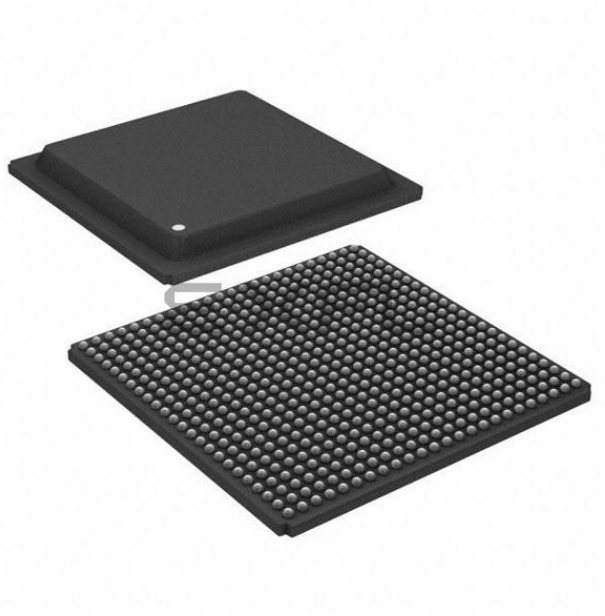

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	Fixed/Floating Point
Interface	Host Interface, Link Port, Multi-Processor
Clock Rate	500MHz
Non-Volatile Memory	External
On-Chip RAM	512kB
Voltage - I/O	2.50V
Voltage - Core	1.05V
Operating Temperature	0°C ~ 85°C (TC)
Mounting Type	Surface Mount
Package / Case	576-BBGA
Supplier Device Package	576-BGA-ED (25x25)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/adsp-ts203sbbpz050

ADSP-TS203S* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- EZ-KIT Lite Evaluation Kit for ADSP-TS201S Processor
- USB-Based Emulator and High Performance USB-Based Emulator

DOCUMENTATION

Application Notes

- AN-911: A Detailed Guide to Powering the TigerSHARC Processors
- EE-104: Setting Up Streams with the VisualDSP Debugger
- EE-110: A Quick Primer on ELF and DWARF File Formats
- EE-120: Interfacing Assembly Language Programs to C
- EE-126: The ABCs of SDRAMemories
- EE-128: DSP in C++: Calling Assembly Class Member Functions From C++
- EE-143: Understanding DMA on the ADSP-TS101
- EE-147: Tuning C Source Code for the TigerSHARC® DSP Compiler
- EE-159: Initializing DSP System & Control Registers From C and C++
- EE-167: Introduction to TigerSHARC® Multiprocessor Systems Using VisualDSP++™
- EE-169: Estimating Power For The ADSP-TS101S
- EE-170: Estimating Power for ADSP-TS201S TigerSHARC® Processors
- EE-174: ADSP-TS101S TigerSHARC® Processor Boot Loader Kernels Operation
- EE-175: Emulator and Evaluation Hardware Troubleshooting Guide for VisualDSP++ Users
- EE-176: Hardware Design Checklist For ADSP-TS101S TigerSHARC® Processors
- EE-178: The ADSP-TS101S TigerSHARC® On-chip SDRAM Controller
- EE-179: ADSP-TS20xS TigerSHARC® System Design Guidelines
- EE-182: Thermal Relief Design for ADSP-TS201S TigerSHARC® Processors
- EE-200: ADSP-TS20x TigerSHARC® Processor Boot Loader Kernels Operation
- EE-202: Using the Expert Linker for Multiprocessor LDFs
- EE-205: Considerations for Porting Code from the ADSP-TS101S TigerSHARC® Processor to the ADSP-TS201S TigerSHARC Processor
- EE-211: 16-bit FIR Filters on ADSP-TS20x TigerSHARC® Processors
- EE-215: A 16-bit IIR Filter on the ADSP-TS20x TigerSHARC® Processor

DUAL COMPUTE BLOCKS

The ADSP-TS203S processor has compute blocks that can execute computations either independently or together as a single-instruction, multiple-data (SIMD) engine. The processor can issue up to two compute instructions per compute block each cycle, instructing the ALU, multiplier, or shifter to perform independent, simultaneous operations. Each compute block can execute eight 8-bit, four 16-bit, two 32-bit, or one 64-bit SIMD computations in parallel with the operation in the other block. These computation units support IEEE 32-bit single-precision floating-point, extended-precision 40-bit floating point, and 8-, 16-, 32-, and 64-bit fixed-point processing.

The compute blocks are referred to as X and Y in assembly syntax, and each block contains three computational units—an ALU, a multiplier, a 64-bit shifter—and a 32-word register file.

- Register File—each compute block has a multiported 32-word, fully orthogonal register file used for transferring data between the computation units and data buses and for storing intermediate results. Instructions can access the registers in the register file individually (word-aligned), in sets of two (dual-aligned), or in sets of four (quad-aligned).
- ALU—the ALU performs a standard set of arithmetic operations in both fixed- and floating-point formats. It also performs logic and permute operations.
- Multiplier—the multiplier performs both fixed- and floating-point multiplication and fixed-point multiply and accumulate.
- Shifter—the 64-bit shifter performs logical and arithmetic shifts, bit and bit stream manipulation, and field deposit and extraction operations.

Using these features, the compute blocks can

- Provide 8 MACS per cycle peak and 7.1 MACS per cycle sustained 16-bit performance and provide 2 MACS per cycle peak and 1.8 MACS per cycle sustained 32-bit performance (based on FIR)
- Execute six single-precision floating-point or execute 24 fixed-point (16-bit) operations per cycle, providing 3G FLOPS or 12.0G/s regular operations performance at 500 MHz
- Perform two complex 16-bit MACS per cycle

DATA ALIGNMENT BUFFER (DAB)

The DAB is a quad-word FIFO that enables loading of quad-word data from nonaligned addresses. Normally, load instructions must be aligned to their data size so that quad words are loaded from a quad-aligned address. Using the DAB significantly improves the efficiency of some applications, such as FIR filters.

DUAL INTEGER ALU (IALU)

The processor has two IALUs that provide powerful address generation capabilities and perform many general-purpose integer operations. The IALUs are referred to as J and K in assembly syntax and have the following features:

- Provide memory addresses for data and update pointers
- Support circular buffering and bit-reverse addressing
- Perform general-purpose integer operations, increasing programming flexibility
- Include a 31-word register file for each IALU

As address generators, the IALUs perform immediate or indirect (pre- and post-modify) addressing. They perform modulus and bit-reverse operations with no constraints placed on memory addresses for the modulus data buffer placement. Each IALU can specify either a single-, dual-, or quad-word access from memory.

The IALUs have hardware support for circular buffers, bit reverse, and zero-overhead looping. Circular buffers facilitate efficient programming of delay lines and other data structures required in digital signal processing, and they are commonly used in digital filters and Fourier transforms. Each IALU provides registers for four circular buffers, so applications can set up a total of eight circular buffers. The IALUs handle address pointer wraparound automatically, reducing overhead, increasing performance, and simplifying implementation. Circular buffers can start and end at any memory location.

Because the IALU's computational pipeline is one cycle deep, in most cases integer results are available in the next cycle. Hardware (register dependency check) causes a stall if a result is unavailable in a given cycle.

PROGRAM SEQUENCER

The ADSP-TS203S processor's program sequencer supports:

- A fully interruptible programming model with flexible programming in assembly and C/C++ languages; handles hardware interrupts with high throughput and no aborted instruction cycles
- A 10-cycle instruction pipeline—four-cycle fetch pipe and six-cycle execution pipe—computation results available two cycles after operands are available
- Supply of instruction fetch memory addresses; the sequencer's instruction alignment buffer (IAB) caches up to five fetched instruction lines waiting to execute; the program sequencer extracts an instruction line from the IAB and distributes it to the appropriate core component for execution
- Management of program structures and program flow determined according to JUMP, CALL, RTI, RTS instructions, loop structures, conditions, interrupts, and software exceptions
- Branch prediction and a 128-entry branch target buffer (BTB) to reduce branch delays for efficient execution of conditional and unconditional branch instructions and zero-overhead looping; correctly predicted branches occur with zero overhead cycles, overcoming the five-to-nine stage branch penalty
- Compact code without the requirement to align code in memory; the IAB handles alignment

Table 7. Pin Definitions—External Port DMA/Flyby

Signal	Type	Term	Description
$\overline{\text{DMAR3–0}}$	I/A	epu	DMA Request Pins. Enable external I/O devices to request DMA services from the processor. In response to $\overline{\text{DMARx}}$, the processor performs DMA transfers according to the DMA channel's initialization. The processor ignores DMA requests from uninitialized channels.
$\overline{\text{IOWR}}$	O/T (pu_0)	nc	I/O Write. When a processor DMA channel initiates a flyby mode read transaction, the processor asserts the $\overline{\text{IOWR}}$ signal during the data cycles. This assertion makes the I/O device sample the data instead of the TigerSHARC.
$\overline{\text{IORD}}$	O/T (pu_0)	nc	I/O Read. When a processor DMA channel initiates a flyby mode write transaction, the processor asserts the $\overline{\text{IORD}}$ signal during the data cycle. This assertion with the $\overline{\text{IOEN}}$ makes the I/O device drive the data instead of the TigerSHARC.
$\overline{\text{IOEN}}$	O/T (pu_0)	nc	I/O Device Output Enable. Enables the output buffers of an external I/O device for fly-by transactions between the device and external memory. Active on flyby transactions.

I = input; **A** = asynchronous; **O** = output; **OD** = open-drain output; **T** = three-state; **P** = power supply; **G** = ground; **pd** = internal pull-down 5 kΩ; **pu** = internal pull-up 5 kΩ; **pd_0** = internal pull-down 5 kΩ on processor ID = 0; **pu_0** = internal pull-up 5 kΩ on processor ID = 0; **pu_od_0** = internal pull-up 500 Ω on processor ID = 0; **pd_m** = internal pull-down 5 kΩ on processor bus master; **pu_m** = internal pull-up 5 kΩ on processor bus master; **pu_ad** = internal pull-up 40 kΩ. For more pull-down and pull-up information, see Electrical Characteristics on Page 21.

Term (termination of unused pins) column symbols: epd = external pull-down approximately 5 kΩ to V_{SS}; epu = external pull-up approximately 5 kΩ to V_{DD_IO}, nc = not connected; na = not applicable (always used); V_{DD_IO} = connect directly to V_{DD_IO}; V_{SS} = connect directly to V_{SS}

Table 8. Pin Definitions—External Port SDRAM Controller

Signal	Type	Term	Description
$\overline{\text{MSSD3–0}}$	I/O/T (pu_0)	nc	Memory Select SDRAM. $\overline{\text{MSSD0}}$, $\overline{\text{MSSD1}}$, $\overline{\text{MSSD2}}$, or $\overline{\text{MSSD3}}$ is asserted whenever the processor accesses SDRAM memory space. $\overline{\text{MSSD3–0}}$ are decoded memory address pins that are asserted whenever the processor issues an SDRAM command cycle (access to ADDR31:30 = 0b01—except reserved spaces shown in Figure 2 on Page 6). In a multiprocessor system, the master processor drives $\overline{\text{MSSD3–0}}$.
$\overline{\text{RAS}}$	I/O/T (pu_0)	nc	Row Address Select. When sampled low, $\overline{\text{RAS}}$ indicates that a row address is valid in a read or write of SDRAM. In other SDRAM accesses, it defines the type of operation to execute according to SDRAM specification.
$\overline{\text{CAS}}$	I/O/T (pu_0)	nc	Column Address Select. When sampled low, $\overline{\text{CAS}}$ indicates that a column address is valid in a read or write of SDRAM. In other SDRAM accesses, it defines the type of operation to execute according to the SDRAM specification.
LDQM	O/T (pu_0)	nc	Low Word SDRAM Data Mask. When sampled high, three-states the SDRAM DQ buffers. LDQM is valid on SDRAM transactions when $\overline{\text{CAS}}$ is asserted, and inactive on read transactions.

I = input; **A** = asynchronous; **O** = output; **OD** = open-drain output; **T** = three-state; **P** = power supply; **G** = ground; **pd** = internal pull-down 5 kΩ; **pu** = internal pull-up 5 kΩ; **pd_0** = internal pull-down 5 kΩ on processor ID = 0; **pu_0** = internal pull-up 5 kΩ on processor ID = 0; **pu_od_0** = internal pull-up 500 Ω on processor ID = 0; **pd_m** = internal pull-down 5 kΩ on processor bus master; **pu_m** = internal pull-up 5 kΩ on processor bus master; **pu_ad** = internal pull-up 40 kΩ. For more pull-down and pull-up information, see Electrical Characteristics on Page 21.

Term (termination of unused pins) column symbols: epd = external pull-down approximately 5 kΩ to V_{SS}; epu = external pull-up approximately 5 kΩ to V_{DD_IO}, nc = not connected; na = not applicable (always used); V_{DD_IO} = connect directly to V_{DD_IO}; V_{SS} = connect directly to V_{SS}

Table 10. Pin Definitions—Flags, Interrupts, and Timer

Signal	Type	Term	Description
FLAG3–0	I/O/A (pu)	nc	FLAG pins. Bidirectional input/output pins can be used as program conditions. Each pin can be configured individually for input or for output. FLAG3–0 are inputs after power-up and reset.
$\overline{\text{IRQ3–0}}$	I/A (pu)	nc	Interrupt Request. When asserted, the processor generates an interrupt. Each of the $\overline{\text{IRQ3–0}}$ pins can be independently set for edge-triggered or level-sensitive operation. After reset, these pins are disabled unless the $\overline{\text{IRQ3–0}}$ strap option and interrupt vectors are initialized for booting.
TMR0E	O	na	Timer 0 expires. This output pulses whenever timer 0 expires. At reset, this is a strap pin. For more information, see Table 16 on Page 18.

I = input; **A** = asynchronous; **O** = output; **OD** = open-drain output; **T** = three-state; **P** = power supply; **G** = ground; **pd** = internal pull-down 5 kΩ; **pu** = internal pull-up 5 kΩ; **pd_0** = internal pull-down 5 kΩ on processor ID = 0; **pu_0** = internal pull-up 5 kΩ on processor ID = 0; **pu_od_0** = internal pull-up 500 Ω on processor ID = 0; **pd_m** = internal pull-down 5 kΩ on processor bus master; **pu_m** = internal pull-up 5 kΩ on processor bus master; **pu_ad** = internal pull-up 40 kΩ. For more pull-down and pull-up information, see Electrical Characteristics on Page 21.

Term (termination of unused pins) column symbols: epd = external pull-down approximately 5 kΩ to V_{SS}; epu = external pull-up approximately 5 kΩ to V_{DD_IO}, nc = not connected; na = not applicable (always used); V_{DD_IO} = connect directly to V_{DD_IO}; V_{SS} = connect directly to V_{SS}

Table 11. Pin Definitions—Link Ports

Signal	Type	Term	Description
LxDATO3–0P	O	nc	Link Ports 1–0 Data 1–0 Transmit LVDS P
LxDATO3–0N	O	nc	Link Ports 1–0 Data 1–0 Transmit LVDS N
LxCLKOUTP	O	nc	Link Ports 1–0 Transmit Clock LVDS P
LxCLKOUTN	O	nc	Link Ports 1–0 Transmit Clock LVDS N
LxACKI	I (pd)	nc	Link Ports 1–0 Receive Acknowledge. Using this signal, the receiver indicates to the transmitter that it may continue the transmission.
$\overline{\text{LxBCMPO}}$	O (pu)	nc	Link Ports 1–0 Block Completion. When the transmission is executed using DMA, this signal indicates to the receiver that the transmitted block is completed. The pull-up resistor is present on $\overline{\text{L0BCMPO}}$ only. At reset, the $\overline{\text{L1BCMPO}}$ pin is a strap pin. For more information, see Table 16 on Page 18.
LxDATI3–0P	I	V_{DD_IO}	Link Ports 1–0 Data 3–0 Receive LVDS P
LxDATI3–0N	I	V_{DD_IO}	Link Ports 1–0 Data 3–0 Receive LVDS N
LxCLKINP	I/A	V_{DD_IO}	Link Ports 1–0 Receive Clock LVDS P
LxCLKINN	I/A	V_{DD_IO}	Link Ports 1–0 Receive Clock LVDS N
LxACKO	O	nc	Link Ports 1–0 Transmit Acknowledge. Using this signal, the receiver indicates to the transmitter that it may continue the transmission.
$\overline{\text{LxBCMPI}}$	I (pd_l)	V_{SS}	Link Ports 1–0 Block Completion. When the reception is executed using DMA, this signal indicates to the receiver that the transmitted block is completed.

I = input; **A** = asynchronous; **O** = output; **OD** = open-drain output; **T** = three-state; **P** = power supply; **G** = ground; **pd** = internal pull-down 5 kΩ; **pu** = internal pull-up 5 kΩ; **pd_0** = internal pull-down 5 kΩ on processor ID = 0; **pu_0** = internal pull-up 5 kΩ on processor ID = 0; **pu_od_0** = internal pull-up 500 Ω on processor ID = 0; **pd_m** = internal pull-down 5 kΩ on processor bus master; **pu_m** = internal pull-up 5 kΩ on processor bus master; **pu_ad** = internal pull-up 40 kΩ. For more pull-down and pull-up information, see Electrical Characteristics on Page 21.

Term (termination of unused pins) column symbols: epd = external pull-down approximately 5 kΩ to V_{SS}; epu = external pull-up approximately 5 kΩ to V_{DD_IO}, nc = not connected; na = not applicable (always used); V_{DD_IO} = connect directly to V_{DD_IO}; V_{SS} = connect directly to V_{SS}

Table 12. Pin Definitions—Impedance Control, Drive Strength Control, and Regulator Enable

Signal	Type	Term	Description
CONTROLIMP0 CONTROLIMP1	I (pd) I (pu)	na na	Impedance Control. As shown in Table 13, the CONTROLIMP1–0 pins select between normal driver mode and A/D driver mode. When using normal mode (recommended), the output drive strength is set relative to maximum drive strength according to Table 14. When using A/D mode, the resistance control operates in the analog mode, where drive strength is continuously controlled to match a specific line impedance as shown in Table 14.
DS2, 0 DS1	I (pu) I (pd)	na	Digital Drive Strength Selection. Selected as shown in Table 14. For drive strength calculation, see Output Drive Currents on Page 34. The drive strength for some pins is preset, not controlled by the DS2–0 pins. The pins that are always at drive strength 7 (100%) include: $\overline{\text{CPA}}$, $\overline{\text{DPA}}$, TDO, $\overline{\text{EMU}}$, and $\overline{\text{RST\_OUT}}$. The drive strength for the ACK pin is always ×2 drive strength 7 (100%).
ENEDREG	I (pu)	V_{SS}	Connect the ENEDREG pin to V_{SS}. Connect the V_{DD_DRAM} pins to a properly decoupled DRAM power supply.

I = input; **A** = asynchronous; **O** = output; **OD** = open-drain output; **T** = three-state; **P** = power supply; **G** = ground; **pd** = internal pull-down 5 kΩ; **pu** = internal pull-up 5 kΩ; **pd_0** = internal pull-down 5 kΩ on processor ID = 0; **pu_0** = internal pull-up 5 kΩ on processor ID = 0; **pu_od_0** = internal pull-up 500 Ω on processor ID = 0; **pd_m** = internal pull-down 5 kΩ on processor bus master; **pu_m** = internal pull-up 5 kΩ on processor bus master; **pu_ad** = internal pull-up 40 kΩ. For more pull-down and pull-up information, see Electrical Characteristics on Page 21.

Term (termination of unused pins) column symbols: epd = external pull-down approximately 5 kΩ to V_{SS}; epu = external pull-up approximately 5 kΩ to V_{DD_IO}, nc = not connected; na = not applicable (always used); V_{DD_IO} = connect directly to V_{DD_IO}; V_{SS} = connect directly to V_{SS}

Table 13. Impedance Control Selection

CONTROLIMP1-0	Driver Mode
00 (recommended)	Normal
01	Reserved
10 (default)	A/D Mode
11	Reserved

Table 14. Drive Strength/Output Impedance Selection

DS2–0 Pins	Drive Strength[1]	Output Impedance[2]
000	Strength 0 (11.1%)	26 Ω
001	Strength 1 (23.8%)	32 Ω
010	Strength 2 (36.5%)	40 Ω
011	Strength 3 (49.2%)	50 Ω
100	Strength 4 (61.9%)	62 Ω
101 (default)	Strength 5 (74.6%)	70 Ω
110	Strength 6 (87.3%)	96 Ω
111	Strength 7 (100%)	120 Ω

[1] CONTROLIMP1 = 0, A/D mode disabled.
[2] CONTROLIMP1 = 1, A/D mode enabled.

Table 15. Pin Definitions—Power, Ground, and Reference

Signal	Type	Term	Description
V_{DD}	P	na	V_{DD} pins for internal logic.
V_{DD_A}	P	na	V_{DD} pins for analog circuits. Pay critical attention to bypassing this supply.
V_{DD_IO}	P	na	V_{DD} pins for I/O buffers.
V_{DD_DRAM}	P	na	V_{DD} pins for internal DRAM.
V_{REF}	I	na	Reference voltage defines the trip point for all input buffers, except SCLK, $\overline{RST\_IN}$, $\overline{POR\_IN}$, $\overline{IRQ3–0}$, FLAG3–0, $\overline{DMAR3–0}$, ID2–0, CONTROLIMP1–0, LxDATO3–0P/N, LxCLKOUTP/N, LxDATI3–0P/N, LxCLKINP/N, TCK, TDI, TMS, and $\overline{TRST}$. V_{REF} can be connected to a power supply or set by a voltage divider circuit as shown in Figure 4. For more information, see Filtering Reference Voltage and Clocks on Page 8.
SCLK_V_{REF}	I	na	System Clock Reference. Connect this pin to a reference voltage as shown in Figure 5. For more information, see Filtering Reference Voltage and Clocks on Page 8.
V_{SS}	G	na	Ground pins.
NC	—	nc	No Connect. Do not connect these pins to anything (not to any supply, signal, or each other). These pins are reserved and must be left unconnected.

I = input; **A** = asynchronous; **O** = output; **OD** = open-drain output; **T** = three-state; **P** = power supply; **G** = ground; **pd** = internal pull-down 5 kΩ; **pu** = internal pull-up 5 kΩ; **pd_0** = internal pull-down 5 kΩ on processor ID = 0; **pu_0** = internal pull-up 5 kΩ on processor ID = 0; **pu_od_0** = internal pull-up 500 Ω on processor ID = 0; **pd_m** = internal pull-down 5 kΩ on processor bus master; **pu_m** = internal pull-up 5 kΩ on processor bus master; **pu_ad** = internal pull-up 40 kΩ. For more pull-down and pull-up information, see Electrical Characteristics on Page 21.

Term (termination of unused pins) column symbols: epd = external pull-down approximately 5 kΩ to V_{SS}; epu = external pull-up approximately 5 kΩ to V_{DD_IO}, nc = not connected; na = not applicable (always used); V_{DD_IO} = connect directly to V_{DD_IO}; V_{SS} = connect directly to V_{SS}

STRAP PIN FUNCTION DESCRIPTIONS

Some pins have alternate functions at reset. Strap options set processor operating modes. During reset, the processor samples the strap option pins. Strap pins have an internal pull-up or pull-down for the default value. If a strap pin is not connected to an overdriving external pull-up, pull-down, or logic load, the processor samples the default value during reset. If strap pins are connected to logic inputs, a stronger external pull-up or pull-down may be required to ensure default value depending on leakage and/or low level input current of the logic load. To set a mode other than the default mode, connect the strap pin to a sufficiently stronger external pull-up or pull-down. Table 16 lists and describes each of the processor's strap pins.

Table 16. Pin Definitions—I/O Strap Pins

Signal	Type (at Reset)	On Pin …	Description
EBOOT	I (pd_0)	$\overline{BMS}$	EPROM Boot. 0 = boot from EPROM immediately after reset (default) 1 = idle after reset and wait for an external device to boot processor through the external port or a link port
IRQEN	I (pd)	$\overline{BM}$	Interrupt Enable. 0 = disable and set $\overline{IRQ3–0}$ interrupts to edge-sensitive after reset (default) 1 = enable and set $\overline{IRQ3–0}$ interrupts to level-sensitive immediately after reset
LINK_DWIDTH	I (pd)	TMR0E	Link Port Input Default Data Width. 0 = 1-bit (default) 1 = 4-bit

I = input; **A** = asynchronous; **O** = output; **OD** = open-drain output; **T** = three-state; **P** = power supply; **G** = ground; **pd** = internal pull-down 5 kΩ; **pu** = internal pull-up 5 kΩ; **pd_0** = internal pull-down 5 kΩ on processor ID = 0; **pu_0** = internal pull-up 5 kΩ on processor ID = 0; **pu_od_0** = internal pull-up 500 Ω on processor ID = 0; **pd_m** = internal pull-down 5 kΩ on processor bus master; **pu_m** = internal pull-up 5 kΩ on processor bus master; **pu_ad** = internal pull-up 40 kΩ. For more pull-down and pull-up information, see Electrical Characteristics on Page 21.

SPECIFICATIONS

Note that component specifications are subject to change with out notice. For information on link port electrical characteristics, see Link Port Low Voltage, Differential-Signal (LVDS) Electrical Characteristics, and Timing on Page 29.

OPERATING CONDITIONS

Parameter	Description	Test Conditions	Grade[1]	Min	Typ	Max	Unit
V_{DD}	Internal Supply Voltage	@ CCLK = 500 MHz	050	1.00	1.05	1.10	V
V_{DD_A}	Analog Supply Voltage	@ CCLK = 500 MHz	050	1.00	1.05	1.10	V
V_{DD_IO}	I/O Supply Voltage		(all)	2.38	2.50	2.63	V
V_{DD_DRAM}	Internal DRAM Supply Voltage	@ CCLK = 500 MHz	050	1.425	1.500	1.575	V
T_{CASE}	Case Operating Temperature		A	–40		+85	°C
T_{CASE}	Case Operating Temperature		B	0		+85	°C
V_{IH1}	High Level Input Voltage[2, 3]	@ V_{DD}, V_{DD_IO} = Max	(all)	1.7		3.63	V
V_{IH2}	High Level Input Voltage[3, 4]	@ V_{DD}, V_{DD_IO} = Max	(all)	1.9		3.63	V
V_{IL}	Low Level Input Voltage[3, 5]	@ V_{DD}, V_{DD_IO} = Min	(all)	–0.33		+0.8	V
I_{DD}	V_{DD} Supply Current, Typical Activity[6]	@ CCLK = 500 MHz, V_{DD} = 1.05 V, T_{CASE} = 25°C	050		2.06		A
I_{DD_A}	V_{DD_A} Supply Current, Typical Activity	@ CCLK = 500 MHz, V_{DD} = 1.05 V, T_{CASE} = 25°C	050		20	50	mA
I_{DD_IO}	V_{DD_IO} Supply Current, Typical Activity[6]	@ SCLK = 62.5 MHz, V_{DD_IO} = 2.5 V, T_{CASE} = 25°C	(all)		0.15		A
I_{DD_DRAM}	V_{DD_DRAM} Supply Current, Typical Activity[6]	@ CCLK = 500 MHz, V_{DD_DRAM} = 1.5 V, T_{CASE} = 25°C	050		0.25	0.40	A
V_{REF}	Voltage Reference		(all)	(V_{DD_IO} × 0.56) ±5%			V
SCLK_V_{REF}	Voltage Reference		(all)	(V_{CLOCK_DRIVE} × 0.56) ±5%			V

[1] Specifications vary for different grades (for example, SABP–060, SABP–050, SWBP–050). For more information on part grades, see Ordering Guide on Page 47.

[2] V_{IH1} specification applies to input and bidirectional pins: SCLKRAT2–0, SCLK, ADDR31–0, DATA63–0, $\overline{RD}$, $\overline{WRL}$, ACK, $\overline{BRST}$, $\overline{BR7–0}$, $\overline{BOFF}$, $\overline{HBR}$, $\overline{HBG}$, $\overline{MSSD3–0}$, $\overline{RAS}$, $\overline{CAS}$, SDCKE, $\overline{SDWE}$, TCK, FLAG3–0, DS2–0, ENEDREG.

[3] Values represent dc case. During transitions, the inputs may overshoot or undershoot to the voltage shown in Table 18, based on the transient duty cycle. The dc case is equivalent to 100% duty cycle.

[4] V_{IH2} specification applies to input and bidirectional pins: TDI, TMS, $\overline{TRST}$, CIMP1–0, ID2–0, $\overline{LxBCMPI}$, LxACKI, $\overline{POR\_IN}$, $\overline{RST\_IN}$, $\overline{IRQ3–0}$, $\overline{CPA}$, $\overline{DPA}$, $\overline{DMAR3–0}$.

[5] Applies to input and bidirectional pins.

[6] For details on internal and external power calculation issues, including other operating conditions, see *EE-170, Estimating Power for the ADSP-TS203S*.

Table 18. Maximum Duty Cycle for Input Transient Voltage

V_{IN} Max (V)[1]	V_{IN} Min (V)[1]	Maximum Duty Cycle[2]
+3.63	–0.33	100%
+3.64	–0.34	90%
+3.70	–0.40	50%
+3.78	–0.48	30%
+3.86	–0.56	17%
+3.93	–0.63	10%

[1] The individual values cannot be combined for analysis of a single instance of overshoot or undershoot. The worst case observed value must fall within one of the voltages specified and the total duration of the overshoot or undershoot (exceeding the 100% case) must be less than or equal to the corresponding duty cycle.

[2] Duty cycle refers to the percentage of time the signal exceeds the value for the 100% case. This is equivalent to the measured duration of a single instance of overshoot or undershoot as a percentage of the period of occurrence. The practical worst case for period of occurrence for either overshoot or undershoot is 2 × t_{SCLK}.

TIMING SPECIFICATIONS

With the exception of $\overline{\text{DMAR3–0}}$, $\overline{\text{IRQ3–0}}$, TMR0E, and FLAG3–0 (input only) pins, all ac timing for the ADSP-TS203S processor is relative to a reference clock edge. Because input setup/hold, output valid/hold, and output enable/disable times are relative to a clock edge, the timing data for the ADSP-TS203S processor has few calculated (formula-based) values. For information on ac timing, see General AC Timing. For information on link port transfer timing, see Link Port Low Voltage, Differential-Signal (LVDS) Electrical Characteristics, and Timing on Page 29.

General AC Timing

Timing is measured on signals when they cross the 1.25 V level as described in Figure 13 on Page 28. All delays (in nanoseconds) are measured between the point that the first signal reaches 1.25 V and the point that the second signal reaches 1.25 V.

The general ac timing data appears in Table 22 and Table 29. All ac specifications are measured with the load specified in Figure 34 on Page 36, and with the output drive strength set to strength 4. In order to calculate the output valid and hold times for different load conditions and/or output drive strengths, refer to Figure 35 on Page 36 through Figure 42 on Page 38 (Rise and Fall Time vs. Load Capacitance) and Figure 43 on Page 38 (Output Valid vs. Load Capacitance and Drive Strength).

The ac asynchronous timing data for the $\overline{\text{IRQ3–0}}$, $\overline{\text{DMAR3–0}}$, FLAG3–0, and TMR0E pins appears in Table 21.

Table 21. AC Asynchronous Signal Specifications

Name	Description	Pulse Width Low (Min)	Pulse Width High (Min)
$\overline{\text{IRQ3–0}}$[1]	Interrupt Request	$2 \times t_{SCLK}$ ns	$2 \times t_{SCLK}$ ns
$\overline{\text{DMAR3–0}}$[1]	DMA Request	$2 \times t_{SCLK}$ ns	$2 \times t_{SCLK}$ ns
FLAG3–0[2]	FLAG3–0 Input	$2 \times t_{SCLK}$ ns	$2 \times t_{SCLK}$ ns
TMR0E[3]	Timer 0 Expired	$4 \times t_{SCLK}$ ns	

[1] These input pins have Schmitt triggers and therefore do not need to be synchronized to a clock reference.
[2] For output specifications on FLAG3–0 pins, see Table 29.
[3] This pin is a strap option. During reset, an internal resistor pulls the pin low.

Table 22. Reference Clocks—Core Clock (CCLK) Cycle Time

Parameter	Description	Grade = 050 (500 MHz) Min	Max	Unit
t_{CCLK}[1]	Core Clock Cycle Time	2.0	12.5	ns

[1] CCLK is the internal processor clock or instruction cycle time. The period of this clock is equal to the system clock period (t_{SCLK}) divided by the system clock ratio (SCLKRAT2–0). For information on available part numbers for different internal processor clock rates, see the Ordering Guide on Page 47.

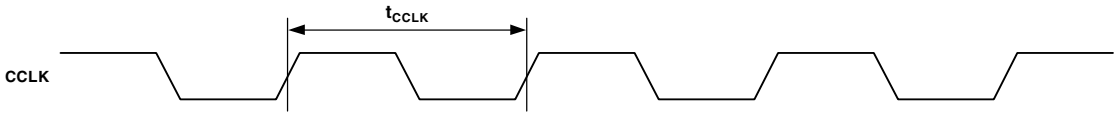

Figure 7. Reference Clocks—Core Clock (CCLK) Cycle Time

Table 25. Power-Up Timing[1]

Parameter		Min	Max	Unit
Timing Requirement				
t_{VDD_DRAM}	V_{DD_DRAM} Stable After V_{DD}, V_{DD_A}, V_{DD_IO} Stable	>0		ms

[1] For information about power supply sequencing and monitoring solutions, please visit www.analog.com/sequencing.

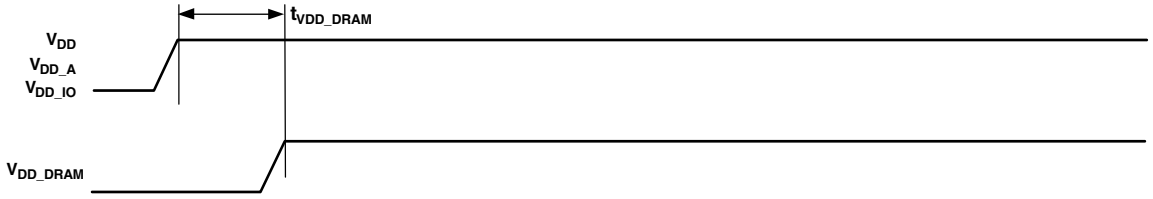

Figure 10. Power-Up Timing

Table 26. Power-Up Reset Timing

Parameter		Min	Max	Unit
Timing Requirements				
$t_{RST\_IN\_PWR}$	$\overline{RST\_IN}$ Deasserted After V_{DD}, V_{DD_A}, V_{DD_IO}, V_{DD_DRAM}, SCLK, and Static/ Strap Pins Stable	2		ms
$t_{TRST\_IN\_PWR}$[1]	$\overline{TRST}$ Asserted During Power-Up Reset	$100 \times t_{SCLK}$		ns
Switching Characteristic				
$t_{RST\_OUT\_PWR}$	$\overline{RST\_OUT}$ Deasserted After $\overline{RST\_IN}$ Deasserted	1.5		ms

[1] Applies after V_{DD}, V_{DD_A}, V_{DD_IO}, V_{DD_DRAM}, and SCLK are stable and before $\overline{RST\_IN}$ deasserted.

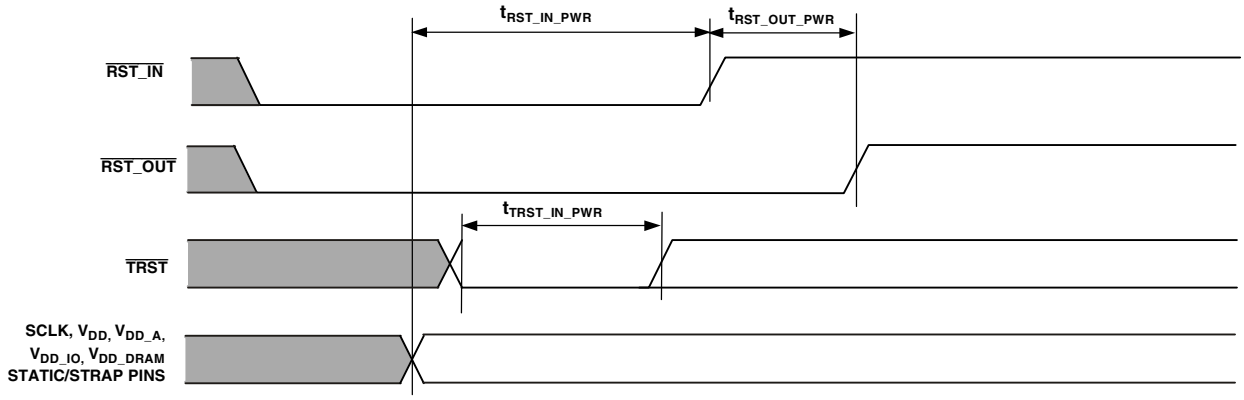

Figure 11. Power-Up Reset Timing

Table 29. AC Signal Specifications

(All values in this table are in nanoseconds.)

Name	Description	Input Setup (Min)	Input Hold (Min)	Output Valid (Max)	Output Hold (Min)	Output Enable (Min)[1]	Output Disable (Max)[1]	Reference Clock
ADDR31–0	External Address Bus	1.5	0.5	4.0	1.0	1.15	2.0	SCLK
DATA31–0	External Data Bus	1.5	0.5	4.0	1.0	1.15	2.0	SCLK
$\overline{\text{MSH}}$	Memory Select HOST Line	—	—	4.0	1.0	1.15	2.0	SCLK
$\overline{\text{MSSD3–0}}$	Memory Select SDRAM Lines	1.5	0.5	4.0	1.0	1.0	2.0	SCLK
$\overline{\text{MS1–0}}$	Memory Select for Static Blocks	—	—	4.0	1.0	1.15	2.0	SCLK
$\overline{\text{RD}}$	Memory Read	1.5	0.5	4.0	1.0	1.15	2.0	SCLK
$\overline{\text{WRL}}$	Write Low Word	1.5	0.5	4.0	1.0	1.15	2.0	SCLK
ACK	Acknowledge for Data High to Low	1.5	0.5	3.6	1.0	1.15	2.0	SCLK
	Acknowledge for Data Low to High	1.5	0.5	4.2	0.9	1.15	2.0	SCLK
SDCKE	SDRAM Clock Enable	1.5	0.5	4.0	1.0	1.15	2.0	SCLK
$\overline{\text{RAS}}$	Row Address Select	1.5	0.5	4.0	1.0	1.15	2.0	SCLK
$\overline{\text{CAS}}$	Column Address Select	1.5	0.5	4.0	1.0	1.15	2.0	SCLK
$\overline{\text{SDWE}}$	SDRAM Write Enable	1.5	0.5	4.0	1.0	1.15	2.0	SCLK
LDQM	Low Word SDRAM Data Mask	—	—	4.0	1.0	1.15	2.0	SCLK
SDA10	SDRAM ADDR10	—	—	4.0	1.0	1.15	2.0	SCLK
$\overline{\text{HBR}}$	Host Bus Request	1.5	0.5	—	—	—	—	SCLK
$\overline{\text{HBG}}$	Host Bus Grant	1.5	0.5	4.0	1.0	1.15	2.0	SCLK
$\overline{\text{BOFF}}$	Back Off Request	1.5	0.5	—	—	—	—	SCLK
$\overline{\text{BUSLOCK}}$	Bus Lock	—	—	4.0	1.0	1.15	2.0	SCLK
$\overline{\text{BRST}}$	Burst Pin	1.5	0.5	4.0	1.0	1.15	2.0	SCLK
$\overline{\text{BR7–0}}$	Multiprocessing Bus Request Pins	1.5	0.5	4.0	1.0	—	—	SCLK
$\overline{\text{BM}}$	Bus Master Debug Aid Only	—	—	4.0	1.0	—	—	SCLK
$\overline{\text{IORD}}$	I/O Read Pin	—	—	4.0	1.0	1.0	2.0	SCLK
$\overline{\text{IOWR}}$	I/O Write Pin	—	—	4.0	1.0	1.15	2.0	SCLK
$\overline{\text{IOEN}}$	I/O Enable Pin	—	—	4.0	1.0	1.15	2.0	SCLK
$\overline{\text{CPA}}$	Core Priority Access High to Low	1.5	0.5	4.0	1.0	0.75	2.0	SCLK
	Core Priority Access Low to High	1.5	0.5	29.5	2.0	0.75	2.0	SCLK
$\overline{\text{DPA}}$	DMA Priority Access High to Low	1.5	0.5	4.0	1.0	0.75	2.0	SCLK
	DMA Priority Access Low to High	1.5	0.5	29.5	2.0	0.75	2.0	SCLK
$\overline{\text{BMS}}$	Boot Memory Select	—	—	4.0	1.0	1.15	2.0	SCLK
FLAG3–0[2]	FLAG Pins	—	—	4.0	1.0	1.15	2.0	SCLK
$\overline{\text{RST\_IN}}$[3, 4]	Global Reset Pin	1.5	2.5	—	—	—	—	SCLK[5]
TMS	Test Mode Select (JTAG)	1.5	0.5	—	—	—	—	TCK
TDI	Test Data Input (JTAG)	1.5	0.5	—	—	—	—	TCK
TDO	Test Data Output (JTAG)	—	—	4.0	1.0	0.75	2.0	TCK[6]
$\overline{\text{TRST}}$[3, 4]	Test Reset (JTAG)	1.5	0.5	—	—	—	—	TCK
$\overline{\text{EMU}}$[7]	Emulation High to Low	—	—	5.5	2.0	1.15	4.0	TCK or SCLK
ID2–0[8]	Static Pins—Must Be Constant	—	—	—	—	—	—	—
CONTROLIMP1–0[8]	Static Pins—Must Be Constant	—	—	—	—	—	—	—
DS2–0[8]	Static Pins—Must Be Constant	—	—	—	—	—	—	—
SCLKRAT2–0[8]	Static Pins—Must Be Constant	—	—	—	—	—	—	—

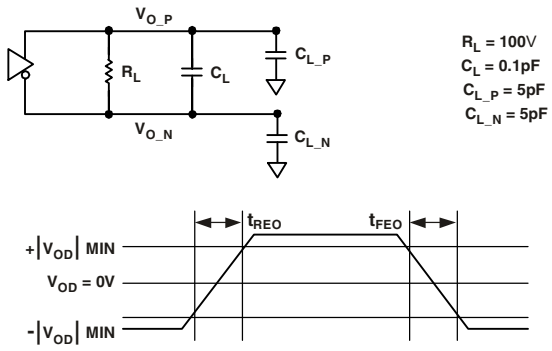

Figure 17. Link Ports—Differential Output Signals Transition Time

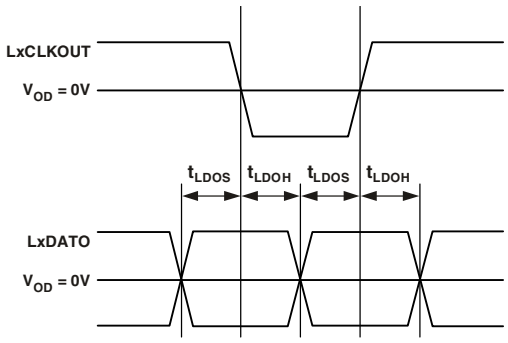

Figure 18. Link Ports—Data Output Setup and Hold[1]

[1] These parameters are valid for both clock edges.

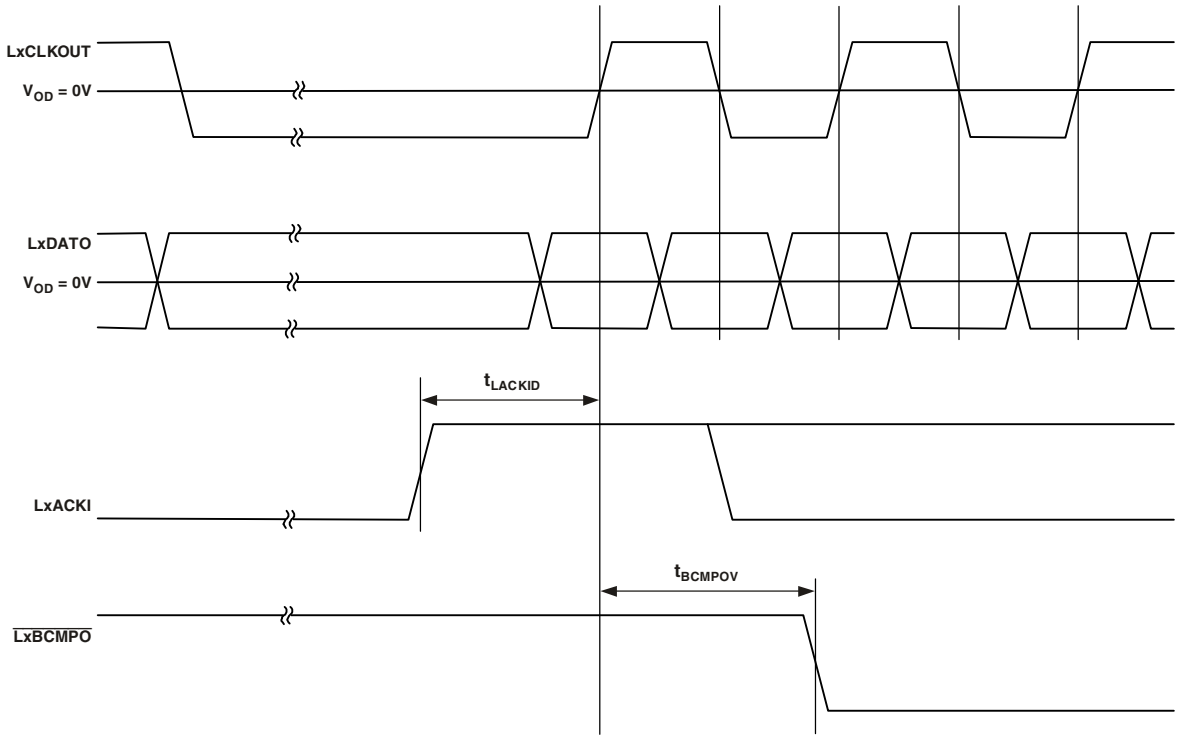

Figure 19. Link Ports—Transmission Start

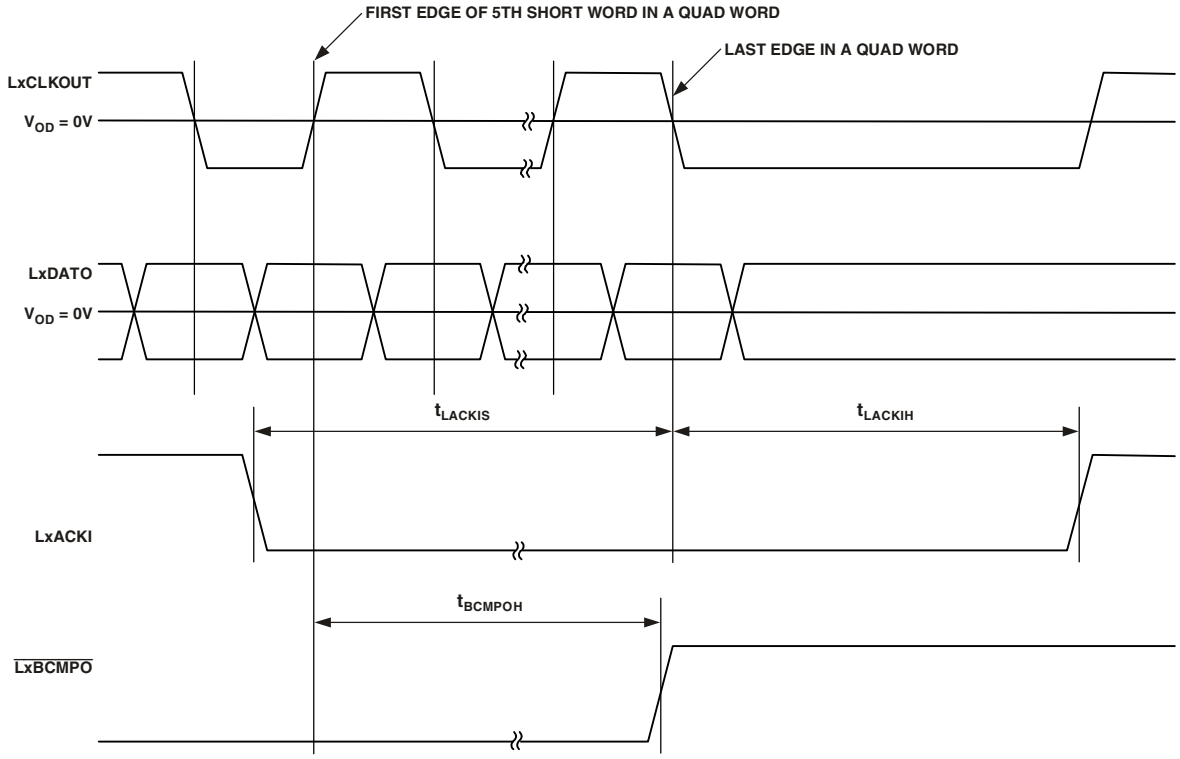

Figure 20. Link Ports—Transmission End and Stops

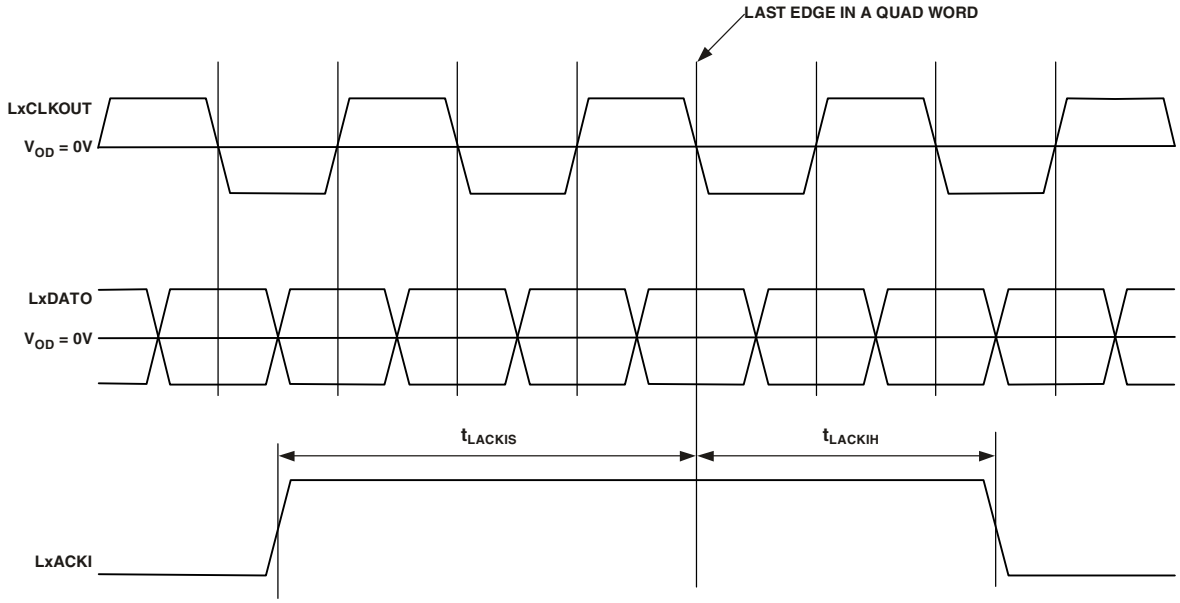

Figure 21. Link Ports—Back to Back Transmission

Link Port—Data In Timing

Table 33 with Figure 22 and Figure 23 provide the data in timing for the LVDS link ports.

Table 33. Link Port—Data In Timing

Parameter	Description	Min	Max	Unit
Inputs				
t_{LCLKIP}	LxCLKIN Period (Figure 23)	Greater of 1.8 or $0.9 \times t_{CCLK}$[1]	12.5	ns
t_{LDIS}	LxDATI Input Setup (Figure 23)	0.20[1, 2]		ns
		0.25[1, 3]		ns
		0.30[1, 4]		ns
		0.35[1, 5]		ns
t_{LDIH}	LxDATI Input Hold (Figure 23)	0.20[1, 2]		ns
		0.25[1, 3]		ns
		0.30[1, 4]		ns
		0.35[1, 5]		ns
t_{BCMPIS}	$\overline{\text{LxBCMPI}}$ Setup (Figure 22)	$2 \times t_{LCLKIP}$[1]		ns
t_{BCMPIH}	$\overline{\text{LxBCMPI}}$ Hold (Figure 22)	$2 \times t_{LCLKIP}$[1]		ns

[1] Timing is relative to the 0 differential voltage (V_{OD} = 0).
[2] $|V_{ID}|$ = 250 mV.
[3] $|V_{ID}|$ = 217 mV.
[4] $|V_{ID}|$ = 206 mV.
[5] $|V_{ID}|$ = 195 mV.

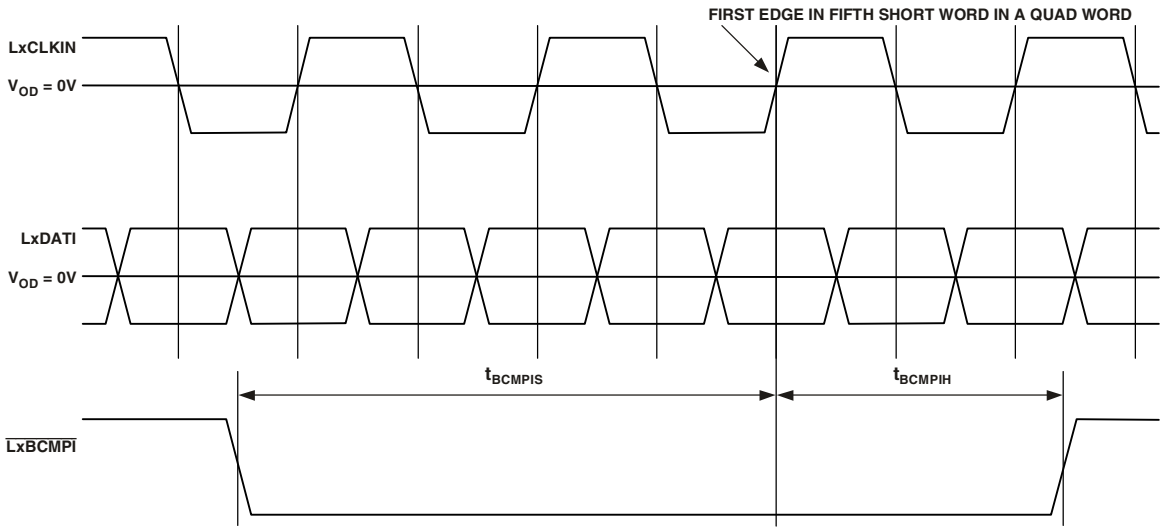

Figure 22. Link Ports—Last Received Quad Word

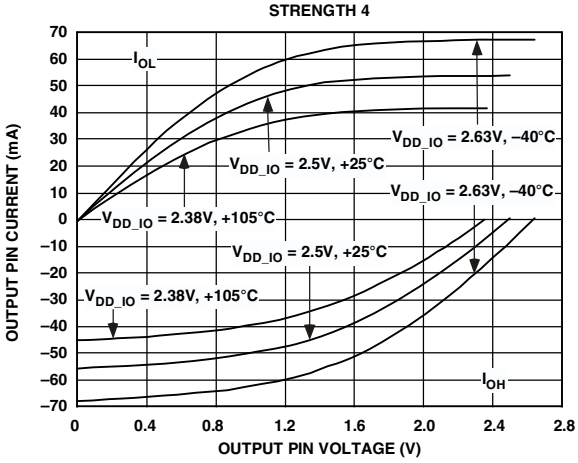

Figure 28. Typical Drive Currents at Strength 4

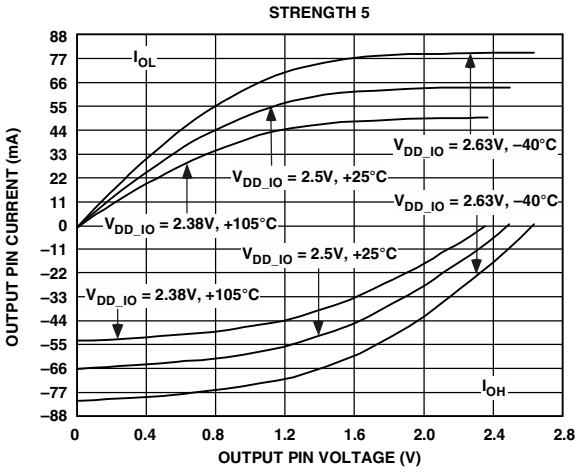

Figure 29. Typical Drive Currents at Strength 5

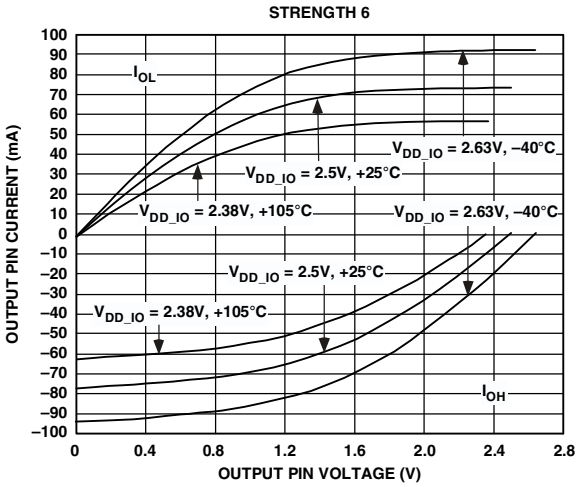

Figure 30. Typical Drive Currents at Strength 6

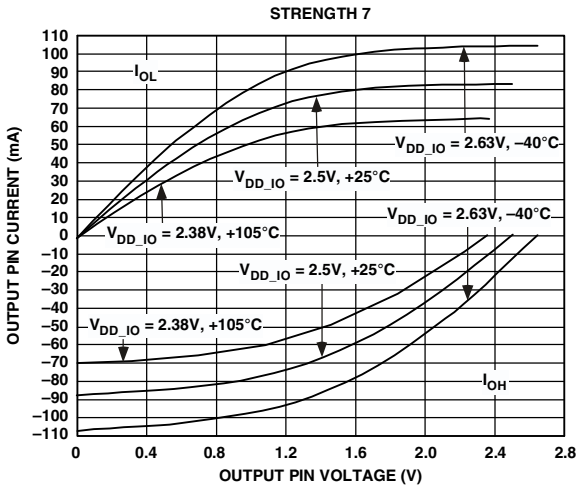

Figure 31. Typical Drive Currents at Strength 7

TEST CONDITIONS

The ac signal specifications (timing parameters) appear in Table 29 on Page 27. These include output disable time, output enable time, and capacitive loading. The timing specifications for the processor apply for the voltage reference levels in Figure 32.

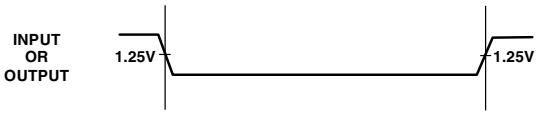

Figure 32. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Output Disable Time

Output pins are considered to be disabled when they stop driving, go into a high impedance state, and start to decay from their output high or low voltage. The time for the voltage on the bus to decay by ΔV is dependent on the capacitive load, C_L and the load current, I_L. This decay time can be approximated by the following equation:

$$t_{DECAY} = (C_L \Delta V)/I_L$$

The output disable time t_{DIS} is the difference between $t_{MEASURED\_DIS}$ and t_{DECAY} as shown in Figure 33. The time $t_{MEASURED\_DIS}$ is the interval from when the reference signal switches to when the output voltage decays ΔV from the measured output high or output low voltage. t_{DECAY} is calculated with test loads C_L and I_L, and with ΔV equal to 0.4 V.

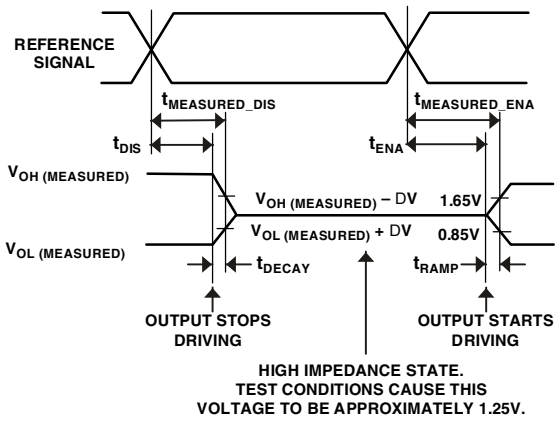

Figure 33. Output Enable/Disable

Output Enable Time

Output pins are considered to be enabled when they have made a transition from a high impedance state to when they start driving. The time for the voltage on the bus to ramp by ΔV is dependent on the capacitive load, C_L, and the drive current, I_D. This ramp time can be approximated by the following equation:

$$t_{RAMP} = (C_L \Delta V)/I_D$$

The output enable time t_{ENA} is the difference between $t_{MEASURED\_ENA}$ and t_{RAMP} as shown in Figure 33. The time $t_{MEASURED\_ENA}$ is the interval from when the reference signal switches to when the output voltage ramps ΔV from the measured three-stated output level. t_{RAMP} is calculated with test load C_L, drive current I_D, and with ΔV equal to 0.4 V.

Capacitive Loading

Output valid and hold are based on standard capacitive loads: 30 pF on all pins (see Figure 34). The delay and hold specifications given should be derated by a drive strength related factor for loads other than the nominal value of 30 pF. Figure 35 through Figure 42 show how output rise time varies with capacitance. Figure 43 graphically shows how output valid varies with load capacitance. (Note that this graph or derating does not apply to output disable delays; see Output Disable Time on Page 35.) The graphs of Figure 35 through Figure 43 may not be linear outside the ranges shown.

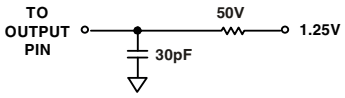

Figure 34. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

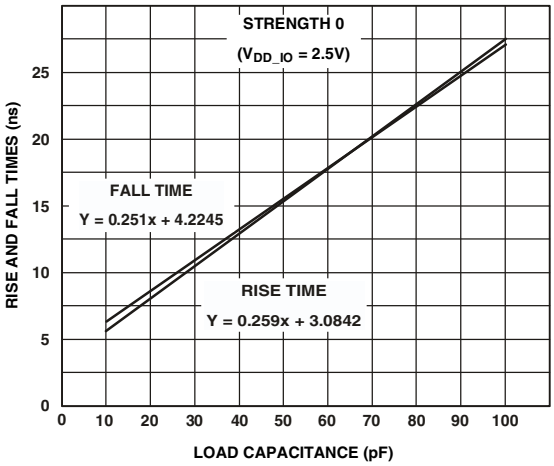

Figure 35. Typical Output Rise and Fall Time (10% to 90%, V_{DD_IO} = 2.5 V) vs. Load Capacitance at Strength 0

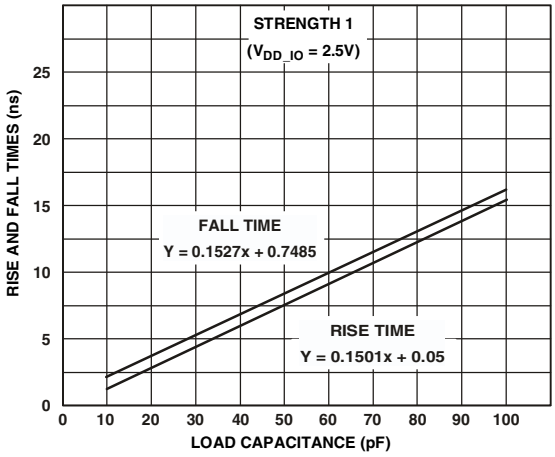

Figure 36. Typical Output Rise and Fall Time (10% to 90%, V_{DD_IO} = 2.5 V) vs. Load Capacitance at Strength 1

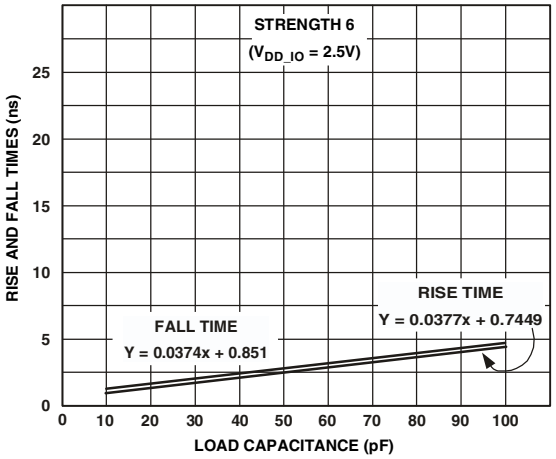

Figure 41. Typical Output Rise and Fall Time (10% to 90%, V_{DD_IO} = 2.5 V) vs. Load Capacitance at Strength 6

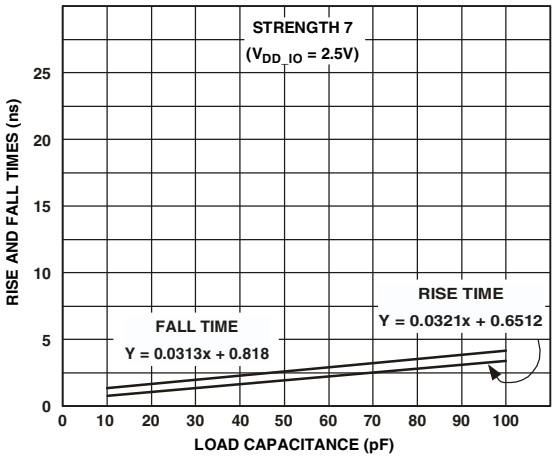

Figure 42. Typical Output Rise and Fall Time (10% to 90%, V_{DD_IO} = 2.5 V) vs. Load Capacitance at Strength 7

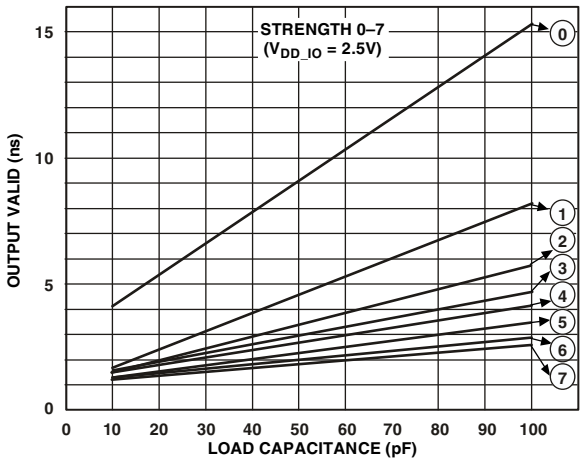

Figure 43. Typical Output Valid (V_{DD_IO} = 2.5 V) vs. Load Capacitance at Max Case Temperature and Strength 0 to 7[1]

[1] The line equations for the output valid vs. load capacitance are:
Strength 0: y = 0.0956x + 3.5662
Strength 1: y = 0.0523x + 3.2144
Strength 2: y = 0.0433x + 3.1319
Strength 3: y = 0.0391x + 2.9675
Strength 4: y = 0.0393x + 2.7653
Strength 5: y = 0.0373x + 2.6515
Strength 6: y = 0.0379x + 2.1206
Strength 7: y = 0.0399x + 1.9080

ENVIRONMENTAL CONDITIONS

The ADSP-TS203S processor is rated for performance under T_{CASE} environmental conditions specified in the Operating Conditions on Page 20.

Thermal Characteristics

The ADSP-TS203S processor is packaged in a 25 mm × 25 mm, thermally enhanced ball grid array (BGA_ED). The processor is specified for a case temperature (T_{CASE}). To ensure that the T_{CASE} data sheet specification is not exceeded, a heat sink and/or an air flow source may be required. Table 34 shows the thermal characteristics of the BGA_ED package. All parameters are based on a JESD51-9 four-layer 2s2p board. All data are based on 3 W power dissipation.

Table 34. Thermal Characteristics

Parameter	Condition	Typical	Unit
θ_{JA}[1]	Airflow = 0 m/s	12.9[2]	°C/W
	Airflow = 1 m/s	10.2	°C/W
	Airflow = 2 m/s	9.0	°C/W
	Airflow = 3 m/s	8.0	°C/W
θ_{JB}[3]	—	7.7	°C/W
θ_{JC}[4]	—	0.7	°C/W

[1] θ_{JA} measured per JEDEC standard JESD51-6.
[2] θ_{JA} = 12.9°C/W for 0 m/s is for vertically mounted boards. For horizontally mounted boards, use 17.0°C/W for 0 m/s.
[3] θ_{JB} measured per JEDEC standard JESD51-9.
[4] θ_{JC} measured by cold plate test method (no approved JEDEC standard).

576-BALL BGA_ED PIN CONFIGURATIONS

Figure 44 shows a summary of pin configurations for the 576-ball BGA_ED package, and Table 35 lists the signal-to-ball assignments.

Table 35. 576-Ball (25 mm × 25 mm) BGA_ED Ball Assignments

Ball No.	Signal Name	Ball No.	Signal Name	Ball No.	Signal Name	Ball No.	Signal Name
A1	V_{SS}	B1	NC	C1	V_{SS}	D1	NC
A2	NC	B2	V_{SS}	C2	V_{SS}	D2	NC
A3	V_{SS}	B3	V_{SS}	C3	V_{SS}	D3	NC
A4	NC	B4	NC	C4	NC	D4	V_{SS}
A5	NC	B5	NC	C5	NC	D5	NC
A6	NC	B6	NC	C6	NC	D6	NC
A7	NC	B7	NC	C7	NC	D7	NC
A8	NC	B8	NC	C8	NC	D8	NC
A9	DATA29	B9	DATA30	C9	DATA31	D9	NC
A10	DATA25	B10	DATA26	C10	DATA27	D10	DATA28
A11	DATA23	B11	DATA24	C11	DATA21	D11	DATA22
A12	DATA19	B12	DATA20	C12	DATA17	D12	DATA18
A13	DATA15	B13	DATA16	C13	V_{SS}	D13	V_{SS}
A14	DATA11	B14	DATA12	C14	DATA13	D14	DATA14
A15	DATA9	B15	DATA10	C15	DATA7	D15	DATA8
A16	DATA5	B16	DATA6	C16	DATA3	D16	DATA4
A17	DATA1	B17	DATA2	C17	ACK	D17	DATA0
A18	$\overline{WRL}$	B18	TM4	C18	$\overline{RD}$	D18	$\overline{BRST}$
A19	ADDR30	B19	ADDR31	C19	ADDR26	D19	ADDR27
A20	ADDR28	B20	ADDR29	C20	ADDR24	D20	ADDR25
A21	ADDR22	B21	ADDR23	C21	ADDR20	D21	V_{SS}
A22	V_{SS}	B22	V_{SS}	C22	V_{SS}	D22	ADDR19
A23	ADDR21	B23	V_{SS}	C23	V_{DD_IO}	D23	ADDR17
A24	V_{SS}	B24	ADDR18	C24	V_{DD_IO}	D24	ADDR16

Table 35. 576-Ball (25 mm × 25 mm) BGA_ED Ball Assignments (Continued)

Ball No.	Signal Name	Ball No.	Signal Name	Ball No.	Signal Name	Ball No.	Signal Name
AA1	FLAG2	AB1	V_{SS}	AC1	FLAG0	AD1	V_{SS}
AA2	FLAG1	AB2	V_{SS}	AC2	V_{SS}	AD2	ID1
AA3	$\overline{IRQ3}$	AB3	V_{SS}	AC3	V_{DD_IO}	AD3	V_{DD_IO}
AA4	V_{SS}	AB4	NC	AC4	TMS	AD4	$\overline{TRST}$
AA5	$\overline{IRQ0}$	AB5	$\overline{IRQ2}$	AC5	$\overline{IOWR}$	AD5	$\overline{IORD}$
AA6	$\overline{IOEN}$	AB6	$\overline{IRQ1}$	AC6	$\overline{DMAR2}$	AD6	$\overline{DMAR3}$
AA7	$\overline{DMAR0}$	AB7	$\overline{DMAR1}$	AC7	$\overline{CPA}$	AD7	$\overline{DPA}$
AA8	$\overline{HBR}$	AB8	$\overline{HBG}$	AC8	$\overline{BOFF}$	AD8	$\overline{BUSLOCK}$
AA9	TM3	AB9	V_{DD_IO}	AC9	NC	AD9	NC
AA10	NC	AB10	NC	AC10	NC	AD10	NC
AA11	NC	AB11	NC	AC11	NC	AD11	NC
AA12	V_{SS}	AB12	V_{SS}	AC12	V_{DD_IO}	AD12	V_{DD_IO}
AA13	V_{DD_IO}	AB13	V_{DD_IO}	AC13	V_{SS}	AD13	V_{DD_IO}
AA14	V_{DD_IO}	AB14	V_{DD_IO}	AC14	V_{DD_IO}	AD14	V_{DD_IO}
AA15	NC	AB15	V_{SS}	AC15	NC	AD15	V_{SS}
AA16	NC	AB16	NC	AC16	TM2	AD16	V_{DD_IO}
AA17	NC	AB17	NC	AC17	NC	AD17	NC
AA18	NC	AB18	NC	AC18	NC	AD18	NC
AA19	V_{SS}	AB19	V_{DD_IO}	AC19	V_{DD_IO}	AD19	V_{DD_IO}
AA20	V_{DD_IO}	AB20	V_{DD_IO}	AC20	V_{DD_IO}	AD20	V_{DD_IO}
AA21	V_{SS}	AB21	NC	AC21	V_{DD_IO}	AD21	V_{DD_IO}
AA22	$\overline{L1BCMPO}$	AB22	V_{SS}	AC22	V_{DD_IO}	AD22	V_{DD_IO}
AA23	L1DATO0_N	AB23	V_{DD_IO}	AC23	V_{SS}	AD23	V_{SS}
AA24	L1DATO0_P	AB24	V_{DD_IO}	AC24	L1ACKI	AD24	V_{SS}

[1] On revision 1.x silicon, the R2 and R3 balls are NC. On revision 0.x silicon, the R2 ball is SCLK, and the R3 ball is SCLK_V_{REF}. For more information on SCLK and SCLK_V_{REF} on revision 0.x silicon, see *EE-179: ADSP-TS20x TigerSHARC System Design Guidelines*.

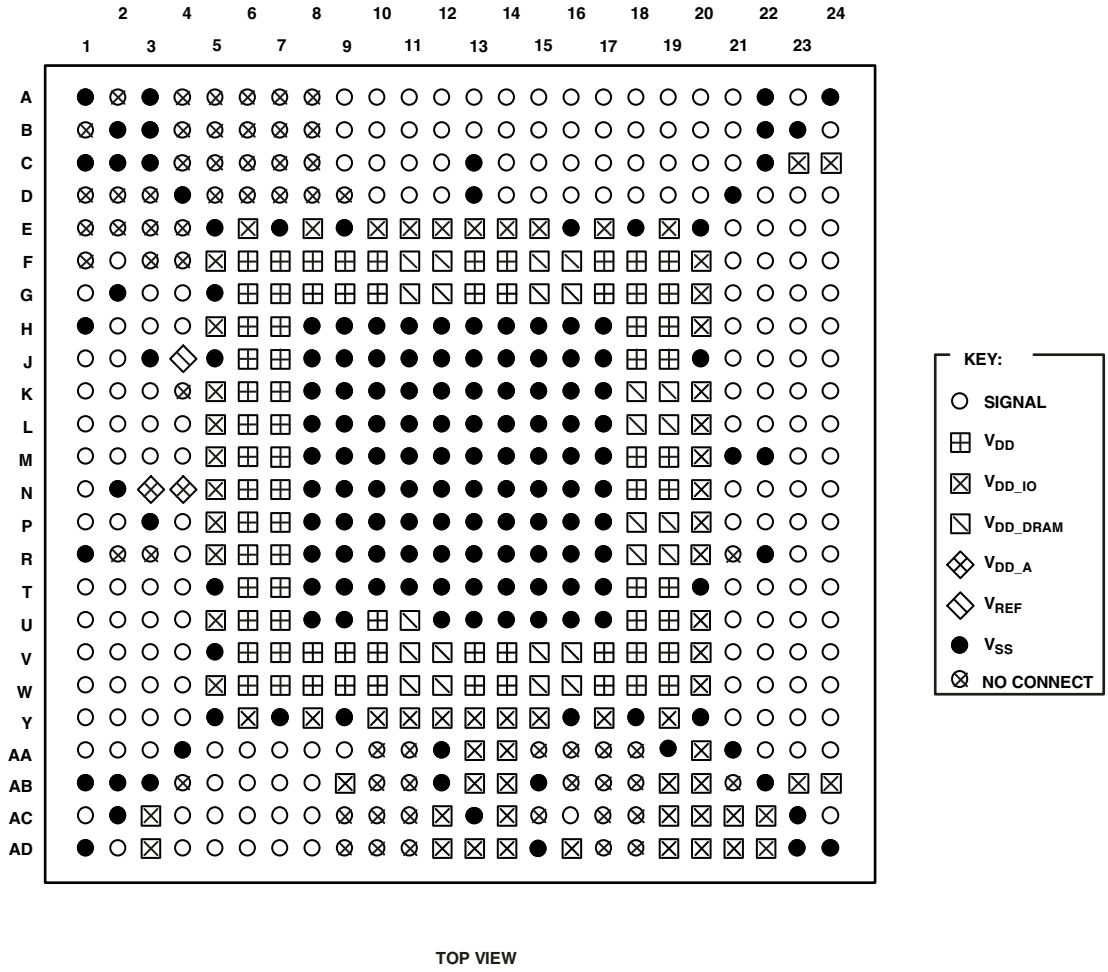

Figure 44. 576-Ball BGA_ED Pin Configurations[1] (Top View, Summary)

[1] For a more detailed pin summary diagram, see *EE-179: ADSP-TS20x TigerSHARC System Design Guidelines*.

OUTLINE DIMENSIONS

The ADSP-TS203S processor is available in a 25 mm × 25 mm, 576-ball metric thermally enhanced ball grid array (BGA_ED) package with 24 rows of balls (BP-576).

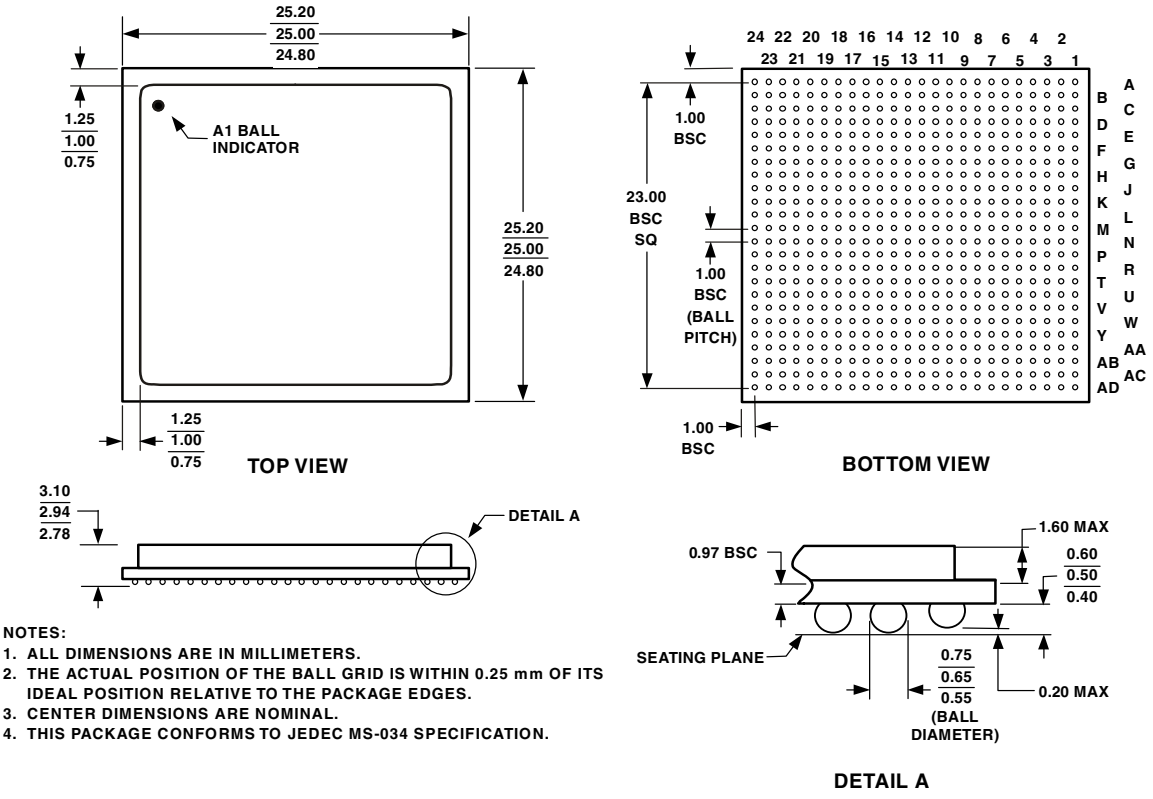

Figure 45. 576-Ball BGA_ED (BP-576)

SURFACE MOUNT DESIGN

The following table is provided as an aide to PCB design. The numbers listed in the table are for reference purposes and should not supersede the PCB design rules. Please reference IPC-7351, *Surface Mount Design and Land Pattern Standard*, for PCB design recommendations.

Package	Ball Attach Type	Solder Mask Opening	Ball Pad Size
576-Ball BGA_ED (BP-576-1)	Nonsolder Mask Defined (NSMD)	0.69	0.56