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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e500v2
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	Security; SEC
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 90°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8533evjanga

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



- Three PCI Express interfaces
 - Two \times 4 link width interfaces and one \times 1 link width interface
 - PCI Express 1.0a compatible
 - Auto-detection of number of connected lanes
 - Selectable operation as root complex or endpoint
 - Both 32- and 64-bit addressing
 - 256-byte maximum payload size
 - Virtual channel 0 only
 - Traffic class 0 only
 - Full 64-bit decode with 32-bit wide windows
- Power management
 - Supports power saving modes: doze, nap, and sleep
 - Employs dynamic power management, which automatically minimizes power consumption of blocks when they are idle
- System performance monitor
 - Supports eight 32-bit counters that count the occurrence of selected events
 - Ability to count up to 512 counter-specific events
 - Supports 64 reference events that can be counted on any of the 8 counters
 - Supports duration and quantity threshold counting
 - Burstiness feature that permits counting of burst events with a programmable time between bursts
 - Triggering and chaining capability
 - Ability to generate an interrupt on overflow
- System access port
 - Uses JTAG interface and a TAP controller to access entire system memory map
 - Supports 32-bit accesses to configuration registers
 - Supports cache-line burst accesses to main memory
 - Supports large block (4-Kbyte) uploads and downloads
 - Supports continuous bit streaming of entire block for fast upload and download
- IEEE Std 1149.1[™]-compliant, JTAG boundary scan
- 783 FC-PBGA package



4.2 Real-Time Clock Timing

The RTC input is sampled by the platform clock (CCB clock). The output of the sampling latch is then used as an input to the counters of the PIC and the TimeBase unit of the e500. There is no jitter specification. The minimum pulse width of the RTC signal should be greater than $2 \times$ the period of the CCB clock. That is, minimum clock high time is $2 \times t_{CCB}$, and minimum clock low time is $2 \times t_{CCB}$. There is no minimum RTC frequency; RTC may be grounded if not needed.

4.3 eTSEC Gigabit Reference Clock Timing

Table 7 provides the eTSEC gigabit reference clocks (EC_GTX_CLK125) AC timing specifications for the MPC8533E.

Parameter/Condition	Symbol	Min	Тур	Max	Unit	Notes
EC_GTX_CLK125 frequency	f _{G125}	—	125	—	MHz	_
EC_GTX_CLK125 cycle time	t _{G125}		8	_	ns	_
EC_GTX_CLK rise and fall time LV_{DD} , $TV_{DD} = 2.5 V$ LV_{DD} , $TV_{DD} = 3.3 V$	t _{G125R} /t _{G125F}	_	_	0.75 1.0	ns	1
EC_GTX_CLK125 duty cycle GMII, TBI 1000Base-T for RGMII, RTBI	t _{G125H} /t _{G125}	45 47	—	55 53	%	2

Table 7. EC_GTX_CLK125 AC Timing Specifications

Notes:

1. Rise and fall times for EC_GTX_CLK125 are measured from 0.5 and 2.0 V for L/TV_{DD} = 2.5 V, and from 0.6 and 2.7 V for L/TVDD = 3.3 V.

EC_GTX_CLK125 is used to generate the GTX clock for the eTSEC transmitter with 2% degradation. EC_GTX_CLK125 duty cycle can be loosened from 47%/53% as long as the PHY device can tolerate the duty cycle generated by the eTSEC GTX_CLK. See Section 8.5.4, "RGMII and RTBI AC Timing Specifications," for duty cycle for 10Base-T and 100Base-T reference clock.

4.4 Platform to FIFO Restrictions

Please note the following FIFO maximum speed restrictions based on platform speed.

For FIFO GMII mode:

FIFO TX/RX clock frequency \leq platform clock frequency \div 4.2

For example, if the platform frequency is 533 MHz, the FIFO Tx/Rx clock frequency should be no more than 127 MHz.

For FIFO encoded mode:

FIFO TX/RX clock frequency \leq platform clock frequency \div 3.2

For example, if the platform frequency is 533 MHz, the FIFO Tx/Rx clock frequency should be no more than 167 MHz.



Enhanced Three-Speed Ethernet (eTSEC), MII Management

8.2 eTSEC DC Electrical Characteristics

All GMII, MII, TBI, RGMII, RTBI, RMII, and FIFO drivers and receivers comply with the DC parametric attributes specified in Table 21 and Table 22. The potential applied to the input of a GMII, MII, TBI, RTBI, RMII, and FIFO receiver may exceed the potential of the receiver's power supply (that is, a GMII driver powered from a 3.6-V supply driving V_{OH} into a GMII receiver powered from a 2.5-V supply). Tolerance for dissimilar GMII driver and receiver supply potentials is implicit in these specifications. The RGMII and RTBI signals are based on a 2.5-V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

Parameter	Symbol	Min	Мах	Unit	Notes
Supply voltage 3.3 V	LV _{DD} TV _{DD}	3.135	3.465	V	1, 2
Output high voltage ($LV_{DD}/TV_{DD} = Min$, $I_{OH} = -4.0 \text{ mA}$)	V _{OH}	2.4	_	V	_
Output low voltage ($LV_{DD}/TV_{DD} = Min$, $I_{OL} = 4.0 mA$)	V _{OL}	—	0.5	V	_
Input high voltage	V _{IH}	1.95	_	V	_
Input low voltage	V _{IL}	—	0.90	V	_
Input high current ($V_{IN} = LV_{DD}$, $V_{IN} = TV_{DD}$)	Ι _Η	—	40	μA	1, 2, 3
Input low current (V _{IN} = GND)	IIL	-600	_	μA	3

Table 21.	GMII, MII,	, TBI, RMII	and FIFO	DC Electrical	Characteristics
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Notes:

1. LV_{DD} supports eTSEC1.

2. TV_{DD} supports eTSEC3.

3. The symbol V_{IN} , in this case, represents the LV_{IN} and TV_{IN} symbols referenced in Table 1 and Table 2.

Table 22. GMII,	MII, RMII,	RGMII, RTBI,	TBI, and FIFC	DC Electric	al Character	istics	
							_

Parameters	Symbol	Min	Max	Unit	Notes
Supply voltage 2.5 V	LV_{DD}/TV_{DD}	2.375	2.625	V	1, 2
Output high voltage ($LV_{DD}/TV_{DD} = Min$, $I_{OH} = -1.0 mA$)	V _{OH}	2.0	_	V	_
Output low voltage ($LV_{DD}/TV_{DD} = Min$, $I_{OL} = 1.0 mA$)	V _{OL}	_	0.4	V	_
Input high voltage	V _{IH}	1.70	_	V	_
Input low voltage	V _{IL}	_	0.7	V	_
Input current ($V_{IN} = 0$, $V_{IN} = LV_{DD}$, $V_{IN} = TV_{DD}$)	I _{IN}	—	±15	μA	1, 2, 3

Notes:

1. LV_{DD} supports eTSEC1.

2. TV_{DD} supports eTSEC3.

3. The symbol V_{IN}, in this case, represents the LV_{IN} and TV_{IN} symbols referenced in Table 1 and Table 2.



Enhanced Three-Speed Ethernet (eTSEC), MII Management

Table 28. MII Receive AC Timing Specifications (continued)

At recommended operating conditions with L/TVDD of 3.3 V \pm 5%.or 2.5 V \pm 5%.

Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit	Notes
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t _{MRDVKH}	10.0	—	—	ns	—
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t _{MRDXKH}	10.0	—	—	ns	—
RX_CLK clock rise (20%–80%)	t _{MRXR}	1.0	—	4.0	ns	—
RX_CLK clock fall time (80%–20%)	t _{MRXF}	1.0	—	4.0	ns	—

Note:

1. The symbols used for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).}}

Figure 13 provides the AC test load for eTSEC.



Figure 13. eTSEC AC Test Load

Figure 14 shows the MII receive AC timing diagram.



Figure 14. MII Receive AC Timing Diagram

8.5 TBI AC Timing Specifications

This section describes the TBI transmit and receive AC timing specifications.



8.5.1 TBI Transmit AC Timing Specifications

Table 29 provides the TBI transmit AC timing specifications.

Table 29. TBI Transmit AC Timing Specifications

At recommended operating conditions with L/TVDD of 3.3 V \pm 5% or 2.5 V \pm 5%

Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit	Notes
GTX_CLK clock period	t _{GTX}	—	8.0	_	ns	—
GTX_CLK to TCG[9:0] delay time	t _{TTKHDX}	0.2	—	5.0	ns	2
GTX_CLK rise (20%–80%)	t _{TTXR}	—	—	1.0	ns	—
GTX_CLK fall time (80%–20%)	t _{TTXF}	—	—	1.0	ns	—

Notes:

1. The symbols used for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{TTKHDV} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, t_{TTKHDX} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, t_{TTKHDX} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the invalid state (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TTX} represents the TBI (T) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).}

Figure 15 shows the TBI transmit AC timing diagram.



Figure 15. TBI Transmit AC Timing Diagram

8.5.2 TBI Receive AC Timing Specifications

Table 30 provides the TBI receive AC timing specifications.

Table 30. TBI Receive AC	Timing Specifications
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At recommended operating conditions with L/TVDD of 3.3 V \pm 5% or 2.5 V \pm 5%.

Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit	Notes
PMA_RX_CLK[0:1] clock period	t _{TRX}	_	16.0	_	ns	_
PMA_RX_CLK[0:1] skew	t _{SKTRX}	7.5		8.5	ns	_

Data valid t_{TTKHDV} to GTX_CLK Min setup time is a function of clock period and max hold time (Min setup = cycle time – Max delay).



8.5.5 RMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.

8.5.5.1 RMII Transmit AC Timing Specifications

The RMII transmit AC timing specifications are in Table 33.

Table 33. RMII Transmit AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V \pm 5% or 2.5 V \pm 5%.

Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit	Notes
REF_CLK clock period	t _{RMT}	15.0	20.0	25.0	ns	—
REF_CLK duty cycle	t _{RMTH}	35	50	65	%	—
REF_CLK peak-to-peak jitter	t _{RMTJ}	-	_	250	ps	—
Rise time REF_CLK (20%–80%)	t _{RMTR}	1.0	_	2.0	ns	—
Fall time REF_CLK (80%–20%)	t _{RMTF}	1.0	_	2.0	ns	—
REF_CLK to RMII data TXD[1:0], TX_EN delay	t _{RMTDX}	1.0	_	10.0	ns	—

Note:

The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t<sub>(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
</sub></sub>

Figure 19 shows the RMII transmit AC timing diagram.



Figure 19. RMII Transmit AC Timing Diagram



Table 40. Local Bus General Timing Parameters (BV_{DD} = 3.3 V)—PLL Enabled (continued)

Parameter	Symbol ¹	Min	Max	Unit	Notes
Local bus clock to output high impedance for LAD/LDP	t _{LBKHOZ2}	_	2.5	ns	5

Notes:

The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{LBIXKH1} symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one (1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
</sub>

2. All timings are in reference to LSYNC_IN for PLL enabled and internal local bus clock for PLL bypass mode.

3. All signals are measured from $BV_{DD}/2$ of the rising edge of LSYNC_IN for PLL enabled or internal local bus clock for PLL bypass mode to $0.4 \times BV_{DD}$ of the signal in question for 3.3-V signaling levels.

4. Input timings are measured at the pin.

5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

- t_{LBOTOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. t_{LBOTOT} is programmed with the LBCR[AHD] parameter.
- 7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at BV_{DD}/2.

Table 41 describes the general timing parameters of the local bus interface at $BV_{DD} = 2.5$ V.

Parameter	Symbol ¹	Min	Мах	Unit	Notes
Local bus cycle time	t _{LBK}	7.5	12	ns	2
Local bus duty cycle	t _{LBKH} /t _{LBK}	43	57	%	—
LCLK[n] skew to LCLK[m] or LSYNC_OUT	t _{LBKSKEW}	—	150	ps	7
Input setup to local bus clock (except LUPWAIT)	t _{LBIVKH1}	2.4	—	ns	3, 4
LUPWAIT input setup to local bus clock	t _{LBIVKH2}	1.8	—	ns	3, 4
Input hold from local bus clock (except LUPWAIT)	t _{LBIXKH1}	1.1	—	ns	3, 4
LUPWAIT input hold from local bus clock	t _{LBIXKH2}	1.1	—	ns	3, 4
LALE output transition to LAD/LDP output transition (LATCH setup and hold time)	t _{lbotot}	1.5	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	t _{LBKHOV1}	—	2.8	ns	—
Local bus clock to data valid for LAD/LDP	t _{LBKHOV2}	—	2.8	ns	3
Local bus clock to address valid for LAD	t _{LBKHOV3}	—	2.8	ns	3
Local bus clock to LALE assertion	t _{LBKHOV4}	—	2.8	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	t _{LBKHOX1}	0.8	—	ns	3
Output hold from local bus clock for LAD/LDP	t _{LBKHOX2}	0.8	—	ns	3
Local bus clock to output high Impedance (except LAD/LDP and LALE)	t _{LBKHOZ1}	—	2.6	ns	5

Table 41. Local Bus General Timing Parameters (BV_{DD} = 2.5 V)—PLL Enabled



Table 41. Local Bus General Timing Parameters (BV_{DD} = 2.5 V)—PLL Enabled (continued)

Parameter	Symbol ¹	Min	Мах	Unit	Notes
Local bus clock to output high impedance for LAD/LDP	t _{LBKHOZ2}	_	2.6	ns	5

Notes:

The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(First two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{LBIXKH1} symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one (1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the output (O) going invalid (X) or output hold time.
</sub>

2. All timings are in reference to LSYNC_IN for PLL enabled and internal local bus clock for PLL bypass mode.

3. All signals are measured from $BV_{DD}/2$ of the rising edge of LSYNC_IN for PLL enabled or internal local bus clock for PLL bypass mode to 0.4 × BV_{DD} of the signal in question for 2.5-V signaling levels.

4. Input timings are measured at the pin.

5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

- 6. t_{LBOTOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. t_{LBOTOT} is programmed with the LBCR[AHD] parameter.
- 7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at BV_{DD}/2.

Table	42	describes	the	general	timing	parameters	of the	local b	bus inte	rface at	$BV_{DD} =$	1.8	V D	C.

Parameter	Symbol ¹	Min	Мах	Unit	Notes
Local bus cycle time	t _{LBK}	7.5	12	ns	2
Local bus duty cycle	t _{LBKH/} t _{LBK}	43	57	%	_
LCLK[n] skew to LCLK[m] or LSYNC_OUT	t _{LBKSKEW}	—	150	ps	7
Input setup to local bus clock (except LUPWAIT)	t _{LBIVKH1}	2.6	—	ns	3, 4
LUPWAIT input setup to local bus clock	t _{LBIVKH2}	1.9	—	ns	3, 4
Input hold from local bus clock (except LUPWAIT)	t _{LBIXKH1}	1.1	—	ns	3, 4
LUPWAIT input hold from local bus clock	t _{LBIXKH2}	1.1	—	ns	3, 4
LALE output transition to LAD/LDP output transition (LATCH setup and hold time)	t _{lbotot}	1.2	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	t _{LBKHOV1}	—	3.2	ns	_
Local bus clock to data valid for LAD/LDP	t _{LBKHOV2}	—	3.2	ns	3
Local bus clock to address valid for LAD	t _{LBKHOV3}	—	3.2	ns	3
Local bus clock to LALE assertion	t _{LBKHOV4}	—	3.2	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	t _{LBKHOX1}	0.9	—	ns	3
Output hold from local bus clock for LAD/LDP	t _{LBKHOX2}	0.9	—	ns	3
Local bus clock to output high Impedance (except LAD/LDP and LALE)	t _{LBKHOZ1}	—	2.6	ns	5

Table 42. Local Bus General Timing Parameters (BV_{DD} = 1.8 V DC)



Figure 24 through Figure 29 show the local bus signals.



Table 43 describes the general timing parameters of the local bus interface at V_{DD} = 3.3 V DC with PLL disabled.

Parameter	Symbol ¹	Min	Мах	Unit	Notes
Local bus cycle time	t _{LBK}	12	—	ns	2
Local bus duty cycle	t _{LBKH/} t _{LBK}	43	57	%	_
Internal launch/capture clock to LCLK delay	t _{lbkhkt}	1.2	4.9	ns	—
Input setup to local bus clock (except LUPWAIT)	t _{LBIVKH1}	7.4	—	ns	4, 5
LUPWAIT input setup to local bus clock	t _{LBIVKL2}	6.75	—	ns	4, 5
Input hold from local bus clock (except LUPWAIT)	t _{LBIXKH1}	-0.2	—	ns	4, 5
LUPWAIT input hold from local bus clock	t _{LBIXKL2}	-0.2	—	ns	4, 5
LALE output transition to LAD/LDP output transition (LATCH hold time)	t _{lbotot}	1.5	_	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	t _{LBKLOV1}	—	1.6	ns	—

Table 43. Local Bus General Timing Parameters—PLL Bypassed



Parameter	Symbol ¹	Min	Max	Unit	Notes
Local bus clock to data valid for LAD/LDP	t _{LBKLOV2}	_	1.6	ns	4
Local bus clock to address valid for LAD, and LALE	t _{LBKLOV3}	_	1.6	ns	4
Output hold from local bus clock (except LAD/LDP and LALE)	t _{LBKLOX1}	-4.1	_	ns	4
Output hold from local bus clock for LAD/LDP	t _{LBKLOX2}	-4.1	_	ns	4
Local bus clock to output high Impedance (except LAD/LDP and LALE)	t _{LBKLOZ1}	_	1.4	ns	7
Local bus clock to output high impedance for LAD/LDP	t _{LBKLOZ2}	_	1.4	ns	7

Table 43. Local Bus General Timing Parameters—PLL Bypassed (continued)

Notes:

- The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{LBIXKH1} symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one (1). Also, t_{LBKH0X} symbolizes local bus timing (LB) for the output (O) going invalid (X) or output hold time.
 </sub>
- All timings are in reference to local bus clock for PLL bypass mode. Timings may be negative with respect to the local bus clock because the actual launch and capture of signals is done with the internal launch/capture clock, which proceeds LCLK by t_{LBKHKT}.
- 3. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at BV_{DD}/2.
- 4. All signals are measured from BV_{DD}/2 of the rising edge of local bus clock for PLL bypass mode to 0.4 × BV_{DD} of the signal in question for 3.3-V signaling levels.
- 5. Input timings are measured at the pin.
- 6. The value of t_{LBOTOT} is the measurement of the minimum time between the negation of LALE and any change in LAD.
- 7. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.



Local Bus



Figure 25. Local Bus Signals (PLL Bypass Mode)

NOTE

In PLL bypass mode, LCLK[n] is the inverted version of the internal clock with the delay of t_{LBKHKT} . In this mode, signals are launched at the rising edge of the internal clock and are captured at falling edge of the internal clock withe the exception of LGTA/LUPWAIT (which is captured on the rising edge of the internal clock).





Figure 28. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 8 or 16 (PLL Enabled)



Figure 33 provides the boundary-scan timing diagram.



Figure 33. Boundary-Scan Timing Diagram

13 l²C

This section describes the DC and AC electrical characteristics for the I²C interfaces of the MPC8533E.

13.1 I²C DC Electrical Characteristics

Table 46 provides the DC electrical characteristics for the I²C interfaces.

Table 46. I²C DC Electrical Characteristics

At recommended operating conditions with OV_{DD} of 3.3 V \pm 5%.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage level	V _{IH}	$0.7\times \text{OV}_{\text{DD}}$	OV _{DD} + 0.3	V	_
Input low voltage level	V _{IL}	-0.3	$0.3\times\text{OV}_{\text{DD}}$	V	_
Low level output voltage	V _{OL}	0	$0.2\times\text{OV}_{\text{DD}}$	V	1
Pulse width of spikes which must be suppressed by the input filter	t _{I2KHKL}	0	50	ns	2
Input current each I/O pin (input voltage is between $0.1 \times OV_{DD}$ and $0.9 \times OV_{DD}$ (max)	I _I	-10	10	μA	3
Capacitance for each I/O pin	CI	_	10	pF	

Notes:

1. Output voltage (open drain or open collector) condition = 3 mA sink current.

2. Refer to the MPC8533E PowerQUICC III Integrated Communications Host Processor Reference Manual for information on the digital filter used.

3. I/O pins will obstruct the SDA and SCL lines if $\ensuremath{\mathsf{OV}_{\mathsf{DD}}}$ is switched off.



l²C

13.2 I²C AC Electrical Specifications

Table 47 provides the AC timing parameters for the I^2C interfaces.

Table 47. I²C AC Electrical Specifications

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 46).

Parameter	Symbol ¹	Min	Max	Unit	Notes
SCL clock frequency	f _{I2C}	0	400	kHz	
Low period of the SCL clock	t _{I2CL}	1.3	_	μs	_
High period of the SCL clock	t _{I2CH}	0.6	_	μs	_
Setup time for a repeated START condition	t _{I2SVKH}	0.6	_	μs	_
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t _{i2SXKL}	0.6	_	μs	—
Data setup time	t _{i2DVKH}	100	_	ns	—
Data hold time: CBUS compatible masters I ² C bus devices	t _{I2DXKL}	0		μs	2
Data output delay time	t _{I2OVKL}	—	0.9		3
Set-up time for STOP condition	t _{I2PVKH}	0.6	_	μs	—
Rise time of both SDA and SCL signals	t _{I2CR}	20 + 0.1 C _b	300	ns	4
Fall time of both SDA and SCL signals	t _{I2CF}	20 + 0.1 C _b	300	ns	4
Bus free time between a STOP and START condition	t _{I2KHDX}	1.3	_	μs	—
Noise margin at the LOW level for each connected device (including hysteresis)	V _{NL}	$0.1 \times OV_{DD}$	_	V	—
Noise margin at the HIGH level for each connected device (including hysteresis)	V _{NH}	$0.2 \times OV_{DD}$	_	V	—

Notes:

- The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{12DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{12C} clock reference (K) going to the high (H) state or setup time. Also, t_{12SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{12C} clock reference (K) going to the stop condition (P) reaching the valid state (V) relative to the t_{12C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
 </sub>
- The MPC8533E provides a hold time of at least 300 ns for the SDA signal (referred to the V_{IH}min of the SCL signal) to bridge the undefined region of the falling edge of SCL.
- 3. The maximum t_{I2DXKL} has only to be met if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.
- 4. C_B = capacitance of one bus line in pF.



Symbol	Parameter	Min	Nom	Мах	Units	Comments
T _{RX-EYE-MEDIAN-to-MAX} -JITTER	Maximum time between the jitter median and maximum deviation from the median		_	0.3	UI	Jitter is defined as the measurement variation of the crossing points ($V_{RX-DIFFp-p}$ = 0 V) in relation to a recovered TX UI. A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI. See Notes 2, 3, and 7.
V _{RX-CM-ACp}	AC peak common mode input voltage	_	_	150	mV	$ \begin{split} & V_{RX-CM-ACp} = V_{RXD+} - V_{RXD-} \div 2 - \\ & V_{RX-CM-DC} \\ & V_{RX-CM-DC} = DC_{(avg)} \text{ of } V_{RX-D+} - V_{RX-D-} /2 \\ & See Note 2. \end{split} $
RL _{RX-DIFF}	Differential return loss	15	—	—	dB	Measured over 50 MHz to 1.25 GHz with the D+ and D– lines biased at +300 and –300 mV, respectively. See Note 4.
RL _{RX-CM}	Common mode return loss	6			dB	Measured over 50 MHz to 1.25 GHz with the D+ and D– lines biased at 0 V. See Note 4.
Z _{RX-DIFF-DC}	DC differential input impedance	80	100	120	Ω	RX DC differential mode impedance. See Note 5.
Z _{RX-DC}	DC input impedance	40	50	60	Ω	Required RX D+ as well as D– DC impedance (50 \pm 20% tolerance). See Notes 2 and 5.
Z _{RX-HIGH-IMP-DC}	Powered down DC input impedance	200 k	_		Ω	Required RX D+ as well as D– DC impedance when the receiver terminations do not have power. See Note 6.
V _{RX-IDLE-DET-DIFFp-p}	Electrical idle detect threshold	65	—	175	mV	$V_{RX-IDLE-DET-DIFFp-p} = 2 \times IV_{RX-D+} - V_{RX-D-}I$ Measured at the package pins of the receiver.
T _{RX-IDLE-DET-DIFF-} ENTERTIME	Unexpected electrical idle enter detect threshold integration time	—	—	10	ms	An unexpected electrical idle ($V_{RX-DIFFp-p}$ < $V_{RX-IDLE-DET-DIFFp-p}$) must be recognized no longer than $T_{RX-IDLE-DET-DIFF-ENTERING}$ to signal an unexpected idle condition.



Table 55. Differential Receiver (RX) Input Specifications (continued)

Symbol	Parameter	Min	Nom	Max	Units	Comments
L _{TX-SKEW}	Total skew			20	ns	Skew across all lanes on a link. This includes variation in the length of SKP ordered set (for example, COM and one to five symbols) at the RX as well as any delay differences arising from the interconnect itself.

Notes:

- 1. No test load is necessarily associated with this value.
- 2. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 54 should be used as the RX device when taking measurements (also refer to the receiver compliance eye diagram shown in Figure 53). If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
- 3. A T_{RX-EYE} = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the transmitter and interconnect collected any 250 consecutive UIs. The TRX-EYE-MEDIAN-to-MAX-JITTER specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.
- 4. The receiver input impedance shall result in a differential return loss greater than or equal to 15 dB with the D+ line biased to 300 mV and the D– line biased to -300 mV and a common mode return loss greater than or equal to 6 dB (no bias required) over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements for is 50 Ω to ground for both the D+ and D– line (that is, as measured by a vector network analyzer with 50- Ω probes, see Figure 54). Note that the series capacitors CTX is optional for the return loss measurement.
- 5. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5-ms transition time before receiver termination values must be met on all unconfigured lanes of a port.
- 6. The RX DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit will not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the RX ground.
- 7. It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

17.5 Receiver Compliance Eye Diagrams

The RX eye diagram in Figure 53 is specified using the passive compliance/test measurement load (see Figure 54) in place of any real PCI Express RX component.

In general, the minimum receiver eye diagram measured with the compliance/test measurement load (see Figure 54) will be larger than the minimum receiver eye diagram measured over a range of systems at the input receiver of any real PCI Express component. The degraded eye diagram at the input receiver is due to traces internal to the package as well as silicon parasitic characteristics which cause the real PCI Express component to vary in impedance from the compliance/test measurement load. The input receiver eye diagram is implementation specific and is not specified. RX component designer should provide additional margin to adequately compensate for the degraded minimum receiver eye diagram (shown in Figure 53) expected at the input receiver based on some adequate combination of system simulations and the return loss measured looking into the RX package and silicon. The RX eye diagram must be aligned in time using the jitter median to locate the center of the eye diagram.



Package Description

18 Package Description

This section details package parameters, pin assignments, and dimensions.

18.1 Package Parameters for the MPC8533E FC-PBGA

The package parameters for flip chip plastic ball grid array (FC-PBGA) are provided in Table 56.

Parameter	PBGA ¹
Package outline	29 mm × 29 mm
Interconnects	783
Ball pitch	1 mm
Ball diameter (typical)	0.6 mm
Solder ball (Pb-free)	96.5% Sn 3.5% Ag

Table 56. Package Parameters

Note:

1. (FC-PBGA) without a lid.



Package Description

Signal	Package Pin Number	Pin Type	Power Supply	Notes		
LCS6/DMA_DACK2	J16	0	BV _{DD}	1		
LCS7/DMA_DDONE2	L18	0	BV _{DD}	1		
LWE0/LBS0/LSDDQM[0]	J22	0	BV _{DD}	4, 8		
LWE1/LBS1/LSDDQM[1]	H22	0	BV _{DD}	4, 8		
LWE2/LBS2/LSDDQM[2]	H23	0	BV _{DD}	4, 8		
LWE3/LBS3/LSDDQM[3]	H21	0	BV _{DD}	4, 8		
LALE	J26	0	BV _{DD}	4, 7, 8		
LBCTL	J25	0	BV _{DD}	4, 7, 8		
LGPL0/LSDA10	J20	0	BV _{DD}	4, 8		
LGPL1/LSDWE	К20	0	BV _{DD}	4, 8		
LGPL2/LOE/LSDRAS	G20	0	BV _{DD}	4, 7, 8		
LGPL3/LSDCAS	H18	0	BV _{DD}	4, 8		
LGPL4/LGTA/LUPWAIT/ LPBSE	L20	I/O	BV _{DD}	28		
LGPL5	K19	0	BV _{DD}	4, 8		
LCKE	L17	0	BV _{DD}	—		
LCLK[0:2]	H24, J24, H25	0	BV _{DD}	—		
LSYNC_IN	D27	I	BV _{DD}	—		
LSYNC_OUT	D28	0	BV _{DD}	—		
	DMA					
DMA_DACK[0:1]	Y13, Y12	0	OV _{DD}	4, 8, 9		
DMA_DREQ[0:1]	AA10, AA11	I	OV _{DD}	—		
DMA_DDONE[0:1]	AA7, Y11	0	OV _{DD}	—		
Programmable Interrupt Controller						
UDE	AH15	I	OV _{DD}	—		
MCP	AG18	I	OV _{DD}	—		
IRQ[0:7]	AG22, AF17, AD21, AF19, AG17, AF16, AC23, AC22	I	OV _{DD}	—		
IRQ[8]	AC19	I	OV _{DD}	—		
IRQ[9]/DMA_DREQ3	AG20	I	OV _{DD}	1		
IRQ[10]/DMA_DACK3	AE27	I/O	OV _{DD}	1		
IRQ[11]/DMA_DDONE3	AE24	I/O	OV _{DD}	1		
IRQ_OUT	AD14	0	OV _{DD}	2		

Table 57. MPC8533E Pinout Listing (continued)



Table 57. MPC8533E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes		
6.The value of LA[28:31] during reset sets the CCB clock to SYSCLK PLL ratio. These pins require 4.7-kΩ pull-up or pull-down						
7.The value of LALE, LGPL	2, and LBCTL at reset set the e500 core clock to	CCB clock PLL ra	tio. These pins req	uire 4.7-k Ω		
 8. Functionally, this pin is an output, but structurally it is an I/O because it either samples configuration input during reset or because it has other manufacturing test functions. Therefore, this pin will be described as an I/O for boundary scan. 						
9.For proper state of these signals during reset, these pins can be left without any pull downs, thus relying on the internal pullup to get the values to the require 2'b11. However, if there is any device on the net which might pull down the value of the net at reset, then a pullup is needed.						
10. This output is actively driven during reset rather than being three-stated during reset.						
11. These JTAG pins have weak internal pull-up P-FETs that are always enabled.						
12. These pins are connected to the V _{DD} /GND planes internally and may be used by the core power supply to improve tracking and regulation.						
13.Anode and cathode of internal thermal diode.						
14. Treat pins AC7, T5, V2, and M7 as spare configuration pins cfg_spare[0:3]. The spare pins are unused POR config pins. It is highly recommended that the customer provide the capability of setting these pins low (that is, pull-down resistor which is not currently stuffed) in order to support new config options should they arise between revisions.						
15.If this pin is connected to a device that pulls down during reset, an external pull-up is required to drive this pin to a safe state during reset.						
16. This pin is only an output in FIFO mode when used as Rx flow control.						
17.Do not connect.						
18. These are test signals for factory use only and must be pulled up (100 Ω to 1 k Ω) to OV _{DD} for normal machine operation.						
19. Independent supplies derived from board V_{DD} .						
20. Recommend a pull-up resistor (1 K~) be placed on this pln to UV _{DD} .						
MSRCID[2:4], and ASLE	EP.	EI_REQ, IRIG_O	UT/READT/QUIES	GCE,		
22.This pin requires an extern driven.	22. This pin requires an external 4.7-kΩ pull-down resistor to prevent PHY from seeing a valid transmit enable before it is actively driven.					
23.General-purpose POR co	23.General-purpose POR configuration of user system.					
4. When a PCI block is disabled, either the POR config pin that selects between internal and external arbiter must be pulled						

- down to select external arbiter if there is any other PCI device connected on the PCI bus, or leave the address pins as No Connect or terminated through 2–10 kΩ pull-up resistors with the default of internal arbiter if the address pins are not connected to any other PCI device. The PCI block will drive the address pins if it is configured to be the PCI arbiter—through POR config pins—irrespective of whether it is disabled via the DEVDISR register or not. It may cause contention if there is any other PCI device connected on the bus.
- 25.MDIC0 is grounded through an 18.2-Ω precision 1% resistor and MDIC1 is connected GV_{DD} through an 18.2-Ω precision 1% resistor. These pins are used for automatic calibration of the DDR IOs.
- 26.Connect to GND.
- 27.Connect to GND.
- 28. For systems that boot from a local bus (GPCM)-controlled flash, a pull-up on LGPL4 is required.



23 Document Revision History

This table provides a revision history for the MPC8533E hardware specification.

Table 71. MPC8533E Document Revision History

Revision	Date	Substantive Change(s)	
8	09/2015	• In Table 10 and Table 12, removed the output leakage current rows and removed table note 4.	
7	06/2014	 In Table 70, "Device Nomenclature," added full Pb-free part code. In Table 70, "Device Nomenclature," added footnotes 3 and 4. 	
6	05/2011	Updated the value of t _{JTKLDX} to 2.5 ns from 4ns in Table 45.	
5	01/2011	Updated Table 70.	
4	09/2010	 Modified local bus information in Section 1.1, "Key Features," to show max local bus frequency as 133 MHz. Added footnote 28 to Table 57. Updated solder-ball parameter in Table 56. 	
3	11/2009	 Update Section 20.3.4, "Temperature Diode," Update Table 56 Package Parameters from 95.5%sn to 96.5%sn 	
2	01/2009	 Update power number table to include 1067 MHz/533 MHz power numbers. Remove Part number tables from Hardware spec. The part numbers are available on Freescale web site product page. Removed I/O power numbers from the Hardware spec. and added the table to bring-up guide applacation note Updated RX_CLK duty cycle min, and max value to meet the industry standard GMII duty cycle. In Table 35, removed note 1 and renumbered remaining note. Update paragraph Section 21.3, "Decoupling Recommendations Update t_{DDKHMP}, t_{DDKHME} in Table 18 Update Figure 5 DDR Output Timing Diagram 	
1	06/2008	Update in Table 18 DDR SDRAM Output AC Timing Specifications tMCK Max value Improvement to Section 16, "High-Speed Serial Interfaces (HSSI) Update Figure 55 Mechanical Dimensions Update in Table 43 Local Bus General Timing Parameters—PLL Bypassed	
0	04/2008	Initial release.	