Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	PowerPC e500v2
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	Security; SEC
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 90°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8533evtang

  - Two key (K1, K2, K1) or three key (K1, K2, K3)
  - ECB and CBC modes for both DES and 3DES
- AESU—Advanced Encryption Standard unit
  - Implements the Rijndael symmetric key cipher
  - ECB, CBC, CTR, and CCM modes
  - 128-, 192-, and 256-bit key lengths
- AFEU—ARC four execution unit
  - Implements a stream cipher compatible with the RC4 algorithm
  - 40- to 128-bit programmable key
- MDEU—message digest execution unit
  - SHA with 160- or 256-bit message digest
  - MD5 with 128-bit message digest
  - HMAC with either algorithm
- KEU—Kasumi execution unit
  - Implements F8 algorithm for encryption and F9 algorithm for integrity checking
  - Also supports A5/3 and GEA-3 algorithms
- RNG—random number generator
- XOR engine for parity checking in RAID storage applications

- Dual I^2C controllers
  - Two-wire interface
  - Multiple master support
  - Master or slave I^2C mode support
  - On-chip digital filtering rejects spikes on the bus
- Boot sequencer
  - Optionally loads configuration data from serial ROM at reset via the I^2C interface
  - Can be used to initialize configuration registers and/or memory
  - Supports extended I^2C addressing mode
  - Data integrity checked with preamble signature and CRC
- DUART
  - Two 4-wire interfaces (SIN, SOUT, $\overline{\text{RTS}}$, $\overline{\text{CTS}}$)
  - Programming model compatible with the original 16450 UART and the PC16550D
- Local bus controller (LBC)
  - Multiplexed 32-bit address and data bus operating at up to 133 MHz
  - Eight chip selects support eight external slaves
  - Up to eight-beat burst transfers
  - The 32-, 16-, and 8-bit port sizes are controlled by an on-chip memory controller.
  - Two protocol engines available on a per chip select basis:

3 Power Characteristics

The estimated typical core power dissipation for the core complex bus (CCB) versus the core frequency for this family of PowerQUICC III devices is shown in Table 4.

Table 4. MPC8533E Core Power Dissipation

Power Mode	Core Frequency (MHz)	Platform Frequency (MHz)	V_{DD} (V)	Junction Temperature (°C)	Power (W)	Notes
Typical	667	333	1.0	65	2.6	1, 2
Thermal				90	3.75	1, 3
Maximum					5.85	1, 4
Typical	800	400	1.0	65	2.9	1, 2
Thermal				90	4.0	1, 3
Maximum					6.0	1, 4
Typical	1000	400	1.0	65	3.6	1, 2
Thermal				90	4.4	1, 3
Maximum					6.2	1, 4
Typical	1067	533	1.0	65	3.9	1, 2
Thermal				90	5.0	1, 3
Maximum					6.5	1, 4

Notes:

1. These values specify the power consumption at nominal voltage and apply to all valid processor bus frequencies and configurations. The values do not include power dissipation for I/O supplies.
2. Typical power is an average value measured at the nominal recommended core voltage (V_{DD}) and 65°C junction temperature (see Table 2) while running the Dhrystone 2.1 benchmark.
3. Thermal power is the average power measured at nominal core voltage (V_{DD}) and maximum operating junction temperature (see Table 2) while running the Dhrystone 2.1 benchmark.
4. Maximum power is the maximum power measured at nominal core voltage (V_{DD}) and maximum operating junction temperature (see Table 2) while running a smoke test which includes an entirely L1-cache-resident, contrived sequence of instructions which keep the execution unit maximally busy.

4 Input Clocks

This section contains the following subsections:

- Section 4.1, “System Clock Timing”
- Section 4.2, “Real-Time Clock Timing”
- Section 4.3, “eTSEC Gigabit Reference Clock Timing”
- Section 4.4, “Platform to FIFO Restrictions”
- Section 4.5, “Other Input Clocks”

4.1 System Clock Timing

Table 5 provides the system clock (SYSCLK) AC timing specifications for the MPC8533E.

Table 5. SYSCLK AC Timing Specifications

At recommended operating conditions (see Table 2) with OV_{DD} = 3.3 V ± 165 mV.

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Notes
SYSCLK frequency	f_{SYSCLK}	33	—	133	MHz	1
SYSCLK cycle time	t_{SYSCLK}	7.5	—	30.3	ns	—
SYSCLK rise and fall time	t_{KH}, t_{KL}	0.6	1.0	2.1	ns	2
SYSCLK duty cycle	t_{KHK}/t_{SYSCLK}	40	—	60	%	—
SYSCLK jitter	—	—	—	±150	ps	3, 4

Notes:
1. **Caution:** The CCB clock to SYSCLK ratio and e500 core to CCB clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB clock frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 19.2, "CCB/SYSCLK PLL Ratio," and Section 19.3, "e500 Core PLL Ratio," for ratio settings.
2. Rise and fall times for SYSCLK are measured at 0.6 and 2.7 V.
3. This represents the total input jitter—short- and long-term.
4. The SYSCLK driver's closed loop jitter bandwidth should be <500 kHz at –20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track SYSCLK drivers with the specified jitter.

4.1.1 SYSCLK and Spread Spectrum Sources

Spread spectrum clock sources are an increasingly popular way to control electromagnetic interference emissions (EMI) by spreading the emitted noise to a wider spectrum and reducing the peak noise magnitude in order to meet industry and government requirements. These clock sources intentionally add long-term jitter in order to diffuse the EMI spectral content. The jitter specification given in Table 5 considers short-term (cycle-to-cycle) jitter only and the clock generator's cycle-to-cycle output jitter should meet the MPC8533E input cycle-to-cycle jitter requirement. Frequency modulation and spread are separate concerns, and the MPC8533E is compatible with spread spectrum sources if the recommendations listed in Table 6 are observed.

Table 6. Spread Spectrum Clock Source Recommendations

At recommended operating conditions. See Table 2.

Parameter	Min	Max	Unit	Notes
Frequency modulation	20	60	kHz	—
Frequency spread	0	1.0	%	1

Note:
1. SYSCLK frequencies resulting from frequency spreading, and the resulting core and VCO frequencies, must meet the minimum and maximum specifications given in Table 5.

It is imperative to note that the processor's minimum and maximum SYSCLK, core, and VCO frequencies must not be exceeded regardless of the type of clock source. Therefore, systems in which the processor is operated at its maximum rated e500 core frequency should avoid violating the stated limits by using down-spreading only.

8.4.1 MII Transmit AC Timing Specifications

Table 27 provides the MII transmit AC timing specifications.

Table 27. MII Transmit AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5% or 2.5 V ± 5%

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
TX_CLK clock period 10 Mbps	t_{MTX}	—	400	—	ns	—
TX_CLK clock period 100 Mbps	t_{MTX}	—	40	—	ns	—
TX_CLK duty cycle	t_{MTXH}/t_{MTX}	35	—	65	%	—
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t_{MTKHDX}	1	5	15	ns	—
TX_CLK data clock rise (20%–80%)	t_{MTXR}	1.0	—	4.0	ns	—
TX_CLK data clock fall (80%–20%)	t_{MTXF}	1.0	—	4.0	ns	—

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 12 shows the MII transmit AC timing diagram.

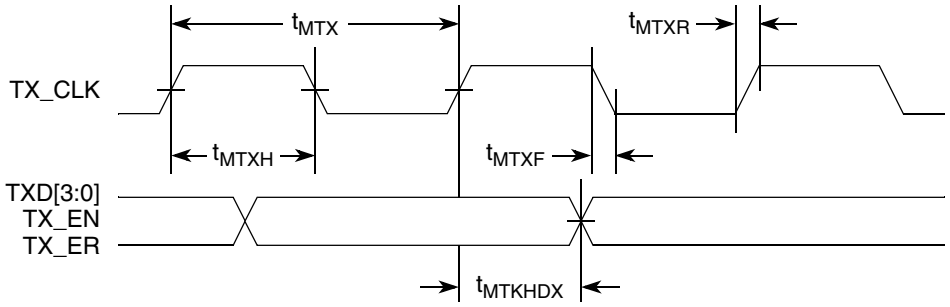

Figure 12. MII Transmit AC Timing Diagram

8.4.2 MII Receive AC Timing Specifications

Table 28 provides the MII receive AC timing specifications.

Table 28. MII Receive AC Timing Specifications

At recommended operating conditions with L/TVDD of 3.3 V ± 5%.or 2.5 V ± 5%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
RX_CLK clock period 10 Mbps	t_{MRX}	—	400	—	ns	—
RX_CLK clock period 100 Mbps	t_{MRX}	—	40	—	ns	—
RX_CLK duty cycle	t_{MRXH}/t_{MRX}	35	—	65	%	—

Table 28. MII Receive AC Timing Specifications (continued)

At recommended operating conditions with L/TVDD of 3.3 V ± 5%.or 2.5 V ± 5%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t_{MRDVKH}	10.0	—	—	ns	—
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t_{MRDXKH}	10.0	—	—	ns	—
RX_CLK clock rise (20%–80%)	t_{MRXR}	1.0	—	4.0	ns	—
RX_CLK clock fall time (80%–20%)	t_{MRXF}	1.0	—	4.0	ns	—

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 13 provides the AC test load for eTSEC.

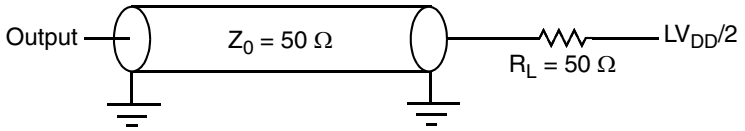

Figure 13. eTSEC AC Test Load

Figure 14 shows the MII receive AC timing diagram.

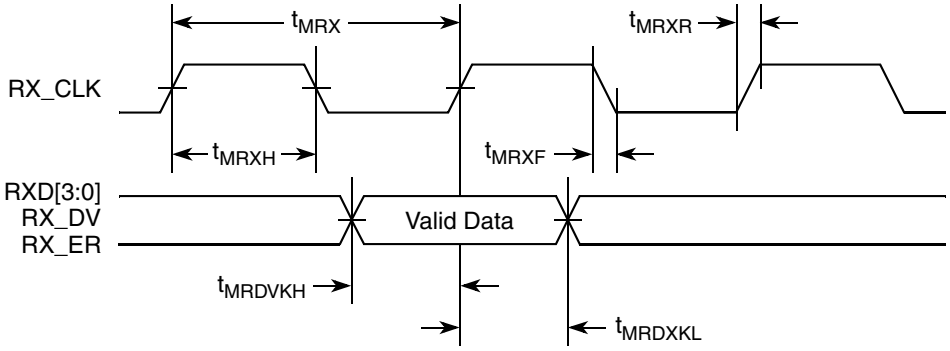

Figure 14. MII Receive AC Timing Diagram

8.5 TBI AC Timing Specifications

This section describes the TBI transmit and receive AC timing specifications.

9 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals MDIO (management data input/output) and MDC (management data clock). The electrical characteristics for GMII, RGMII, RMII, TBI, and RTBI are specified in "Section 8, "Enhanced Three-Speed Ethernet (eTSEC), MII Management."

9.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in Table 35.

Table 35. MII Management DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit	Notes
Supply voltage (3.3 V)	OV_{DD}	3.135	3.465	V	—
Output high voltage (OV_{DD} = Min, I_{OH} = –1.0 mA)	V_{OH}	2.10	3.60	V	—
Output low voltage (OV_{DD} = Min, I_{OL} = 1.0 mA)	V_{OL}	GND	0.50	V	—
Input high voltage	V_{IH}	1.95	—	V	—
Input low voltage	V_{IL}	—	0.90	V	—
Input high current (OV_{DD} = Max, V_{IN} = 2.1 V)	I_{IH}	—	40	μA	1
Input low current (OV_{DD} = Max, V_{IN} = 0.5 V)	I_{IL}	–600	—	μA	—

Note:
1. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

9.2 MII Management AC Electrical Specifications

Table 36 provides the MII management AC timing specifications.

Table 36. MII Management AC Timing Specifications

At recommended operating conditions with OV_{DD} is 3.3 V ± 5%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
MDC frequency	f_{MDC}	—	2.5	—	MHz	2
MDC period	t_{MDC}	—	400	—	ns	—
MDC clock pulse width high	t_{MDCH}	32	—	—	ns	—
MDC to MDIO delay	t_{MDKHDX}	$(16 \times t_{plb\_clk}) - 3$	—	$(16 \times t_{plb\_clk}) + 3$	ns	3, 4
MDIO to MDC setup time	t_{MDDVKH}	5	—	—	ns	—
MDIO to MDC hold time	t_{MDDXKH}	0	—	—	ns	—
MDC rise time	t_{MDCR}	—	—	10	ns	—

Table 36. MII Management AC Timing Specifications (continued)

At recommended operating conditions with OV_{DD} is 3.3 V ± 5%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
MDC fall time	t_{MDHF}	—	—	10	ns	—

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This parameter is dependent on the platform clock frequency (MIIMCFG [MgmtClk] field determines the clock frequency of the MgmtClk Clock EC_MDC).
3. This parameter is dependent on the platform clock frequency. The delay is equal to 16 platform clock periods ±3 ns. For example, with a platform clock of 333 MHz, the min/max delay is 48 ns ± 3 ns. Similarly, if the platform clock is 400 MHz, the min/max delay is 40 ns ± 3 ns).
4. t_{plb_clk} is the platform (CCB) clock.

Figure 22 shows the MII management AC timing diagram.

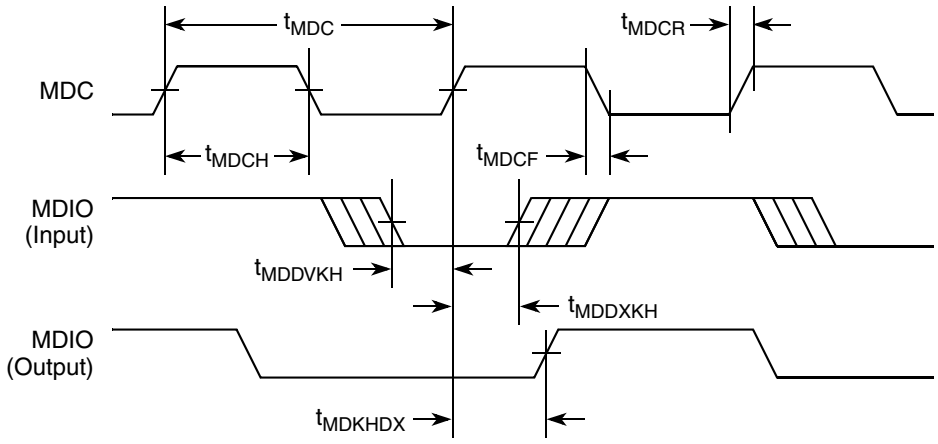

Figure 22. MII Management Interface Timing Diagram

10 Local Bus

This section describes the DC and AC electrical specifications for the local bus interface of the MPC8533E.

10.1 Local Bus DC Electrical Characteristics

Table 37 provides the DC electrical characteristics for the local bus interface operating at BV_{DD} = 3.3 V DC.

Table 37. Local Bus DC Electrical Characteristics (3.3 V DC)

Parameter	Symbol	Min	Max	Unit	Notes
High-level input voltage	V_{IH}	2	BV_{DD} + 0.3	V	—
Low-level input voltage	V_{IL}	–0.3	0.8	V	—
Input current (BV_{IN} = 0 V or BV_{IN} = BOV_{DD})	I_{IN}	—	±5	μA	1
High-level output voltage (BV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	2.4	—	V	—
Low-level output voltage (BV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:
1. The symbol BV_{IN}, in this case, represents the BV_{IN} symbol referenced in Table 1 and Table 2.

Table 38 provides the DC electrical characteristics for the local bus interface operating at BV_{DD} = 2.5 V DC.

Table 38. Local Bus DC Electrical Characteristics (2.5 V DC)

Parameter	Symbol	Min	Max	Unit	Notes
High-level input voltage	V_{IH}	1.70	BV_{DD} + 0.3	V	—
Low-level input voltage	V_{IL}	–0.3	0.7	V	—
Input current (BV_{IN} = 0 V or BV_{IN} = BV_{DD})	I_{IN}	—	±15	μA	1
High-level output voltage (BV_{DD} = min, I_{OH} = –1 mA)	V_{OH}	2.0	—	V	—
Low-level output voltage (BV_{DD} = min, I_{OL} = 1 mA)	V_{OL}	—	0.4	V	—

Note:
1. The symbol BV_{IN}, in this case, represents the BV_{IN} symbol referenced in Table 1 and Table 2.

Table 39 provides the DC electrical characteristics for the local bus interface operating at BV_{DD} = 1.8 V DC.

Table 39. Local Bus DC Electrical Characteristics (1.8 V DC)

Parameter	Symbol	Min	Max	Unit	Notes
High-level input voltage	V_{IH}	1.3	BV_{DD} + 0.3	V	—
Low-level input voltage	V_{IL}	–0.3	0.6	V	—
Input current (BV_{IN} = 0 V or BV_{IN} = BV_{DD})	I_{IN}	—	±15	μA	1

Figure 24 through Figure 29 show the local bus signals.

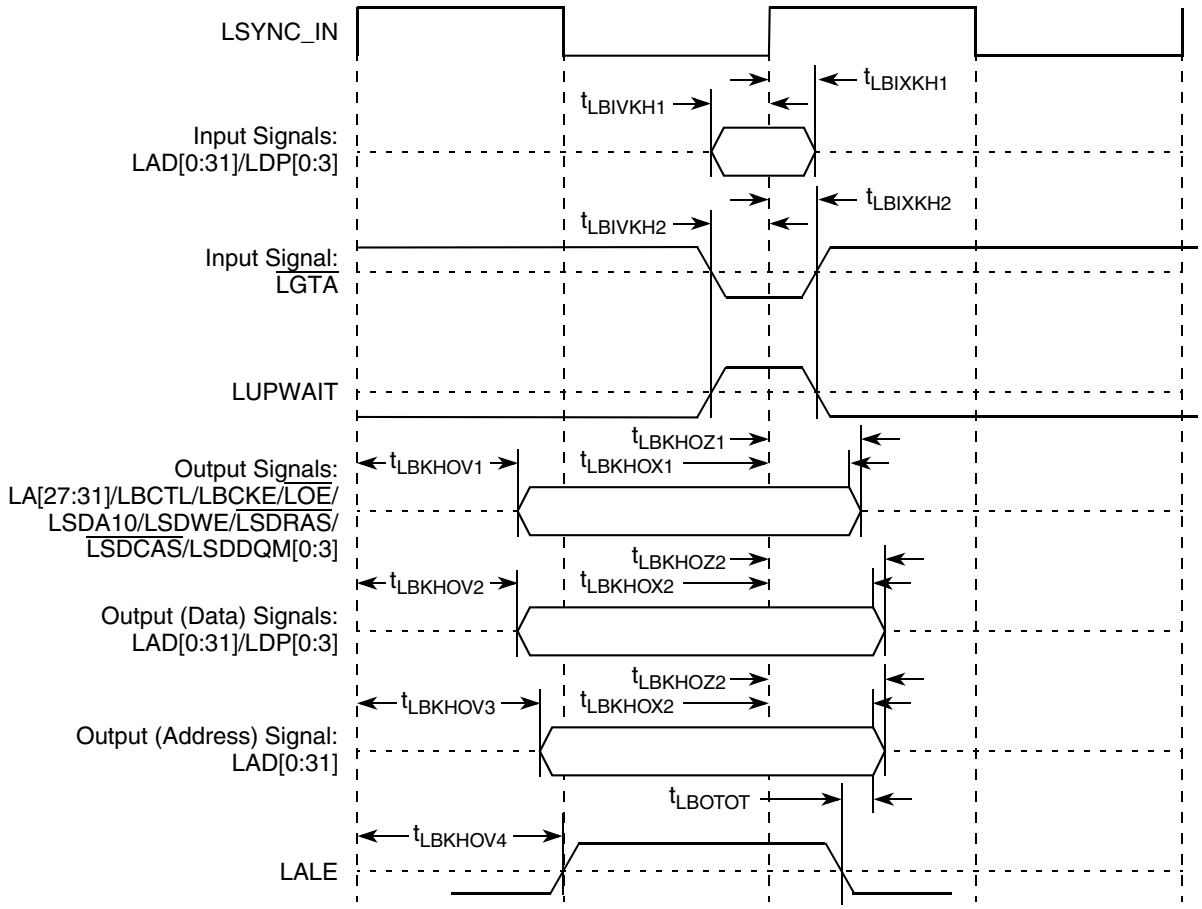

Figure 24. Local Bus Signals (PLL Enabled)

Table 43 describes the general timing parameters of the local bus interface at V_{DD} = 3.3 V DC with PLL disabled.

Table 43. Local Bus General Timing Parameters—PLL Bypassed

Parameter	Symbol[1]	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	12	—	ns	2
Local bus duty cycle	t_{LBKH}/t_{LBK}	43	57	%	—
Internal launch/capture clock to LCLK delay	t_{LBKHKT}	1.2	4.9	ns	—
Input setup to local bus clock (except LUPWAIT)	$t_{LBIVKH1}$	7.4	—	ns	4, 5
LUPWAIT input setup to local bus clock	$t_{LBIVKL2}$	6.75	—	ns	4, 5
Input hold from local bus clock (except LUPWAIT)	$t_{LBIXKH1}$	–0.2	—	ns	4, 5
LUPWAIT input hold from local bus clock	$t_{LBIXKL2}$	–0.2	—	ns	4, 5
LALE output transition to LAD/LDP output transition (LATCH hold time)	t_{LBOTOT}	1.5	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	$t_{LBKLOV1}$	—	1.6	ns	—

Figure 33 provides the boundary-scan timing diagram.

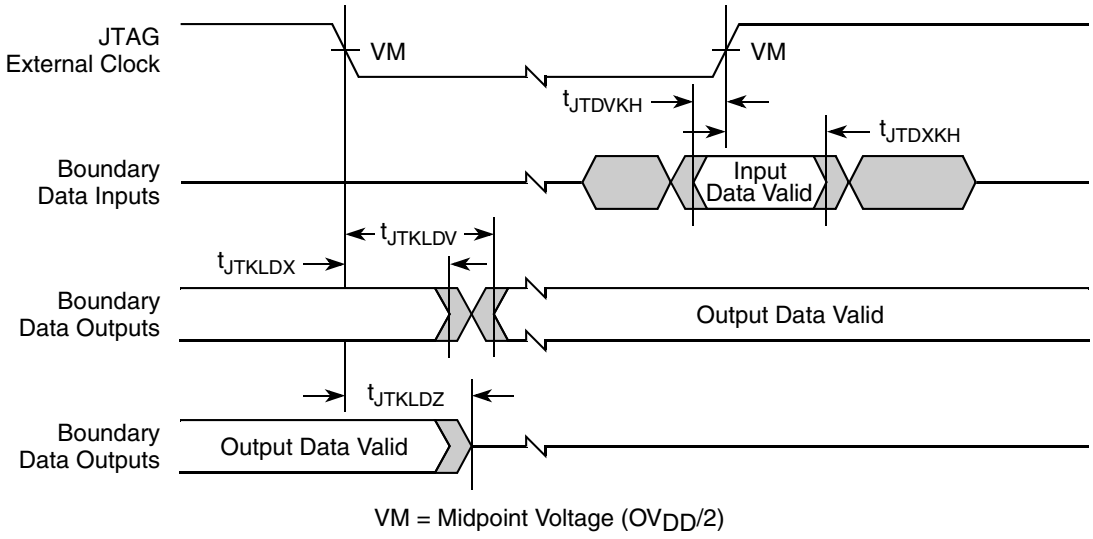

Figure 33. Boundary-Scan Timing Diagram

13 I²C

This section describes the DC and AC electrical characteristics for the I²C interfaces of the MPC8533E.

13.1 I²C DC Electrical Characteristics

Table 46 provides the DC electrical characteristics for the I²C interfaces.

Table 46. I²C DC Electrical Characteristics

At recommended operating conditions with OV_{DD} of 3.3 V ± 5%.

Parameter	Symbol	Min	Max	Unit	Notes
Input high voltage level	V_{IH}	$0.7 \times OV_{DD}$	$OV_{DD} + 0.3$	V	—
Input low voltage level	V_{IL}	–0.3	$0.3 \times OV_{DD}$	V	—
Low level output voltage	V_{OL}	0	$0.2 \times OV_{DD}$	V	1
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	2
Input current each I/O pin (input voltage is between $0.1 \times OV_{DD}$ and $0.9 \times OV_{DD}$(max)	I_I	–10	10	μA	3
Capacitance for each I/O pin	C_I	—	10	pF	—

Notes:
1. Output voltage (open drain or open collector) condition = 3 mA sink current.
2. Refer to the *MPC8533E PowerQUICC III Integrated Communications Host Processor Reference Manual* for information on the digital filter used.
3. I/O pins will obstruct the SDA and SCL lines if OV_{DD} is switched off.

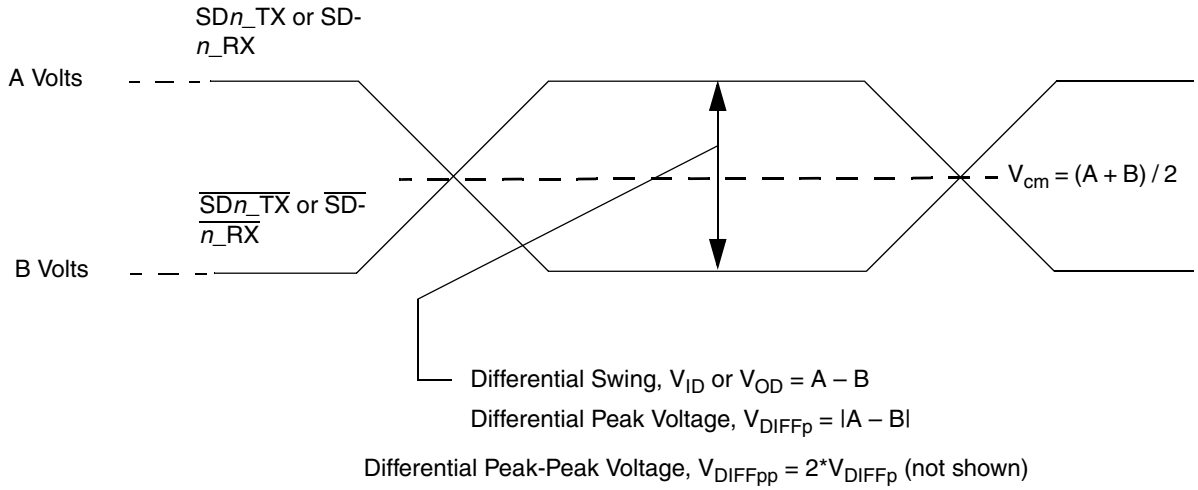

Figure 40. Differential Voltage Definitions for Transmitter or Receiver

To illustrate these definitions using real values, consider the case of a CML (Current Mode Logic) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and $\overline{\text{TD}}$, has a swing that goes between 2.5 V and 2.0 V. Using these values, the peak-to-peak voltage swing of each signal (TD or $\overline{\text{TD}}$) is 500 mV p-p, which is referred as the single-ended swing for each signal. In this example, since the differential signaling environment is fully symmetrical, the transmitter output's differential swing (V_{OD}) has the same amplitude as each signal's single-ended swing. The differential output signal ranges between 500 mV and –500 mV, in other words, V_{OD} is 500 mV in one phase and –500 mV in the other phase. The peak differential voltage (V_{DIFFp}) is 500 mV. The peak-to-peak differential voltage ($V_{DIFFp-p}$) is 1000 mV p-p.

16.2 SerDes Reference Clocks

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clocks inputs are SD1_REF_CLK and $\overline{\text{SD1\_REF\_CLK}}$ for PCI Express1 PCI Express2. SD2_REF_CLK and $\overline{\text{SD2\_REF\_CLK}}$ for the PCI Express3. The following sections describe the SerDes reference clock requirements and some application information.

16.2.1 SerDes Reference Clock Receiver Characteristics

Figure 41 shows a receiver reference diagram of the SerDes reference clocks.

- The supply voltage requirements for XV_{DD_SRDS2} are specified in Table 1 and Table 2.
- SerDes reference clock receiver reference circuit structure
  - The SD*n*_REF_CLK and $\overline{\text{SD}n\text{\_REF\_CLK}}$ are internally AC-coupled differential inputs as shown in Figure 41. Each differential clock input (SD*n*_REF_CLK or $\overline{\text{SD}n\text{\_REF\_CLK}}$) has a 50-Ω termination to SGND_SRDS*n* (xcorevss) followed by on-chip AC-coupling.
  - The external reference clock driver must be able to drive this termination.

— The SerDes reference clock input can be either differential or single-ended. Refer to the differential mode and single-ended mode description below for further detailed requirements.

- The maximum average current requirement that also determines the common mode voltage range:
  — When the SerDes reference clock differential inputs are DC coupled externally with the clock driver chip, the maximum average current allowed for each input pin is 8 mA. In this case, the exact common mode input voltage is not critical as long as it is within the range allowed by the maximum average current of 8 mA (refer to the following bullet for more detail), since the input is AC-coupled on-chip.
  — This current limitation sets the maximum common mode input voltage to be less than 0.4 V (0.4 V/50 = 8 mA) while the minimum common mode input level is 0.1 V above SGND_SRDS*n* (xcorevss). For example, a clock with a 50/50 duty cycle can be produced by a clock driver with output driven by its current source from 0mA to 16mA (0–0.8 V), such that each phase of the differential input has a single-ended swing from 0 V to 800 mV with the common mode voltage at 400 mV.
  — If the device driving the SD*n*_REF_CLK and $\overline{\text{SD}n\text{\_REF\_CLK}}$ inputs cannot drive 50 Ω to SGND_SRDS*n* (xcorevss) DC, or it exceeds the maximum input current limitations, then it must be AC-coupled off-chip.
- The input amplitude requirement
  — This requirement is described in detail in the following sections.

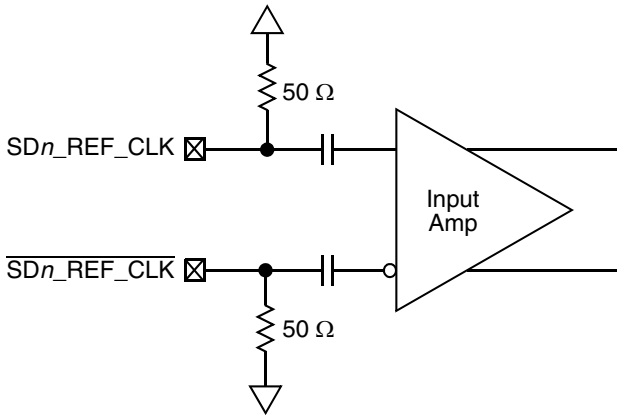

Figure 41. Receiver of SerDes Reference Clocks

16.2.2 DC Level Requirement for SerDes Reference Clocks

The DC level requirement for the MPC8533E SerDes reference clock inputs is different depending on the signaling mode used to connect the clock driver chip and SerDes reference clock inputs as described below.

- **Differential Mode**
  — The input amplitude of the differential clock must be between 400 and 1600 mV differential peak-peak (or between 200 and 800 mV differential peak). In other words, each signal wire of the differential pair must have a single-ended swing less than 800 mV and greater than 200 mV. This requirement is the same for both external DC-coupled or AC-coupled connection.

Figure 45 shows the SerDes reference clock connection reference circuits for HCSL type clock driver. It assumes that the DC levels of the clock driver chip is compatible with MPC8533E SerDes reference clock input's DC requirement.

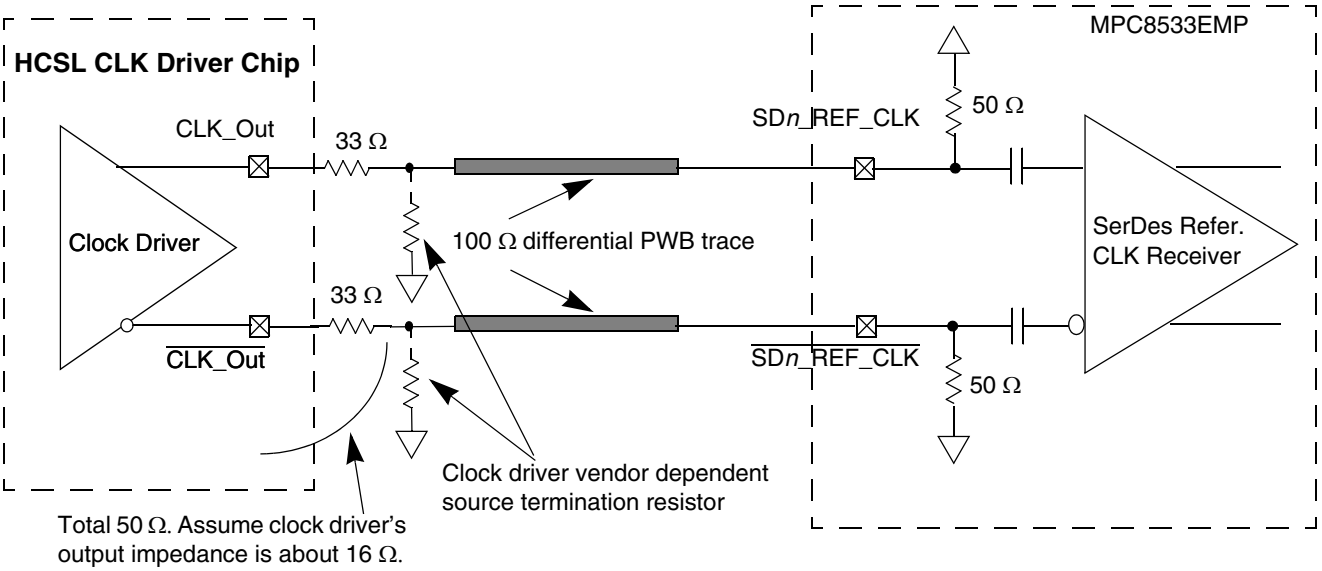

Figure 45. DC-Coupled Differential Connection with HCSL Clock Driver (Reference Only)

Figure 46 shows the SerDes reference clock connection reference circuits for LVDS type clock driver. Since LVDS clock driver's common mode voltage is higher than the MPC8533E SerDes reference clock input's allowed range (100 to 400mV), AC-coupled connection scheme must be used. It assumes the LVDS output driver features 50-Ω termination resistor. It also assumes that the LVDS transmitter establishes its own common mode level without relying on the receiver or other external component.

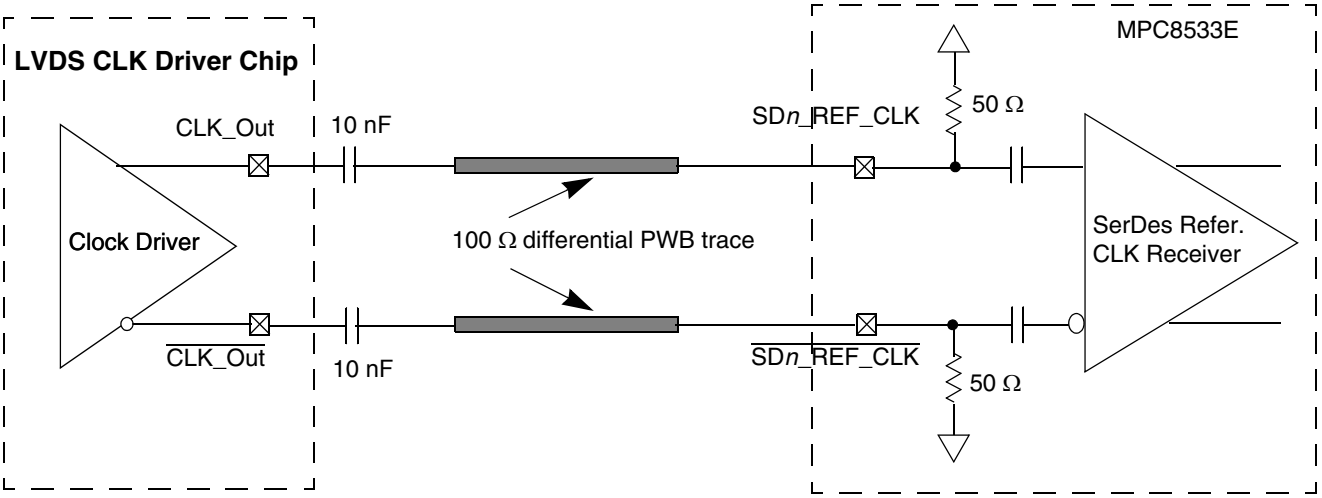

Figure 46. AC-Coupled Differential Connection with LVDS Clock Driver (Reference Only)

Figure 47 shows the SerDes reference clock connection reference circuits for LVPECL type clock driver. Since LVPECL driver's DC levels (both common mode voltages and output swing) are incompatible with MPC8533E SerDes reference clock input's DC requirement, AC-coupling has to be used. Figure 47

16.2.4 AC Requirements for SerDes Reference Clocks

The clock driver selected should provide a high quality reference clock with low phase noise and cycle-to-cycle jitter. Phase noise less than 100 kHz can be tracked by the PLL and data recovery loops and is less of a problem. Phase noise above 15 MHz is filtered by the PLL. The most problematic phase noise occurs in the 1–15 MHz range. The source impedance of the clock driver should be 50 Ω to match the transmission line and reduce reflections which are a source of noise to the system.

Table 52 describes some AC parameters common to SGMII, and PCI Express protocols.

Table 52. SerDes Reference Clock Common AC Parameters

Parameter	Symbol	Min	Max	Unit	Notes
Rising Edge Rate	Rise Edge Rate	1.0	4.0	V/ns	2, 3
Falling Edge Rate	Fall Edge Rate	1.0	4.0	V/ns	2, 3
Differential Input High Voltage	V_{IH}	+200	—	mV	2
Differential Input Low Voltage	V_{IL}	—	–200	mV	2
Rising edge rate (SD*n*_REF_CLK) to falling edge rate ($\overline{\text{SD}n\text{\_REF\_CLK}}$) matching	Rise-Fall Matching	—	20	%	1, 4

Notes:
1. Measurement taken from single ended waveform.
2. Measurement taken from differential waveform.
3. Measured from –200 mV to +200 mV on the differential waveform (derived from SD*n*_REF_CLK minus $\overline{\text{SD}n\text{\_REF\_CLK}}$). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing. See Figure 49.
4. Matching applies to rising edge rate for SD*n*_REF_CLK and falling edge rate for $\overline{\text{SD}n\text{\_REF\_CLK}}$. It is measured using a 200 mV window centered on the median cross point where SD*n*_REF_CLK rising meets $\overline{\text{SD}n\text{\_REF\_CLK}}$ falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The rise edge rate of SD*n*_REF_CLK should be compared to the fall edge rate of $\overline{\text{SD}n\text{\_REF\_CLK}}$, the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 50.

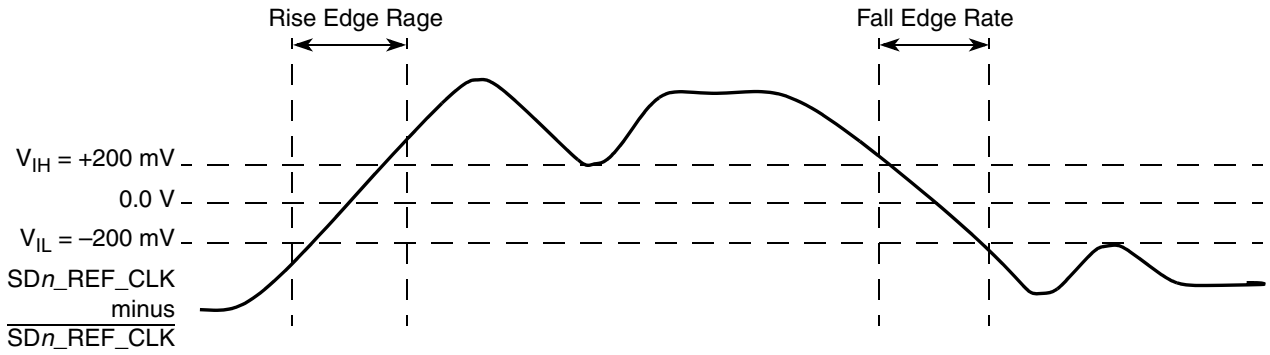

Figure 49. Differential Measurement Points for Rise and Fall Time

Table 57. MPC8533E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
LCS6/DMA_DACK2	J16	O	BV_{DD}	1
LCS7/DMA_DDONE2	L18	O	BV_{DD}	1
LWE0/LBS0/LSDDQM[0]	J22	O	BV_{DD}	4, 8
LWE1/LBS1/LSDDQM[1]	H22	O	BV_{DD}	4, 8
LWE2/LBS2/LSDDQM[2]	H23	O	BV_{DD}	4, 8
LWE3/LBS3/LSDDQM[3]	H21	O	BV_{DD}	4, 8
LALE	J26	O	BV_{DD}	4, 7, 8
LBCTL	J25	O	BV_{DD}	4, 7, 8
LGPL0/LSDA10	J20	O	BV_{DD}	4, 8
LGPL1/LSDWE	K20	O	BV_{DD}	4, 8
LGPL2/LOE/LSDRAS	G20	O	BV_{DD}	4, 7, 8
LGPL3/LSDCAS	H18	O	BV_{DD}	4, 8
LGPL4/LGTA/LUPWAIT/ LPBSE	L20	I/O	BV_{DD}	28
LGPL5	K19	O	BV_{DD}	4, 8
LCKE	L17	O	BV_{DD}	—
LCLK[0:2]	H24, J24, H25	O	BV_{DD}	—
LSYNC_IN	D27	I	BV_{DD}	—
LSYNC_OUT	D28	O	BV_{DD}	—
DMA				
DMA_DACK[0:1]	Y13, Y12	O	OV_{DD}	4, 8, 9
DMA_DREQ[0:1]	AA10, AA11	I	OV_{DD}	—
DMA_DDONE[0:1]	AA7, Y11	O	OV_{DD}	—
Programmable Interrupt Controller				
UDE	AH15	I	OV_{DD}	—
MCP	AG18	I	OV_{DD}	—
IRQ[0:7]	AG22, AF17, AD21, AF19, AG17, AF16, AC23, AC22	I	OV_{DD}	—
IRQ[8]	AC19	I	OV_{DD}	—
IRQ[9]/DMA_DREQ3	AG20	I	OV_{DD}	1
IRQ[10]/DMA_DACK3	AE27	I/O	OV_{DD}	1
IRQ[11]/DMA_DDONE3	AE24	I/O	OV_{DD}	1
IRQ_OUT	AD14	O	OV_{DD}	2

Table 57. MPC8533E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
V_{DD}	L16, L14, M13, M15, M17, N12, N14, N16, N18, P13, P15, P17, R12, R14, R16, R18, T13, T15, T17, U12, U14, U16, U18,	Power for core (1.0 V)	V_{DD}	—
SVDD_SRDS	M27, N25, P28, R24, R26, T24, T27, U25, W24, W26, Y24, Y27, AA25, AB28, AD27	Core power for SerDes 1 transceivers (1.0 V)	SV_{DD}	—
SVDD_SRDS2	AB1, AC26, AD2, AE26, AG2	Core power for SerDes 2 transceivers (1.0 V)	SV_{DD}	—
XVDD_SRDS	M21, N23, P20, R22, T20, U23, V21, W22, Y20	Pad power for SerDes 1 transceivers (1.0 V)	XV_{DD}	—
XVDD_SRDS2	Y6, AA6, AA23, AF5, AG5	Pad power for SerDes 2 transceivers (1.0 V)	XV_{DD}	—
XGND_SRDS	M20, M24, N22, P21, R23, T21, U22, V20, W23, Y21	—	—	—
XGND_SRDS2	Y4, AA4, AA22, AD4, AE4, AH4	—	—	—
SGND_SRDS	M28, N26, P24, P27, R25, T28, U24, U26, V24, W25, Y28, AA24, AA26, AB24, AB27, AC24, AD28	—	—	—
AGND_SRDS	V27	SerDes PLL GND	—	—
SGND_SRDS2	Y2, AA1, AB3, AC2, AC3, AC25, AD3, AD24, AE3, AE1, AE25, AF3, AH2	—	—	—
AGND_SRDS2	AF1	SerDes PLL GND	—	—
AVDD_LBIU	C28	Power for local bus PLL (1.0 V)	—	19
AVDD_PCI1	AH20	Power for PCI PLL (1.0 V)	—	19
AVDD_CORE	AH14	Power for e500 PLL (1.0 V)	—	19
AVDD_PLAT	AH18	Power for CCB PLL (1.0 V)	—	19

Table 66 provides the thermal resistance with heat sink in open flow.

Table 66. Thermal Resistance with Heat Sink in Open Flow

Heat Sink with Thermal Grease	Air Flow	Thermal Resistance (°C/W)
Wakefield 53 × 53 × 25 mm pin fin	Natural convection	6.1
Wakefield 53 × 53 × 25 mm pin fin	1 m/s	3.0
Aavid 35 × 31 × 23 mm pin fin	Natural convection	8.1
Aavid 35 × 31 × 23 mm pin fin	1 m/s	4.3
Aavid 30 × 30 × 9.4 mm pin fin	Natural convection	11.6
Aavid 30 × 30 × 9.4 mm pin fin	1 m/s	6.7
Aavid 43 × 41 × 16.5 mm pin fin	Natural convection	8.3
Aavid 43 × 41 × 16.5 mm pin fin	1 m/s	4.3

Simulations with heat sinks were done with the package mounted on the 2s2p thermal test board. The thermal interface material was a typical thermal grease such as Dow Corning 340 or Wakefield 120 grease. For system thermal modeling, the MPC8533E thermal model without a lid is shown in Figure 56. The substrate is modeled as a block 29 × 29 × 1.18 mm with an in-plane conductivity of 18.0 W/m•K and a through-plane conductivity of 1.0 W/m•K. The solder balls and air are modeled as a single block 29 × 29 × 0.58 mm with an in-plane conductivity of 0.034 W/m•K and a through plane conductivity of 12.1 W/m•K. The die is modeled as 7.6 × 8.4 mm with a thickness of 0.75 mm. The bump/underfill layer is modeled as a collapsed thermal resistance between the die and substrate assuming a conductivity of 6.5 W/m•K in the thickness dimension of 0.07 mm. The die is centered on the substrate. The thermal model uses approximate dimensions to reduce grid. Please refer to Figure 55 for actual dimensions.

20.2 Recommended Thermal Model

Table 67 shows the MPC8533E thermal model.

Table 67. MPC8533EThermal Model

Conductivity	Value	Units
Die (7.6 × 8.4 × 0.75mm)		
Silicon	Temperature dependent	—
Bump/Underfill (7.6 × 8.4 × 0.070 mm) Collapsed Thermal Resistance		
Kz	6.5	W/m•K
Substrate (29 × 29 × 1.18 mm)		
Kx	18	W/m•K
Ky	18	
Kz	1.0	

Table 67. MPC8533EThermal Model (continued)

Conductivity	Value	Units
Solder and Air (29 × 29 × 0.58 mm)		
Kx	0.034	W/m•K
Ky	0.034	
Kz	12.1	

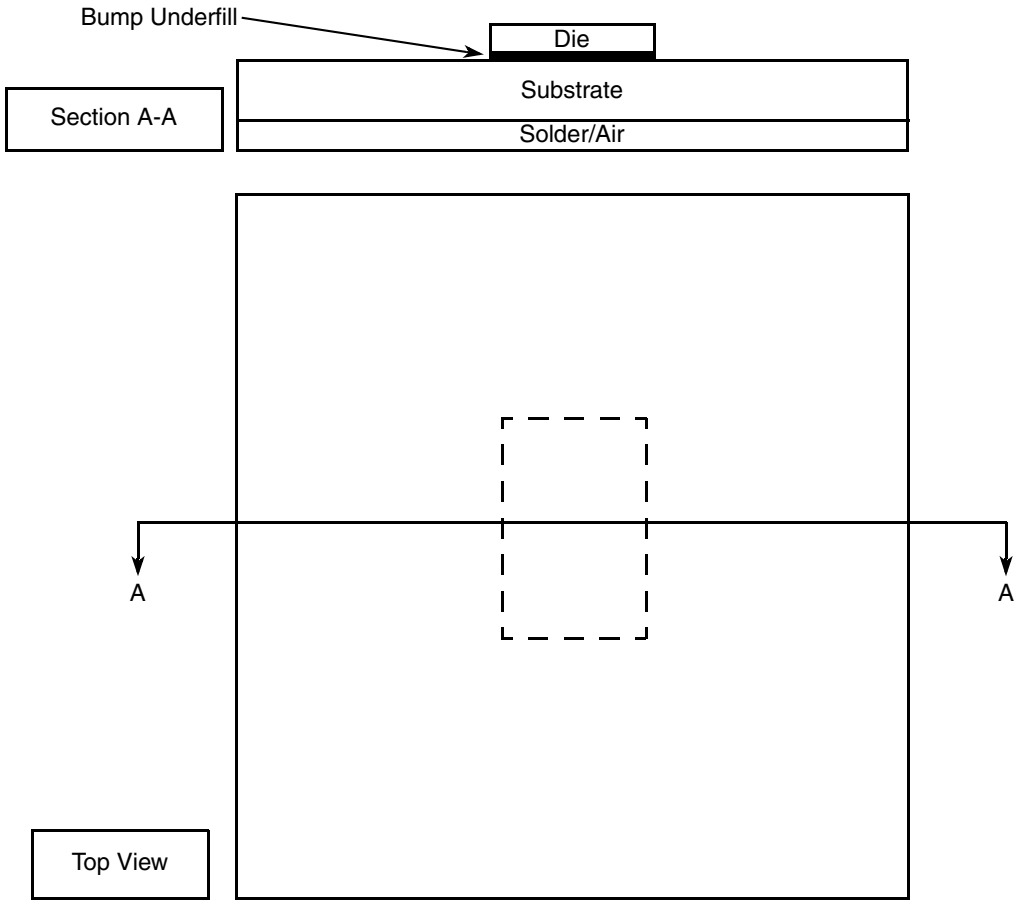

Figure 56. System Level Thermal Model for MPC8533E (Not to Scale)

The Flotherm library files of the parts have a dense grid to accurately capture the laminar boundary layer for flow over the part in standard JEDEC environments, as well as the heat spreading in the board under the package. In a real system, however, the part will require a heat sink to be mounted on it. In this case, the predominant heat flow path will be from the die to the heat sink. Grid density lower than currently in the package library file will suffice for these simulations. The user will need to determine the optimal grid for their specific case.

Heat sinks are attached to the package by means of a spring clip to holes in the printed-circuit board (see Figure 57). Therefore, the synthetic grease offers the best thermal performance, especially at the low interface pressure.

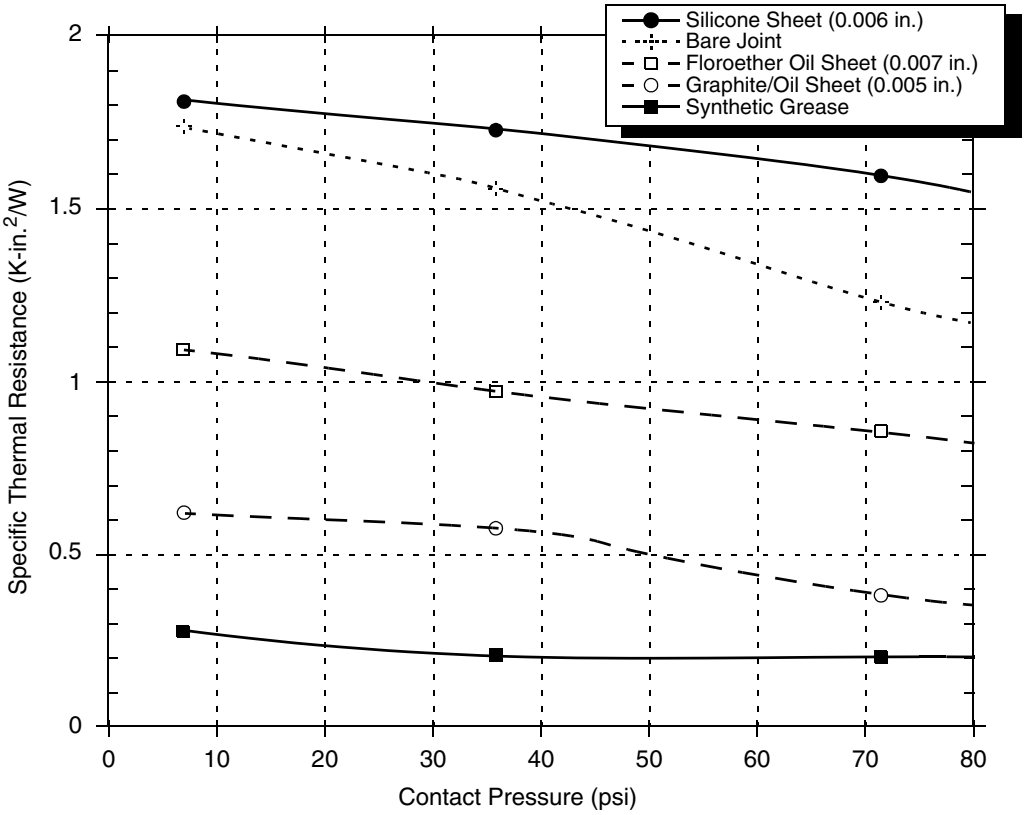

Figure 59. Thermal Performance of Select Thermal Interface Materials

The system board designer can choose between several types of thermal interface. There are several commercially-available thermal interfaces provided by the following vendors:

Chomerics, Inc. 781-935-4850
77 Dragon Ct.
Woburn, MA 01801
Internet: www.chomerics.com

Dow-Corning Corporation800-248-2481
Corporate Center
P.O.Box 999
Midland, MI 48686-0997
Internet: www.dow.com

Shin-Etsu MicroSi, Inc.888-642-7674
10028 S. 51st St.
Phoenix, AZ 85044
Internet: www.microsi.com

The Bergquist Company800-347-4572
18930 West 78th St.

Option 2

- If PCI arbiter is disabled during POR,
- All AD pins will be in the input state. Therefore, all ADs pins need to be grouped together and tied to OV_{DD} through a single (or multiple) 10-kΩ resistor(s).
- All PCI control pins can be grouped together and tied to OV_{DD} through a single 10-kΩ resistor.

21.12 Guideline for LBIU Termination

If the LBIU parity pins are not used, the following list shows the termination recommendation:

- For LDP[0:3]: tie them to ground or the power supply rail via a 4.7-kΩ resistor.
- For LPBSE: tie it to the power supply rail via a 4.7-kΩ resistor (pull-up resistor).

22 Device Nomenclature

Ordering information for the parts fully covered by this hardware specifications document is provided in Section 22.3, "Part Marking." Contact your local Freescale sales office or regional marketing team for order information.

22.1 Industrial and Commercial Tier Qualification

The MPC8533E device has been tested to meet the commercial tier qualification. Table 69 provides a description for commercial and industrial qualifications.

Table 69. Commercial and Industrial Description

Tier[1]	Typical Application Use Time	Power-On Hours	Example of Typical Applications
Commercial	5 years	Part-time/ Full-Time	PC's, consumer electronics, office automation, SOHO networking, portable telecom products, PDAs, etc.
Industrial	10 years	Typically Full-Time	Installed telecom equipment, work stations, servers, warehouse equipment, etc.

Note:
1. Refer to Table 2 for operating temperature ranges. Temperature is independent of tier and varies per product.