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## Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

## Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | PowerPC e500v2 |
| Number of Cores/Bus Width | 1 Core, 32-Bit |
| Speed | 667MHz |
| Co-Processors/DSP | - |
| RAM Controllers | DDR, DDR2 |
| Graphics Acceleration | No |
| Display & Interface Controllers | - |
| Ethernet | 10/100/1000Mbps (2) |
| SATA | - |
| USB | - |
| Voltage - I/O | 1.8V, 2.5V, 3.3V |
| Operating Temperature | 0°C ~ 90°C (TA) |
| Security Features | - |
| Package / Case | 783-BBGA, FCBGA |
| Supplier Device Package | 783-FCPBGA (29x29) |
| Purchase URL | https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8533vjalfa |

- Three PCI Express interfaces
  - Two ×4 link width interfaces and one ×1 link width interface
  - PCI Express 1.0a compatible
  - Auto-detection of number of connected lanes
  - Selectable operation as root complex or endpoint
  - Both 32- and 64-bit addressing
  - 256-byte maximum payload size
  - Virtual channel 0 only
  - Traffic class 0 only
  - Full 64-bit decode with 32-bit wide windows
- Power management
  - Supports power saving modes: doze, nap, and sleep
  - Employs dynamic power management, which automatically minimizes power consumption of blocks when they are idle
- System performance monitor
  - Supports eight 32-bit counters that count the occurrence of selected events
  - Ability to count up to 512 counter-specific events
  - Supports 64 reference events that can be counted on any of the 8 counters
  - Supports duration and quantity threshold counting
  - Burstiness feature that permits counting of burst events with a programmable time between bursts
  - Triggering and chaining capability
  - Ability to generate an interrupt on overflow
- System access port
  - Uses JTAG interface and a TAP controller to access entire system memory map
  - Supports 32-bit accesses to configuration registers
  - Supports cache-line burst accesses to main memory
  - Supports large block (4-Kbyte) uploads and downloads
  - Supports continuous bit streaming of entire block for fast upload and download
- IEEE Std 1149.1™-compliant, JTAG boundary scan
- 783 FC-PBGA package

Figure 1 shows the MPC8533E block diagram.

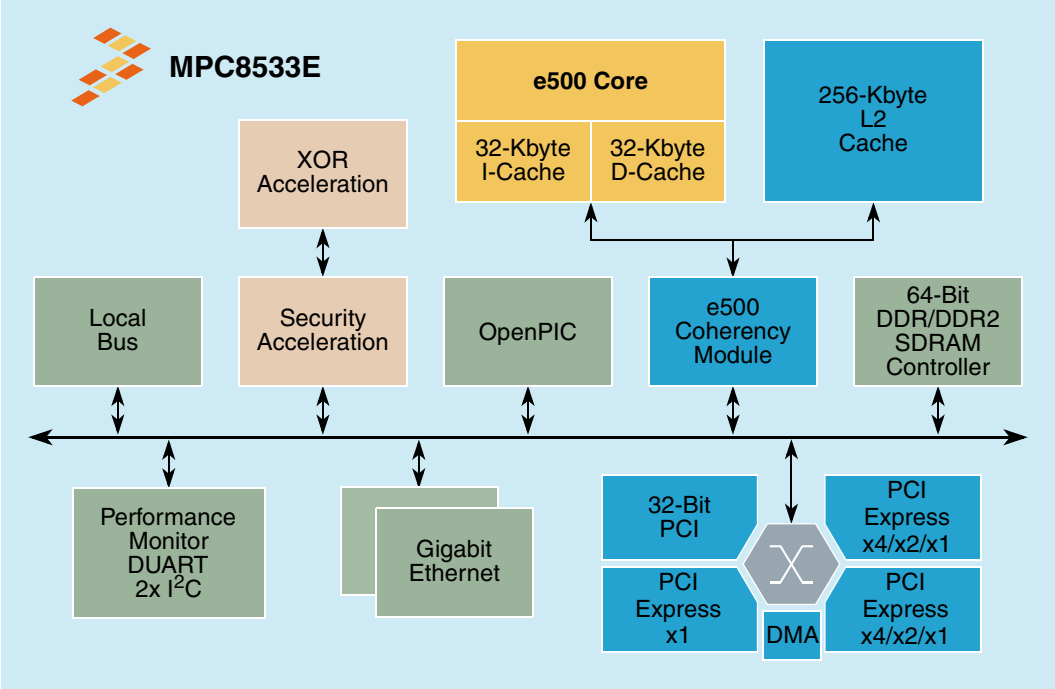


**Figure 1. MPC8533E Block Diagram**

# 2 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8533E. This device is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but are included for a more complete reference. These are not purely I/O buffer design specifications.

## 2.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

### 2.1.1 Absolute Maximum Ratings

Table 1 provides the absolute maximum ratings.

**Table 1. Absolute Maximum Ratings[1]**

| Characteristic | Symbol | Max Value | Unit | Notes |
|---|---|---|---|---|
| Core supply voltage | $V_{DD}$ | –0.3 to 1.1 | V | — |
| PLL supply voltage | $AV_{DD}$ | –0.3 to 1.1 | V | — |
| Core power supply for SerDes transceivers | $SV_{DD}$ | –0.3 to 1.1 | V | — |
| Pad power supply for SerDes transceivers | $XV_{DD}$ | –0.3 to 1.1 | V | — |

# 3 Power Characteristics

The estimated typical core power dissipation for the core complex bus (CCB) versus the core frequency for this family of PowerQUICC III devices is shown in Table 4.

**Table 4. MPC8533E Core Power Dissipation**

| Power Mode | Core Frequency (MHz) | Platform Frequency (MHz) | $V_{DD}$ (V) | Junction Temperature (°C) | Power (W) | Notes |
|---|---|---|---|---|---|---|
| Typical | 667 | 333 | 1.0 | 65 | 2.6 | 1, 2 |
| Thermal | | | | 90 | 3.75 | 1, 3 |
| Maximum | | | | | 5.85 | 1, 4 |
| Typical | 800 | 400 | 1.0 | 65 | 2.9 | 1, 2 |
| Thermal | | | | 90 | 4.0 | 1, 3 |
| Maximum | | | | | 6.0 | 1, 4 |
| Typical | 1000 | 400 | 1.0 | 65 | 3.6 | 1, 2 |
| Thermal | | | | 90 | 4.4 | 1, 3 |
| Maximum | | | | | 6.2 | 1, 4 |
| Typical | 1067 | 533 | 1.0 | 65 | 3.9 | 1, 2 |
| Thermal | | | | 90 | 5.0 | 1, 3 |
| Maximum | | | | | 6.5 | 1, 4 |

**Notes:**

1. These values specify the power consumption at nominal voltage and apply to all valid processor bus frequencies and configurations. The values do not include power dissipation for I/O supplies.
2. Typical power is an average value measured at the nominal recommended core voltage ($V_{DD}$) and 65°C junction temperature (see Table 2) while running the Dhrystone 2.1 benchmark.
3. Thermal power is the average power measured at nominal core voltage ($V_{DD}$) and maximum operating junction temperature (see Table 2) while running the Dhrystone 2.1 benchmark.
4. Maximum power is the maximum power measured at nominal core voltage ($V_{DD}$) and maximum operating junction temperature (see Table 2) while running a smoke test which includes an entirely L1-cache-resident, contrived sequence of instructions which keep the execution unit maximally busy.

# 4 Input Clocks

This section contains the following subsections:

- Section 4.1, “System Clock Timing”
- Section 4.2, “Real-Time Clock Timing”
- Section 4.3, “eTSEC Gigabit Reference Clock Timing”
- Section 4.4, “Platform to FIFO Restrictions”
- Section 4.5, “Other Input Clocks”

Figure 5 shows the DDR SDRAM output timing diagram.

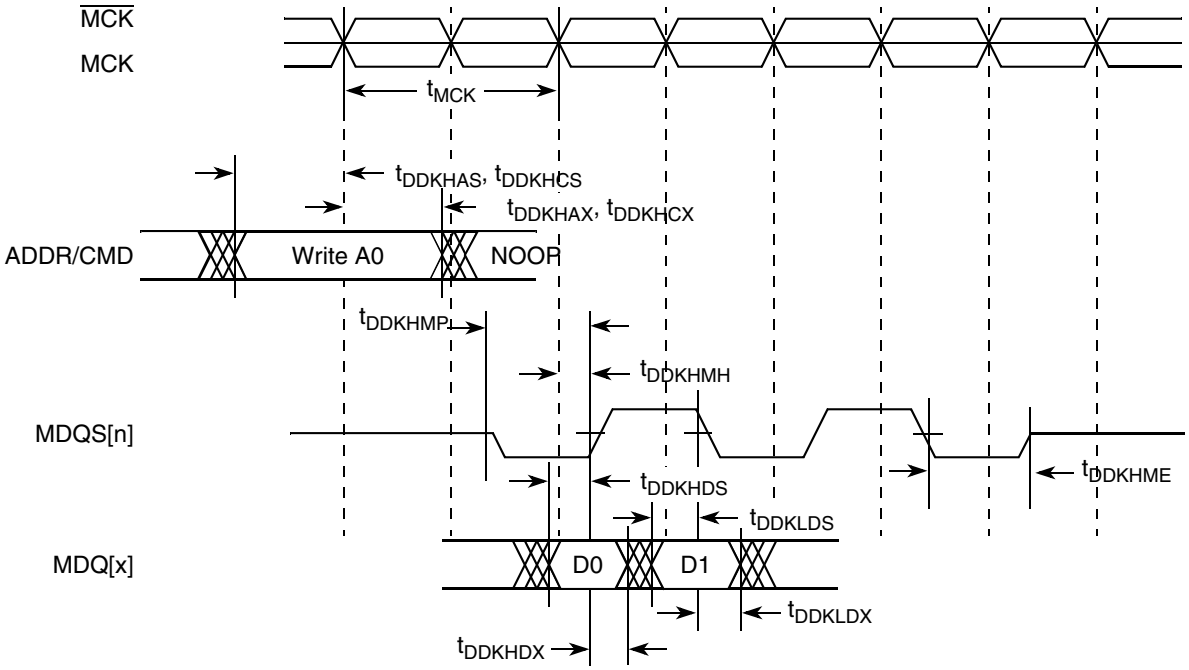


**Figure 5. DDR and DDR2 SDRAM Output Timing Diagram**

Figure 6 provides the AC test load for the DDR bus.

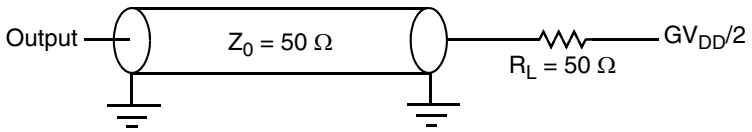


**Figure 6. DDR AC Test Load**

# 7 DUART

This section describes the DC and AC electrical specifications for the DUART interface of the MPC8533E.

## 7.1 DUART DC Electrical Characteristics

Table 19 provides the DC electrical characteristics for the DUART interface.

**Table 19. DUART DC Electrical Characteristics**

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| High-level input voltage | $V_{IH}$ | 2 | $OV_{DD}$ + 0.3 | V | — |
| Low-level input voltage | $V_{IL}$ | –0.3 | 0.8 | V | — |
| Input current ($V_{IN}$ = 0 V or $V_{IN}$ = $V_{DD}$) | $I_{IN}$ | — | ±5 | μA | 1 |
| High-level output voltage ($OV_{DD}$ = min, $I_{OH}$ = –2 mA) | $V_{OH}$ | 2.4 | — | V | — |

**Table 24. FIFO Mode Receive AC Timing Specification (continued)**

At recommended operating conditions with L/TVDD of 3.3 V ± 5% or 2.5 V ± 5%

| Parameter/Condition | Symbol | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Rise time RX_CLK (20%–80%) | $t_{FIRR}$ | — | — | 0.75 | ns | — |
| Fall time RX_CLK (80%–20%) | $t_{FIRF}$ | — | — | 0.75 | ns | — |
| RXD[7:0], RX_DV, RX_ER setup time to RX_CLK | $t_{FIRDV}$ | 1.5 | — | — | ns | — |
| RX_CLK to RXD[7:0], RX_DV, RX_ER hold time | $t_{FIRDX}$ | 0.5 | — | — | ns | — |

Timing diagrams for FIFO appear in Figure 7 and Figure 8.

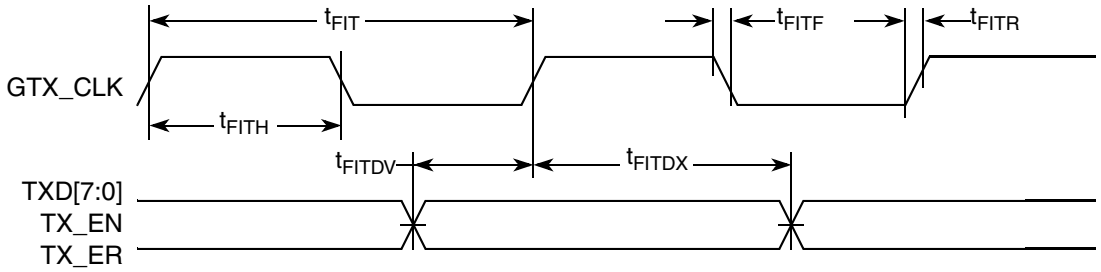


**Figure 7. FIFO Transmit AC Timing Diagram**

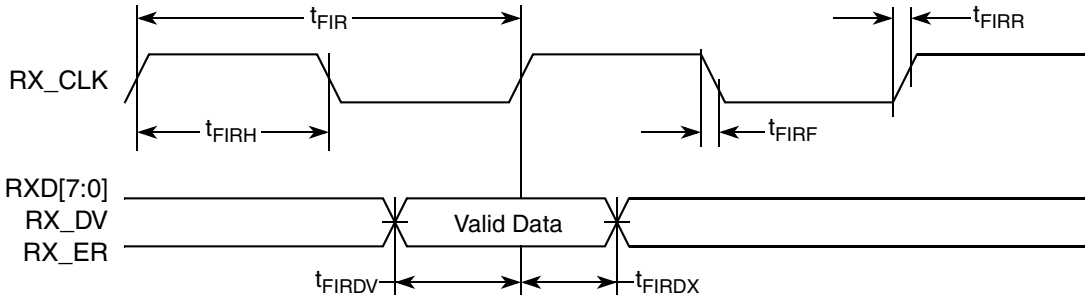


**Figure 8. FIFO Receive AC Timing Diagram**

## 8.3.2 GMII AC Timing Specifications

This section describes the GMII transmit and receive AC timing specifications.

### 8.3.2.1 GMII Transmit AC Timing Specifications

Table 25 provides the GMII transmit AC timing specifications.

**Table 25. GMII Transmit AC Timing Specifications**

At recommended operating conditions with L/TVDD of 3.3 V ± 5% or 2.5 V ± 5%

| Parameter/Condition | Symbol[1] | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| GTX_CLK clock period | $t_{GTX}$ | — | 8.0 | — | ns | — |
| GTX_CLK to GMII data TXD[7:0], TX_ER, TX_EN delay | $t_{GTKHDX}$ | 0.2 | — | 5.0 | ns | 2 |
| GTX_CLK data clock rise time (20%-80%) | $t_{GTXR}$ | — | — | 1.0 | ns | — |

**Table 30. TBI Receive AC Timing Specifications (continued)**

At recommended operating conditions with L/TVDD of 3.3 V ± 5% or 2.5 V ± 5%.

| Parameter/Condition | Symbol[1] | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| PMA_RX_CLK[0:1] duty cycle | $t_{TRXH}/t_{TRX}$ | 40 | — | 60 | % | — |
| RCG[9:0] setup time to rising PMA_RX_CLK | $t_{TRDVKH}$ | 2.5 | — | — | ns | — |
| PMA_RX_CLK to RCG[9:0] hold time | $t_{TRDXKH}$ | 1.5 | — | — | ns | — |
| PMA_RX_CLK[0:1] clock rise time (20%-80%) | $t_{TRXR}$ | 0.7 | — | 2.4 | ns | — |
| PMA_RX_CLK[0:1] clock fall time (80%-20%) | $t_{TRXF}$ | 0.7 | — | 2.4 | ns | — |

**Note:**

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{TRDVKH}$ symbolizes TBI receive timing (TR) with respect to the time data input signals (D) reach the valid state (V) relative to the $t_{TRX}$ clock reference (K) going to the high (H) state or setup time. Also, $t_{TRDXKH}$ symbolizes TBI receive timing (TR) with respect to the time data input signals (D) went invalid (X) relative to the $t_{TRX}$ clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of $t_{TRX}$ represents the TBI (T) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall). For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (TRX).

Figure 16 shows the TBI receive AC timing diagram.

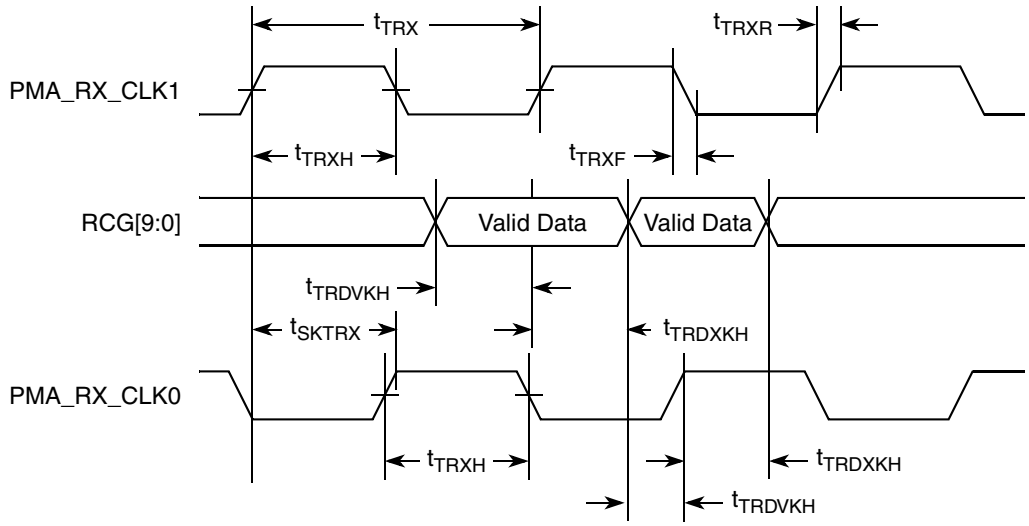


**Figure 16. TBI Receive AC Timing Diagram**

## 8.5.3 TBI Single-Clock Mode AC Specifications

When the eTSEC is configured for TBI modes, all clocks are supplied from external sources to the relevant eTSEC interface. In single-clock TBI mode, when TBICON[CLKSEL] = 1, a 125-MHz TBI receive clock is supplied on the TSEC*n*_RX_CLK pin (no receive clock is used on TSEC*n*_TX_CLK in this mode, whereas for the dual-clock mode this is the PMA1 receive clock). The 125-MHz transmit clock is applied on the TSEC_GTX_CLK125 pin in all TBI modes.

### 8.5.5.2 RMII Receive AC Timing Specifications

Table 34 shows the RMII receive AC timing specifications.

**Table 34. RMII Receive AC Timing Specifications**

At recommended operating conditions with $LV_{DD}$ of 3.3 V ± 5%.or 2.5 V ± 5%.

| Parameter/Condition | Symbol[1] | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| REF_CLK clock period | $t_{RMR}$ | 15.0 | 20.0 | 25.0 | ns | — |
| REF_CLK duty cycle | $t_{RMRH}$ | 35 | 50 | 65 | % | — |
| REF_CLK peak-to-peak jitter | $t_{RMRJ}$ | — | — | 250 | ps | — |
| Rise time REF_CLK (20%–80%) | $t_{RMRR}$ | 1.0 | — | 2.0 | ns | — |
| Fall time REF_CLK (80%–20%) | $t_{RMRF}$ | 1.0 | — | 2.0 | ns | — |
| RXD[1:0], CRS_DV, RX_ER setup time to REF_CLK rising edge | $t_{RMRDV}$ | 4.0 | — | — | ns | — |
| RXD[1:0], CRS_DV, RX_ER hold time to REF_CLK rising edge | $t_{RMRDX}$ | 2.0 | — | — | ns | — |

**Note:**

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{MRDVKH}$ symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the $t_{MRX}$ clock reference (K) going to the high (H) state or setup time. Also, $t_{MRDXKL}$ symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the $t_{MRX}$ clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of $t_{MRX}$ represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 20 provides the AC test load for eTSEC.

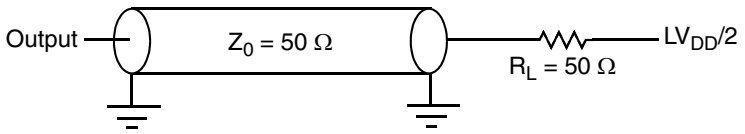


**Figure 20. eTSEC AC Test Load**

Figure 21 shows the RMII receive AC timing diagram.

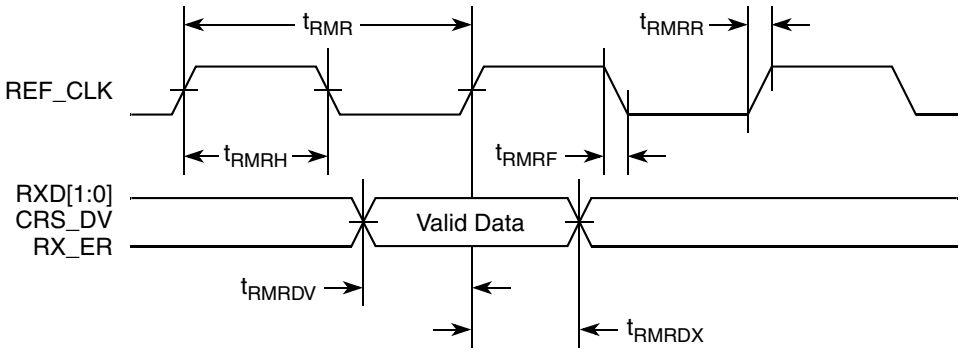


**Figure 21. RMII Receive AC Timing Diagram**

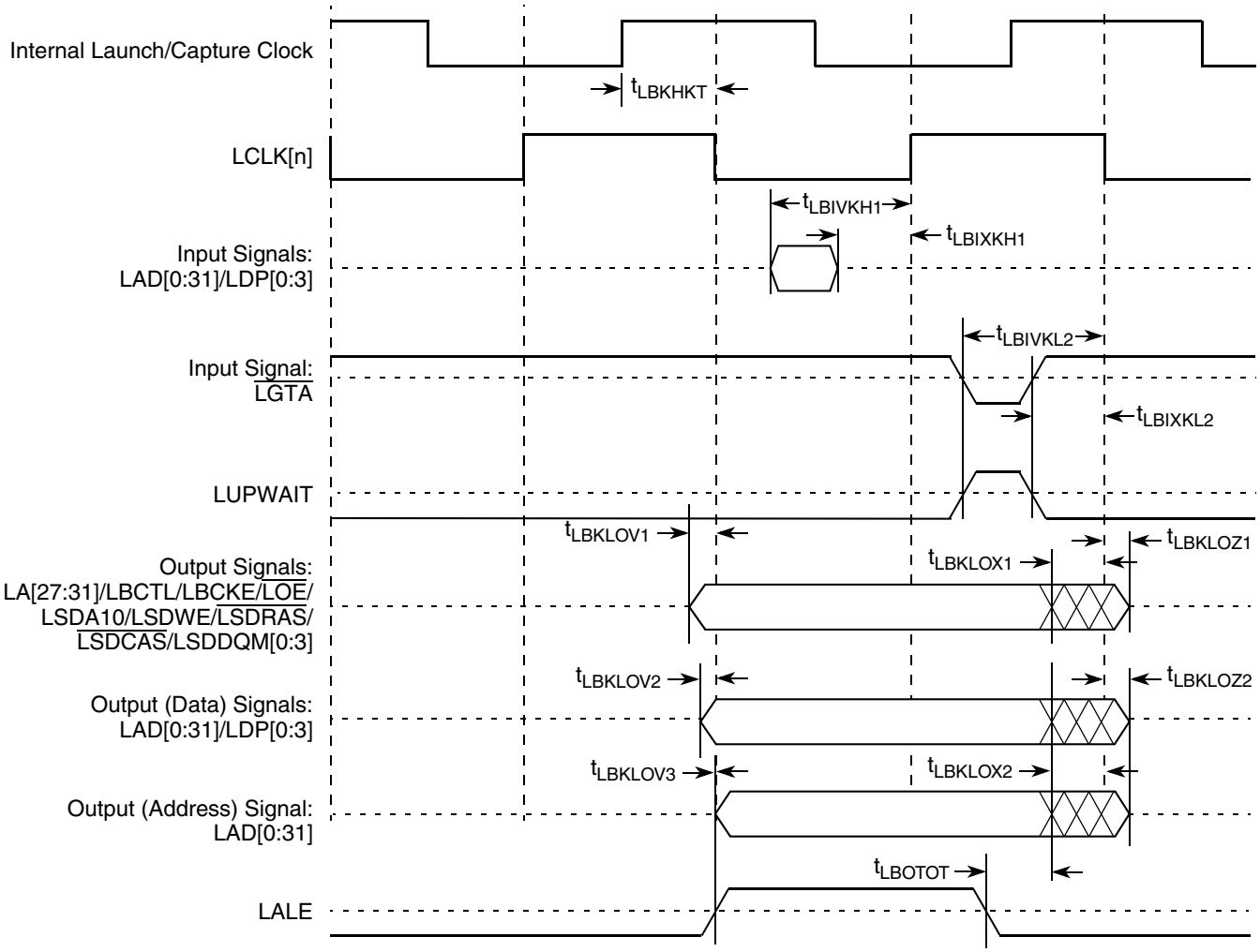


**Figure 25. Local Bus Signals (PLL Bypass Mode)**

## NOTE

In PLL bypass mode, LCLK[n] is the inverted version of the internal clock with the delay of $t_{LBKHKT}$. In this mode, signals are launched at the rising edge of the internal clock and are captured at falling edge of the internal clock withe the exception of $\overline{\text{LGTA}}$/LUPWAIT (which is captured on the rising edge of the internal clock).

# 12 JTAG

This section describes the AC electrical specifications for the IEEE 1149.1 (JTAG) interface of the MPC8533E.

## 12.1 JTAG DC Electrical Characteristics

Table 44 provides the DC electrical characteristics for the JTAG interface.

**Table 44. JTAG DC Electrical Characteristics**

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| High-level input voltage | $V_{IH}$ | 2 | $OV_{DD}$ + 0.3 | V | — |
| Low-level input voltage | $V_{IL}$ | –0.3 | 0.8 | V | — |
| Input current ($OV_{IN}$ = 0 V or $OV_{IN}$ = $OV_{DD}$) | $I_{IN}$ | — | ±5 | μA | 1 |
| High-level output voltage ($OV_{DD}$ = min, $I_{OH}$ = –2 mA) | $V_{OH}$ | 2.4 | — | V | — |
| Low-level output voltage ($OV_{DD}$ = min, $I_{OL}$ = 2 mA) | $V_{OL}$ | — | 0.4 | V | — |

**Note:**
1. Note that the symbol $V_{IN}$, in this case, represents the $OV_{IN}$.

## 12.2 JTAG AC Electrical Specifications

Table 45 provides the JTAG AC timing specifications as defined in Figure 30 through Figure 33.

**Table 45. JTAG AC Timing Specifications (Independent of SYSCLK)[1]**

At recommended operating conditions (see Table 3).

| Parameter | Symbol[2] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| JTAG external clock frequency of operation | $f_{JTG}$ | 0 | 33.3 | MHz | — |
| JTAG external clock cycle time | $t_{JTG}$ | 30 | — | ns | — |
| JTAG external clock pulse width measured at 1.4 V | $t_{JTKHKL}$ | 15 | — | ns | — |
| JTAG external clock rise and fall times | $t_{JTGR}$ & $t_{JTGF}$ | 0 | 2 | ns | — |
| $\overline{TRST}$ assert time | $t_{TRST}$ | 25 | — | ns | 3 |
| Input setup times:<br>Boundary-scan data<br>TMS, TDI | <br>$t_{JTDVKH}$<br>$t_{JTIVKH}$ | <br>4<br>0 | <br>—<br>— | ns | 4 |
| Input hold times:<br>Boundary-scan data<br>TMS, TDI | <br>$t_{JTDXKH}$<br>$t_{JTIXKH}$ | <br>20<br>25 | <br>—<br>— | ns | 4 |
| Valid times:<br>Boundary-scan data<br>TDO | <br>$t_{JTKLDV}$<br>$t_{JTKLOV}$ | <br>4<br>4 | <br>20<br>25 | ns | 5 |
| Output hold times:<br>Boundary-scan data<br>TDO | <br>$t_{JTKLDX}$<br>$t_{JTKLOX}$ | <br>2.5<br>4 | <br>—<br>— | ns | 5 |

# 17 PCI Express

This section describes the DC and AC electrical specifications for the PCI Express bus of the MPC8533E.

## 17.1 DC Requirements for PCI Express SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$

For more information, see Section 16.2, "SerDes Reference Clocks."

## 17.2 AC Requirements for PCI Express SerDes Clocks

Table 53 provides the AC requirements for the PCI Express SerDes clocks.

**Table 53. SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ AC Requirements**

| Symbol[2] | Parameter Description | Min | Typ | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $t_{REF}$ | REFCLK cycle time | — | 10 | — | ns | 1 |
| $t_{REFCJ}$ | REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles | — | — | 100 | ps | — |
| $t_{REFPJ}$ | Phase jitter. Deviation in edge location with respect to mean edge location | –50 | — | 50 | ps | — |

**Notes:**
1. Typical based on *PCI Express Specification 2.0*.
2. Guaranteed by characterization.

## 17.3 Clocking Dependencies

The ports on the two ends of a link must transmit data at a rate that is within 600 parts per million (ppm) of each other at all times. This is specified to allow bit rate clock sources with a ±300 ppm tolerance.

## 17.4 Physical Layer Specifications

The following is a summary of the specifications for the physical layer of PCI Express on this device. For further details as well as the specifications of the transport and data link layer please refer to the *PCI Express Base Specification*. *Rev. 1.0a*.

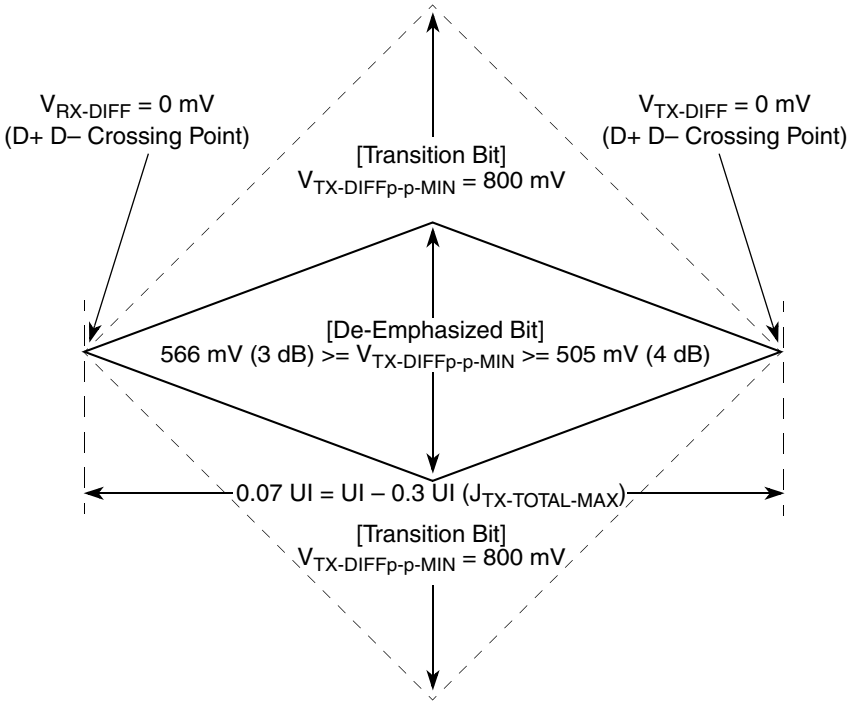


**Figure 52. Minimum Transmitter Timing and Voltage Output Compliance Specifications**

## 17.4.3 Differential Receiver (RX) Input Specifications

Table 55 defines the specifications for the differential input at all receivers. The parameters are specified at the component pins.

**Table 55. Differential Receiver (RX) Input Specifications**

| Symbol | Parameter | Min | Nom | Max | Units | Comments |
|---|---|---|---|---|---|---|
| UI | Unit interval | 399.88 | 400 | 400.12 | ps | Each UI is 400 ps ± 300 ppm. UI does not account for spread spectrum clock dictated variations. See Note 1. |
| $V_{RX-DIFFp-p}$ | Differential peak-to-peak input voltage | 0.175 | — | 1.200 | V | $V_{RX-DIFFp-p} = 2 \times \lvert V_{RX-D+} - V_{RX-D-} \rvert$<br>See Note 2. |
| $T_{RX-EYE}$ | Minimum receiver eye width | 0.4 | — | — | UI | The maximum interconnect media and transmitter jitter that can be tolerated by the receiver can be derived as $T_{RX-MAX-JITTER} = 1 - T_{RX-EYE} = 0.6$ UI.<br>See Notes 2 and 3. |

**Table 57. MPC8533E Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| LCS6/DMA_DACK2 | J16 | O | $BV_{DD}$ | 1 |
| LCS7/DMA_DDONE2 | L18 | O | $BV_{DD}$ | 1 |
| LWE0/LBS0/LSDDQM[0] | J22 | O | $BV_{DD}$ | 4, 8 |
| LWE1/LBS1/LSDDQM[1] | H22 | O | $BV_{DD}$ | 4, 8 |
| LWE2/LBS2/LSDDQM[2] | H23 | O | $BV_{DD}$ | 4, 8 |
| LWE3/LBS3/LSDDQM[3] | H21 | O | $BV_{DD}$ | 4, 8 |
| LALE | J26 | O | $BV_{DD}$ | 4, 7, 8 |
| LBCTL | J25 | O | $BV_{DD}$ | 4, 7, 8 |
| LGPL0/LSDA10 | J20 | O | $BV_{DD}$ | 4, 8 |
| LGPL1/LSDWE | K20 | O | $BV_{DD}$ | 4, 8 |
| LGPL2/LOE/LSDRAS | G20 | O | $BV_{DD}$ | 4, 7, 8 |
| LGPL3/LSDCAS | H18 | O | $BV_{DD}$ | 4, 8 |
| LGPL4/LGTA/LUPWAIT/ LPBSE | L20 | I/O | $BV_{DD}$ | 28 |
| LGPL5 | K19 | O | $BV_{DD}$ | 4, 8 |
| LCKE | L17 | O | $BV_{DD}$ | — |
| LCLK[0:2] | H24, J24, H25 | O | $BV_{DD}$ | — |
| LSYNC_IN | D27 | I | $BV_{DD}$ | — |
| LSYNC_OUT | D28 | O | $BV_{DD}$ | — |
| **DMA** | | | | |
| DMA_DACK[0:1] | Y13, Y12 | O | $OV_{DD}$ | 4, 8, 9 |
| DMA_DREQ[0:1] | AA10, AA11 | I | $OV_{DD}$ | — |
| DMA_DDONE[0:1] | AA7, Y11 | O | $OV_{DD}$ | — |
| **Programmable Interrupt Controller** | | | | |
| UDE | AH15 | I | $OV_{DD}$ | — |
| MCP | AG18 | I | $OV_{DD}$ | — |
| IRQ[0:7] | AG22, AF17, AD21, AF19, AG17, AF16, AC23, AC22 | I | $OV_{DD}$ | — |
| IRQ[8] | AC19 | I | $OV_{DD}$ | — |
| IRQ[9]/DMA_DREQ3 | AG20 | I | $OV_{DD}$ | 1 |
| IRQ[10]/DMA_DACK3 | AE27 | I/O | $OV_{DD}$ | 1 |
| IRQ[11]/DMA_DDONE3 | AE24 | I/O | $OV_{DD}$ | 1 |
| IRQ_OUT | AD14 | O | $OV_{DD}$ | 2 |

**Table 57. MPC8533E Pinout Listing (continued)**

| Signal | Package Pin Number | Pin Type | Power Supply | Notes |
|---|---|---|---|---|
| **DFT** | | | | |
| L1_TSTCLK | AC20 | I | $OV_{DD}$ | 18 |
| L2_TSTCLK | AE17 | I | $OV_{DD}$ | 18 |
| $\overline{\text{LSSD\_MODE}}$ | AH19 | I | $OV_{DD}$ | 18 |
| $\overline{\text{TEST\_SEL}}$ | AH13 | I | $OV_{DD}$ | 3 |
| **Thermal Management** | | | | |
| TEMP_ANODE | Y3 | — | — | 13 |
| TEMP_CATHODE | AA3 | — | — | 13 |
| **Power Management** | | | | |
| ASLEEP | AH17 | O | $OV_{DD}$ | 8, 15, 21 |
| **Power and Ground Signals** | | | | |
| GND | D5, M10, F4, D26, D23, C12, C15, E20, D8, B10, E3, J14, K21, F8, A3, F16, E12, E15, D17, L1, F21, H1, G13, G15, G18, C6, A14, A7, G25, H4, C20, J12, J15, J17, F27, M5, J27, K11, L26, K7, K8, L12, L15, M14, M16, M18, N13, N15, N17, N2, P5, P14, P16, P18, R13, R15, R17, T14, T16, T18, U13, U15, U17, AA8, U6, Y10, AC21, AA17, AC16, V4, AD7, AD18, AE23, AF11, AF14, AG23, AH9, A27, B28, C27 | — | — | — |
| $OV_{DD}$[1:17] | Y16, AB7, AB10, AB13, AC6, AC18, AD9, AD11, AE13, AD15, AD20, AE5, AE22, AF10, AF20, AF24, AF27 | Power for PCI and other standards (3.3 V) | $OV_{DD}$ | — |
| $LV_{DD}$[1:2] | R4, U3 | Power for TSEC1 interfaces (2.5 V, 3.3 V) | $LV_{DD}$ | — |
| $TV_{DD}$[1:2] | N8, R10 | Power for TSEC3 interfaces (2.5 V, 3.3 V) | $TV_{DD}$ | — |
| $GV_{DD}$ | B1, B11, C7, C9, C14, C17, D4, D6, R3, D15, E2, E8,C24, E18, F5, E14, C21, G3, G7, G9, G11, H5, H12, E22, F15, J10, K3, K12, K14, H14, D20, E11, M1, N5 | Power for DDR1 and DDR2 DRAM I/O voltage (1.8 V, 2.5 V) | $GV_{DD}$ | — |
| $BV_{DD}$ | L23, J18, J19, F20, F23, H26, J21, J23 | Power for local bus (1.8 V, 2.5 V, 3.3 V) | $BV_{DD}$ | — |

Note that there is no default for this PLL ratio; these signals must be pulled to the desired values. Also note that the DDR data rate is the determining factor in selecting the CCB bus frequency, since the CCB frequency must equal the DDR data rate.

**Table 60. CCB Clock Ratio**

| Binary Value of LA[28:31] Signals | CCB:SYSCLK Ratio | Binary Value of LA[28:31] Signals | CCB:SYSCLK Ratio |
|---|---|---|---|
| 0000 | 16:1 | 1000 | 8:1 |
| 0001 | Reserved | 1001 | 9:1 |
| 0010 | Reserved | 1010 | 10:1 |
| 0011 | 3:1 | 1011 | Reserved |
| 0100 | 4:1 | 1100 | 12:1 |
| 0101 | 5:1 | 1101 | Reserved |
| 0110 | 6:1 | 1110 | Reserved |
| 0111 | Reserved | 1111 | Reserved |

## 19.3 e500 Core PLL Ratio

Table 61 describes the clock ratio between the e500 core complex bus (CCB) and the e500 core clock. This ratio is determined by the binary value of LBCTL, LALE, and LGPL2 at power up, as shown in Table 61.

**Table 61. e500 Core to CCB Clock Ratio**

| Binary Value of LBCTL, LALE, LGPL2 Signals | e500 core:CCB Clock Ratio | Binary Value of LBCTL, LALE, LGPL2 Signals | e500 core:CCB Clock Ratio |
|---|---|---|---|
| 000 | 4:1 | 100 | 2:1 |
| 001 | Reserved | 101 | 5:2 |
| 010 | Reserved | 110 | 3:1 |
| 011 | 3:2 | 111 | 7:2 |

## 19.4 PCI Clocks

For specifications on the PCI_CLK, refer to the *PCI 2.2 Local Bus Specifications*.

The use of PCI_CLK is optional if SYSCLK is in the range of 33–66 MHz. If SYSCLK is outside this range then use of PCI_CLK is required as a separate PCI clock source, asynchronous with respect to SYSCLK.

## 19.5 Security Controller PLL Ratio

Table 62 shows the SEC frequency ratio.

**Table 62. SEC Frequency Ratio**

| Signal Name | Value (Binary) | CCB CLK:SEC CLK |
|---|---|---|
| LWE_B | 0 | 2:1[1] |
| | 1 | 3:1[2] |

**Notes:**
1. In 2:1 mode the CCB frequency must be operating ≤ 400 MHz.
2. In 3:1 mode any valid CCB can be used. The 3:1 mode is the default ratio for security block.

## 19.6 Frequency Options

### 19.6.1 SYSCLK to Platform Frequency Options

Table 63 shows the expected frequency values for the platform frequency when using a CCB clock to SYSCLK ratio in comparison to the memory bus clock speed.

**Table 63. Frequency Options of SYSCLK with Respect to Memory Bus Speeds**

| CCB to SYSCLK Ratio | SYSCLK (MHz) | | | | | | |
|---|---|---|---|---|---|---|---|
| | 33.33 | 41.66 | 66.66 | 83 | 100 | 111 | 133.33 |
| | Platform /CCB Frequency (MHz) | | | | | | |
| 2 | | | | | | | — |
| 3 | | | | | — | 333 | 400 |
| 4 | | | — | 333 | 400 | 445 | 533 |
| 5 | | | 333 | 415 | 500 | | |
| 6 | | | 400 | 500 | | | |
| 8 | | 333 | 533 | | | | |
| 9 | | 375 | | | | | |
| 10 | 333 | 417 | | | | | |
| 12 | 400 | 500 | | | | | |
| 16 | 533 | | | | | | |

where:

$I_{fw}$ = Forward current
$I_s$ = Saturation current
$V_d$ = Voltage at diode
$V_f$ = Voltage forward biased
$V_H$ = Diode voltage while $I_H$ is flowing
$V_L$ = Diode voltage while $I_L$ is flowing
$I_H$ = Larger diode bias current
$I_L$ = Smaller diode bias current
q = Charge of electron ($1.6 \times 10^{-19}$ C)
n = Ideality factor (normally 1.0)
K = Boltzman's constant ($1.38 \times 10^{-23}$ Joules/K)
T = Temperature (Kelvins)

The ratio of $I_H$ to $I_L$ is usually selected to be 10:1. The above simplifies to the following:

$$\mathbf{V_H - V_L = 1.986 \times 10^{-4} \times nT}$$

Solving for T, the equation becomes:

$$\mathbf{nT} = \frac{V_H - V_L}{1.986 \times 10^{-4}}$$

# 21 System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC8533E.

## 21.1 System Clocking

This device includes six PLLs:

- The platform PLL generates the platform clock from the externally supplied SYSCLK input. The frequency ratio between the platform and SYSCLK is selected using the platform PLL ratio configuration bits as described in Section 19.2, "CCB/SYSCLK PLL Ratio."
- The e500 core PLL generates the core clock as a slave to the platform clock. The frequency ratio between the e500 core clock and the platform clock is selected using the e500 PLL ratio configuration bits as described in Section 19.3, "e500 Core PLL Ratio."
- The PCI PLL generates the clocking for the PCI bus.
- The local bus PLL generates the clock for the local bus.
- There are two PLLs for the SerDes block.

## 21.5 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. All unused active low inputs should be tied to $V_{DD}$, $TV_{DD}$, $BV_{DD}$, $OV_{DD}$, $GV_{DD}$, and $LV_{DD}$ as required. All unused active high inputs should be connected to GND. All NC (no connect) signals must remain unconnected. Power and ground connections must be made to all external $V_{DD}$, $TV_{DD}$, $BV_{DD}$, $OV_{DD}$, $GV_{DD}$, and $LV_{DD}$, and GND pins of the device.

## 21.6 Pull-Up and Pull-Down Resistor Requirements

The MPC8533E requires weak pull-up resistors (2–10 kΩ is recommended) on open drain type pins including $I^2C$ pins and MPIC interrupt pins.

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 65. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion will give unpredictable results.

The following pins must NOT be pulled down during power-on reset: TSEC3_TXD[3], $\overline{\text{HRESET\_REQ}}$, TRIG_OUT/READY/$\overline{\text{QUIESCE}}$, MSRCID[2:4], ASLEEP. The $\overline{\text{DMA\_DACK}}$[0:1] and $\overline{\text{TEST\_SEL}}$ pins must be set to a proper state during POR configuration. Refer to the pinout listing table (Table 57) for more details. Refer to the *PCI 2.2 Local Bus Specifications,* for all pullups required for PCI.

## 21.7 Output Buffer DC Impedance

The MPC8533E drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for $I^2C$). To measure $Z_0$ for the single-ended drivers, an external resistor is connected from the chip pad to $OV_{DD}$ or GND. Then, the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 63). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and $R_P$ is trimmed until the voltage at the pad equals $OV_{DD}/2$. $R_P$ then becomes the

## 21.10 Guidelines for High-Speed Interface Termination

This section provides guidelines for when the SerDes interface is either not used at all or only partly used.

### 21.10.1 SerDes Interface Entirely Unused

If the high-speed SerDes interface is not used at all, the unused pin should be terminated as described in this section. However, the SerDes must always have power applied to its supply pins.

The following pins must be left unconnected (float):

- SD_TX[0:7]
- $\overline{\text{SD\_TX}}$[0:7]

The following pins must be connected to GND:

- SD_RX[0:7]
- $\overline{\text{SD\_RX}}$[0:7]
- SD_REF_CLK
- $\overline{\text{SD\_REF\_CLK}}$

### 21.10.2 SerDes Interface Partly Unused

If only part of the high speed SerDes interface pins are used, the remaining high-speed serial I/O pins should be terminated as described in this section.

The following pins must be left unconnected (float) if not used:

- SD_TX[0:7]
- $\overline{\text{SD\_TX}}$[0:7]

The following pins must be connected to GND if not used:

- SD_RX[0:7]
- $\overline{\text{SD\_RX}}$[0:7]
- SD_REF_CLK
- $\overline{\text{SD\_REF\_CLK}}$

## 21.11 Guideline for PCI Interface Termination

PCI termination, if not used at all, is done as follows.

Option 1

- If PCI arbiter is enabled during POR,
- All AD pins will be driven to the stable states after POR. Therefore, all ADs pins can be floating.
- All PCI control pins can be grouped together and tied to $OV_{DD}$ through a single 10-kΩ resistor.
- It is optional to disable PCI block through DEVDISR register after POR reset.

Option 2

- If PCI arbiter is disabled during POR,
- All AD pins will be in the input state. Therefore, all ADs pins need to be grouped together and tied to $OV_{DD}$ through a single (or multiple) 10-kΩ resistor(s).
- All PCI control pins can be grouped together and tied to $OV_{DD}$ through a single 10-kΩ resistor.

## 21.12 Guideline for LBIU Termination

If the LBIU parity pins are not used, the following list shows the termination recommendation:

- For LDP[0:3]: tie them to ground or the power supply rail via a 4.7-kΩ resistor.
- For LPBSE: tie it to the power supply rail via a 4.7-kΩ resistor (pull-up resistor).

# 22 Device Nomenclature

Ordering information for the parts fully covered by this hardware specifications document is provided in Section 22.3, "Part Marking." Contact your local Freescale sales office or regional marketing team for order information.

## 22.1 Industrial and Commercial Tier Qualification

The MPC8533E device has been tested to meet the commercial tier qualification. Table 69 provides a description for commercial and industrial qualifications.

**Table 69. Commercial and Industrial Description**

| Tier[1] | Typical Application Use Time | Power-On Hours | Example of Typical Applications |
|---|---|---|---|
| Commercial | 5 years | Part-time/ Full-Time | PC's, consumer electronics, office automation, SOHO networking, portable telecom products, PDAs, etc. |
| Industrial | 10 years | Typically Full-Time | Installed telecom equipment, work stations, servers, warehouse equipment, etc. |

**Note:**
1. Refer to Table 2 for operating temperature ranges. Temperature is independent of tier and varies per product.

# 23 Document Revision History

This table provides a revision history for the MPC8533E hardware specification.

**Table 71. MPC8533E Document Revision History**

| Revision | Date | Substantive Change(s) |
|---|---|---|
| 8 | 09/2015 | • In Table 10 and Table 12, removed the output leakage current rows and removed table note 4. |
| 7 | 06/2014 | • In Table 70, “Device Nomenclature,” added full Pb-free part code.<br>• In Table 70, “Device Nomenclature,” added footnotes 3 and 4. |
| 6 | 05/2011 | • Updated the value of $t_{JTKLDX}$ to 2.5 ns from 4ns in Table 45. |
| 5 | 01/2011 | • Updated Table 70. |
| 4 | 09/2010 | • Modified local bus information in Section 1.1, “Key Features,” to show max local bus frequency as 133 MHz.<br>• Added footnote 28 to Table 57.<br>• Updated solder-ball parameter in Table 56. |
| 3 | 11/2009 | • Update Section 20.3.4, “Temperature Diode,”<br>• Update Table 56 Package Parameters from 95.5%sn to 96.5%sn |
| 2 | 01/2009 | •<br>• Update power number table to include 1067 MHz/533 MHz power numbers.<br>• Remove Part number tables from Hardware spec. The part numbers are available on Freescale web site product page.<br>• Removed I/O power numbers from the Hardware spec. and added the table to bring-up guide applacation note<br>• Updated RX_CLK duty cycle min, and max value to meet the industry standard GMII duty cycle.<br>• In Table 35, removed note 1 and renumbered remaining note.<br>• Update paragraph Section 21.3, “Decoupling Recommendations<br>• Update $t_{DDKHMP}$, $t_{DDKHME}$ in Table 18<br>• Update Figure 5 DDR Output Timing Diagram |
| 1 | 06/2008 | Update in Table 18 DDR SDRAM Output AC Timing Specifications tMCK Max value<br>Improvement to Section 16, “High-Speed Serial Interfaces (HSSI)<br>Update Figure 55 Mechanical Dimensions<br>Update in Table 43 Local Bus General Timing Parameters—PLL Bypassed |
| 0 | 04/2008 | Initial release. |