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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of **Embedded - Microprocessors**

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	PowerPC e500v2
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	-
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 90°C (TA)
Security Features	-
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8533vjaqga

Email: info@E-XFL.COM

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- General-purpose chip select machine (GPCM)
- Three user programmable machines (UPMs)
- Parity support
- Default boot ROM chip select with configurable bus width (8, 16, or 32 bits)
- Two enhanced three-speed Ethernet controllers (eTSECs)
 - Three-speed support (10/100/1000 Mbps)
 - Two IEEE Std 802.3[™], IEEE 802.3u, IEEE 802.3x, IEEE 802.3z, IEEE 802.3ac, and IEEE 802.3ab-compliant controllers
 - Support for various Ethernet physical interfaces:
 - 1000 Mbps full-duplex IEEE 802.3 GMII, IEEE 802.3z TBI, RTBI, and RGMII.
 - 10/100 Mbps full- and half-duplex IEEE 802.3 MII, IEEE 802.3 RGMII, and RMII.
 - Flexible configuration for multiple PHY interface configurations.
 - TCP/IP acceleration and QoS features available
 - IP v4 and IP v6 header recognition on receive
 - IP v4 header checksum verification and generation
 - TCP and UDP checksum verification and generation
 - Per-packet configurable acceleration
 - Recognition of VLAN, stacked (queue in queue) VLAN, 802.2, PPPoE session, MPLS stacks, and ESP/AH IP-security headers
 - Supported in all FIFO modes
 - Quality of service support:
 - Transmission from up to eight physical queues
 - Reception to up to eight physical queues
 - Full- and half-duplex Ethernet support (1000 Mbps supports only full duplex):
 - IEEE 802.3 full-duplex flow control (automatic PAUSE frame generation or software-programmed PAUSE frame generation and recognition)
 - Programmable maximum frame length supports jumbo frames (up to 9.6 Kbytes) and IEEE Std 802.1TM virtual local area network (VLAN) tags and priority
 - VLAN insertion and deletion
 - Per-frame VLAN control word or default VLAN for each eTSEC
 - Extracted VLAN control word passed to software separately
 - Retransmission following a collision
 - CRC generation and verification of inbound/outbound frames
 - Programmable Ethernet preamble insertion and extraction of up to 7 bytes
 - MAC address recognition:
 - Exact match on primary and virtual 48-bit unicast addresses
 - VRRP and HSRP support for seamless router fail-over
 - Up to 16 exact-match MAC addresses supported



- Three PCI Express interfaces
 - Two \times 4 link width interfaces and one \times 1 link width interface
 - PCI Express 1.0a compatible
 - Auto-detection of number of connected lanes
 - Selectable operation as root complex or endpoint
 - Both 32- and 64-bit addressing
 - 256-byte maximum payload size
 - Virtual channel 0 only
 - Traffic class 0 only
 - Full 64-bit decode with 32-bit wide windows
- Power management
 - Supports power saving modes: doze, nap, and sleep
 - Employs dynamic power management, which automatically minimizes power consumption of blocks when they are idle
- System performance monitor
 - Supports eight 32-bit counters that count the occurrence of selected events
 - Ability to count up to 512 counter-specific events
 - Supports 64 reference events that can be counted on any of the 8 counters
 - Supports duration and quantity threshold counting
 - Burstiness feature that permits counting of burst events with a programmable time between bursts
 - Triggering and chaining capability
 - Ability to generate an interrupt on overflow
- System access port
 - Uses JTAG interface and a TAP controller to access entire system memory map
 - Supports 32-bit accesses to configuration registers
 - Supports cache-line burst accesses to main memory
 - Supports large block (4-Kbyte) uploads and downloads
 - Supports continuous bit streaming of entire block for fast upload and download
- IEEE Std 1149.1[™]-compliant, JTAG boundary scan
- 783 FC-PBGA package

Electrical Characteristics

Characteristic		Symbol	Recommended Value	Unit	Notes
Three-speed Ethernet I/O voltage		LV _{DD} (eTSEC1)	3.3 V ± 165 mV 2.5 V ± 125 mV	V	4
		TV _{DD} (eTSEC3)	3.3 V ± 165 mV 2.5 V ± 125 mV		
PCI, DUART, PCI Express, system control and power management, I^2C , and JTAG I/O voltage		OV _{DD}	3.3 V ± 165 mV	V	3
Local bus I/O voltage		BV _{DD}	3.3 V ± 165 mV 2.5 V ± 125 mV 1.8 V ± 90 mV	V	5
Input voltage	DDR and DDR2 DRAM signals	MV _{IN}	GND to GV _{DD}	V	2
	DDR and DDR2 DRAM reference	MV _{REF}	GND to GV _{DD} /2	V	2
	Three-speed Ethernet signals	LV _{IN} TV _{IN}	GND to LV _{DD} GND to TV _{DD}	V	4
	Local bus signals	BV _{IN}	GND to BV _{DD}	V	5
	PCI, Local bus, DUART, SYSCLK, system control and power management, I ² C, and JTAG signals	OV _{IN}	GND to OV _{DD}	V	3
Junction tempera	ture range	Тj	0 to 90	°C	_

Table 2. Recommended Operating Conditions (continued)

Notes:

1. This voltage is the input to the filter discussed in Section 21.2, "PLL Power Supply Filtering," and not necessarily the voltage at the AV_{DD} pin, which may be reduced from V_{DD} by the filter.

2. Caution: MV_{IN} must not exceed GV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

3. Caution: OV_{IN} must not exceed OV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

4. **Caution:** T/LV_{IN} must not exceed T/ LV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

5. Caution: BV_{IN} must not exceed BV_{DD} by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.



Table 19. DUART DC Electrical Characteristics (continued)

Parameter	Symbol	Min	Мах	Unit	Notes
Low-level output voltage ($OV_{DD} = min, I_{OL} = 2 mA$)	V _{OL}		0.4	V	

Note:

1. Note that the symbol V_{IN} , in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.

7.2 DUART AC Electrical Specifications

Table 20 provides the AC timing parameters for the DUART interface.

Table 20. DUART AC Timing Specifications

Parameter	Value	Unit	Notes
Minimum baud rate	CCB clock/1,048,576	baud	1
Maximum baud rate	CCB clock/16	baud	2
Oversample rate	16	—	3

Notes:

- 1. CCB clock refers to the platform clock.
- 2. Actual attainable baud rate will be limited by the latency of interrupt processing.

3. The middle of a start bit is detected as the eighth sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each sixteenth sample.

8 Enhanced Three-Speed Ethernet (eTSEC), MII Management

This section provides the AC and DC electrical characteristics for enhanced three-speed and MII management.

8.1 Enhanced Three-Speed Ethernet Controller (eTSEC) (10/100/1000 Mbps)—GMII/MII/TBI/RGMII/RTBI/RMII/FIFO Electrical Characteristics

The electrical characteristics specified here apply to all gigabit media independent interface (GMII), 8-bit FIFO interface (FIFO), serial media independent interface (MII), ten-bit interface (TBI), reduced gigabit media independent interface (RGMII), reduced ten-bit interface (RTBI), and reduced media independent interface (RMII) signals except management data input/output (MDIO) and management data clock (MDC). The 8-bit FIFO interface can operate at 3.3 or 2.5 V. The RGMII and RTBI interfaces are defined for 2.5 V, while the MII, GMII, TBI, and RMII interfaces can be operated at 3.3 or 2.5 V. Whether the GMII, MII, or TBI interface is operated at 3.3 or 2.5 V, the timing is compliant with IEEE 802.3. The RGMII and RTBI interfaces follow the *Reduced Gigabit Media-Independent Interface (RGMII) Specification Version 1.3* (12/10/2000). The RMII interface follows the *RMII Consortium RMII Specification Version 1.2* (3/20/1998). The electrical characteristics for MDIO and MDC are specified in Section 9, "Ethernet Management Interface Electrical Characteristics."



8.3 FIFO, GMII,MII, TBI, RGMII, RMII, and RTBI AC Timing Specifications

The AC timing specifications for FIFO, GMII, MII, TBI, RGMII, RMII, and RTBI are presented in this section.

8.3.1 FIFO AC Specifications

The basis for the AC specifications for the eTSEC FIFO modes is the double data rate RGMII and RTBI specifications, since they have similar performance and are described in a source-synchronous fashion like FIFO modes. However, the FIFO interface provides deliberate skew between the transmitted data and source clock in GMII fashion.

When the eTSEC is configured for FIFO modes, all clocks are supplied from external sources to the relevant eTSEC interface. That is, the transmit clock must be applied to the eTSEC*n* TSEC*n*_TX_CLK, while the receive clock must be applied to pin TSEC*n*_RX_CLK. The eTSEC internally uses the transmit clock to synchronously generate transmit data and outputs an echoed copy of the transmit clock back out onto the TSEC*n*_GTX_CLK pin (while transmit data appears on TSEC*n*_TXD[7:0], for example). It is intended that external receivers capture eTSEC transmit data using the clock on TSEC*n*_GTX_CLK as a source-synchronous timing reference. Typically, the clock edge that launched the data can be used, since the clock is delayed by the eTSEC to allow acceptable set-up margin at the receiver.

Parameter/Condition	Symbol	Min	Тур	Max	Unit	Notes
TX_CLK, GTX_CLK clock period	t _{FIT}	—	8.0	_	ns	—
TX_CLK, GTX_CLK duty cycle	t _{FITH}	45	50	55	%	—
TX_CLK, GTX_CLK peak-to-peak jitter	t _{FITJ}	—	—	250	ps	—
Rise time TX_CLK (20%-80%)	t _{FITR}	—	—	0.75	ns	—
Fall time TX_CLK (80%-20%)	t _{FITF}	—	—	0.75	ns	—
GTX_CLK to FIFO data TXD[7:0], TX_ER, TX_EN hold time	t _{FITDX}	0.5	_	3.0	ns	1

Table 23. FIFO Mode Transmit AC Timing Specification

A summary of the FIFO AC specifications appears in Table 23 and Table 24.

At recommended operating conditions with L/TVDD of 3.3 V \pm 5% or 2.5 V \pm 5%

Note:

1. Data valid t_{FITDV} to GTX_CLK Min setup time is a function of clock period and max hold time.

(Min setup = Cycle time – Max hold).

Table 24. FIFO Mode Receive AC Timing Specification

At recommended operating conditions with L/TVDD of 3.3 V \pm 5% or 2.5 V \pm 5%

Parameter/Condition	Symbol	Min	Тур	Max	Unit	Notes
RX_CLK clock period	t _{FIR}	_	8.0	_	ns	—
RX_CLK duty cycle	t _{FIRH} /t _{FIRH}	45	50	55	%	—
RX_CLK peak-to-peak jitter	t _{FIRJ}			250	ps	



Table 24. FIFO Mode Receive AC Timing Specification (continued)

At recommended operating conditions with L/TVDD of 3.3 V \pm 5% or 2.5 V \pm 5%

Parameter/Condition	Symbol	Min	Тур	Max	Unit	Notes
Rise time RX_CLK (20%–80%)	t _{FIRR}	—	—	0.75	ns	_
Fall time RX_CLK (80%–20%)	t _{FIRF}	—	—	0.75	ns	_
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t _{FIRDV}	1.5	—	—	ns	_
RX_CLK to RXD[7:0], RX_DV, RX_ER hold time	t _{FIRDX}	0.5	—	—	ns	—

Timing diagrams for FIFO appear in Figure 7 and Figure 8.



Figure 8. FIFO Receive AC Timing Diagram

8.3.2 GMII AC Timing Specifications

This section describes the GMII transmit and receive AC timing specifications.

8.3.2.1 GMII Transmit AC Timing Specifications

Table 25 provides the GMII transmit AC timing specifications.

Table 25. GMII Transmit AC Timing Specifications

At recommended operating conditions with L/TVDD of 3.3 V \pm 5% or 2.5 V \pm 5%

Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit	Notes
GTX_CLK clock period	t _{GTX}		8.0		ns	_
GTX_CLK to GMII data TXD[7:0], TX_ER, TX_EN delay	^t GTKHDX	0.2	_	5.0	ns	2
GTX_CLK data clock rise time (20%-80%)	t _{GTXR}			1.0	ns	_



Table 25. GMII Transmit AC Timing Specifications (continued)

At recommended operating conditions with L/TVDD of 3.3 V \pm 5% or 2.5 V \pm 5%

Parameter/Condition	Symbol ¹	Min	Тур	Мах	Unit	Notes
GTX_CLK data clock fall time (80%-20%)	t _{GTXF}		—	1.0	ns	

Notes:

- The symbols used for timing specifications follow the pattern t_{(first two letters of functional block)(signal)(state)} (reference)(state) for inputs and t_(first two letters of functional block) (reference)(state)(signal)(state) for outputs. For example, t_{GTKHDV} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) reaching the valid state (V) to state or setup time. Also, t_{GTKHDX} symbolizes GMII transmit timing (GT) with respect to the high state (H) relative to the time date input signals (D) reaching the valid state (V) to state or setup time. Also, t_{GTKHDX} symbolizes GMII transmit timing (GT) with respect to the t_{GTX} clock reference (K) going to the high state (H) relative to the time date input signals (D) going invalid (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GTX} represents the GMII(G) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
- Data valid t_{GTKHDV} to GTX_CLK Min setup time is a function of clock period and max hold time (Min setup = cycle time Max delay).

Figure 9 shows the GMII transmit AC timing diagram.



Figure 9. GMII Transmit AC Timing Diagram

8.3.2.2 GMII Receive AC Timing Specifications

Table 26 provides the GMII receive AC timing specifications.

Table 26. GMII Receive AC Timing Specifications

At recommended operating conditions with L/TVDD of 3.3 V \pm 5% or 2.5 V \pm 5%

Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit	Notes
RX_CLK clock period	t _{GRX}	—	8.0	—	ns	—
RX_CLK duty cycle	t _{GRXH} /t _{GRX}	35	—	65	%	—
RXD[7:0], RX_DV, RX_ER setup time to RX_CLK	t _{GRDVKH}	2.0	—	—	ns	—
RX_CLK to RXD[7:0], RX_DV, RX_ER hold time	t _{GRDXKH}	0.5	—	—	ns	—
RX_CLK clock rise (20%–80%)	t _{GRXR}	_	—	1.0	ns	—



Table 26. GMII Receive AC Timing Specifications (continued)

At recommended operating conditions with L/TVDD of 3.3 V \pm 5% or 2.5 V \pm 5%

Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit	Notes
RX_CLK clock fall time (80%–20%)	t _{GRXF}		—	1.0	ns	—

Note:

1. The symbols used for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{GRDVKH} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{RX} clock reference (K) going to the high state (H) or setup time. Also, t_{GRDXKL} symbolizes GMII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{GRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{GRX} represents the GMII (G) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).}

Figure 10 provides the AC test load for eTSEC.



Figure 10. eTSEC AC Test Load

Figure 11 shows the GMII receive AC timing diagram.



Figure 11. GMII Receive AC Timing Diagram

8.4 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.



Table 28. MII Receive AC Timing Specifications (continued)

At recommended operating conditions with L/TVDD of 3.3 V \pm 5%.or 2.5 V \pm 5%.

Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit	Notes
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t _{MRDVKH}	10.0	—	—	ns	—
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t _{MRDXKH}	10.0	—	—	ns	—
RX_CLK clock rise (20%–80%)	t _{MRXR}	1.0	—	4.0	ns	—
RX_CLK clock fall time (80%–20%)	t _{MRXF}	1.0	—	4.0	ns	—

Note:

1. The symbols used for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).}}

Figure 13 provides the AC test load for eTSEC.



Figure 13. eTSEC AC Test Load

Figure 14 shows the MII receive AC timing diagram.



Figure 14. MII Receive AC Timing Diagram

8.5 TBI AC Timing Specifications

This section describes the TBI transmit and receive AC timing specifications.



8.5.1 TBI Transmit AC Timing Specifications

Table 29 provides the TBI transmit AC timing specifications.

Table 29. TBI Transmit AC Timing Specifications

At recommended operating conditions with L/TVDD of 3.3 V \pm 5% or 2.5 V \pm 5%

Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit	Notes
GTX_CLK clock period	t _{GTX}	—	8.0	_	ns	—
GTX_CLK to TCG[9:0] delay time	t _{TTKHDX}	0.2	—	5.0	ns	2
GTX_CLK rise (20%–80%)	t _{TTXR}	—	—	1.0	ns	—
GTX_CLK fall time (80%–20%)	t _{TTXF}	—	—	1.0	ns	—

Notes:

1. The symbols used for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{TTKHDV} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, t_{TTKHDX} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the valid state (V) or setup time. Also, t_{TTKHDX} symbolizes the TBI transmit timing (TT) with respect to the time from t_{TTX} (K) going high (H) until the referenced data signals (D) reach the invalid state (X) or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{TTX} represents the TBI (T) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).}

Figure 15 shows the TBI transmit AC timing diagram.



Figure 15. TBI Transmit AC Timing Diagram

8.5.2 TBI Receive AC Timing Specifications

Table 30 provides the TBI receive AC timing specifications.

Table 30. TBI Receive AC	Timing Specifications
--------------------------	-----------------------

At recommended operating conditions with L/TVDD of 3.3 V \pm 5% or 2.5 V \pm 5%.

Parameter/Condition	Symbol ¹	Min	Тур	Max	Unit	Notes
PMA_RX_CLK[0:1] clock period	t _{TRX}	_	16.0	_	ns	_
PMA_RX_CLK[0:1] skew	t _{SKTRX}	7.5		8.5	ns	_

Data valid t_{TTKHDV} to GTX_CLK Min setup time is a function of clock period and max hold time (Min setup = cycle time – Max delay).



8.5.5 RMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.

8.5.5.1 RMII Transmit AC Timing Specifications

The RMII transmit AC timing specifications are in Table 33.

Table 33. RMII Transmit AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V \pm 5% or 2.5 V \pm 5%.

Parameter/Condition	Symbol ¹	Min	Тур	Мах	Unit	Notes
REF_CLK clock period	t _{RMT}	15.0	20.0	25.0	ns	—
REF_CLK duty cycle	t _{RMTH}	35	50	65	%	—
REF_CLK peak-to-peak jitter	t _{RMTJ}	-	_	250	ps	—
Rise time REF_CLK (20%–80%)	t _{RMTR}	1.0	_	2.0	ns	—
Fall time REF_CLK (80%–20%)	t _{RMTF}	1.0	_	2.0	ns	—
REF_CLK to RMII data TXD[1:0], TX_EN delay	t _{RMTDX}	1.0	_	10.0	ns	—

Note:

The symbols used for timing specifications follow the pattern of t<sub>(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t<sub>(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
</sub></sub>

Figure 19 shows the RMII transmit AC timing diagram.



Figure 19. RMII Transmit AC Timing Diagram







Figure 26. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 4 (PLL Enabled)



JTAG

Table 45. JTAG AC Timing Specifications (Independent of SYSCLK)¹ (continued)

At recommended operating conditions (see Table 3).

Parameter	Symbol ²	Min	Max	Unit	Notes
JTAG external clock to output high impedance: Boundary-scan data TDO	t _{JTKLDZ} t _{JTKLOZ}	3 3	19 9	ns	5

Notes:

- All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Figure 30). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
- 2. The symbols used for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)(reference)(state) for inputs and t_{(first two letters of functional block)(reference)(state)(signal)(state)} for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).}
- 3. TRST is an asynchronous level sensitive signal. The setup time is for test purposes only.
- 4. Non-JTAG signal input timing with respect to t_{TCLK}.
- 5. Non-JTAG signal output timing with respect to t_{TCLK}.

Figure 30 provides the AC test load for TDO and the boundary-scan outputs.



Figure 30. AC Test Load for the JTAG Interface

Figure 31 provides the JTAG clock input timing diagram.



 $VM = Midpoint Voltage (OV_{DD}/2)$

Figure 31. JTAG Clock Input Timing Diagram

Figure 32 provides the TRST timing diagram.





Figure 34 provides the AC test load for the I^2C .



Figure 34. I²C AC Test Load

Figure 35 shows the AC timing diagram for the I^2C bus.



Figure 35. I²C Bus AC Timing Diagram

14 GPIO

This section describes the DC and AC electrical specifications for the GPIO interface of the MPC8533E.

14.1 GPIO DC Electrical Characteristics

Table 48 provides the DC electrical characteristics for the GPIO interface.

Parameter	Symbol	Min	Мах	Unit	Notes
High-level input voltage	V _{IH}	2	OV _{DD} + 0.3	V	
Low-level input voltage	V _{IL}	-0.3	0.8	V	
Input current ($V_{IN} = 0 V \text{ or } V_{IN} = V_{DD}$)	I _{IN}	—	±5	μA	1
High-level output voltage ($OV_{DD} = mn$, $I_{OH} = -2 mA$)	V _{OH}	2.4	—	V	
Low-level output voltage ($OV_{DD} = min, I_{OL} = 2 mA$)	V _{OL}	—	0.4	V	_

Note:

1. Note that the symbol V_{IN} , in this case, represents the OV_{IN} symbol referenced in Table 1 and Table 2.





Using this waveform, the definitions are as follows. To simplify illustration, the following definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment.

1. Single-Ended Swing

The transmitter output signals and the receiver input signals SDn_TX , $\overline{SDn_TX}$, SDn_RX and $\overline{SDn_RX}$ each have a peak-to-peak swing of A - B Volts. This is also referred as each signal wire's Single-Ended Swing.

2. Differential Output Voltage, V_{OD} (or Differential Output Swing):

The Differential Output Voltage (or Swing) of the transmitter, V_{OD} , is defined as the difference of the two complimentary output voltages: $V_{SDn_TX} - V_{\overline{SDn_TX}}$. The V_{OD} value can be either positive or negative.

3. Differential Input Voltage, V_{ID} (or Differential Input Swing):

The Differential Input Voltage (or Swing) of the receiver, V_{ID} , is defined as the difference of the two complimentary input voltages: $V_{SDn_RX} - V_{\overline{SDn_RX}}$. The V_{ID} value can be either positive or negative.

4. Differential Peak Voltage, VDIFFp

The peak value of the differential transmitter output signal or the differential receiver input signal is defined as Differential Peak Voltage, $V_{DIFFp} = |A - B|$ Volts.

5. Differential Peak-to-Peak, V_{DIFFp-p}

Since the differential output signal of the transmitter and the differential input signal of the receiver each range from A – B to –(A – B) Volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as Differential Peak-to-Peak Voltage, $V_{DIFFp-p} = 2*V_{DIFFp} = 2*|(A – B)|$ Volts, which is twice of differential swing in amplitude, or twice of the differential peak. For example, the output differential peak-peak voltage can also be calculated as $V_{TX-DIFFp-p} = 2*|V_{OD}|$.

6. Differential Waveform

The differential waveform is constructed by subtracting the inverting signal ($\overline{\text{SD}n_TX}$, for example) from the non-inverting signal ($\overline{\text{SD}n_TX}$, for example) within a differential pair. There is only one signal trace curve in a differential waveform. The voltage represented in the differential waveform is not referenced to ground. Refer to Figure 40 as an example for differential waveform.

7. Common Mode Voltage, V_{cm}

The Common Mode Voltage is equal to one half of the sum of the voltages between each conductor of a balanced interchange circuit and ground. In this example, for SerDes output, $V_{cm_out} = V_{SDn_TX} + V_{\overline{SDn_TX}} = (A + B)/2$, which is the arithmetic mean of the two complimentary output voltages within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. Sometimes, it may be even different between the receiver input and driver output circuits within the same component. It is also referred as the DC offset in some occasions.



18.2 Mechanical Dimensions of the MPC8533E FC-PBGA

Figure 55 shows the mechanical dimensions and bottom surface nomenclature of the MPC8533E, 783 FC-PBGA package without a lid.



Notes:

- 1. All dimensions are in millimeters.
- 2. Dimensions and tolerances per ASME Y14.5M-1994.
- 3. Maximum solder ball diameter measured parallel to datum A.
- 4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
- 5. Parallelism measurement shall exclude any effect of mark on top surface of package.
- 6. Capacitors may not be present on all parts. Care must be taken not to short exposed metal capacitor pads.
- 7. All dimensions are symmetric across the package center lines, unless dimensioned otherwise.

Figure 55. Mechanical Dimensions and Bottom Surface Nomenclature of the MPC8533E FC-PBGA without a Lid



Clocking

19.5 Security Controller PLL Ratio

Table 62 shows the SEC frequency ratio.

Table 62. SEC Frequency Ratio

Signal Name	Value (Binary)	CCB CLK:SEC CLK
LWE_B	0	2:1 ¹
	1	3:1 ²

Notes:

1. In 2:1 mode the CCB frequency must be operating \leq 400 MHz.

2. In 3:1 mode any valid CCB can be used. The 3:1 mode is the default ratio for security block.

19.6 Frequency Options

19.6.1 SYSCLK to Platform Frequency Options

Table 63 shows the expected frequency values for the platform frequency when using a CCB clock to SYSCLK ratio in comparison to the memory bus clock speed.

CCB to SYSCLK Ratio	SYSCLK (MHz)						
	33.33	41.66	66.66	83	100	111	133.33
			Platform	CCB Freque	ncy (MHz)		
2							—
3						333	400
4			—	333	400	445	533
5			333	415	500		
6			400	500			
8		333	533		_		
9		375					
10	333	417					
12	400	500					
16	533		-				

 Table 63. Frequency Options of SYSCLK with Respect to Memory Bus Speeds



19.6.2 Platform to FIFO Restrictions

Please note the following FIFO maximum speed restrictions based on platform speed. Refer to Section 4.4, "Platform to FIFO Restrictions," for additional information.

Platform Speed (MHz)	Maximum FIFO Speed for Reference Clocks TSEC <i>n</i> _TX_CLK, TSEC <i>n</i> _RX_CLK (MHz) ¹
533	126
400	94

Table 64. FIFO Maximum Speed Restrictions

Note:

1. FIFO speed should be less than 24% of the platform speed.

20 Thermal

This section describes the thermal specifications of the MPC8533E.

20.1 Thermal Characteristics

Table 65 provides the package thermal characteristics.

 Table 65. Package Thermal Characteristics

Characteristic	JEDEC Board	Symbol	Value	Unit	Notes
Junction-to-ambient natural convection	Single layer board (1s)	R_{\thetaJA}	26	°C/W	1, 2
Junction-to-ambient natural convection	Four layer board (2s2p)	R_{\thetaJA}	21	°C/W	1, 2
Junction-to-ambient (@200 ft/min)	Single layer board (1s)	R_{\thetaJA}	21	°C/W	1, 2
Junction-to-ambient (@200 ft/min)	Four layer board (2s2p)	R_{\thetaJA}	17	°C/W	1, 2
Junction-to-board thermal	—	$R_{\theta JB}$	12	°C/W	3
Junction-to-case thermal	_	$R_{ ext{ heta}JC}$	<0.1	°C/W	4

Notes:

 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, airflow, power dissipation of other components on the board, and board thermal resistance.

2. Per JEDEC JESD51-2 and JESD51-6 with the board (JESD51-9) horizontal.

3. Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

4. Thermal resistance between the active surface of the die and the case top surface determined by the cold plate method (MIL SPEC-883 Method 1012.1) with the calculated case temperature. Actual thermal resistance is less than 0.1°C/W.



Thermal

Table 66 provides the thermal resistance with heat sink in open flow.

Heat Sink with Thermal Grease	Air Flow	Thermal Resistance (°C/W)
Wakefield $53 \times 53 \times 25$ mm pin fin	Natural convection	6.1
Wakefield 53 \times 53 \times 25 mm pin fin	1 m/s	3.0
Aavid $35 \times 31 \times 23$ mm pin fin	Natural convection	8.1
Aavid $35 \times 31 \times 23$ mm pin fin	1 m/s	4.3
Aavid $30 \times 30 \times 9.4$ mm pin fin	Natural convection	11.6
Aavid $30 \times 30 \times 9.4$ mm pin fin	1 m/s	6.7
Aavid $43 \times 41 \times 16.5$ mm pin fin	Natural convection	8.3
Aavid $43 \times 41 \times 16.5$ mm pin fin	1 m/s	4.3

Table 66. Thermal Resistance with Heat Sink in Open Flow

Simulations with heat sinks were done with the package mounted on the 2s2p thermal test board. The thermal interface material was a typical thermal grease such as Dow Corning 340 or Wakefield 120 grease. For system thermal modeling, the MPC8533E thermal model without a lid is shown in Figure 56. The substrate is modeled as a block $29 \times 29 \times 1.18$ mm with an in-plane conductivity of 18.0 W/m•K and a through-plane conductivity of 1.0 W/m•K. The solder balls and air are modeled as a single block $29 \times 29 \times 0.58$ mm with an in-plane conductivity of 0.034 W/m•K and a through plane conductivity of 12.1 W/m•K. The die is modeled as 7.6×8.4 mm with a thickness of 0.75 mm. The bump/underfill layer is modeled as a collapsed thermal resistance between the die and substrate assuming a conductivity of 6.5 W/m•K in the thickness dimension of 0.07 mm. The die is centered on the substrate. The thermal model uses approximate dimensions to reduce grid. Please refer to Figure 55 for actual dimensions.

20.2 Recommended Thermal Model

Table 67 shows the MPC8533E thermal model.

Conductivity	Value	Units
Die (7.6 × 8.4 × 0.75mm)		
Silicon	Temperature dependent	_
Bump/Underfill (7.6 \times 8.4 \times 0.070 mm) Collapsed Thermal Resistance		
Kz	6.5	W/m∙K
Substrate (29 × 29 × 1.18 mm)		
Кх	18	W/m∙K
Ку	18	
Kz	1.0	



been encoded such that a high voltage level puts the device into the default state and external resistors are needed only when non-default settings are required by the user.

Careful board layout with stubless connections to these pull-down resistors coupled with the large value of the pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.

The platform PLL ratio and e500 PLL ratio configuration pins are not equipped with these default pull-up devices.

21.9 JTAG Configuration Signals

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 65. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion will give unpredictable results.

Boundary-scan testing is enabled through the JTAG interface signals. The TRST signal is optional in the IEEE 1149.1 specification, but is provided on all processors built on Power ArchitectureTM technology. The device requires TRST to be asserted during reset conditions to ensure the JTAG boundary logic does not interfere with normal chip operation. While it is possible to force the TAP controller to the reset state using only the TCK and TMS signals, generally systems will assert TRST during the power-on reset flow. Simply tying TRST to HRESET is not practical because the JTAG interface is also used for accessing the common on-chip processor (COP) function.

The COP function of these processors allow a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert HRESET or TRST in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic. The arrangement shown in Figure 65 allows the COP port to independently assert HRESET or TRST, while ensuring that the target can drive HRESET as well.

The COP interface has a standard header, shown in Figure 64, for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.

There is no standardized way to number the COP header; consequently, many different pin numbers have been observed from emulator vendors. Some are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom, while still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 64 is common to all known emulators.