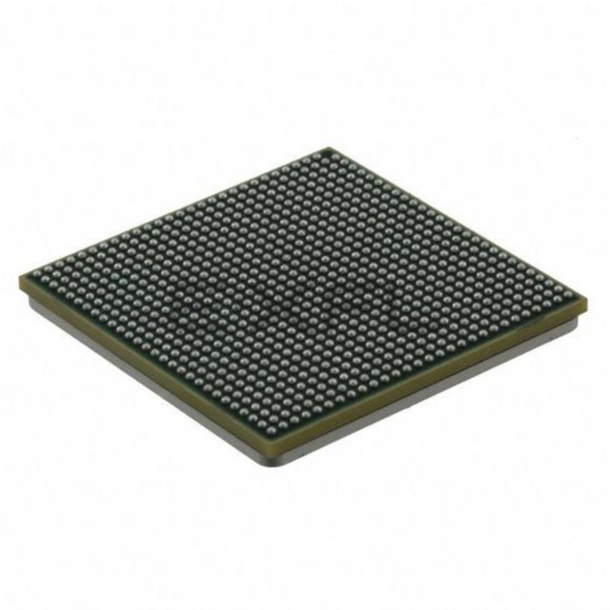

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

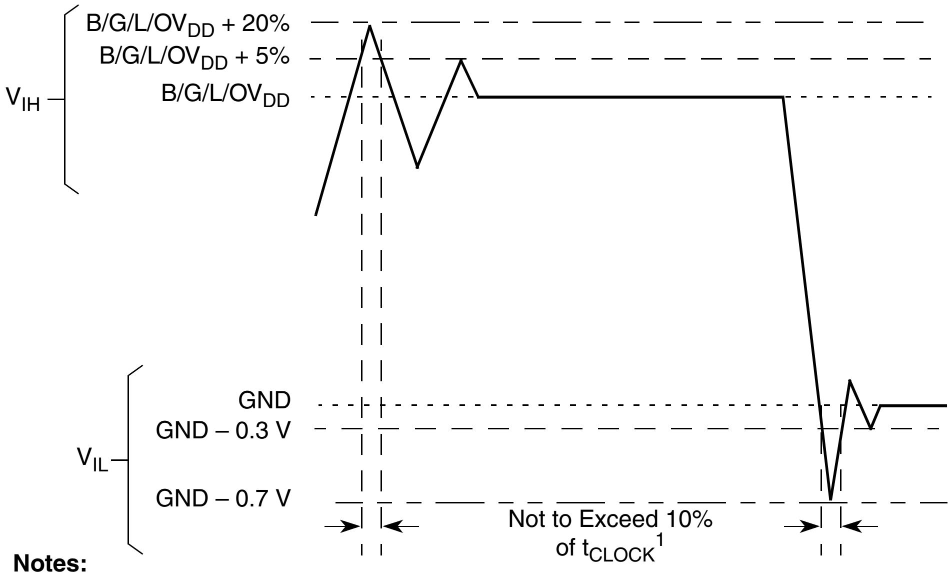
Details	
Product Status	Obsolete
Core Processor	PowerPC e500v2
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	667MHz
Co-Processors/DSP	-
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 90°C (TA)
Security Features	-
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8533vtalf

— Double-precision floating-point APU. Provides an instruction set for double-precision (64-bit) floating-point instructions that use the 64-bit GPRs.
— 36-bit real addressing
— Embedded vector and scalar single-precision floating-point APUs. Provide an instruction set for single-precision (32-bit) floating-point instructions.
— Memory management unit (MMU). Especially designed for embedded applications. Supports 4-Kbyte–4-Gbyte page sizes.
— Enhanced hardware and software debug support
— Performance monitor facility that is similar to, but separate from, the device performance monitor

The e500 defines features that are not implemented on this device. It also generally defines some features that this device implements more specifically. An understanding of these differences can be critical to ensure proper operations.

- 256-Kbyte L2 cache/SRAM
  — Flexible configuration
  — Full ECC support on 64-bit boundary in both cache and SRAM modes
  — Cache mode supports instruction caching, data caching, or both.
  — External masters can force data to be allocated into the cache through programmed memory ranges or special transaction types (stashing).
    – 1, 2, or 4 ways can be configured for stashing only.
  — Eight-way set-associative cache organization (32-byte cache lines)
  — Supports locking entire cache or selected lines. Individual line locks are set and cleared through Book E instructions or by externally mastered transactions.
  — Global locking and flash clearing done through writes to L2 configuration registers
  — Instruction and data locks can be flash cleared separately.
  — SRAM features include the following:
    – I/O devices access SRAM regions by marking transactions as snoopable (global).
    – Regions can reside at any aligned location in the memory map.
    – Byte-accessible ECC is protected using read-modify-write transaction accesses for smaller-than-cache-line accesses.
- Address translation and mapping unit (ATMU)
  — Eight local access windows define mapping within local 36-bit address space.
  — Inbound and outbound ATMUs map to larger external address spaces.
    – Three inbound windows plus a configuration window on PCI and PCI Express
    – Four outbound windows plus default translation for PCI and PCI Express
- DDR/DDR2 memory controller
  — Programmable timing supporting DDR and DDR2 SDRAM
  — 64-bit data interface

Figure 2 shows the undershoot and overshoot voltages at the interfaces of the MPC8533E.



Notes:

1. t_{CLOCK} refers to the clock period associated with the respective interface:
   For I^2C and JTAG, t_{CLOCK} references SYSCLK.
   For DDR, t_{CLOCK} references MCLK.
   For eTSEC, t_{CLOCK} references EC_GTX_CLK125.
   For LBIU, t_{CLOCK} references LCLK.
   For PCI, t_{CLOCK} references PCI_CLK or SYSCLK.
2. Please note that with the PCI overshoot allowed (as specified above), the device does not fully comply with the maximum AC ratings and device protection guideline outlined in Section 4.2.2.3 of the *PCI 2.2 Local Bus Specifications*.

Figure 2. Overshoot/Undershoot Voltage for $GV_{DD}/OV_{DD}/LV_{DD}/BV_{DD}/TV_{DD}$

The core voltage must always be provided at nominal 1.0 V (see Table 2 for actual recommended core voltage). Voltage to the processor interface I/Os are provided through separate sets of supply pins and must be provided at the voltages shown in Table 2. The input voltage threshold scales with respect to the associated I/O supply voltage. OV_{DD} and LV_{DD} based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR2 SDRAM interface uses a single-ended differential receiver referenced the externally supplied MV_{REF} signal (nominally set to $GV_{DD}/2$) as is appropriate for the SSTL2 electrical signaling standard.

8.2 eTSEC DC Electrical Characteristics

All GMII, MII, TBI, RGMII, RTBI, RMII, and FIFO drivers and receivers comply with the DC parametric attributes specified in Table 21 and Table 22. The potential applied to the input of a GMII, MII, TBI, RTBI, RMII, and FIFO receiver may exceed the potential of the receiver's power supply (that is, a GMII driver powered from a 3.6-V supply driving V_{OH} into a GMII receiver powered from a 2.5-V supply). Tolerance for dissimilar GMII driver and receiver supply potentials is implicit in these specifications. The RGMII and RTBI signals are based on a 2.5-V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

Table 21. GMII, MII, TBI, RMII and FIFO DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit	Notes
Supply voltage 3.3 V	LV_{DD} TV_{DD}	3.135	3.465	V	1, 2
Output high voltage (LV_{DD}/TV_{DD} = Min, I_{OH} = –4.0 mA)	V_{OH}	2.4	—	V	—
Output low voltage (LV_{DD}/TV_{DD} = Min, I_{OL} = 4.0 mA)	V_{OL}	—	0.5	V	—
Input high voltage	V_{IH}	1.95	—	V	—
Input low voltage	V_{IL}	—	0.90	V	—
Input high current (V_{IN} = LV_{DD}, V_{IN} = TV_{DD})	I_{IH}	—	40	μA	1, 2, 3
Input low current (V_{IN} = GND)	I_{IL}	–600	—	μA	3

Notes:
1. LV_{DD} supports eTSEC1.
2. TV_{DD} supports eTSEC3.
3. The symbol V_{IN}, in this case, represents the LV_{IN} and TV_{IN} symbols referenced in Table 1 and Table 2.

Table 22. GMII, MII, RMII, RGMII, RTBI, TBI, and FIFO DC Electrical Characteristics

Parameters	Symbol	Min	Max	Unit	Notes
Supply voltage 2.5 V	LV_{DD}/TV_{DD}	2.375	2.625	V	1, 2
Output high voltage (LV_{DD}/TV_{DD} = Min, I_{OH} = –1.0 mA)	V_{OH}	2.0	—	V	—
Output low voltage (LV_{DD}/TV_{DD} = Min, I_{OL} = 1.0 mA)	V_{OL}	—	0.4	V	—
Input high voltage	V_{IH}	1.70	—	V	—
Input low voltage	V_{IL}	—	0.7	V	—
Input current (V_{IN} = 0, V_{IN} = LV_{DD}, V_{IN} = TV_{DD})	I_{IN}	—	±15	μA	1, 2, 3

Notes:
1. LV_{DD} supports eTSEC1.
2. TV_{DD} supports eTSEC3.
3. The symbol V_{IN}, in this case, represents the LV_{IN} and TV_{IN} symbols referenced in Table 1 and Table 2.

Table 32. RGMII and RTBI AC Timing Specifications (continued)

At recommended operating conditions with L/TV_{DD} of 2.5 V ± 5%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
Fall time (20%–80%)	t_{RGTF}	—	—	0.75	ns	—

Notes:
1. In general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t_{RGT} represents the TBI (T) receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
2. This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns will be added to the associated clock signal.
3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.
5. Guaranteed by design.

Figure 18 shows the RGMII and RTBI AC timing and multiplexing diagrams.

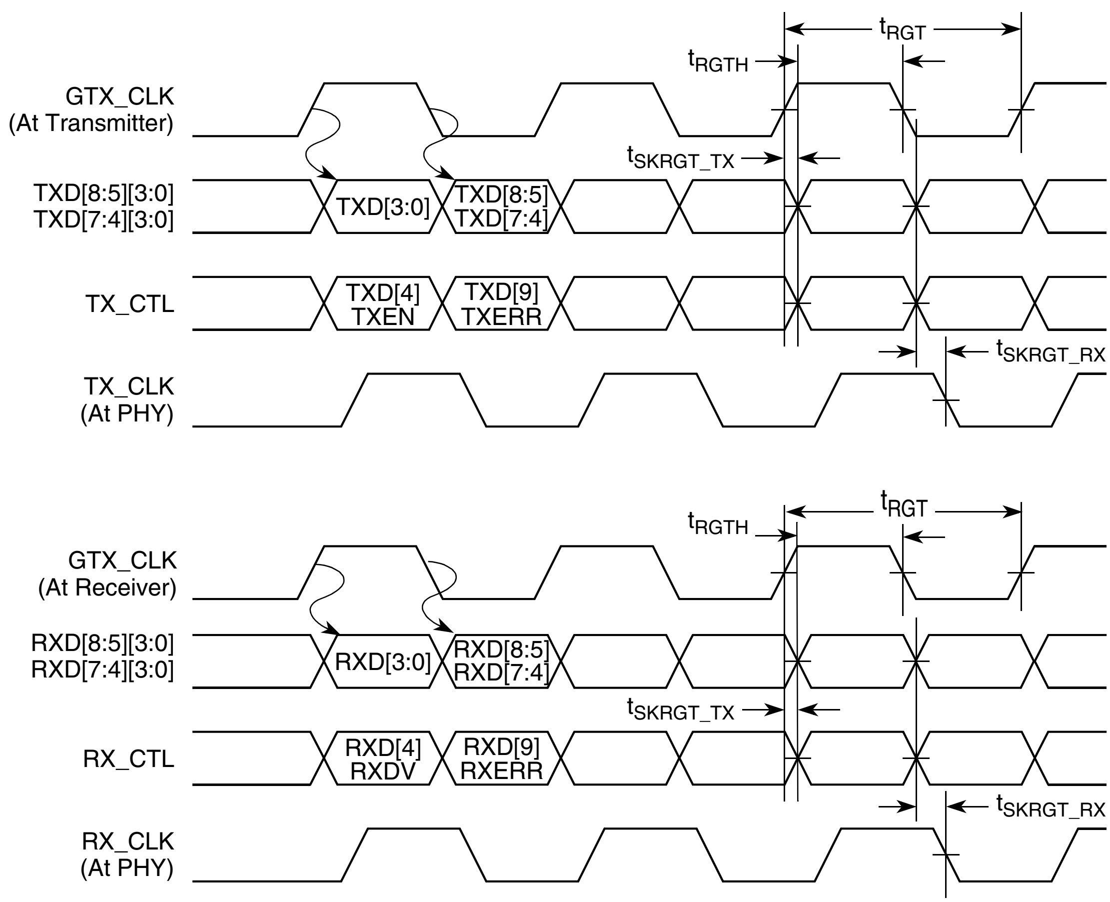


Figure 18. RGMII and RTBI AC Timing and Multiplexing Diagrams

8.5.5 RMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.

8.5.5.1 RMII Transmit AC Timing Specifications

The RMII transmit AC timing specifications are in Table 33.

Table 33. RMII Transmit AC Timing Specifications

At recommended operating conditions with L/TV_{DD} of 3.3 V ± 5% or 2.5 V ± 5%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
REF_CLK clock period	t_{RMT}	15.0	20.0	25.0	ns	—
REF_CLK duty cycle	t_{RMTH}	35	50	65	%	—
REF_CLK peak-to-peak jitter	t_{RMTJ}	—	—	250	ps	—
Rise time REF_CLK (20%–80%)	t_{RMTR}	1.0	—	2.0	ns	—
Fall time REF_CLK (80%–20%)	t_{RMTF}	1.0	—	2.0	ns	—
REF_CLK to RMII data TXD[1:0], TX_EN delay	t_{RMTDX}	1.0	—	10.0	ns	—

Note:

1. The symbols used for timing specifications follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)(reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

Figure 19 shows the RMII transmit AC timing diagram.

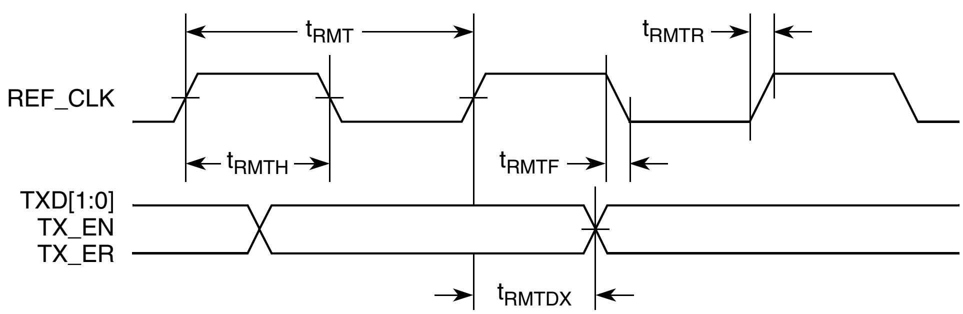


Figure 19. RMII Transmit AC Timing Diagram

Table 39. Local Bus DC Electrical Characteristics (1.8 V DC) (continued)

Parameter	Symbol	Min	Max	Unit	Notes
High-level output voltage (BV_{DD} = min, I_{OH} = –2 mA)	V_{OH}	1.35	—	V	—
Low-level output voltage (BV_{DD} = min, I_{OL} = 2 mA)	V_{OL}	—	0.45	V	—

10.2 Local Bus AC Electrical Specifications

Table 40 describes the general timing parameters of the local bus interface at BV_{DD} = 3.3 V. For information about the frequency range of local bus see Section 19.1, "Clock Ranges."

Table 40. Local Bus General Timing Parameters (BV_{DD} = 3.3 V)—PLL Enabled

Parameter	Symbol[1]	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	7.5	12	ns	2
Local bus duty cycle	t_{LBKH}/t_{LBK}	43	57	%	—
LCLK[n] skew to LCLK[m] or LSYNC_OUT	$t_{LBKSKEW}$	—	150	ps	7, 8
Input setup to local bus clock (except LUPWAIT)	$t_{LBIVKH1}$	2.5	—	ns	3, 4
LUPWAIT input setup to local bus clock	$t_{LBIVKH2}$	1.85	—	ns	3, 4
Input hold from local bus clock (except LUPWAIT)	$t_{LBIXKH1}$	1.0	—	ns	3, 4
LUPWAIT input hold from local bus clock	$t_{LBIXKH2}$	1.0	—	ns	3, 4
LALE output transition to LAD/LDP output transition (LATCH setup and hold time)	t_{LBOTOT}	1.5	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	$t_{LBKHOV1}$	—	2.9	ns	—
Local bus clock to data valid for LAD/LDP	$t_{LBKHOV2}$	—	2.8	ns	—
Local bus clock to address valid for LAD	$t_{LBKHOV3}$	—	2.7	ns	3
Local bus clock to LALE assertion	$t_{LBKHOV4}$	—	2.7	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	$t_{LBKHOX1}$	0.7	—	ns	3
Output hold from local bus clock for LAD/LDP	$t_{LBKHOX2}$	0.7	—	ns	3
Local bus clock to output high Impedance (except LAD/LDP and LALE)	$t_{LBKHOZ1}$	—	2.5	ns	5

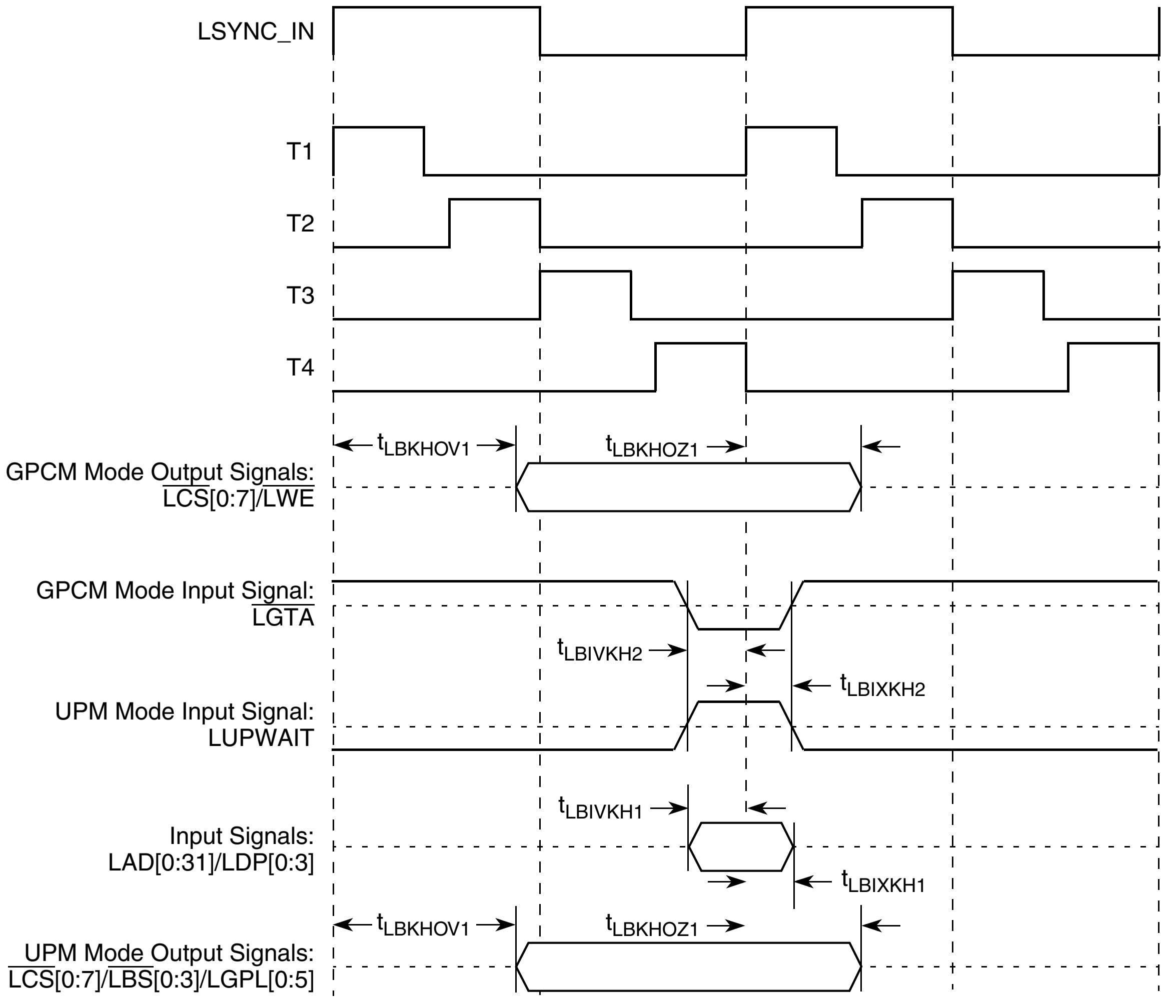


Figure 28. Local Bus Signals, GPCM/UPM Signals for LCCR[CLKDIV] = 8 or 16 (PLL Enabled)

Figure 38 shows the PCI input AC timing conditions.

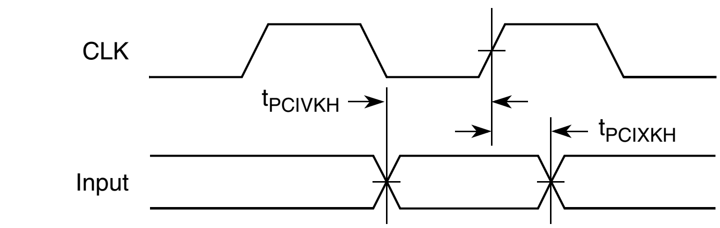


Figure 38. PCI Input AC Timing Measurement Conditions

Figure 39 shows the PCI output AC timing conditions.

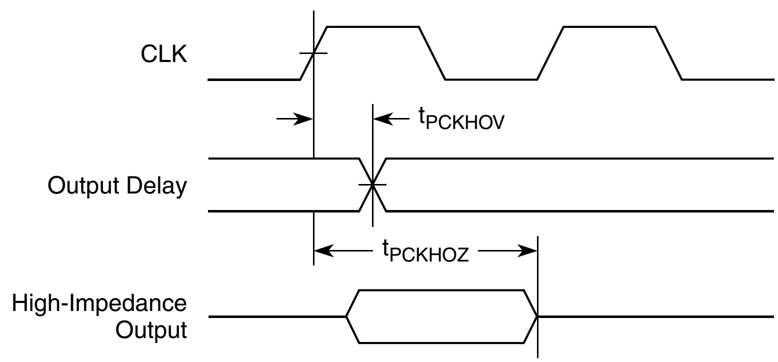


Figure 39. PCI Output AC Timing Measurement Condition

16 High-Speed Serial Interfaces (HSSI)

The MPC8533E features two serializer/deserializer (SerDes) interfaces to be used for high-speed serial interconnect applications.Both SerDes1 and SerDes2 can be used for PCI Express data transfers application.This section describes the common portion of SerDes DC electrical specifications, which is the DC requirement for SerDes Reference Clocks. The SerDes data lane's transmitter and receiver reference circuits are also shown.

16.1 Signal Terms Definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals.

Figure 40 shows how the signals are defined. For illustration purpose, only one SerDes lane is used for description. The figure shows waveform for either a transmitter output (SD*n*_TX and $\overline{\text{SD}n\text{\_TX}}$) or a receiver input (SD*n*_RX and $\overline{\text{SD}n\text{\_RX}}$). Each signal swings between A Volts and B Volts where A > B.

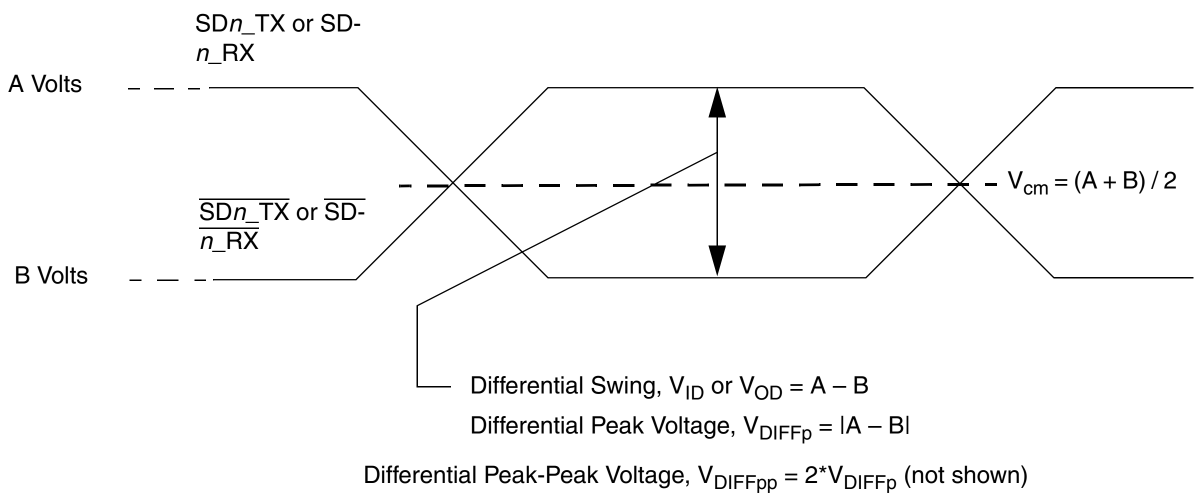


Figure 40. Differential Voltage Definitions for Transmitter or Receiver

To illustrate these definitions using real values, consider the case of a CML (Current Mode Logic) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and $\overline{\text{TD}}$, has a swing that goes between 2.5 V and 2.0 V. Using these values, the peak-to-peak voltage swing of each signal (TD or $\overline{\text{TD}}$) is 500 mV p-p, which is referred as the single-ended swing for each signal. In this example, since the differential signaling environment is fully symmetrical, the transmitter output's differential swing (V_{OD}) has the same amplitude as each signal's single-ended swing. The differential output signal ranges between 500 mV and –500 mV, in other words, V_{OD} is 500 mV in one phase and –500 mV in the other phase. The peak differential voltage (V_{DIFFp}) is 500 mV. The peak-to-peak differential voltage ($V_{DIFFp-p}$) is 1000 mV p-p.

16.2 SerDes Reference Clocks

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clocks inputs are SD1_REF_CLK and $\overline{\text{SD1\_REF\_CLK}}$ for PCI Express1 PCI Express2. SD2_REF_CLK and $\overline{\text{SD2\_REF\_CLK}}$ for the PCI Express3. The following sections describe the SerDes reference clock requirements and some application information.

16.2.1 SerDes Reference Clock Receiver Characteristics

Figure 41 shows a receiver reference diagram of the SerDes reference clocks.

- The supply voltage requirements for XV_{DD_SRDS2} are specified in Table 1 and Table 2.
- SerDes reference clock receiver reference circuit structure
  - — The SD*n*_REF_CLK and $\overline{\text{SD}n\text{\_REF\_CLK}}$ are internally AC-coupled differential inputs as shown in Figure 41. Each differential clock input (SD*n*_REF_CLK or $\overline{\text{SD}n\text{\_REF\_CLK}}$) has a 50-Ω termination to SGND_SRDS*n* (xcorevss) followed by on-chip AC-coupling.
  - — The external reference clock driver must be able to drive this termination.

16.2.4 AC Requirements for SerDes Reference Clocks

The clock driver selected should provide a high quality reference clock with low phase noise and cycle-to-cycle jitter. Phase noise less than 100 kHz can be tracked by the PLL and data recovery loops and is less of a problem. Phase noise above 15 MHz is filtered by the PLL. The most problematic phase noise occurs in the 1–15 MHz range. The source impedance of the clock driver should be 50 Ω to match the transmission line and reduce reflections which are a source of noise to the system.

Table 52 describes some AC parameters common to SGMII, and PCI Express protocols.

Table 52. SerDes Reference Clock Common AC Parameters

Parameter	Symbol	Min	Max	Unit	Notes
Rising Edge Rate	Rise Edge Rate	1.0	4.0	V/ns	2, 3
Falling Edge Rate	Fall Edge Rate	1.0	4.0	V/ns	2, 3
Differential Input High Voltage	V_{IH}	+200	—	mV	2
Differential Input Low Voltage	V_{IL}	—	–200	mV	2
Rising edge rate (SD*n*_REF_CLK) to falling edge rate ($\overline{\text{SD}n\text{\_REF\_CLK}}$) matching	Rise-Fall Matching	—	20	%	1, 4

Notes:
1. Measurement taken from single ended waveform.
2. Measurement taken from differential waveform.
3. Measured from –200 mV to +200 mV on the differential waveform (derived from SD*n*_REF_CLK minus $\overline{\text{SD}n\text{\_REF\_CLK}}$). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing. See Figure 49.
4. Matching applies to rising edge rate for SD*n*_REF_CLK and falling edge rate for $\overline{\text{SD}n\text{\_REF\_CLK}}$. It is measured using a 200 mV window centered on the median cross point where SD*n*_REF_CLK rising meets $\overline{\text{SD}n\text{\_REF\_CLK}}$ falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The rise edge rate of SD*n*_REF_CLK should be compared to the fall edge rate of $\overline{\text{SD}n\text{\_REF\_CLK}}$, the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 50.

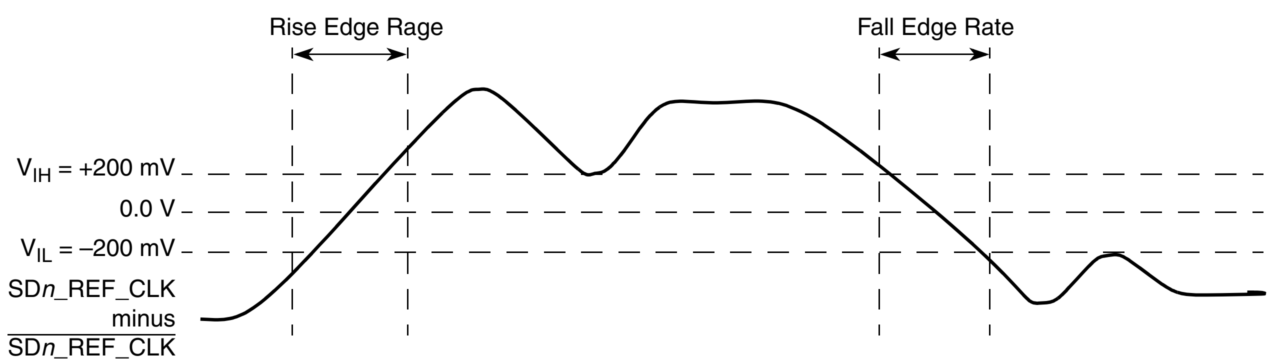


Figure 49. Differential Measurement Points for Rise and Fall Time

Table 54. Differential Transmitter (TX) Output Specifications (continued)

Symbol	Parameter	Min	Nom	Max	Unit	Comments
$V_{TX\text{-}RCV\text{-}DETECT}$	Amount of voltage change allowed during receiver detection	—	—	600	mV	The total amount of voltage change that a transmitter can apply to sense whether a low impedance receiver is present. See Note 6.
$V_{TX\text{-}DC\text{-}CM}$	TX DC common mode voltage	0	—	3.6	V	The allowed DC common mode voltage under any conditions. See Note 6.
$I_{TX\text{-}SHORT}$	TX short circuit current limit	—	—	90	mA	The total current the transmitter can provide when shorted to its ground.
$T_{TX\text{-}IDLE\text{-}MIN}$	Minimum time spent in electrical idle	50	—	—	UI	Minimum time a transmitter must be in electrical idle utilized by the receiver to start looking for an electrical idle exit after successfully receiving an electrical idle ordered set.
$T_{TX\text{-}IDLE\text{-}SET\text{-}TO\text{-}IDLE}$	Maximum time to transition to a valid electrical idle after sending an electrical Idle ordered set	—	—	20	UI	After sending an electrical idle ordered set, the transmitter must meet all electrical idle specifications within this time. This is considered a debounce time for the transmitter to meet electrical idle after transitioning from LO.
$T_{TX\text{-}IDLE\text{-}TO\text{-}DIFF\text{-}DATA}$	Maximum time to transition to valid TX specifications after leaving an electrical idle condition	—	—	20	UI	Maximum time to meet all TX specifications when transitioning from electrical idle to sending differential data. This is considered a debounce time for the TX to meet all TX specifications after leaving electrical idle.
$RL_{TX\text{-}DIFF}$	Differential return loss	12	—	—	dB	Measured over 50 MHz to 1.25 GHz. See Note 4.
$RL_{TX\text{-}CM}$	Common mode return loss	6	—	—	dB	Measured over 50 MHz to 1.25 GHz. See Note 4.
$Z_{TX\text{-}DIFF\text{-}DC}$	DC differential TX impedance	80	100	120	Ω	TX DC differential mode low impedance.
$Z_{TX\text{-}DC}$	Transmitter DC impedance	40	—	—	Ω	Required TX D+ as well as D– DC Impedance during all states.
$L_{TX\text{-}SKEW}$	Lane-to-lane output skew	—	—	500 + 2 UI	ps	Static skew between any two transmitter lanes within a single link.
C_{TX}	AC coupling capacitor	75	—	200	nF	All transmitters shall be AC coupled. The AC coupling is required either within the media or within the transmitting component itself.

Table 54. Differential Transmitter (TX) Output Specifications (continued)

Symbol	Parameter	Min	Nom	Max	Unit	Comments
$T_{crosslink}$	Crosslink random timeout	0	—	1	ms	This random timeout helps resolve conflicts in crosslink configuration by eventually resulting in only one downstream and one upstream port. See Note 7.

Notes:
1. No test load is necessarily associated with this value.
2. Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 54 and measured over any 250 consecutive TX UIs. (Also refer to the transmitter compliance eye diagram shown in Figure 52.)
3. A $T_{TX\text{-}EYE}$ = 0.70 UI provides for a total sum of deterministic and random jitter budget of $T_{TX\text{-}JITTER\text{-}MAX}$ = 0.30 UI for the transmitter collected over any 250 consecutive TX UIs. The $T_{TX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$ median is less than half of the total TX jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.
4. The transmitter input impedance shall result in a differential return loss greater than or equal to 12 dB and a common mode return loss greater than or equal to 6 dB over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements is 50 Ω to ground for both the D+ and D– line (that is, as measured by a vector network analyzer with 50-Ω probes—see Figure 54.) Note that the series capacitors C_{TX} is optional for the return loss measurement.
5. Measured between 20%–80% at transmitter package pins into a test load as shown in Figure 54 for both $V_{TX\text{-}D+}$ and $V_{TX\text{-}D-}$.
6. See Section 4.3.1.8 of the *PCI Express Base Specifications, Rev 1.0a.*
7. See Section 4.2.6.3 of the *PCI Express Base Specifications, Rev 1.0a.*

17.4.2 Transmitter Compliance Eye Diagrams

The TX eye diagram in Figure 52 is specified using the passive compliance/test measurement load (see Figure 54) in place of any real PCI Express interconnect +RX component.

There are two eye diagrams that must be met for the transmitter. Both eye diagrams must be aligned in time using the jitter median to locate the center of the eye diagram. The different eye diagrams will differ in voltage depending whether it is a transition bit or a de-emphasized bit. The exact reduced voltage level of the de-emphasized bit will always be relative to the transition bit.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

NOTE

It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function (that is, least squares and median deviation fits).

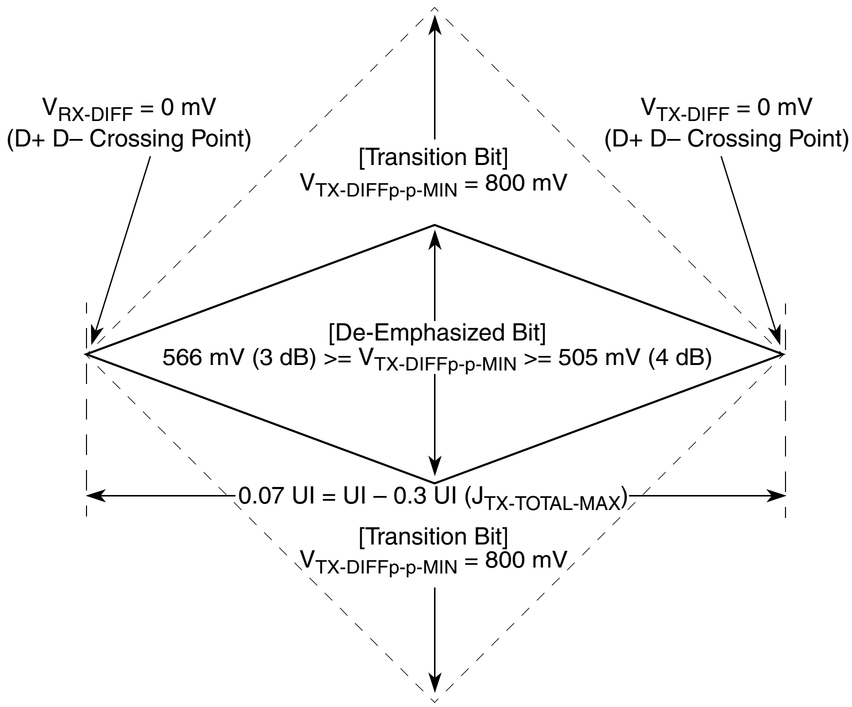


Figure 52. Minimum Transmitter Timing and Voltage Output Compliance Specifications

17.4.3 Differential Receiver (RX) Input Specifications

Table 55 defines the specifications for the differential input at all receivers. The parameters are specified at the component pins.

Table 55. Differential Receiver (RX) Input Specifications

Symbol	Parameter	Min	Nom	Max	Units	Comments
UI	Unit interval	399.88	400	400.12	ps	Each UI is 400 ps ± 300 ppm. UI does not account for spread spectrum clock dictated variations. See Note 1.
$V_{RX\text{-}DIFFp\text{-}p}$	Differential peak-to-peak input voltage	0.175	—	1.200	V	$V_{RX\text{-}DIFFp\text{-}p} = 2 \times \lvert V_{RX\text{-}D+} - V_{RX\text{-}D-}\rvert$ See Note 2.
$T_{RX\text{-}EYE}$	Minimum receiver eye width	0.4	—	—	UI	The maximum interconnect media and transmitter jitter that can be tolerated by the receiver can be derived as $T_{RX\text{-}MAX\text{-}JITTER} = 1 - T_{RX\text{-}EYE} = 0.6$ UI. See Notes 2 and 3.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

NOTE

The reference impedance for return loss measurements is 50 Ω to ground for both the D+ and D– line (that is, as measured by a vector network analyzer with 50-Ω probes, see Figure 53). Note that the series capacitors, CTX, are optional for the return loss measurement.

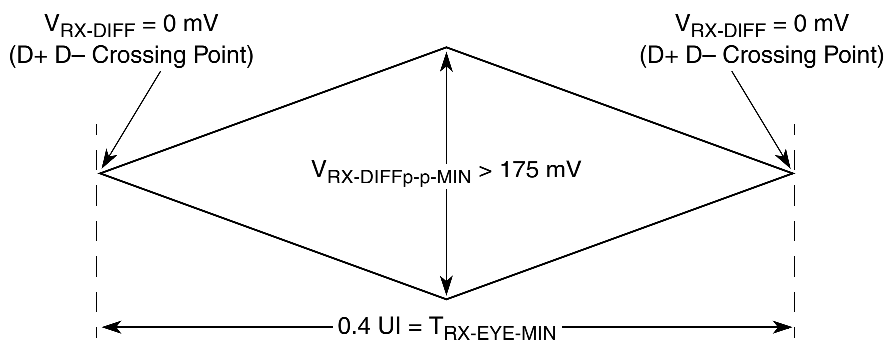


Figure 53. Minimum Receiver Eye Timing and Voltage Compliance Specification

17.5.1 Compliance Test and Measurement Load

The AC timing and voltage parameters must be verified at the measurement point, as specified within 0.2 inches of the package pins, into a test/measurement load shown in Figure 54.

NOTE

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D– not being exactly matched in length at the package pin boundary.

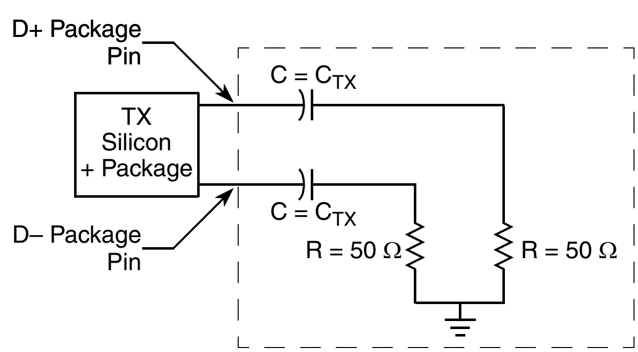
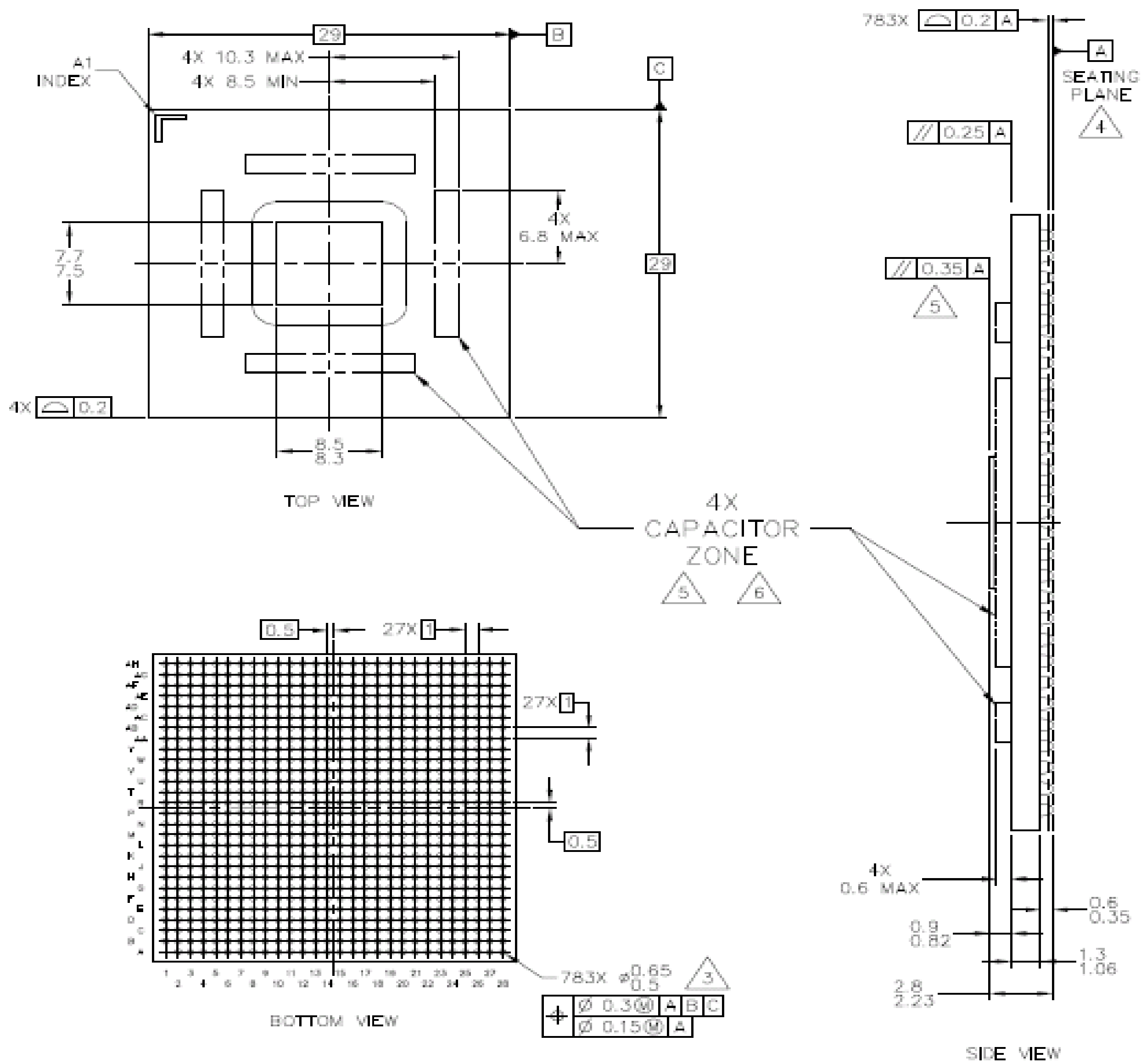


Figure 54. Compliance Test/Measurement Load

18.2 Mechanical Dimensions of the MPC8533E FC-PBGA

Figure 55 shows the mechanical dimensions and bottom surface nomenclature of the MPC8533E, 783 FC-PBGA package without a lid.



Notes:
1. All dimensions are in millimeters.
2. Dimensions and tolerances per ASME Y14.5M-1994.
3. Maximum solder ball diameter measured parallel to datum A.
4. Datum A, the seating plane, is determined by the spherical crowns of the solder balls.
5. Parallelism measurement shall exclude any effect of mark on top surface of package.
6. Capacitors may not be present on all parts. Care must be taken not to short exposed metal capacitor pads.
7. All dimensions are symmetric across the package center lines, unless dimensioned otherwise.

Figure 55. Mechanical Dimensions and Bottom Surface Nomenclature of the MPC8533E FC-PBGA without a Lid

18.3 Pinout Listings

Table 57 provides the pinout listing for the MPC8533E 783 FC-PBGA package.

NOTE

The naming convention of TSEC1 and TSEC3 is used to allow the splitting voltage rails for the eTSEC blocks and to ease the port of existing PowerQUICC III software.

NOTE

The DMA_DACK[0:1] and TEST_SEL pins must be set to a proper state during POR configuration. Please refer to Table 57 for more details.

Table 57. MPC8533E Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Notes
		PCI		
PCI1_AD[31:0]	AE8, AD8, AF8, AH12, AG12, AB9, AC9, AE9, AD10, AE10, AC11, AB11, AB12, AC12, AF12, AE11, Y14, AE15, AC15, AB15, AA15, AD16, Y15, AB16, AF18, AE18, AC17, AE19, AD19, AB17, AB18, AA16	I/O	OV_{DD}	—
PCI1_C_BE[3:0]	AC10, AE12, AA14, AD17	I/O	OV_{DD}	—
PCI1_GNT[4:1]	AE7, AG11,AH11, AC8	O	OV_{DD}	4, 8, 24
PCI1_GNT0	AE6	I/O	OV_{DD}	—
PCI1_IRDY	AF13	I/O	OV_{DD}	2
PCI1_PAR	AB14	I/O	OV_{DD}	—
PCI1_PERR	AE14	I/O	OV_{DD}	2
PCI1_SERR	AC14	I/O	OV_{DD}	2
PCI1_STOP	AA13	I/O	OV_{DD}	2
PCI1_TRDY	AD13	I/O	OV_{DD}	2
PCI1_REQ[4:1]	AF9, AG10, AH10, AD6	I	OV_{DD}	—
PCI1_REQ0	AB8	I/O	OV_{DD}	—
PCI1_CLK	AH26	I	OV_{DD}	—
PCI1_DEVSEL	AC13	I/O	OV_{DD}	2
PCI1_FRAME	AD12	I/O	OV_{DD}	2
PCI1_IDSEL	AG6	I	OV_{DD}	—

Table 57. MPC8533E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
UART_SIN[0:1]	AG7, AH6	I	OV_{DD}	—
UART_SOUT[0:1]	AH7, AF7	O	OV_{DD}	—
I^{2}C interface				
IIC1_SCL	AG21	I/O	OV_{DD}	20
IIC1_SDA	AH21	I/O	OV_{DD}	20
IIC2_SCL	AG13	I/O	OV_{DD}	20
IIC2_SDA	AG14	I/O	OV_{DD}	20
SerDes 1				
SD1_RX[0:7]	N28, P26, R28, T26, Y26, AA28, AB26, AC28	I	XV_{DD}	—
$\overline{\text{SD1\_RX}}$[0:7]	N27, P25, R27, T25, Y25, AA27, AB25, AC27	I	XV_{DD}	—
SD1_TX[0:7]	M23, N21, P23, R21, U21, V23, W21, Y23	O	XV_{DD}	—
$\overline{\text{SD1\_TX}}$[0:7]	M22, N20, P22, R20, U20, V22, W20, Y22	O	XV_{DD}	—
SD1_PLL_TPD	V28	O	XV_{DD}	17
SD1_REF_CLK	U28	I	XV_{DD}	—
$\overline{\text{SD1\_REF\_CLK}}$	U27	I	XV_{DD}	—
SD1_TST_CLK	T22		—	—
$\overline{\text{SD1\_TST\_CLK}}$	T23		—	—
SerDes 2				
SD2_RX[0]	AD25	I	XV_{DD}	—
SD2_RX[2]	AD1	I	XV_{DD}	26
SD2_RX[3]	AB2	I	XV_{DD}	26
$\overline{\text{SD2\_RX}}$[0]	AD26	I	XV_{DD}	—
$\overline{\text{SD2\_RX}}$[2]	AC1	I	XV_{DD}	26
$\overline{\text{SD2\_RX}}$[3]	AA2	I	XV_{DD}	26
SD2_TX[0]	AA21	O	XV_{DD}	—
SD2_TX[2]	AC4	O	XV_{DD}	17
SD2_TX[3]	AA5	O	XV_{DD}	17
$\overline{\text{SD2\_TX}}$[0]	AA20	O	XV_{DD}	—
$\overline{\text{SD2\_TX}}$[2]	AB4	O	XV_{DD}	17
$\overline{\text{SD2\_TX}}$[3]	Y5	O	XV_{DD}	17
SD2_PLL_TPD	AG3	O	XV_{DD}	17
SD2_REF_CLK	AE2	I	XV_{DD}	—

International Electronic Research Corporation (IERC)818-842-7277
413 North Moss St.
Burbank, CA 91502
Internet: www.ctscorp.com

Millennium Electronics (MEI)408-436-8770
Loroco Sites
671 East Brokaw Road
San Jose, CA 95112
Internet: www.mei-thermal.com

Tyco Electronics800-522-6752
Chip Coolers™
P.O. Box 3668
Harrisburg, PA 17105-3668
Internet: www.chipcoolers.com

Wakefield Engineering603-635-2800
33 Bridge St.
Pelham, NH 03076
Internet: www.wakefield.com

Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost. Several heat sinks offered by Aavid Thermalloy, Advanced Thermal Solutions, Alpha Novatech, IERC, Chip Coolers, Millennium Electronics, and Wakefield Engineering offer different heat sink-to-ambient thermal resistances, that will allow the MPC8533E to function in various environments.

20.3.1 Internal Package Conduction Resistance

For the packaging technology, shown in Table 65, the intrinsic internal conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance
- The die junction-to-board thermal resistance

Heat sinks are attached to the package by means of a spring clip to holes in the printed-circuit board (see Figure 57). Therefore, the synthetic grease offers the best thermal performance, especially at the low interface pressure.

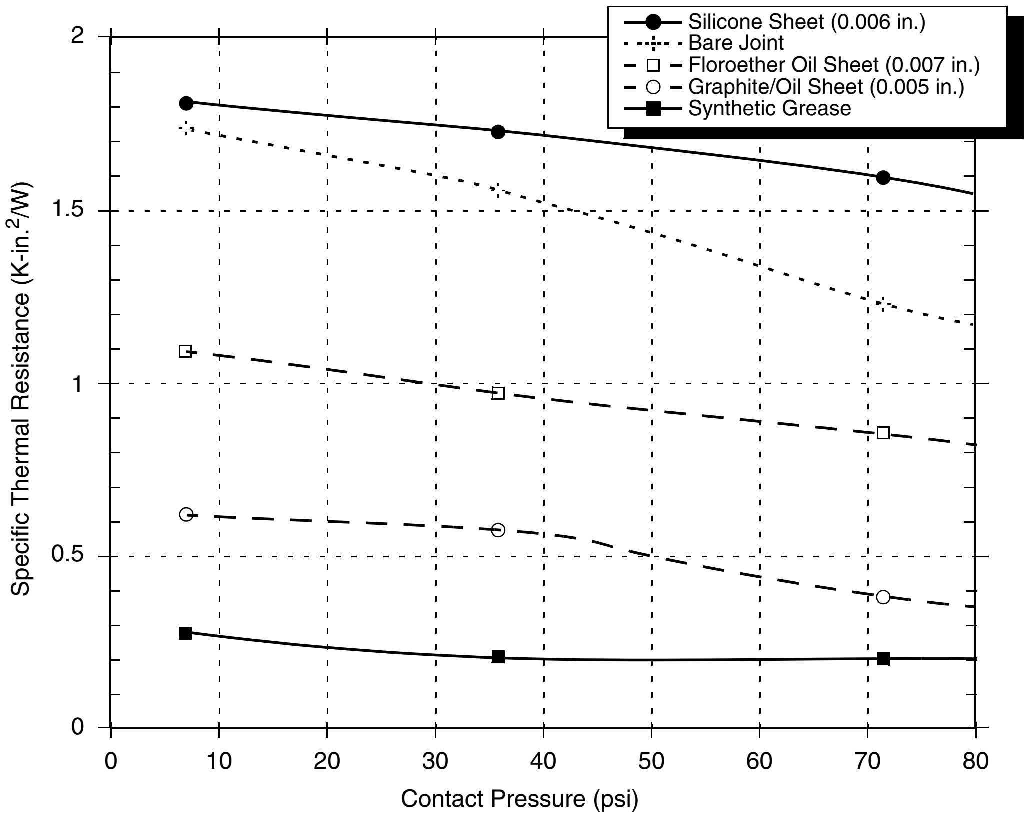


Figure 59. Thermal Performance of Select Thermal Interface Materials

The system board designer can choose between several types of thermal interface. There are several commercially-available thermal interfaces provided by the following vendors:

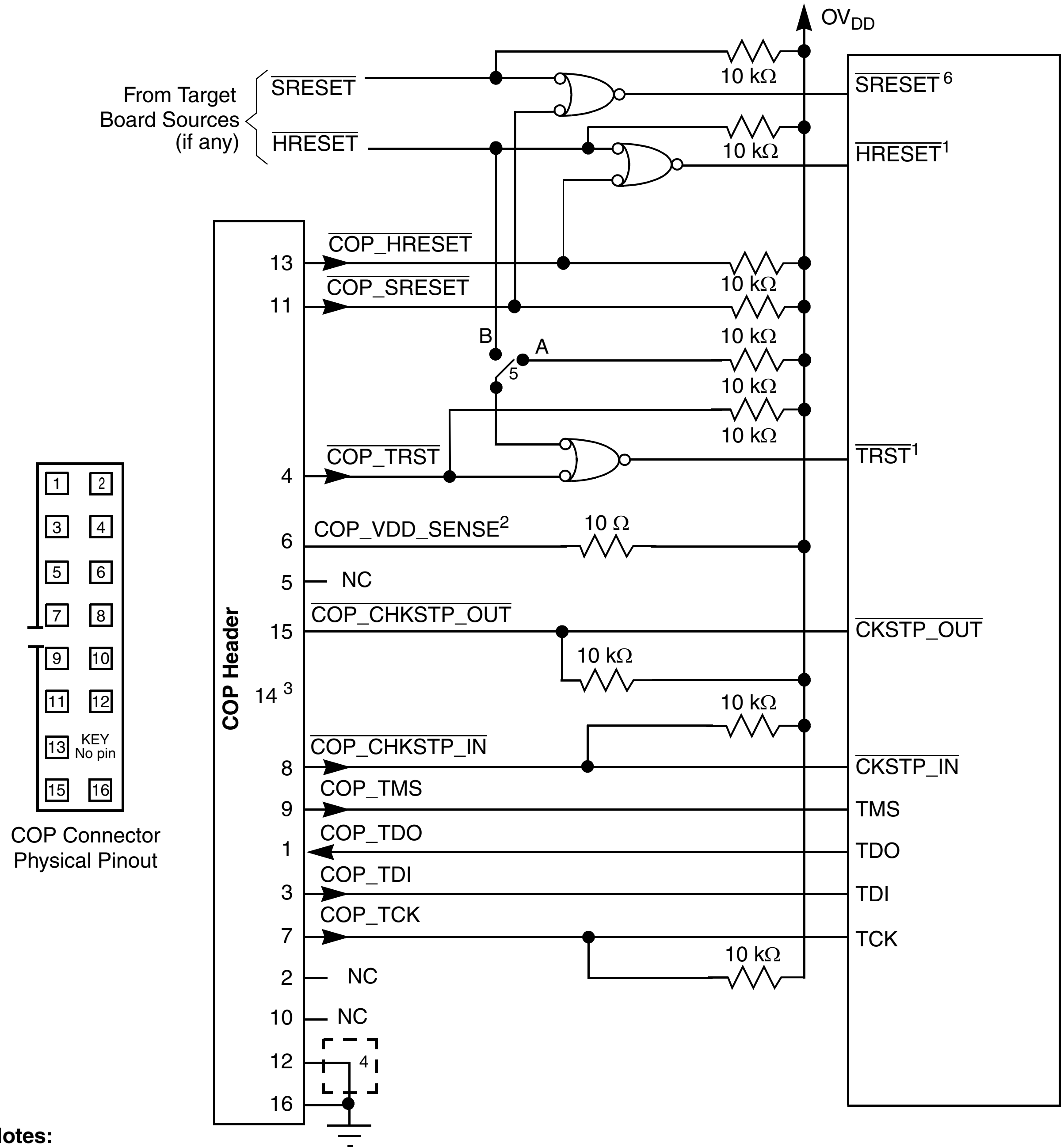
Chomerics, Inc. 781-935-4850
77 Dragon Ct.
Woburn, MA 01801
Internet: www.chomerics.com

Dow-Corning Corporation800-248-2481
Corporate Center
P.O.Box 999
Midland, MI 48686-0997
Internet: www.dow.com

Shin-Etsu MicroSi, Inc.888-642-7674
10028 S. 51st St.
Phoenix, AZ 85044
Internet: www.microsi.com

The Bergquist Company800-347-4572
18930 West 78th St.

Figure 65 shows the JTAG interface connection.



Notes:

1. The COP port and target board should be able to independently assert HRESET and TRST to the processor in order to fully control the processor as shown here.
2. Populate this with a 10-Ω resistor for short-circuit/current-limiting protection.
3. The KEY location (pin 14) is not physically present on the COP header.
4. Although pin 12 is defined as a No Connect, some debug tools may use pin 12 as an additional GND pin for improved signal integrity.
5. This switch is included as a precaution for BSDL testing. The switch should be closed to position A during BSDL testing to avoid accidentally asserting the TRST line. If BSDL testing is not being performed, this switch should be closed to position B.
6. Asserting SRESET causes a machine check interrupt to the e500 core.

Figure 65. JTAG Interface Connection