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Understanding <u>Embedded - Microprocessors</u>

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of <u>Embedded - Microprocessors</u>

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Active
Core Processor	PowerPC e500v2
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	-
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	-
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 90°C (TA)
Security Features	-
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8533vtaqga

- — Double-precision floating-point APU. Provides an instruction set for double-precision (64-bit) floating-point instructions that use the 64-bit GPRs.
- — 36-bit real addressing
- — Embedded vector and scalar single-precision floating-point APUs. Provide an instruction set for single-precision (32-bit) floating-point instructions.
- — Memory management unit (MMU). Especially designed for embedded applications. Supports 4-Kbyte–4-Gbyte page sizes.
- — Enhanced hardware and software debug support
- — Performance monitor facility that is similar to, but separate from, the device performance monitor

The e500 defines features that are not implemented on this device. It also generally defines some features that this device implements more specifically. An understanding of these differences can be critical to ensure proper operations.

- 256-Kbyte L2 cache/SRAM
  - — Flexible configuration
  - — Full ECC support on 64-bit boundary in both cache and SRAM modes
  - — Cache mode supports instruction caching, data caching, or both.
  - — External masters can force data to be allocated into the cache through programmed memory ranges or special transaction types (stashing).
    - – 1, 2, or 4 ways can be configured for stashing only.
  - — Eight-way set-associative cache organization (32-byte cache lines)
  - — Supports locking entire cache or selected lines. Individual line locks are set and cleared through Book E instructions or by externally mastered transactions.
  - — Global locking and flash clearing done through writes to L2 configuration registers
  - — Instruction and data locks can be flash cleared separately.
  - — SRAM features include the following:
    - – I/O devices access SRAM regions by marking transactions as snoopable (global).
    - – Regions can reside at any aligned location in the memory map.
    - – Byte-accessible ECC is protected using read-modify-write transaction accesses for smaller-than-cache-line accesses.
- Address translation and mapping unit (ATMU)
  - — Eight local access windows define mapping within local 36-bit address space.
  - — Inbound and outbound ATMUs map to larger external address spaces.
    - – Three inbound windows plus a configuration window on PCI and PCI Express
    - – Four outbound windows plus default translation for PCI and PCI Express
- DDR/DDR2 memory controller
  - — Programmable timing supporting DDR and DDR2 SDRAM
  - — 64-bit data interface

MPC8533E PowerQUICC III Integrated Processor Hardware Specifications, Rev. 8

- Three PCI Express interfaces
  - Two ×4 link width interfaces and one ×1 link width interface
  - PCI Express 1.0a compatible
  - Auto-detection of number of connected lanes
  - Selectable operation as root complex or endpoint
  - Both 32- and 64-bit addressing
  - 256-byte maximum payload size
  - Virtual channel 0 only
  - Traffic class 0 only
  - Full 64-bit decode with 32-bit wide windows
- Power management
  - Supports power saving modes: doze, nap, and sleep
  - Employs dynamic power management, which automatically minimizes power consumption of blocks when they are idle
- System performance monitor
  - Supports eight 32-bit counters that count the occurrence of selected events
  - Ability to count up to 512 counter-specific events
  - Supports 64 reference events that can be counted on any of the 8 counters
  - Supports duration and quantity threshold counting
  - Burstiness feature that permits counting of burst events with a programmable time between bursts
  - Triggering and chaining capability
  - Ability to generate an interrupt on overflow
- System access port
  - Uses JTAG interface and a TAP controller to access entire system memory map
  - Supports 32-bit accesses to configuration registers
  - Supports cache-line burst accesses to main memory
  - Supports large block (4-Kbyte) uploads and downloads
  - Supports continuous bit streaming of entire block for fast upload and download
- IEEE Std 1149.1™-compliant, JTAG boundary scan
- 783 FC-PBGA package

4.2 Real-Time Clock Timing

The RTC input is sampled by the platform clock (CCB clock). The output of the sampling latch is then used as an input to the counters of the PIC and the TimeBase unit of the e500. There is no jitter specification. The minimum pulse width of the RTC signal should be greater than 2 × the period of the CCB clock. That is, minimum clock high time is $2 \times t_{CCB}$, and minimum clock low time is $2 \times t_{CCB}$. There is no minimum RTC frequency; RTC may be grounded if not needed.

4.3 eTSEC Gigabit Reference Clock Timing

Table 7 provides the eTSEC gigabit reference clocks (EC_GTX_CLK125) AC timing specifications for the MPC8533E.

Table 7. EC_GTX_CLK125 AC Timing Specifications

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Notes
EC_GTX_CLK125 frequency	f_{G125}	—	125	—	MHz	—
EC_GTX_CLK125 cycle time	t_{G125}	—	8	—	ns	—
EC_GTX_CLK rise and fall time LV_{DD}, TV_{DD} = 2.5 V LV_{DD}, TV_{DD} = 3.3 V	t_{G125R}/t_{G125F}	—	—	0.75 1.0	ns	1
EC_GTX_CLK125 duty cycle GMII, TBI 1000Base-T for RGMII, RTBI	t_{G125H}/t_{G125}	45 47	—	55 53	%	2

Notes:
1. Rise and fall times for EC_GTX_CLK125 are measured from 0.5 and 2.0 V for L/TV_{DD} = 2.5 V, and from 0.6 and 2.7 V for L/TVDD = 3.3 V.
2. EC_GTX_CLK125 is used to generate the GTX clock for the eTSEC transmitter with 2% degradation. EC_GTX_CLK125 duty cycle can be loosened from 47%/53% as long as the PHY device can tolerate the duty cycle generated by the eTSEC GTX_CLK. See Section 8.5.4, "RGMII and RTBI AC Timing Specifications," for duty cycle for 10Base-T and 100Base-T reference clock.

4.4 Platform to FIFO Restrictions

Please note the following FIFO maximum speed restrictions based on platform speed.

For FIFO GMII mode:

FIFO TX/RX clock frequency ≤ platform clock frequency ÷ 4.2

For example, if the platform frequency is 533 MHz, the FIFO Tx/Rx clock frequency should be no more than 127 MHz.

For FIFO encoded mode:

FIFO TX/RX clock frequency ≤ platform clock frequency ÷ 3.2

For example, if the platform frequency is 533 MHz, the FIFO Tx/Rx clock frequency should be no more than 167 MHz.

Table 12. DDR SDRAM DC Electrical Characteristics for GV$_{DD}$(typ) = 2.5 V (continued)

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Output low current (V$_{OUT}$ = 0.42 V)	I$_{OL}$	16.2	—	mA	—

Notes:

1. GV$_{DD}$ is expected to be within 50 mV of the DRAM GV$_{DD}$ at all times.

2. MV$_{REF}$ is expected to be equal to 0.5 × GV$_{DD}$, and to track GV$_{DD}$ DC variations as measured at the receiver. Peak-to-peak noise on MV$_{REF}$ may not exceed ±2% of the DC value.

3. V$_{TT}$ is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV$_{REF}$. This rail should track variations in the DC level of MV$_{REF}$.

Table 13 provides the DDR I/O capacitance when GV$_{DD}$(typ) = 2.5 V.

Table 13. DDR SDRAM Capacitance for GV$_{DD}$(typ) = 2.5 V

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/output capacitance: DQ, DQS	C$_{IO}$	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C$_{DIO}$	—	0.5	pF	1

Note:

1. This parameter is sampled. GV$_{DD}$ = 2.5 V ± 0.125 V, f = 1 MHz, T$_A$ = 25°C, V$_{OUT}$ = GV$_{DD}$/2, V$_{OUT}$ (peak-to-peak) = 0.2 V.

Table 14 provides the current draw characteristics for MV$_{REF}$.

Table 14. Current Draw Characteristics for MV$_{REF}$

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Current draw for MV$_{REF}$	I$_{MVREF}$	—	500	μA	1

Note:

1. The voltage regulator for MV$_{REF}$ must be able to supply up to 500 μA current.

6.2 DDR SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR SDRAM interface.

6.2.1 DDR SDRAM Input AC Timing Specifications

Table 15 provides the input AC timing specifications for the DDR SDRAM when GV$_{DD}$(typ) = 1.8 V.

Table 15. DDR2 SDRAM Input AC Timing Specifications for 1.8-V Interface

At recommended operating conditions.

Parameter	Symbol	Min	Max	Unit	Notes
AC input low voltage	V$_{IL}$	—	MV$_{REF}$ – 0.25	V	—
AC input high voltage	V$_{IH}$	MV$_{REF}$ + 0.25	—	V	—

8.2   eTSEC DC Electrical Characteristics

All GMII, MII, TBI, RGMII, RTBI, RMII, and FIFO drivers and receivers comply with the DC parametric attributes specified in Table 21 and Table 22. The potential applied to the input of a GMII, MII, TBI, RTBI, RMII, and FIFO receiver may exceed the potential of the receiver's power supply (that is, a GMII driver powered from a 3.6-V supply driving V_{OH} into a GMII receiver powered from a 2.5-V supply). Tolerance for dissimilar GMII driver and receiver supply potentials is implicit in these specifications. The RGMII and RTBI signals are based on a 2.5-V CMOS interface voltage as defined by JEDEC EIA/JESD8-5.

Table 21. GMII, MII, TBI, RMII and FIFO DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit	Notes
Supply voltage 3.3 V	LV_{DD} TV_{DD}	3.135	3.465	V	1, 2
Output high voltage (LV_{DD}/TV_{DD} = Min, I_{OH} = −4.0 mA)	V_{OH}	2.4	—	V	—
Output low voltage (LV_{DD}/TV_{DD} = Min, I_{OL} = 4.0 mA)	V_{OL}	—	0.5	V	—
Input high voltage	V_{IH}	1.95	—	V	—
Input low voltage	V_{IL}	—	0.90	V	—
Input high current (V_{IN} = LV_{DD}, V_{IN} = TV_{DD})	I_{IH}	—	40	µA	1, 2, 3
Input low current (V_{IN} = GND)	I_{IL}	−600	—	µA	3

Notes:
1. LV_{DD} supports eTSEC1.
2. TV_{DD} supports eTSEC3.
3. The symbol V_{IN}, in this case, represents the LV_{IN} and TV_{IN} symbols referenced in Table 1 and Table 2.

Table 22. GMII, MII, RMII, RGMII, RTBI, TBI, and FIFO DC Electrical Characteristics

Parameters	Symbol	Min	Max	Unit	Notes
Supply voltage 2.5 V	LV_{DD}/TV_{DD}	2.375	2.625	V	1, 2
Output high voltage (LV_{DD}/TV_{DD} = Min, I_{OH} = −1.0 mA)	V_{OH}	2.0	—	V	—
Output low voltage (LV_{DD}/TV_{DD} = Min, I_{OL} = 1.0 mA)	V_{OL}	—	0.4	V	—
Input high voltage	V_{IH}	1.70	—	V	—
Input low voltage	V_{IL}	—	0.7	V	—
Input current (V_{IN} = 0, V_{IN} = LV_{DD}, V_{IN} = TV_{DD})	I_{IN}	—	±15	µA	1, 2, 3

Notes:
1. LV_{DD} supports eTSEC1.
2. TV_{DD} supports eTSEC3.
3. The symbol V_{IN}, in this case, represents the LV_{IN} and TV_{IN} symbols referenced in Table 1 and Table 2.

8.5.5 RMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.

8.5.5.1 RMII Transmit AC Timing Specifications

The RMII transmit AC timing specifications are in Table 33.

Table 33. RMII Transmit AC Timing Specifications

At recommended operating conditions with L/TV$_{DD}$ of 3.3 V ± 5% or 2.5 V ± 5%.

Parameter/Condition	Symbol[1]	Min	Typ	Max	Unit	Notes
REF_CLK clock period	t$_{RMT}$	15.0	20.0	25.0	ns	—
REF_CLK duty cycle	t$_{RMTH}$	35	50	65	%	—
REF_CLK peak-to-peak jitter	t$_{RMTJ}$	—	—	250	ps	—
Rise time REF_CLK (20%–80%)	t$_{RMTR}$	1.0	—	2.0	ns	—
Fall time REF_CLK (80%–20%)	t$_{RMTF}$	1.0	—	2.0	ns	—
REF_CLK to RMII data TXD[1:0], TX_EN delay	t$_{RMTDX}$	1.0	—	10.0	ns	—

Note:

1. The symbols used for timing specifications follow the pattern of t$_{(first two letters of functional block)(signal)(state)(reference)(state)}$ for inputs and t$_{(first two letters of functional block)(reference)(state)(signal)(state)}$ for outputs. For example, t$_{MTKHDX}$ symbolizes MII transmit timing (MT) for the time t$_{MTX}$ clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t$_{MTX}$ represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
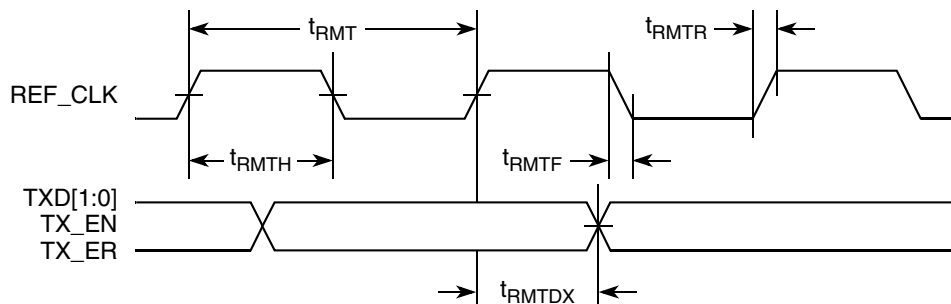
Figure 19 shows the RMII transmit AC timing diagram.

Figure 19. RMII Transmit AC Timing Diagram

Table 40. Local Bus General Timing Parameters (BV$_{DD}$ = 3.3 V)—PLL Enabled (continued)

Parameter	Symbol[1]	Min	Max	Unit	Notes
Local bus clock to output high impedance for LAD/LDP	$t_{LBKHOZ2}$	—	2.5	ns	5

Notes:

1. The symbols used for timing specifications follow the pattern of $t_{(first\ two\ letters\ of\ functional\ block)(signal)(state)(reference)(state)}$ for inputs and $t_{(first\ two\ letters\ of\ functional\ block)(reference)(state)(signal)(state)}$ for outputs. For example, $t_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t_{LBK} clock reference (K) goes high (H), in this case for clock one (1). Also, t_{LBKHOX} symbolizes local bus timing (LB) for the t_{LBK} clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.

2. All timings are in reference to LSYNC_IN for PLL enabled and internal local bus clock for PLL bypass mode.

3. All signals are measured from BV$_{DD}$/2 of the rising edge of LSYNC_IN for PLL enabled or internal local bus clock for PLL bypass mode to $0.4 \times$ BV$_{DD}$ of the signal in question for 3.3-V signaling levels.

4. Input timings are measured at the pin.

5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

6. t_{LBOTOT} is a measurement of the minimum time between the negation of LALE and any change in LAD. t_{LBOTOT} is programmed with the LBCR[AHD] parameter.

7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at BV$_{DD}$/2.

describes the general timing parameters of the local bus interface at BV$_{DD}$ = 2.5 V.

Table 41. Local Bus General Timing Parameters (BV$_{DD}$ = 2.5 V)—PLL Enabled

Parameter	Symbol[1]	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	7.5	12	ns	2
Local bus duty cycle	t_{LBKH}/t_{LBK}	43	57	%	—
LCLK[n] skew to LCLK[m] or LSYNC_OUT	$t_{LBKSKEW}$	—	150	ps	7
Input setup to local bus clock (except LUPWAIT)	$t_{LBIVKH1}$	2.4	—	ns	3, 4
LUPWAIT input setup to local bus clock	$t_{LBIVKH2}$	1.8	—	ns	3, 4
Input hold from local bus clock (except LUPWAIT)	$t_{LBIXKH1}$	1.1	—	ns	3, 4
LUPWAIT input hold from local bus clock	$t_{LBIXKH2}$	1.1	—	ns	3, 4
LALE output transition to LAD/LDP output transition (LATCH setup and hold time)	t_{LBOTOT}	1.5	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	$t_{LBKHOV1}$	—	2.8	ns	—
Local bus clock to data valid for LAD/LDP	$t_{LBKHOV2}$	—	2.8	ns	3
Local bus clock to address valid for LAD	$t_{LBKHOV3}$	—	2.8	ns	3
Local bus clock to LALE assertion	$t_{LBKHOV4}$	—	2.8	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	$t_{LBKHOX1}$	0.8	—	ns	3
Output hold from local bus clock for LAD/LDP	$t_{LBKHOX2}$	0.8	—	ns	3
Local bus clock to output high Impedance (except LAD/LDP and LALE)	$t_{LBKHOZ1}$	—	2.6	ns	5

Table 41. Local Bus General Timing Parameters (BV$_{DD}$ = 2.5 V)—PLL Enabled (continued)

Parameter	Symbol[1]	Min	Max	Unit	Notes
Local bus clock to output high impedance for LAD/LDP	t$_{LBKHOZ2}$	—	2.6	ns	5

Notes:

1. The symbols used for timing specifications follow the pattern of t$_{(first two letters of functional block)(signal)(state)(reference)(state)}$ for inputs and t$_{(First two letters of functional block)(reference)(state)(signal)(state)}$ for outputs. For example, t$_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t$_{LBK}$ clock reference (K) goes high (H), in this case for clock one (1). Also, t$_{LBKHOX}$ symbolizes local bus timing (LB) for the t$_{LBK}$ clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.

2. All timings are in reference to LSYNC_IN for PLL enabled and internal local bus clock for PLL bypass mode.

3. All signals are measured from BV$_{DD}$/2 of the rising edge of LSYNC_IN for PLL enabled or internal local bus clock for PLL bypass mode to 0.4 × BV$_{DD}$ of the signal in question for 2.5-V signaling levels.

4. Input timings are measured at the pin.

5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

6. t$_{LBOTOT}$ is a measurement of the minimum time between the negation of LALE and any change in LAD. t$_{LBOTOT}$ is programmed with the LBCR[AHD] parameter.

7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at BV$_{DD}$/2.

Table 42 describes the general timing parameters of the local bus interface at BV$_{DD}$ = 1.8 V DC.

Table 42. Local Bus General Timing Parameters (BV$_{DD}$ = 1.8 V DC)

Parameter	Symbol[1]	Min	Max	Unit	Notes
Local bus cycle time	t$_{LBK}$	7.5	12	ns	2
Local bus duty cycle	t$_{LBKH}$/t$_{LBK}$	43	57	%	—
LCLK[n] skew to LCLK[m] or LSYNC_OUT	t$_{LBKSKEW}$	—	150	ps	7
Input setup to local bus clock (except LUPWAIT)	t$_{LBIVKH1}$	2.6	—	ns	3, 4
LUPWAIT input setup to local bus clock	t$_{LBIVKH2}$	1.9	—	ns	3, 4
Input hold from local bus clock (except LUPWAIT)	t$_{LBIXKH1}$	1.1	—	ns	3, 4
LUPWAIT input hold from local bus clock	t$_{LBIXKH2}$	1.1	—	ns	3, 4
LALE output transition to LAD/LDP output transition (LATCH setup and hold time)	t$_{LBOTOT}$	1.2	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	t$_{LBKHOV1}$	—	3.2	ns	—
Local bus clock to data valid for LAD/LDP	t$_{LBKHOV2}$	—	3.2	ns	3
Local bus clock to address valid for LAD	t$_{LBKHOV3}$	—	3.2	ns	3
Local bus clock to LALE assertion	t$_{LBKHOV4}$	—	3.2	ns	3
Output hold from local bus clock (except LAD/LDP and LALE)	t$_{LBKHOX1}$	0.9	—	ns	3
Output hold from local bus clock for LAD/LDP	t$_{LBKHOX2}$	0.9	—	ns	3
Local bus clock to output high Impedance (except LAD/LDP and LALE)	t$_{LBKHOZ1}$	—	2.6	ns	5

Table 42. Local Bus General Timing Parameters (BV$_{DD}$ = 1.8 V DC) (continued)

Parameter	Symbol[1]	Min	Max	Unit	Notes
Local bus clock to output high impedance for LAD/LDP	t$_{LBKHOZ2}$	—	2.6	ns	5

Notes:

1. The symbols used for timing specifications follow the pattern of t$_{(first two letters of functional block)(signal)(state)(reference)(state)}$ for inputs and t$_{(first two letters of functional block)(reference)(state)(signal)(state)}$ for outputs. For example, t$_{LBIXKH1}$ symbolizes local bus timing (LB) for the input (I) to go invalid (X) with respect to the time the t$_{LBK}$ clock reference (K) goes high (H), in this case for clock one (1). Also, t$_{LBKHOX}$ symbolizes local bus timing (LB) for the t$_{LBK}$ clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.

2. All timings are in reference to LSYNC_IN for PLL enabled and internal local bus clock for PLL bypass mode.

3. All signals are measured from BV$_{DD}$/2 of the rising edge of LSYNC_IN for PLL enabled or internal local bus clock for PLL bypass mode to 0.4 × BV$_{DD}$ of the signal in question for 1.8-V signaling levels.

4. Input timings are measured at the pin.

5. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

6. t$_{LBOTOT}$ is a measurement of the minimum time between the negation of LALE and any change in LAD. t$_{LBOTOT}$ is programmed with the LBCR[AHD] parameter.

7. Maximum possible clock skew between a clock LCLK[m] and a relative clock LCLK[n]. Skew measured between complementary signals at BV$_{DD}$/2.
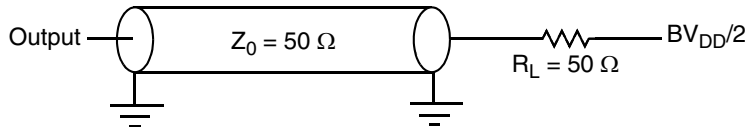
Figure 23 provides the AC test load for the local bus.

Figure 23. Local Bus AC Test Load

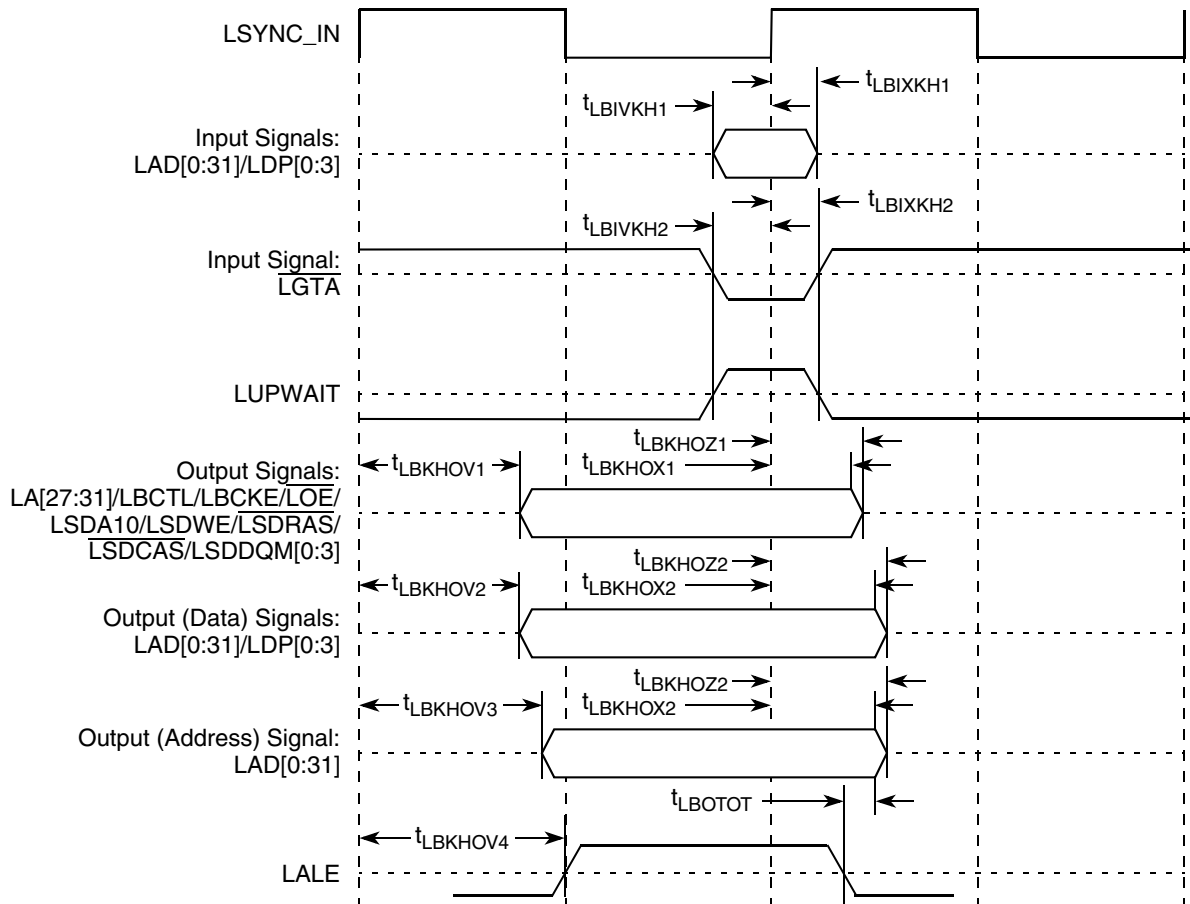Figure 24 through Figure 29 show the local bus signals.

Figure 24. Local Bus Signals (PLL Enabled)

Table 43 describes the general timing parameters of the local bus interface at $V_{DD} = 3.3$ V DC with PLL disabled.

Table 43. Local Bus General Timing Parameters—PLL Bypassed

Parameter	Symbol[1]	Min	Max	Unit	Notes
Local bus cycle time	t_{LBK}	12	—	ns	2
Local bus duty cycle	t_{LBKH}/t_{LBK}	43	57	%	—
Internal launch/capture clock to LCLK delay	t_{LBKHKT}	1.2	4.9	ns	—
Input setup to local bus clock (except LUPWAIT)	$t_{LBIVKH1}$	7.4	—	ns	4, 5
LUPWAIT input setup to local bus clock	$t_{LBIVKL2}$	6.75	—	ns	4, 5
Input hold from local bus clock (except LUPWAIT)	$t_{LBIXKH1}$	−0.2	—	ns	4, 5
LUPWAIT input hold from local bus clock	$t_{LBIXKL2}$	−0.2	—	ns	4, 5
LALE output transition to LAD/LDP output transition (LATCH hold time)	t_{LBOTOT}	1.5	—	ns	6
Local bus clock to output valid (except LAD/LDP and LALE)	$t_{LBKLOV1}$	—	1.6	ns	—

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

NOTE

The reference impedance for return loss measurements is 50 Ω to ground for both the D+ and D– line (that is, as measured by a vector network analyzer with 50-Ω probes, see Figure 53). Note that the series capacitors, CTX, are optional for the return loss measurement.
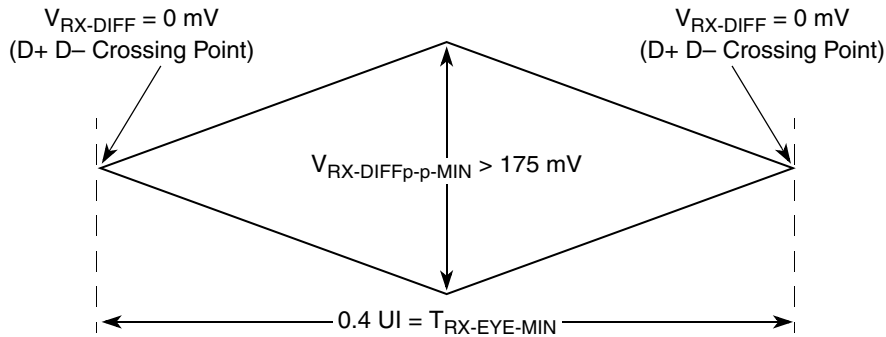

Figure 53. Minimum Receiver Eye Timing and Voltage Compliance Specification

17.5.1 Compliance Test and Measurement Load

The AC timing and voltage parameters must be verified at the measurement point, as specified within 0.2 inches of the package pins, into a test/measurement load shown in Figure 54.

NOTE

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D– not being exactly matched in length at the package pin boundary.
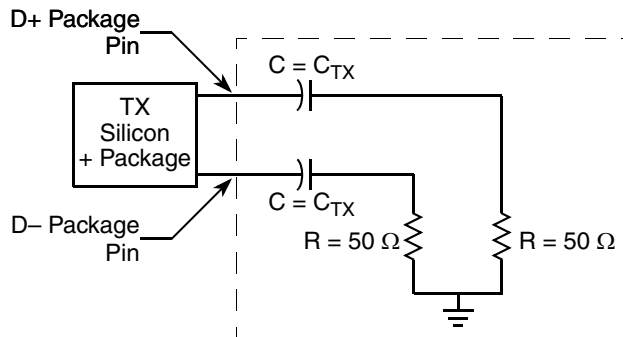

Figure 54. Compliance Test/Measurement Load

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Table 57. MPC8533E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
$\overline{\text{LCS6}}$/DMA_DACK2	J16	O	BV$_{DD}$	1
$\overline{\text{LCS7}}$/DMA_DDONE2	L18	O	BV$_{DD}$	1
$\overline{\text{LWE0}}$/$\overline{\text{LBS0}}$/LSDDQM[0]	J22	O	BV$_{DD}$	4, 8
$\overline{\text{LWE1}}$/$\overline{\text{LBS1}}$/LSDDQM[1]	H22	O	BV$_{DD}$	4, 8
$\overline{\text{LWE2}}$/$\overline{\text{LBS2}}$/LSDDQM[2]	H23	O	BV$_{DD}$	4, 8
$\overline{\text{LWE3}}$/$\overline{\text{LBS3}}$/LSDDQM[3]	H21	O	BV$_{DD}$	4, 8
LALE	J26	O	BV$_{DD}$	4, 7, 8
LBCTL	J25	O	BV$_{DD}$	4, 7, 8
LGPL0/LSDA10	J20	O	BV$_{DD}$	4, 8
LGPL1/$\overline{\text{LSDWE}}$	K20	O	BV$_{DD}$	4, 8
LGPL2/$\overline{\text{LOE}}$/$\overline{\text{LSDRAS}}$	G20	O	BV$_{DD}$	4, 7, 8
LGPL3/$\overline{\text{LSDCAS}}$	H18	O	BV$_{DD}$	4, 8
LGPL4/$\overline{\text{LGTA}}$/LUPWAIT/ LPBSE	L20	I/O	BV$_{DD}$	28
LGPL5	K19	O	BV$_{DD}$	4, 8
LCKE	L17	O	BV$_{DD}$	—
LCLK[0:2]	H24, J24, H25	O	BV$_{DD}$	—
LSYNC_IN	D27	I	BV$_{DD}$	—
LSYNC_OUT	D28	O	BV$_{DD}$	—
DMA				
$\overline{\text{DMA_DACK}}$[0:1]	Y13, Y12	O	OV$_{DD}$	4, 8, 9
$\overline{\text{DMA_DREQ}}$[0:1]	AA10, AA11	I	OV$_{DD}$	—
$\overline{\text{DMA_DDONE}}$[0:1]	AA7, Y11	O	OV$_{DD}$	—
Programmable Interrupt Controller				
$\overline{\text{UDE}}$	AH15	I	OV$_{DD}$	—
$\overline{\text{MCP}}$	AG18	I	OV$_{DD}$	—
IRQ[0:7]	AG22, AF17, AD21, AF19, AG17, AF16, AC23, AC22	I	OV$_{DD}$	—
IRQ[8]	AC19	I	OV$_{DD}$	—
IRQ[9]/$\overline{\text{DMA_DREQ3}}$	AG20	I	OV$_{DD}$	1
IRQ[10]/$\overline{\text{DMA_DACK3}}$	AE27	I/O	OV$_{DD}$	1
IRQ[11]/$\overline{\text{DMA_DDONE3}}$	AE24	I/O	OV$_{DD}$	1
$\overline{\text{IRQ_OUT}}$	AD14	O	OV$_{DD}$	2

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Table 57. MPC8533E Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Notes
Ethernet Management Interface				
EC_MDC	AC7	O	OV$_{DD}$	4, 8, 14
EC_MDIO	Y9	I/O	OV$_{DD}$	—
Gigabit Reference Clock				
EC_GTX_CLK125	T2	I	LV$_{DD}$	—
Three-Speed Ethernet Controller (Gigabit Ethernet 1)				
TSEC1_RXD[7:0]	U10, U9, T10, T9, U8, T8, T7, T6	I	LV$_{DD}$	—
TSEC1_TXD[7:0]	T5, U5, V5, V3, V2, V1, U2, U1	O	LV$_{DD}$	4, 8, 14
TSEC1_COL	R5	I	LV$_{DD}$	—
TSEC1_CRS	T4	I/O	LV$_{DD}$	16
TSEC1_GTX_CLK	T1	O	LV$_{DD}$	—
TSEC1_RX_CLK	V7	I	LV$_{DD}$	—
TSEC1_RX_DV	U7	I	LV$_{DD}$	—
TSEC1_RX_ER	R9	I	LV$_{DD}$	4, 8
TSEC1_TX_CLK	V6	I	LV$_{DD}$	—
TSEC1_TX_EN	U4	O	LV$_{DD}$	22
TSEC1_TX_ER	T3	O	LV$_{DD}$	—
Three-Speed Ethernet Controller (Gigabit Ethernet 3)				
TSEC3_RXD[7:0]	P11, N11, M11, L11, R8, N10, N9, P10	I	LV$_{DD}$	—
TSEC3_TXD[7:0]	M7, N7, P7, M8, L7, R6, P6, M6	O	LV$_{DD}$	4, 8, 14
TSEC3_COL	M9	I	LV$_{DD}$	—
TSEC3_CRS	L9	I/O	LV$_{DD}$	16
TSEC3_GTX_CLK	R7	O	LV$_{DD}$	—
TSEC3_RX_CLK	P9	I	LV$_{DD}$	—
TSEC3_RX_DV	P8	I	LV$_{DD}$	—
TSEC3_RX_ER	R11	I	LV$_{DD}$	—
TSEC3_TX_CLK	L10	I	LV$_{DD}$	—
TSEC3_TX_EN	N6	O	LV$_{DD}$	22
TSEC3_TX_ER	L8	O	LV$_{DD}$	4, 8
DUART				
$\overline{UART\_CTS}$[0:1]	AH8, AF6	I	OV$_{DD}$	—
$\overline{UART\_RTS}$[0:1]	AG8, AG9	O	OV$_{DD}$	—

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19 Clocking

This section describes the PLL configuration of the MPC8533E. Note that the platform clock is identical to the core complex bus (CCB) clock.

19.1 Clock Ranges

Table 58 provides the clocking specifications for the processor cores and Table 59 provides the clocking specifications for the memory bus.

Table 58. Processor Core Clocking Specifications

Characteristic	Maximum Processor Core Frequency								Unit	Notes
	667 MHz		800 MHz		1000 MHz		1067 MHz			
	Min	Max	Min	Max	Min	Max	Min	Max		
e500 core processor frequency	667	667	667	800	667	1000	667	1067	MHz	1, 2

Notes:
1. **Caution:** The CCB to SYSCLK ratio and e500 core to CCB ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 19.2, "CCB/SYSCLK PLL Ratio," and Section 19.3, "e500 Core PLL Ratio," for ratio settings.
2. The minimum e500 core frequency is based on the minimum platform frequency of 333 MHz.

Table 59. Memory Bus Clocking Specifications

Characteristic	Maximum Processor Core Frequency		Unit	Notes
	667, 800, 1000, 1067 MHz			
	Min	Max		
Memory bus clock speed	166	266	MHz	1, 2

Notes:
1. **Caution:** The CCB clock to SYSCLK ratio and e500 core to CCB clock ratio settings must be chosen such that the resulting SYSCLK frequency, e500 (core) frequency, and CCB clock frequency do not exceed their respective maximum or minimum operating frequencies. Refer to Section 19.2, "CCB/SYSCLK PLL Ratio," and Section 19.3, "e500 Core PLL Ratio," for ratio settings.
2. The memory bus speed is half of the DDR/DDR2 data rate, hence, half of the platform clock frequency.

19.2 CCB/SYSCLK PLL Ratio

The CCB clock is the clock that drives the e500 core complex bus (CCB), and is also called the platform clock. The frequency of the CCB is set using the following reset signals (see Table 60):

- SYSCLK input signal
- Binary value on LA[28:31] at power up

Table 67. MPC8533EThermal Model (continued)

Conductivity	Value	Units
Solder and Air (29 × 29 × 0.58 mm)		
Kx	0.034	W/m•K
Ky	0.034	
Kz	12.1	
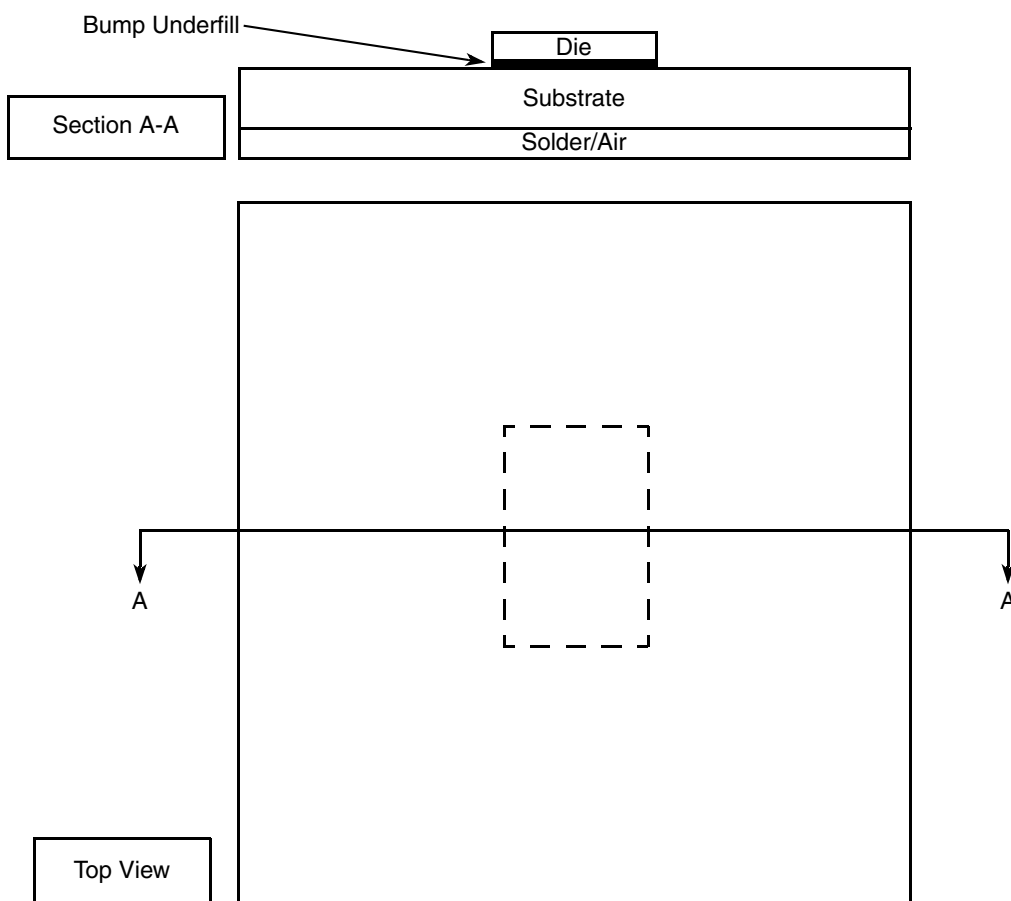
Figure 56. System Level Thermal Model for MPC8533E (Not to Scale)

The Flotherm library files of the parts have a dense grid to accurately capture the laminar boundary layer for flow over the part in standard JEDEC environments, as well as the heat spreading in the board under the package. In a real system, however, the part will require a heat sink to be mounted on it. In this case, the predominant heat flow path will be from the die to the heat sink. Grid density lower than currently in the package library file will suffice for these simulations. The user will need to determine the optimal grid for their specific case.

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20.3 Thermal Management Information

This section provides thermal management information for the flip chip plastic ball grid array (FC-PBGA) package for air-cooled applications. Proper thermal control design is primarily dependent on the system-level design—the heat sink, airflow, and thermal interface material. The MPC8533E implements several features designed to assist with thermal management, including the temperature diode. The temperature diode allows an external device to monitor the die temperature in order to detect excessive temperature conditions and alert the system; see Section 20.3.4, "Temperature Diode," for more information.

The recommended attachment method to the heat sink is illustrated in Figure 57. The heat sink should be attached to the printed-circuit board with the spring force centered over the die. This spring force should not exceed 10 pounds force (45 Newton).
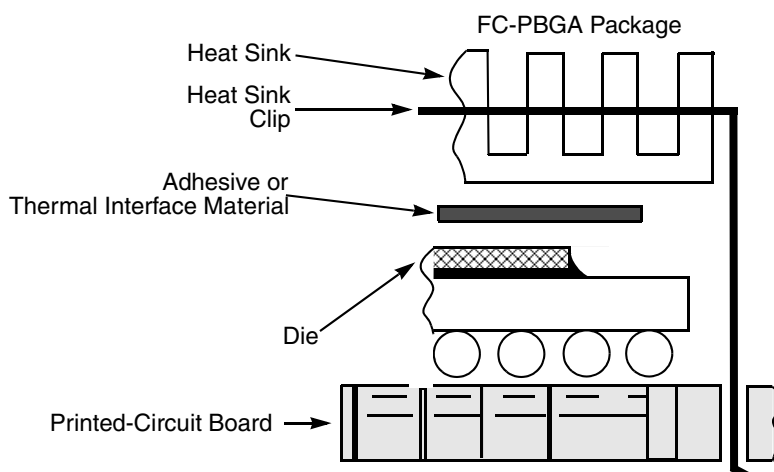

Figure 57. Package Exploded Cross-Sectional View with Several Heat Sink Options

The system board designer can choose between several types of heat sinks to place on the device. There are several commercially-available heat sinks from the following vendors:

> Aavid Thermalloy 603-224-9988
> 80 Commercial St.
> Concord, NH 03301
> Internet: www.aavidthermalloy.com

> Advanced Thermal Solutions 781-769-2800
> 89 Access Road #27.
> Norwood, MA02062
> Internet: www.qats.com

> Alpha Novatech 408-567-8082
> 473 Sapena Ct. #12
> Santa Clara, CA 95054
> Internet: www.alphanovatech.com

Heat sinks are attached to the package by means of a spring clip to holes in the printed-circuit board (see Figure 57). Therefore, the synthetic grease offers the best thermal performance, especially at the low interface pressure.
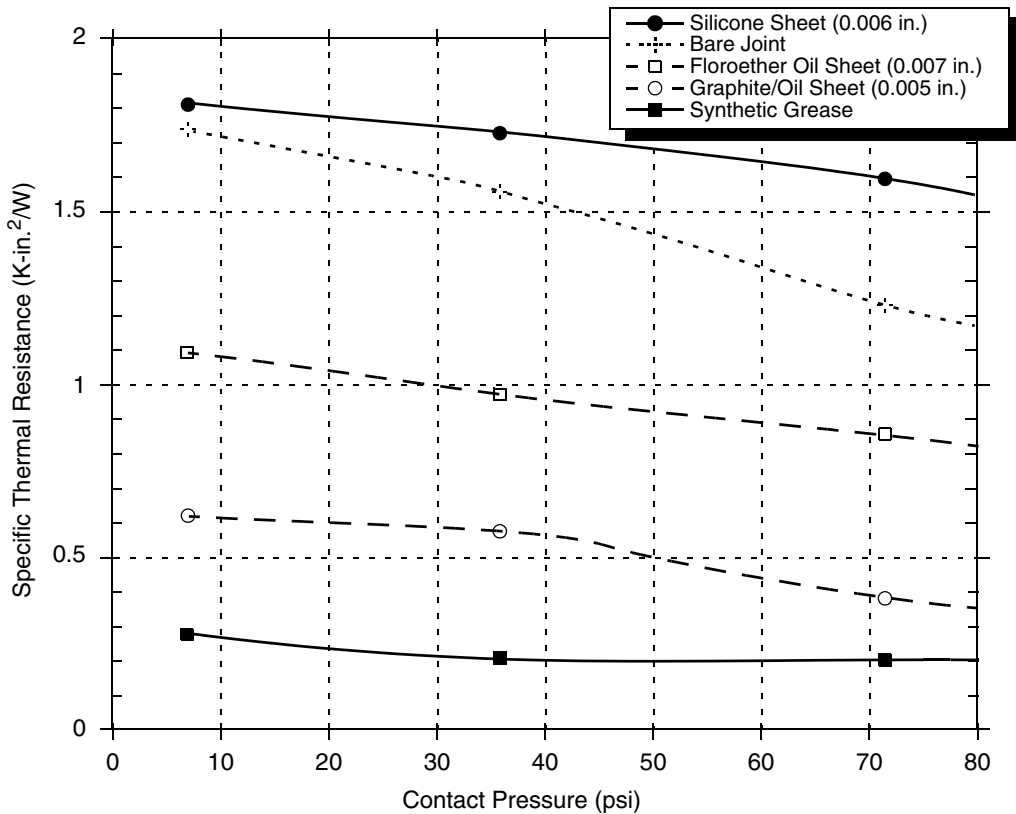

Figure 59. Thermal Performance of Select Thermal Interface Materials

The system board designer can choose between several types of thermal interface. There are several commercially-available thermal interfaces provided by the following vendors:

Chomerics, Inc. 781-935-4850
77 Dragon Ct.
Woburn, MA 01801
Internet: www.chomerics.com

Dow-Corning Corporation800-248-2481
Corporate Center
P.O.Box 999
Midland, MI 48686-0997
Internet: www.dow.com

Shin-Etsu MicroSi, Inc.888-642-7674
10028 S. 51st St.
Phoenix, AZ 85044
Internet: www.microsi.com

The Bergquist Company800-347-4572
18930 West 78th St.

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21.5 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. All unused active low inputs should be tied to V_{DD}, TV_{DD}, BV_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} as required. All unused active high inputs should be connected to GND. All NC (no connect) signals must remain unconnected. Power and ground connections must be made to all external V_{DD}, TV_{DD}, BV_{DD}, OV_{DD}, GV_{DD}, and LV_{DD}, and GND pins of the device.

21.6 Pull-Up and Pull-Down Resistor Requirements

The MPC8533E requires weak pull-up resistors (2–10 kΩ is recommended) on open drain type pins including I^2C pins and MPIC interrupt pins.

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 65. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion will give unpredictable results.

The following pins must NOT be pulled down during power-on reset: TSEC3_TXD[3], $\overline{HRESET\_REQ}$, TRIG_OUT/READY/$\overline{QUIESCE}$, MSRCID[2:4], ASLEEP. The $\overline{DMA\_DACK}[0:1]$ and $\overline{TEST\_SEL}$ pins must be set to a proper state during POR configuration. Refer to the pinout listing table (Table 57) for more details. Refer to the *PCI 2.2 Local Bus Specifications,* for all pullups required for PCI.

21.7 Output Buffer DC Impedance

The MPC8533E drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for I^2C). To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to OV_{DD} or GND. Then, the value of each resistor is varied until the pad voltage is $OV_{DD}/2$ (see Figure 63). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and R_P is trimmed until the voltage at the pad equals $OV_{DD}/2$. R_P then becomes the

Figure 65 shows the JTAG interface connection.
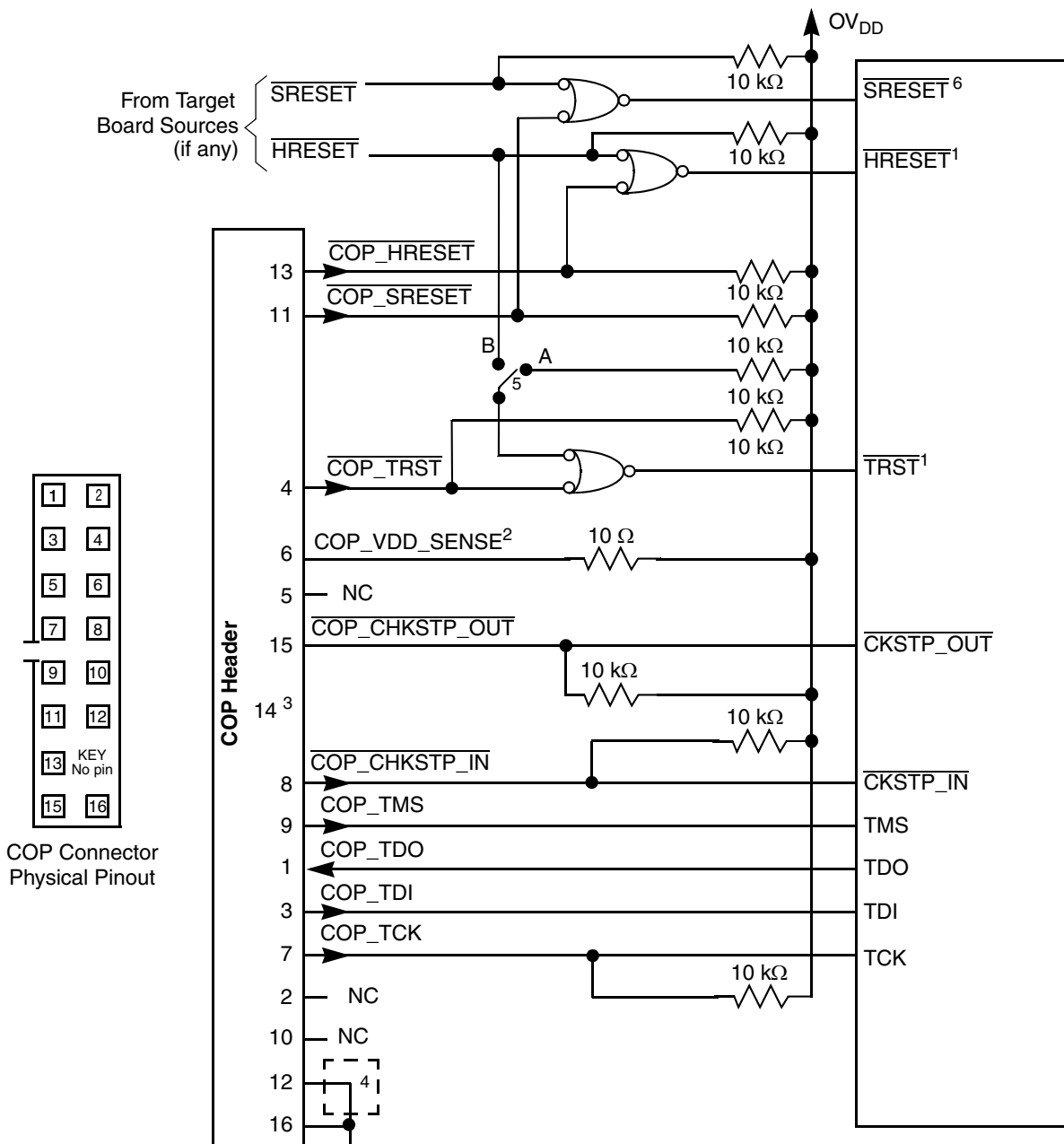
Notes:
1. The COP port and target board should be able to independently assert $\overline{HRESET}$ and $\overline{TRST}$ to the processor in order to fully control the processor as shown here.
2. Populate this with a 10-Ω resistor for short-circuit/current-limiting protection.
3. The KEY location (pin 14) is not physically present on the COP header.
4. Although pin 12 is defined as a No Connect, some debug tools may use pin 12 as an additional GND pin for improved signal integrity.
5. This switch is included as a precaution for BSDL testing. The switch should be closed to position A during BSDL testing to avoid accidentally asserting the $\overline{TRST}$ line. If BSDL testing is not being performed, this switch should be closed to position B.
6. Asserting $\overline{SRESET}$ causes a machine check interrupt to the e500 core.

Figure 65. JTAG Interface Connection

21.10 Guidelines for High-Speed Interface Termination

This section provides guidelines for when the SerDes interface is either not used at all or only partly used.

21.10.1 SerDes Interface Entirely Unused

If the high-speed SerDes interface is not used at all, the unused pin should be terminated as described in this section. However, the SerDes must always have power applied to its supply pins.

The following pins must be left unconnected (float):

- SD_TX[0:7]
- $\overline{\text{SD\_TX}}$[0:7]

The following pins must be connected to GND:

- SD_RX[0:7]
- $\overline{\text{SD\_RX}}$[0:7]
- SD_REF_CLK
- $\overline{\text{SD\_REF\_CLK}}$

21.10.2 SerDes Interface Partly Unused

If only part of the high speed SerDes interface pins are used, the remaining high-speed serial I/O pins should be terminated as described in this section.

The following pins must be left unconnected (float) if not used:

- SD_TX[0:7]
- $\overline{\text{SD\_TX}}$[0:7]

The following pins must be connected to GND if not used:

- SD_RX[0:7]
- $\overline{\text{SD\_RX}}$[0:7]
- SD_REF_CLK
- $\overline{\text{SD\_REF\_CLK}}$

21.11 Guideline for PCI Interface Termination

PCI termination, if not used at all, is done as follows.

Option 1

- If PCI arbiter is enabled during POR,
- All AD pins will be driven to the stable states after POR. Therefore, all ADs pins can be floating.
- All PCI control pins can be grouped together and tied to OV_{DD} through a single 10-kΩ resistor.
- It is optional to disable PCI block through DEVDISR register after POR reset.