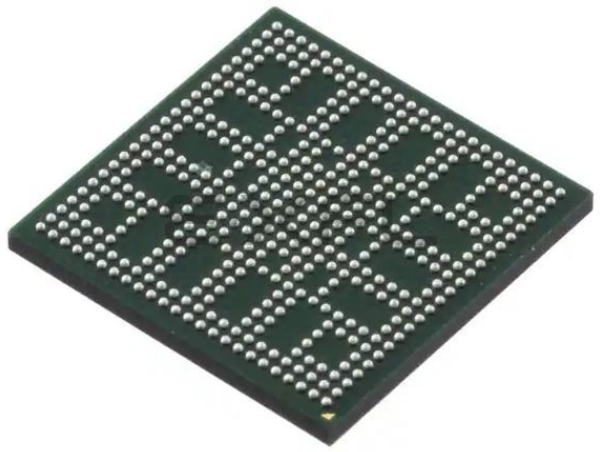

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, LVDDR3, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + PHY (3)
Voltage - I/O	1.2V, 1.8V, 3.0V
Operating Temperature	0°C ~ 95°C (TJ)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	432-TFBGA
Supplier Device Package	432-MAPBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6l2dvn10ac

Table 2. i.MX 6SoloLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
IOMUXC	IOMUX Control	System Control Peripherals	This module enables flexible IO multiplexing. Each IO pad has default and several alternate functions. The alternate functions are software configurable.
KPP	Key Pad Port	Connectivity Peripherals	KPP Supports 8 x 8 external key pad matrix. KPP features are: • Open drain design • Glitch suppression circuit design • Multiple keys detection • Standby key press detection
LCDIF	LCD Interface	Multimedia Peripherals	The LCDIF provides display data for external LCD panels from simple text-only displays to WVGA, 16/18/24 bpp color TFT panels. The LCDIF supports all of these different interfaces by providing fully programmable functionality and sharing register space, FIFOs, and ALU resources at the same time. The LCDIF supports RGB (DOTCLK) modes as well as system mode including both VSYNC and WSYNC modes.
MMDC	DDR Controller	Connectivity Peripherals	DDR Controller has the following features: • Support 16/32-bit DDR3-800 or LPDDR2-800 • Supports up to 2 GByte DDR memory space
OCOTP_ CTRL	OTP Controller	Security	The On-Chip OTP controller (OCOTP_CTRL) provides an interface for reading, programming, and/or overriding identification and control information stored in on-chip fuse elements. The module supports electrically-programmable poly fuses (eFUSEs). The OCOTP_CTRL also provides a set of volatile software-accessible signals that can be used for software control of hardware elements, not requiring non-volatility. The OCOTP_CTRL provides the primary user-visible mechanism for interfacing with on-chip fuse elements. Among the uses for the fuses are unique chip identifiers, mask revision numbers, cryptographic keys, JTAG secure mode, boot characteristics, and various control signals, requiring permanent non-volatility.
OCRAM	On-Chip Memory Controller	Data Path	The On-Chip Memory controller (OCRAM) module is designed as an interface between system's AXI bus and internal (on-chip) SRAM memory module. In i.MX 6SoloLite processor, the OCRAM is used for controlling the 128 KB multimedia RAM through a 64-bit AXI bus.
OCRAM_L2	On-Chip Memory Controller for L2 Cache	Data Path	The On-Chip Memory controller for L2 cache (OCRAM_L2) module is designed as an interface between system's AXI bus and internal (on-chip) L2 cache memory module during boot mode.
OSC 32 kHz	OSC 32 kHz	Clocking	Generates 32.768 kHz clock from external crystal.
PMU	Power Management functions	Data Path	Integrated power management unit. Used to provide power to various SoC domains.
PWM-1 PWM-2 PWM-3 PWM-4	Pulse Width Modulation	Connectivity Peripherals	The pulse-width modulator (PWM) has a 16-bit counter and is optimized to generate sound from stored sample audio images and it can also generate tones. It uses 16-bit resolution and a 4x16 data FIFO to generate sound.

Table 2. i.MX 6SoloLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
PXP	PiXel Processing Pipeline	Display Peripherals	A high-performance pixel processor capable of 1 pixel/clock performance for combined operations, such as color-space conversion, alpha blending, gamma-mapping, and rotation. The PXP isenhanced with features specifically for gray scale applications. In addition, the PXP supports traditional pixel/frame processing paths for still-image and video processing applications, allowing it to interface with either of the integrated EPD controllers.
RAM 128 KB	Internal RAM	Internal Memory	Internal RAM, which is accessed through OCRAM memory controller.
RNGB	Random Number Generator	Security	Random number generating module.
ROM 96KB	Boot ROM	Internal Memory	Supports secure and regular Boot Modes. Includes read protection on 4K region for content protection.
ROMCP	ROM Controller with Patch	Data Path	ROM Controller with ROM Patch support.
SDMA	Smart Direct Memory Access	System Control Peripherals	The SDMA is multi-channel flexible DMA engine. It helps in maximizing system performance by off-loading the various cores in dynamic data routing. It has the following features: • Powered by a 16-bit Instruction-Set micro-RISC engine • Multi-channel DMA supporting up to 32 time-division multiplexed DMA channels • 48 events with total flexibility to trigger any combination of channels • Memory accesses including linear, FIFO, and 2D addressing • Shared peripherals between ARM and SDMA • Very fast Context-Software switching with 2-level priority based preemptive multi-tasking • DMA units with auto-flush and prefetch capability • Flexible address management for DMA transfers (increment, decrement, and no address changes on source and destination address) • DMA ports can handle unit-directional and bi-directional flows (copy mode) • Up to 8-word buffer for configurable burst transfers • Support of byte-swapping and CRC calculations • Library of Scripts and API is available
SJC	System JTAG Controller	System Control Peripherals	The SJC provides JTAG interface, which complies with JTAG TAP standards, to internal logic. The i.MX 6SoloLite processor uses JTAG port for production, testing, and system debugging. In addition, the SJC provides BSR (Boundary Scan Register) standard support, which complies with IEEE1149.1 and IEEE1149.6 standards. The JTAG port must be accessible during platform initial laboratory bring-up, for manufacturing tests and troubleshooting, as well as for software debugging by authorized entities. The i.MX 6SoloLite SJC incorporates three security modes for protecting against unauthorized accesses. Modes are selected through eFUSE configuration.
SNVS	Secure Non-Volatile Storage	Security	Secure Non-Volatile Storage, including Secure Real Time Clock, Security State Machine, Master Key Control, and Violation/Tamper Detection and reporting.
SPDIF	Sony Phillips Digital Interface	Multimedia Peripherals	A standard audio file transfer format, developed jointly by the Sony and Phillips corporations. Has Transmitter and Receiver functionality.

Table 2. i.MX 6SoloLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
uSDHC-1 uSDHC-2 uSDHC-2 uSDHC-4	SD/MMC and SDXC Enhanced Multi-Media Card / Secure Digital Host Controller	Connectivity Peripherals	i.MX 6SoloLite specific SoC characteristics: All four MMC/SD/SDIO controller IPs are identical and are based on the uSDHC IP. They are: • Conforms to the SD Host Controller Standard Specification version 3.0. • Fully compliant with MMC command/response sets and Physical Layer as defined in the Multimedia Card System Specification, v4.2/4.3/4.4/4.41/4.5 including high-capacity (size > 2 GB) cards HC MMC. Hardware reset as specified for eMMC cards is supported at ports 3 and 4 only. • Fully compliant with SD command/response sets and Physical Layer as defined in the SD Memory Card Specifications, v3.0 including high-capacity SDHC cards up to 32 GB and SDXC cards up to 2 TB. • Fully compliant with SDIO command/response sets and interrupt/read-wait mode as defined in the SDIO Card Specification, Part E1, v1.10 • Fully compliant with SD Card Specification, Part A2, SD Host Controller Standard Specification, v2.00 All four ports support: • 1-bit or 4-bit transfer mode specifications for SD and SDIO cards up to UHS-I SDR104 mode (104 MB/s max) • 1-bit, 4-bit, or 8-bit transfer mode specifications for MMC cards up to 52 MHz in both SDR and DDR modes (104 MB/s max) • 4-bit or 8-bit transfer mode specifications for eMMC chips up to 200 MHz in HS200 mode (200 MB/s max) However, the SoC level integration and I/O muxing logic restrict the functionality to the following: • Instances 1 and 2 are primarily intended to serve as external slots or interfaces to on-board SDIO devices. These ports are equipped with “Card detection” and “Write Protection” pads and do not support hardware reset. • All ports can work with 1.8 V and 3.3 V cards. There are two completely independent I/O power domains for Ports 1 and 2 in four bit configuration (SD interface). Port 3 is placed in an independent power domain and port 4 shares its power domain with other interfaces.
WDOG-1	Watchdog	Timer Peripherals	The Watchdog Timer supports two comparison points during each counting period. Each of the comparison points is configurable to evoke an interrupt to the ARM core, and a second point evokes an external event on the WDOG line.
WDOG-2 (TZ)	Watchdog (TrustZone)	Timer Peripherals	The TrustZone Watchdog (TZ WDOG) timer module protects against TrustZone starvation by providing a method of escaping normal mode and forcing a switch to the TZ mode. TZ starvation is a situation where the normal OS prevents switching to the TZ mode. Such situation is undesirable as it can compromise the system’s security. Once the TZ WDOG module is activated, it must be serviced by TZ software on a periodic basis. If servicing does not take place, the timer times out. Upon a time-out, the TZ WDOG asserts a TZ mapped interrupt that forces switching to the TZ mode. If it is still not served, the TZ WDOG asserts a security violation signal to the CSU. The TZ WDOG module cannot be programmed or deactivated by a normal mode Software.
XTALOSC	Crystal Oscillator I/F	Clocking	The XTALOSC module enables connectivity to external crystal oscillator device. In a typical application use-case, it is used for 24 MHz oscillator.

Table 10 shows the interface frequency requirements.

Table 10. External Input Clock Frequency

Parameter Description	Symbol	Min	Typ	Max	Unit
RTC_XTALI Oscillator[1, 2]	f_{ckil}	—	32.768[(see 3)]/32.0	—	kHz
XTALI Oscillator[4, 2]	f_{xtal}	—	24	—	MHz

1 External oscillator or a crystal with internal oscillator amplifier.

2 The required frequency stability of this clock source is application dependent. For recommendations, see Hardware Development Guide for i.MX 6Dual, 6Quad, 6Solo, 6DualLite Families of Applications Processors (IMX6DQ6SDLHDG).

3 Recommended nominal frequency 32.768 kHz.

4 External oscillator or a fundamental frequency crystal with internal oscillator amplifier.

The typical values shown in Table 10 are required for use with NXP BSPs to ensure precise time keeping and USB operation. For RTC_XTALI operation, two clock sources are available:

- On-chip 40 kHz ring oscillator: This clock source has the following characteristics:
  - Approximately 25 µA more Idd than crystal oscillator
  - Approximately ±50% tolerance
  - No external component required
  - Starts up quicker than 32 kHz crystal oscillator
- External crystal oscillator with on-chip support circuit
  - At power up, ring oscillator is utilized. After crystal oscillator is stable, the clock circuit switches over to the crystal oscillator automatically.
  - Higher accuracy than ring oscillator
  - If no external crystal is present, then the ring oscillator is utilized

The decision to choose a clock source should be taken based on real-time clock use and precision time-out.

4.1.5 Maximum Supply Currents

The Power Virus numbers shown in Table 11 represent a use case designed specifically to show the maximum current consumption possible. All cores are running at the defined maximum frequency and are limited to L1 cache accesses only to ensure no pipeline stalls. Although a valid condition, it would have a very limited practical use case, if at all, and be limited to an extremely low duty cycle unless the intention was to specifically show the worst case power consumption.

The NXP power management IC, MMPF0100xxxx, which is targeted for the i.MX 6 series processor family, supports the power consumption shown in Table 11, however a robust thermal design is required for the increased system power dissipation.

See the *i.MX 6SoloLite Power Consumption Measurement Application Note* (AN4580) for more details on typical power consumption under various use case definitions.

For information on external capacitor requirements for this regulator, see the Hardware Development Guide for i.MX 6SoloLite Applications Processors (IMX6SLHDG).

For additional information, see the i.MX 6SoloLite reference manual.

4.4 PLL's Electrical Characteristics

4.4.1 Audio/Video PLL's Electrical Parameters

Table 14. Audio/Video PLL's Electrical Parameters

Parameter	Value
Clock output range	650 MHz ~1.3 GHz
Reference clock	24 MHz
Lock time	<11250 reference cycles (450 μs)

4.4.2 528 MHz PLL

Table 15. 528 MHz PLL's Electrical Parameters

Parameter	Value
Clock output range	528 MHz PLL output
Reference clock	24 MHz
Lock time	<11250 reference cycles (15 μs)

4.4.3 Ethernet PLL

Table 16. Ethernet PLL's Electrical Parameters

Parameter	Value
Clock output range	500 MHz
Reference clock	24 MHz
Lock time	<11250 reference cycles (450 μs)

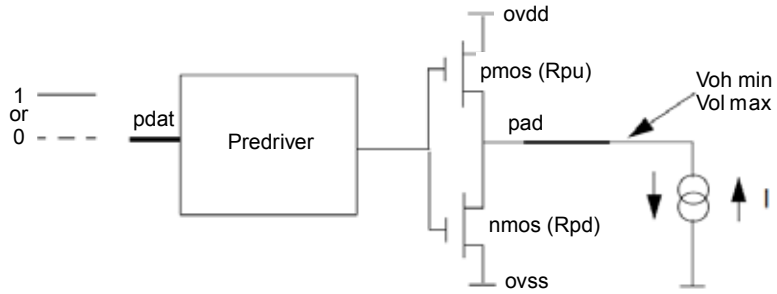

Figure 4. Circuit for Parameters Voh and Vol for I/O Cells

4.6.1 XTALI and RTC_XTALI (Clock Inputs) DC Parameters

Table 20 shows the DC parameters for the clock inputs.

Table 20. XTALI and RTC_XTALI DC Parameters

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
XTALI high-level DC input voltage	Vih	—	0.8 x NVCC_PLL_OUT	—	NVCC_PLL_ OUT	V
XTALI low-level DC input voltage	Vil	—	0	—	0.2V	V
RTC_XTALI high-level DC input voltage	Vih	—	0.8	—	1.1[1]	V
RTC_XTALI low-level DC input voltage	Vil	—	0	—	0.2V	V
Input capacitance	C_{IN}	Simulated data	—	5	—	pF
XTALI input leakage at startup	$I_{XTALI\_STARTUP}$	Power-on startup for 0.15 msec with a driven 24 MHz RTC clock @1.1 V. [2]	—	—	600	µA
DC input current	I_{XTALI_DC}	—	—	—	2.5	µA

[1] This voltage specification must not be exceeded and, as such, is an absolute maximum specification.

[2] This current draw is present even if an external clock source directly drives XTALI.

NOTE

The Vil and Vih specifications only apply when an external clock source is used. If a crystal is used, Vil and Vih do not apply.

4.6.2 Dual Voltage General Purpose IO Cell Set (DVGPIO) DC Parameters

Table 21 shows DC parameters for GPIO pads. The parameters in Table 21 are guaranteed per the operating ranges in Table 9, unless otherwise noted.

4.9.1 Reset Timings Parameters

Figure 8 shows the reset timing and Table 31 lists the timing parameters.

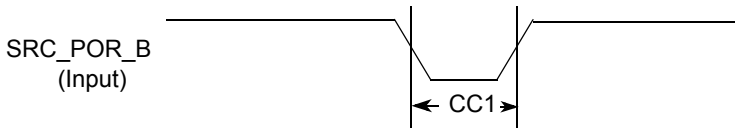

Figure 8. Reset Timing Diagram

Table 31. Reset Timing Parameters

ID	Parameter	Min	Max	Unit
CC1	Duration of POR_B to be qualified as valid.	1	—	XTALOSC_RTC_XTALI

4.9.2 WDOG Reset Timing Parameters

Figure 9 shows the WDOG reset timing and Table 32 lists the timing parameters.

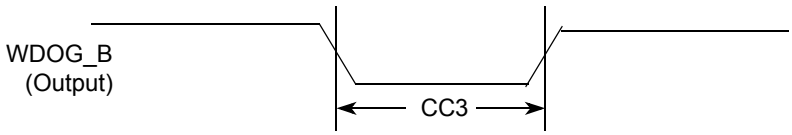

Figure 9. WDOG_B Timing Diagram

Table 32. WDOG_B Timing Parameters

ID	Parameter	Min	Max	Unit
CC3	Duration of WDOG_B Assertion	1	—	RTC_XTALI cycle

NOTE

RTC_XTALI is approximately 32 kHz. RTC_XTALI cycle is one period or approximately 30 µs.

NOTE

WDOG_B output signals (for each one of the Watchdog modules) do not have dedicated bins, but are muxed out through the IOMUX. See the IOMUX manual for detailed information.

4.9.3.2 General EIM Timing-Synchronous Mode

Figure 10, Figure 11, and Table 34 specify the timings related to the EIM module. All EIM output control signals may be asserted and deasserted by an internal clock synchronized to the BCLK rising edge according to corresponding assertion/negation control fields.

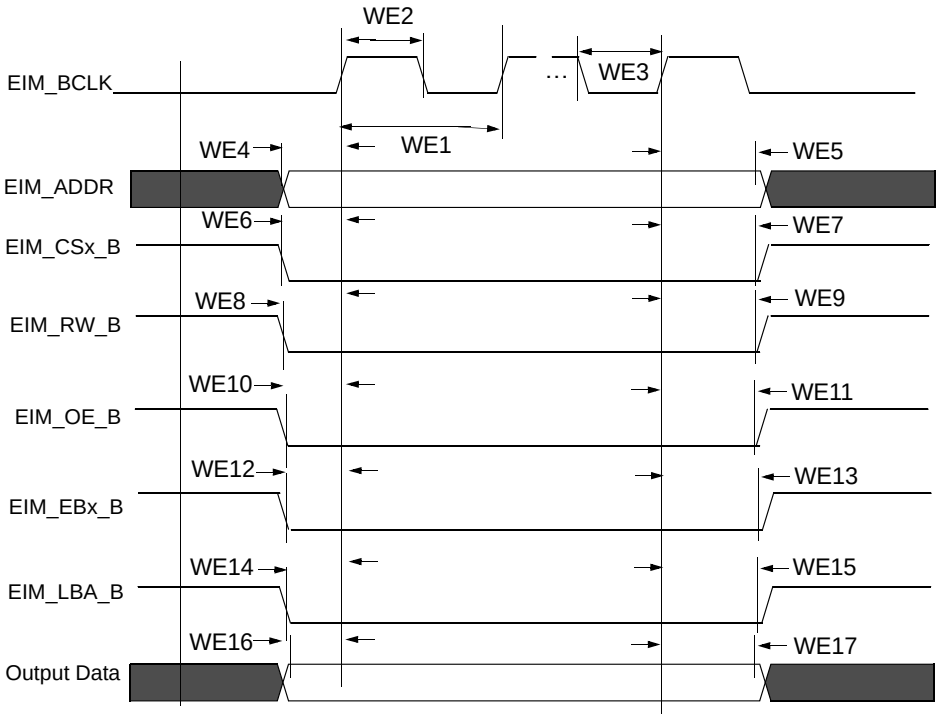

Figure 10. EIM Output Timing Diagram

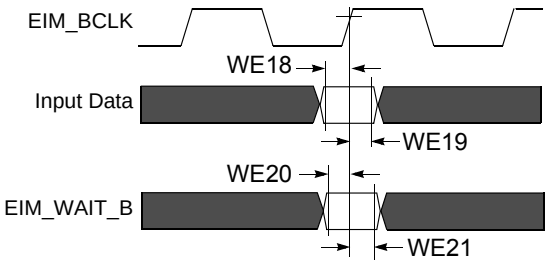

Figure 11. EIM Input Timing Diagram

4.9.3.3 Examples of EIM Synchronous Accesses

Table 34. EIM Bus Timing Parameters

ID	Parameter	Min[1]	Max[1]	Unit
WE1	EIM_BCLK cycle time[2]	t × (k+1)	—	ns
WE2	EIM_BCLK high level width	0.4 × t × (k+1)	—	ns
WE3	EIM_BCLK low level width	0.4 × t × (k+1)	—	ns
WE4	Clock rise to address valid	-0.5 × t × (k+1) -1.25	-0.5 × t × (k+1) +2.25	ns

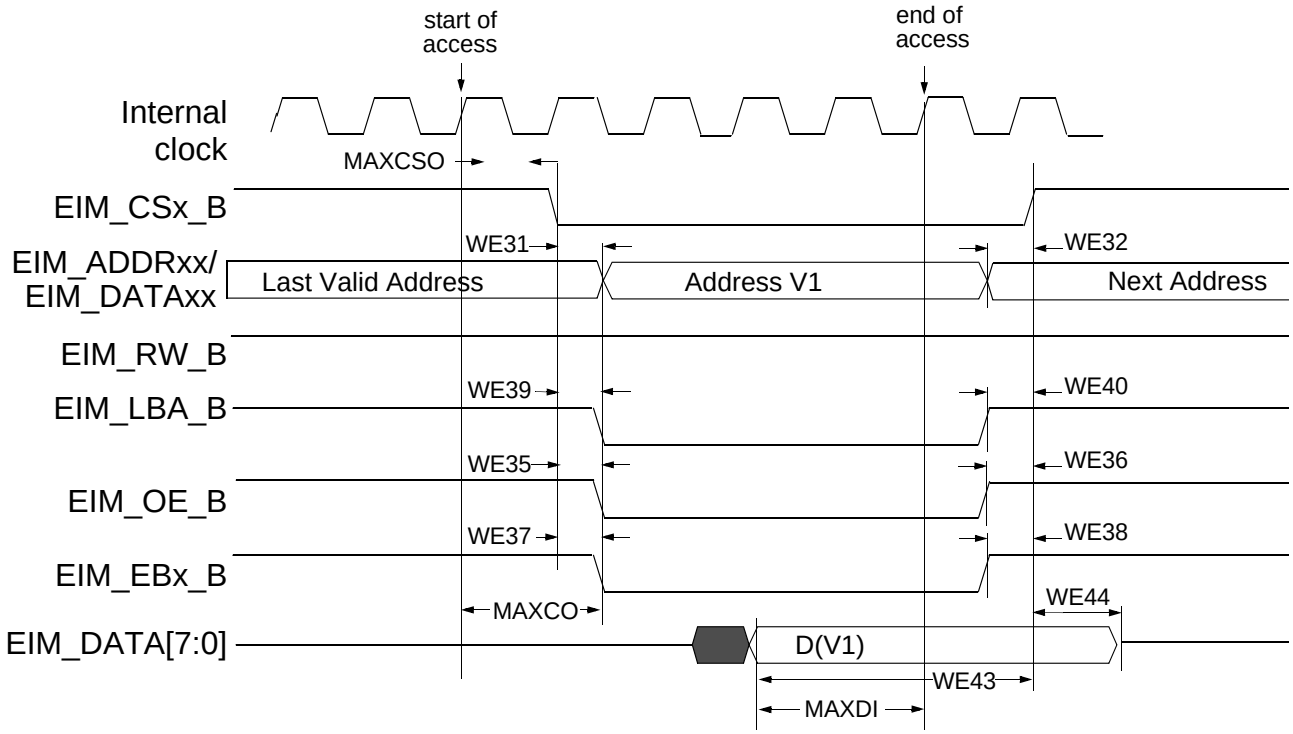

Figure 16. Asynchronous Memory Read Access (RWSC = 5)

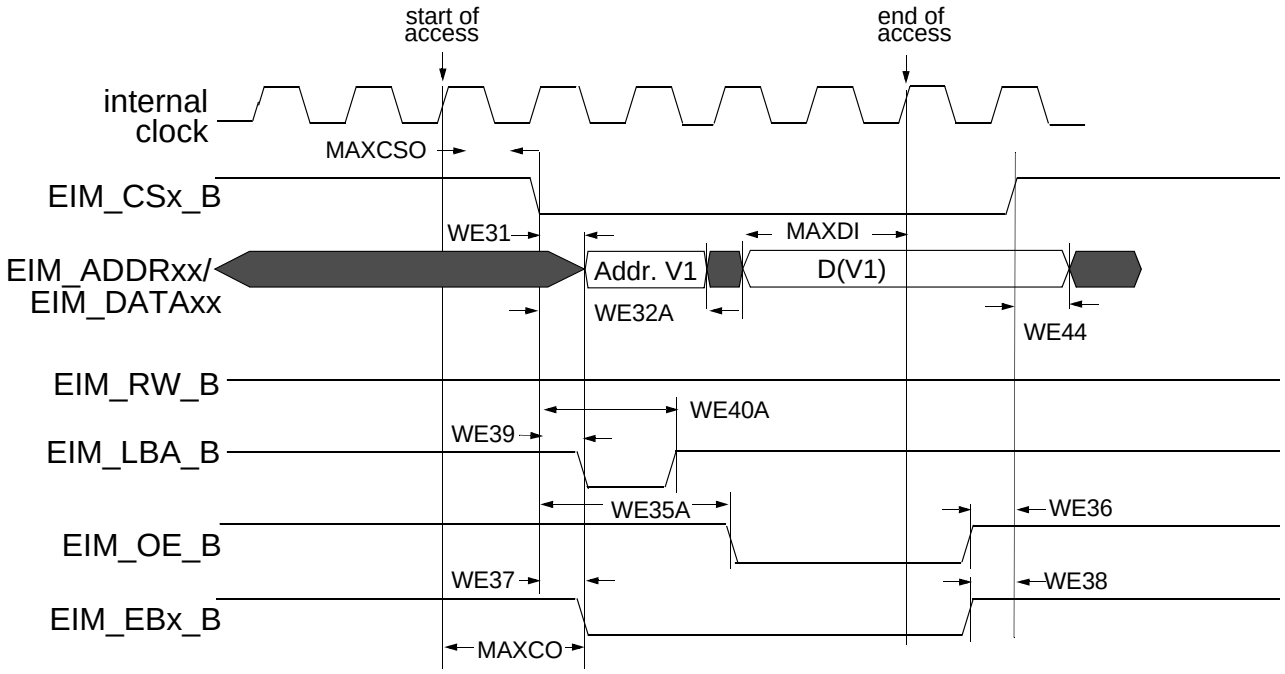

Figure 17. Asynchronous A/D Muxed Read Access (RWSC = 5)

4.10.3.2 ECSPI Slave Mode Timing

Figure 26 depicts the timing of ECSPI in slave mode and Table 40 lists the ECSPI slave mode timing characteristics.

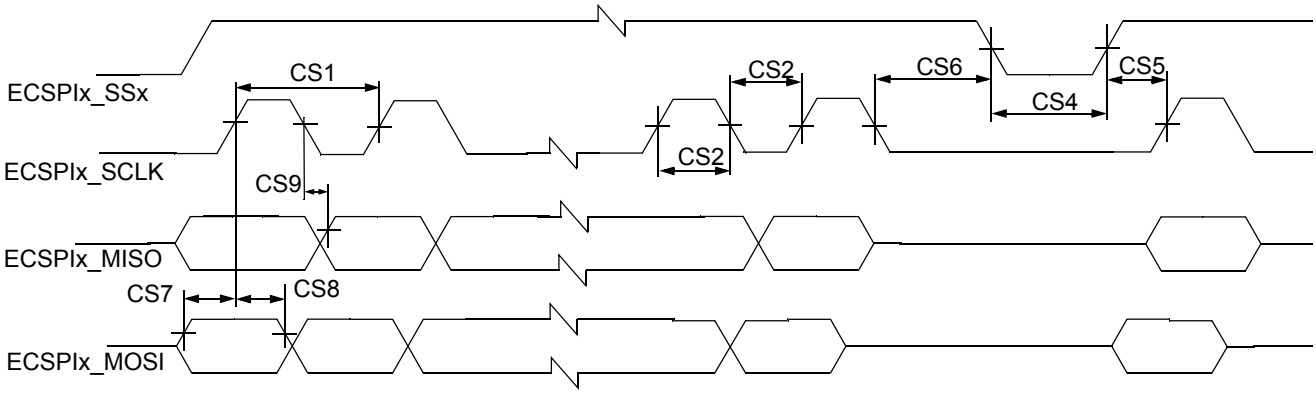

Figure 26. ECSPI Slave Mode Timing Diagram

NOTE

ECSPIx_MISO is always driven (not tri-stated) between actual data transmissions. This limits the ECSPI to be connected between a single master and a single slave.

Table 40. ECSPI Slave Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	ECSPIx_SCLK Cycle Time–Read ECSPIx_SCLK Cycle Time–Write	t_{clk}	40 15	—	ns
CS2	ECSPIx_SCLK High or Low Time–Read ECSPIx_SCLK High or Low Time–Write	t_{SW}	20 7	—	ns
CS4	ECSPIx_SSx pulse width	t_{CSLH}	Half SCLK period	—	ns
CS5	ECSPIx_SSx Lead Time (CS setup time)	t_{SCS}	5	—	ns
CS6	ECSPIx_SSx Lag Time (CS hold time)	t_{HCS}	5	—	ns
CS7	ECSPIx_MOSI Setup Time	t_{Smosi}	4	—	ns
CS8	ECSPIx_MOSI Hold Time	t_{Hmosi}	4	—	ns
CS9	ECSPIx_MISO Propagation Delay (C_{LOAD} = 20 pF)	t_{PDmiso}	4	17	ns

4.10.4 Ultra High Speed SD/SDIO/MMC Host Interface (uSDHC) AC Timing

This section describes the electrical information of the uSDHC, which includes SD/eMMC4.3 (Single Data Rate) timing and eMMC4.4/4.41 (Dual Date Rate) timing.

4.10.4.1 SD/eMMC4.3 (Single Data Rate) AC Timing Parameters

Figure 27 depicts the timing of SD/eMMC4.3, and Table 41 lists the SD/eMMC4.3 timing characteristics.

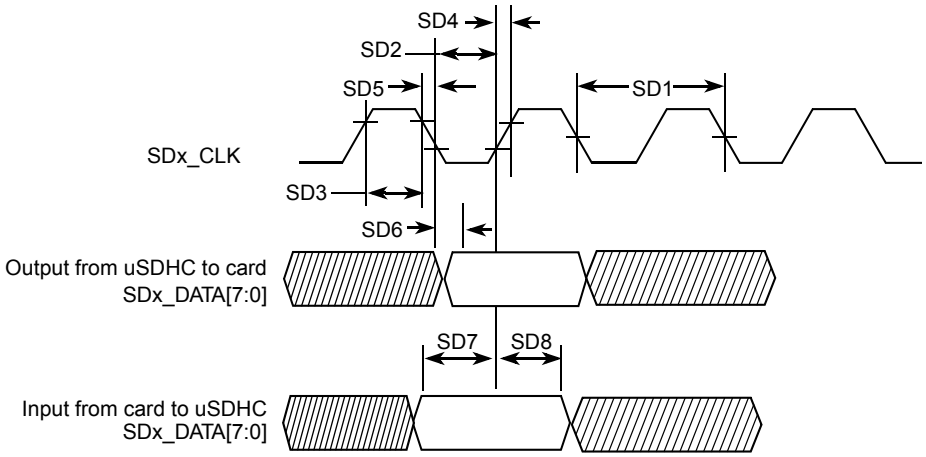

Figure 27. SD/eMMC4.3 Timing Diagram

Table 41. SD/eMMC4.3 Interface Timing Parameters

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock[1]					
SD1	Clock Frequency (Low Speed)	f_{PP}[2]	0	400	kHz
	Clock Frequency (SD/SDIO Full Speed/High Speed)	f_{PP}[3]	0	25/50	MHz
	Clock Frequency (MMC Full Speed/High Speed)	f_{PP}[4]	0	20/52	MHz
	Clock Frequency (Identification Mode)	f_{OD}	100	400	kHz
SD2	Clock Low Time	t_{WL}	7	—	ns
SD3	Clock High Time	t_{WH}	7	—	ns
eSDHC Output/Card Inputs SDx_CMD, SDx_DATAx (Reference to CLK)					
SD6	eSDHC Output Delay	t_{OD}	–6.6	3.6	ns
eSDHC Input/Card Outputs SDx_CMD, SDx_DATAx (Reference to CLK)					
SD7	eSDHC Input Setup Time	t_{ISU}	2.5	—	ns
SD8	eSDHC Input Hold Time[5]	t_{IH}	1.5	—	ns

1 Clock duty cycle will be in the range of 47% to 53%.

2 In low speed mode, card clock must be lower than 400 kHz, voltage ranges from 2.7 to 3.6 V.

3 In normal (full) speed mode for SD/SDIO card, clock frequency can be any value between 0–25 MHz. In high-speed mode, clock frequency can be any value between 0–50 MHz.

4 In normal (full) speed mode for MMC card, clock frequency can be any value between 0–20 MHz. In high-speed mode, clock frequency can be any value between 0–52 MHz.

4.10.8 Pulse Width Modulator (PWM) Timing Parameters

This section describes the electrical information of the PWM. The PWM can be programmed to select one of three clock signals as its source frequency. The selected clock signal is passed through a prescaler before being input to the counter. The output is available at the pulse-width modulator output (PWMx_OUT) external pin (see external signals table in the i.MX 6SoloLite reference manual for PWM pin assignments).

Figure 33 depicts the timing of the PWM, and Table 47 lists the PWM timing parameters.

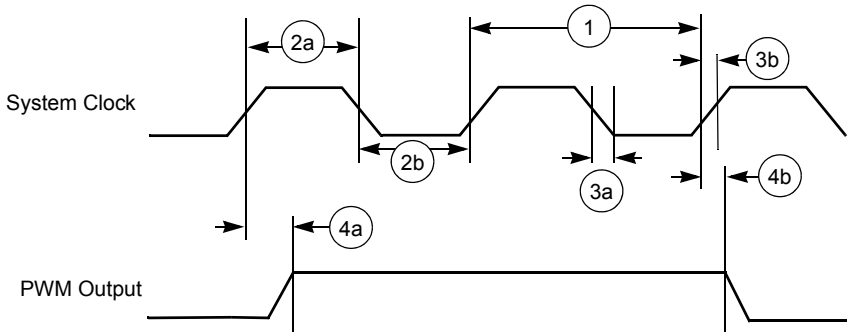

Figure 33. PWM Timing Diagram

Table 47. PWM Output Timing Parameters

Reference Number	Parameter	Min	Max	Unit
1	System CLK frequency[1]	0	ipg_clk	MHz
2a	Clock high time	12.29	—	ns
2b	Clock low time	9.91	—	ns

1 CL of PWMx_OUT = 30 pF

4.10.9 SCAN JTAG Controller (SJC) Timing Parameters

Figure 34 depicts the SJC test clock input timing. Figure 35 depicts the SJC boundary scan timing. Figure 36 depicts the SJC test access port. Signal parameters are listed in Table 48.

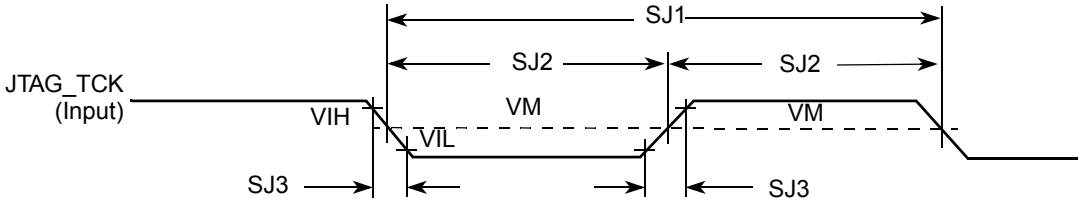

Figure 34. Test Clock Input Timing Diagram

Table 52. SSI Receiver with Internal Clock Timing Parameters (continued)

ID	Parameter	Min	Max	Unit
Oversampling Clock Operation				
SS47	Oversampling clock period	15.04	—	ns
SS48	Oversampling clock high period	6.0	—	ns
SS49	Oversampling clock rise time	—	3.0	ns
SS50	Oversampling clock low period	6.0	—	ns
SS51	Oversampling clock fall time	—	3.0	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TXC/RXC = 0) and a non-inverted frame sync (TXFS/RXFS = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal TXC/RXC and/or the frame sync TXFS/RXFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- The terms, WL and BL, refer to Word Length(WL) and Bit Length(BL).
- For internal Frame Sync operation using external clock, the FS timing is same as that of TXD (for example, during AC97 mode of operation).

Table 62. Fuses and Associated Pins Used for Boot (continued)

Ball Name	Direction at Reset	eFuse Name
LCD_DAT19 Input		BOOT_CFG4[3]
LCD_DAT20 Input		BOOT_CFG4[4]
LCD_DAT21 Input		BOOT_CFG4[5]
LCD_DAT22	Input	BOOT_CFG4[6]
LCD_DAT23 Input		BOOT_CFG4[7]

[1] Pin value overrides fuse settings for BT_FUSE_SEL = '0'. Signal Configuration as Fuse Override Input at Power Up. These are special I/O lines that control the boot up configuration during product development. In production, the boot configuration can be controlled by fuses.

5.2 Boot Devices Interfaces Allocation

Table 63 lists the interfaces that can be used by the boot process in accordance with the specific boot mode configuration. The table also describes the interface's specific modes and IOMUXC allocation, which are configured during boot when appropriate.

Table 63. Interfaces Allocation During Boot

Interface	IP Instance	Allocated Ball Names During Boot	Comment
SPI	ECSPI-1	ECSPI1_MISO, ECSPI1_MOSI, ECSPI1_SCLK, ECSPI1_SS0, I2C1_SCL, I2C1_SDA, ECSPI2_SS0	—
SPI	ECSPI-2	ECSPI2_MISO, ECSPI2_MOSI, ECSPI2_SCLK, ECSPI2_SS0, EPDC_SDCE0, EPDC_GDCLK, EPDC_GDOE	—
SPI	ECSPI-3	EPDC_D9, EPDC_D8, EPDC_D11, EPDC_D10, EPDC_D12, EPDC_D13, EPDC_D14	—
SPI	ECSPI-4	EPDC_D1, EPDC_D0, EPDC_D3, EPDC_D2, EPDC_D2, EPDC_D5, EPDC_D6	—
EIM	EIM	LCD_DAT[21:6], KEY_COL[7:0], KEY_ROW[7:0], EPDC_D[15:8], EPDC_VCOM0, EPDC_VCOM1, EPDC_BDR0, EPDC_PWRCTRL[2:0], EPDC_SDCE1	—
SD/MMC	USDHC-1	Refer to the table "SD/MMC IOMUX Pin Configuration" in the System Boot Chapter of the **i.MX 6SoloLite Applications Processor Reference Manual**	1, 4, or 8 bit Fastboot
SD/MMC	USDHC-2	Refer to the table "SD/MMC IOMUX Pin Configuration" in the System Boot Chapter of the **i.MX 6SoloLite Applications Processor Reference Manual**	1, 4, or 8 bit Fastboot
SD/MMC	USDHC-3	Refer to the table "SD/MMC IOMUX Pin Configuration" in the System Boot Chapter of the **i.MX 6SoloLite Applications Processor Reference Manual**	1, 4, or 8 bit Fastboot (UHSI not supported)
SD/MMC	USDHC-4	Refer to the table "SD/MMC IOMUX Pin Configuration" in the System Boot Chapter of the **i.MX 6SoloLite Applications Processor Reference Manual**	1, 4, or 8 bit Fastboot
I2C	I2C-1	I2C1_SCL, I2C1_SDA	—

Table 66. 13 x 13 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group[1]	Ball Type	Out of Reset Condition[2]			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value[3]
EPDC_D15	A13	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO1_GPIO[22]	Input	Keeper
EPDC_D2	B17	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO1_GPIO[9]	Input	Keeper
EPDC_D3	A16	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO1_GPIO[10]	Input	Keeper
EPDC_D4	B16	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO1_GPIO[11]	Input	Keeper
EPDC_D5	A15	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO1_GPIO[12]	Input	Keeper
EPDC_D6	B15	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO1_GPIO[13]	Input	Keeper
EPDC_D7	C15	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO1_GPIO[14]	Input	Keeper
EPDC_D8	D15	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO1_GPIO[15]	Input	Keeper
EPDC_D9	F15	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO1_GPIO[16]	Input	Keeper
EPDC_GDCLK	A12	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO1_GPIO[31]	Input	Keeper
EPDC_GDOE	B13	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[0]	Input	Keeper
EPDC_GDRL	B12	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[1]	Input	Keeper
EPDC_GDSP	A11	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[2]	Input	Keeper
EPDC_PWRCOM	B11	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[11]	Input	Keeper
EPDC_PWRCTRL0	D11	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[7]	Input	Keeper
EPDC_PWRCTRL1	E11	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[8]	Input	Keeper
EPDC_PWRCTRL2	F11	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[9]	Input	Keeper
EPDC_PWRCTRL3	G12	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[10]	Input	Keeper
EPDC_PWRINT	F10	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[12]	Input	Keeper
EPDC_PWRSTAT	E10	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[13]	Input	Keeper
EPDC_PWRWAKEUP	D10	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[14]	Input	Keeper
EPDC_SDCE0	C11	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO1_GPIO[27]	Input	Keeper

Table 66. 13 x 13 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group[1]	Ball Type	Out of Reset Condition[2]			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value[3]
EPDC_SDCE1	A10	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO1_GPIO[28]	Input	Keeper
EPDC_SDCE2	B9	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO1_GPIO[29]	Input	Keeper
EPDC_SDCE3	A9	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO1_GPIO[30]	Input	Keeper
EPDC_SDCLK	B10	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO1_GPIO[23]	Input	Keeper
EPDC_SDLE	B8	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO1_GPIO[24]	Input	Keeper
EPDC_SDOE	E7	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO1_GPIO[25]	Input	Keeper
EPDC_SDSHR	F7	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO1_GPIO[26]	Input	Keeper
EPDC_VCOM0	C7	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[3]	Input	Keeper
EPDC_VCOM1	D7	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[4]	Input	Keeper
FEC_CRS_DV	AC9	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO4_GPIO[25]	Input	Keeper
FEC_MDC	AA7	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO4_GPIO[23]	Input	Keeper
FEC_MDIO	AB7	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO4_GPIO[20]	Input	Keeper
FEC_REF_CLK	W10	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO4_GPIO[26]	Input	Keeper
FEC_RX_ER	AD9	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO4_GPIO[19]	Input	Keeper
FEC_RXD0	AA10	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO4_GPIO[17]	Input	Keeper
FEC_RXD1	AC10	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO4_GPIO[18]	Input	Keeper
FEC_TX_CLK	AC8	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO4_GPIO[21]	Input	Keeper
FEC_TX_EN	AD10	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO4_GPIO[22]	Input	Keeper
FEC_TXD0	Y10	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO4_GPIO[24]	Input	Keeper
FEC_TXD1	W11	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO4_GPIO[16]	Input	Keeper
HSIC_DAT	AA6	NVCC_1P2V	DDR	—	USB_H_DATA	Input	PD (100K)
HSIC_STROBE	AB6	NVCC_1P25	DDR	—	USB_H_STROBE	Input	PD (100K)

Table 66. 13 x 13 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group[1]	Ball Type	Out of Reset Condition[2]			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value[3]
I2C1_SCL	AC13	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[12]	Input	Keeper
I2C1_SDA	AD13	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[13]	Input	Keeper
I2C2_SCL	E18	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[14]	Input	Keeper
I2C2_SDA	D18	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[15]	Input	Keeper
JTAG_MOD	Y14	NVCC33_IO	GPIO	ALT5	JTAG_MODE	—	PU (100K)
JTAG_TCK	AA14	NVCC33_IO	GPIO	ALT5	JTAG_TCK	—	PU (47K)
JTAG_TDI	W14	NVCC33_IO	GPIO	ALT5	JTAG_TDI	—	PU (47K)
JTAG_TDO	W15	NVCC33_IO	GPIO	ALT5	JTAG_TDO	—	Keeper
JTAG_TMS	Y15	NVCC33_IO	GPIO	ALT5	JTAG_TMS	—	PU (47K)
JTAG_TRSTB	AA15	NVCC33_IO	GPIO	ALT5	JTAG_TRSTB	—	PU (47K)
KEY_COL0	G23	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[24]	Input	Keeper
KEY_COL1	F23	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[26]	Input	Keeper
KEY_COL2	E23	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[28]	Input	Keeper
KEY_COL3	E22	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[30]	Input	Keeper
KEY_COL4	E20	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO4_GPIO[0]	Input	Keeper
KEY_COL5	D24	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO4_GPIO[2]	Input	Keeper
KEY_COL6	D22	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO4_GPIO[4]	Input	Keeper
KEY_COL7	C23	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO4_GPIO[6]	Input	Keeper
KEY_ROW0	G24	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[25]	Input	Keeper
KEY_ROW1	F24	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[27]	Input	Keeper
KEY_ROW2	E24	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[29]	Input	Keeper
KEY_ROW3	E21	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[31]	Input	Keeper
KEY_ROW4	E19	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO4_GPIO[1]	Input	Keeper
KEY_ROW5	D23	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO4_GPIO[3]	Input	Keeper

Table 68. 13 x 13 mm, 0.5 mm Pitch Ball Map (continued)

	1	2	3	4	5	6	7	8
A	GND	DRAM_SDQS3_B	DRAM_D24	GND	DRAM_D27	DRAM_D29	GND	DRAM_D31
B	DRAM_D14	DRAM_D15	DRAM_SDQS3	DRAM_D25	DRAM_D26	DRAM_D28	DRAM_D30	EPDC_SDLE
C	DRAM_D12	DRAM_D13	DRAM_DQM3	**NC**	**NC**	GND	EPDC_VCOM0	**NC**
D	GND	GND	DRAM_D11	**NC**	**NC**	DRAM_RESET	EPDC_VCOM1	**NC**
E	DRAM_D9	DRAM_D8	DRAM_D10	DRAM_SDODT1	GND	NVCC_DRAM	EPDC_SDOE	**NC**
F	DRAM_SDQS1	DRAM_SDQS1_B	**NC**	**NC**	**NC**	**NC**	EPDC_SDSHR	**NC**
G	GND	DRAM_DQM1	**NC**	**NC**	**NC**	**NC**	NVCC_DRAM	GND
H	DRAM_SDBA2	ZQPAD	GND	DRAM_A7	DRAM_A13	NVCC_DRAM	GND	**NC**
J	DRAM_SDBA0	DRAM_A10	DRAM_A8	DRAM_A9	GND	NVCC_DRAM	VDD_SOC_CAP	VDD_SOC_CAP
K	GND	DRAM_A15	**NC**	**NC**	**NC**	**NC**	VDD_SOC_CAP	VDD_SOC_CAP
L	DRAM_SDCLK_0	DRAM_CS1	**NC**	**NC**	**NC**	**NC**	GND	**NC**
M	DRAM_SDCLK_0_B	DRAM_SDCKE1	DRAM_A5	DRAM_A6	GND	NVCC_DRAM_2P5	GND	GND
N	DRAM_RAS	DRAM_CS0	GND	DRAM_A4	DRAM_VREF	NVCC_DRAM	GND	GND
P	DRAM_CAS	SDCKE0	**NC**	**NC**	**NC**	**NC**	NVCC_DRAM	**NC**
R	GND	DRAM_A14	**NC**	**NC**	**NC**	**NC**	VDD_PU_CAP	VDD_PU_CAP
T	DRAM_SDBA1	DRAM_A11	DRAM_A2	DRAM_A3	GND	NVCC_DRAM	VDD_PU_CAP	VDD_PU_CAP
U	DRAM_SDWE	DRAM_A12	GND	DRAM_A0	DRAM_A1	NVCC_DRAM	GND	**NC**
V	GND	DRAM_DQM0	**NC**	**NC**	**NC**	**NC**	NVCC_DRAM	GND
W	DRAM_SDQS0_B	DRAM_SDQS0	**NC**	**NC**	**NC**	**NC**	NVCC_1P2	**NC**
Y	DRAM_D6	DRAM_D7	DRAM_D5	DRAM_SDODT0	GND	NVCC_DRAM	PWM1	**NC**
AA	GND	GND	DRAM_D4	**NC**	**NC**	HSIC_DAT	FEC_MDC	**NC**
AB	DRAM_D3	DRAM_D2	DRAM_DQM2	**NC**	**NC**	HSIC_STROBE	FEC_MDIO	**NC**
AC	DRAM_D1	DRAM_D0	DRAm_SDQS2	DRAM_D22	DRAM_D21	DRAM_D19	DRAM_D17	FEC_TX_CLK
AD	GND	DRAM_SDQS2_B	DRAM_D23	GND	DRAM_D20	DRAM_D18	GND	DRAM_D16

Table 70. i.MX 6SoloLite Data Sheet Document Revision History (continued)

Rev. Number	Date	Substantive Change(s)
4 *Continued*	11/2016	• Section 4.2.2, “Power-Down Sequence,” Replaced contents of section with sentence: “There are no special requirements on the power-down sequence other than …”. • Section 4.5.2, “OSC32K”: Removed text regarding coin cell from third paragraph and removed second NOTE about third party coin cell manufacturer. • Section 4.6, “I/O DC Parameters”: Removed second bullet regarding single voltage GPIO cell set. • Section 4.6.1, “XTALI and RTC_XTALI (Clock Inputs) DC Parameters” Added NOTE after table.Table 20, "XTALI and RTC_XTALI DC Parameters”: – Added parameter rows: Input capacitance; XTALI input leakage; and DC input current. – Added new footnote, “This voltage specification…” • Section 4.6.3, “*Single Voltage General Purpose I/O (GPIO) DC Parameters”* removed section. • Section 4.8, “Output Buffer Impedance Parameters”: Removed second bullet “Single voltage General Purpose I/O cell set …”. • Table 28, "DVGPIO Output Buffer Average Impedance (OVDD 1.8 V)”: Changed all Typical values. • Table 29, "DVGPIO Output Buffer Average Impedance (OVDD 3.3 V)”: Changed all Typical values. • Section 4.8.2, “*Single Voltage GPIO Output Buffer Impedance*”: removed section. • Table 34, "EIM Bus Timing Parameters, Updates throughout table to include min/max values. • Table 35, "EIM Asynchronous Timing Parameters Table Relative Chip Select, Updates throughout table to include min/max values. • Section 4.9.4, “Multi-Mode DDR Controller (MMDC),” created this new section. • Removed: Section 4.9.5, “DDR SDRAM Specific Parameters (DDR3 and LPDDR2),” Section 4.9.5.1, “DDR3 Parameters,” and Section 4.9.5.2, “LPDDR2 Parameters.” • Table 37, "CSI Gated Clock Mode Timing Parameters,” – Parameter P5 reduced (improved) from 10ns to 7.5 ns. – Parameter P6 reduced (improved) from 10ns to 7.5 ns. – Parameter P7 corrected to 66 MHz (no functional change). • Table 38, "CSI Ungated Clock Mode Timing Parameters,” – Parameter P4 reduced (improved) from 10ns to 7.5 ns. – Parameter P5 reduced (improved) from 10ns to 7.5 ns. – Parameter P6 corrected to 66 MHz (no functional change). • Section 4.10.3.1, “ECSPI Master Mode Timing,” Added new NOTE under Figure 25. • Section 4.10.3.2, “ECSPI Slave Mode Timing,” Added new NOTE under Figure 26. • Section 4.10.4.3, “SDR50/SDR104 AC Timing Parameters,” Figure 29 updated to correct SD5. • Table 43, "SDR50/SDR104 Interface Timing Parameters,” – SD2, changed minimum value to “0.46”, and changed maximum value to “0.54”. – SD3, changed minimum value to “0.46”, and changed maximum value to “0.54”. – SD2 (parameter Clock High Time), parameter name corrected to SD3. – SD5, changed maximum value to “0.74”. • Section 4.10.5, “HS200 Mode Timing Parameters,” Added this new section. • Section 4.10.14, “USB PHY Parameters,” Added new text to second paragraph “USB Host with the amendments below…” • Table 63, "Interfaces Allocation During Boot USDHC-1–USDHC-4 row, replaced existing text with “Refer to the table “SD/MMC…” • Table 65, "13 x 13 mm Supplies Contact Assignment,” – GPANAIO: changed remark from “Analog pad” to “Analog output for NXP use…” – ZQPAD: changed remark to “Connect ZQPAD to…” • Table 66, "13 x 13 mm Functional Contact Assignments,” DRAM_SDCLK_0, corrected “Input” to “Output” and Value to “0”. • Section 6.2.2, “13 x 13 mm Ground, Power, Sense, Not Connected, and Reference Contact Assignments,” Added new text “For most of the signals…” after Table 66. • Table 68, "13 x 13 mm, 0.5 mm Pitch Ball Map,” ball AD6 name corrected to “DRAM_D18”.

Table 70. i.MX 6SoloLite Data Sheet Document Revision History (continued)

Rev. Number	Date	Substantive Change(s)
Rev. 3	02/2014	• Section 1.2,Feature description for: - Camera sensors: Added to Parallel Camera port “and up to 66 MHz peak”. - Miscellaneous IPs and interfaces; Changed from: “Three I2S/SSI/AC97 supported,” to “SSI block is capable of supporting audio sample frequencies up to 192 kHZ stereo inputs and outputs with I2S mode.” • Table 2, Modules List: UART1–5, Brief Description; Changed bullet about programmable baud rate to “up to 5 MHz.” • Table 2, Modules List: uSDHC1–4, Brief Description; Changed bullet about Fully compliant with SD command/response to include “and SDXC cards up to 2TB.” • Table 9, operating range for GPIO supplies: Added NVCC_1P2V min/typ/max values for LPDDR2, DDR3L, DDR3. • Section 4.1.4, External Clock Sources; added Note, “The internal oscillator may run high …” • Table 11, Maximum Supply currents: Added row; NVCC_LVDS2P5. • Section 4.2.1, Power-Up Sequence: reworded third bulleted item regarding POR control. • Section 4.2.1, Power-Up Sequence: removed Note. • Section 4.5.1, OSC24K, first paragraph corrected ‘*powered from*’ signal from NVCC_1P2 to NVCC_1P2V. • Section 4.5.2, OSC32K, Changed second paragraph and added CAUTION. • Table 31 Reset Timing Parameters, changed Unit from XTALI cycle to XTALOSC_RTC_XTALI cycle. • Section 4.5.2, External Interface Module; enhanced wording to first paragraph to describe operating frequency for data transfers, and to explain register settings are valid for entire range of frequencies. • Table 34, EIM Bus Timing Parameters; reworded footnotes for clarity.
Rev. 3.0	02/2014	• Table 45, DDR3 Write Cycle; changed footnote 3, outputs from “DDR_VREF” to “DRAM_VREF”. • Figure 25, LPDDR2 Command and Address Timing Diagram; changed signal name from “DRAM_CAS_B” to “DRAM_ADDRxx”. • Table 47, LPDDR2 Timing Parameters; changed footnote 2, outputs from “DDR_VREF” to “DRAM_VREF”. • Table 48, LPDDR2 Write Cycle; changed footnote 3, outputs from “DDR_VREF” to “DRAM_VREF”. • Table 49, LPDDR2 Read Cycle; changed footnote 3, outputs from “DDR_VREF” to “DRAM_VREF”. • Table 65, 13x13mm Supplies Contact Assignment; changed Supply Rail Name “DDR_VREF” to “DRAM_VREF”. • Table 65, 13x13mm Supplies Contact Assignment; changed ZQPAD ball position from “AE17” to “H2”. • Table 68, 13x13mm Functional Contact Assignment; Changed the following signals to include active-low “_B” in the Default Function column: DRAM_CAS_B; DRAM_CS0_B; DRAM_CS1_B; DRAM_RAS_B; DRAM_RESET_B. • Table 68, 13x13mm Functional Contact Assignment; Changed the Ball Name of DRAM_WE_B to DRAM_SDWE. • Table 68, 13 x 13 mm, 0.5 mm Pitch Ball Map; Y19, changed from “ON/OFF” to “NVCC_PLL. • Table 68, 13 x 13 mm, 0.5 mm Pitch Ball Map; W18, changed from “TEST_MODE” to “ON/OFF”. • Table 68, 13 x 13 mm, 0.5 mm Pitch Ball Map; U15, changed from “NVCC_PLL” to “TEST_MODE”. • Table 68, 13 x 13 mm, 0.5 mm Pitch Ball Map; U11 & U10, changed from “NHVCC_3V3” to “NVCC33_IO”.
Rev. 2.2	8/2013	Substantive Changes are as follows: • Section 1.2, “Features,” corrected value of OCRAM from 256KB to 128KB: The SoC-level memory system consists of the following additional components: — Boot ROM, including HAB (96 KB) — Internal multimedia / shared, fast access RAM (OCRAM, 128 KB) • Removed parenthetical statement (input slope <= 5 ns) from Table 31, “Reset Timing Parameters” CC1: Duration of POR_B to be qualified as valid. The parenthetical statement was a typographical error and is not a specification requirement for this device.