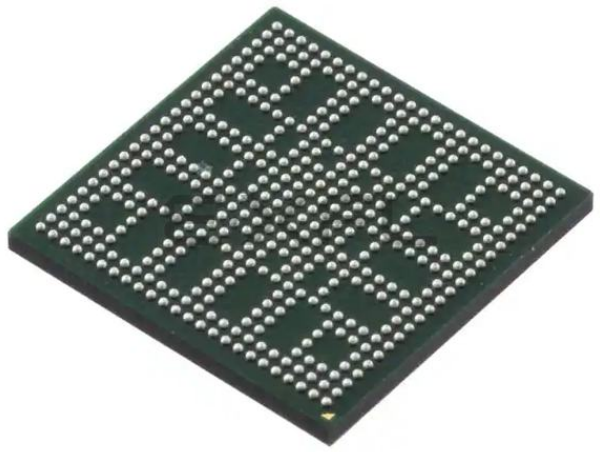

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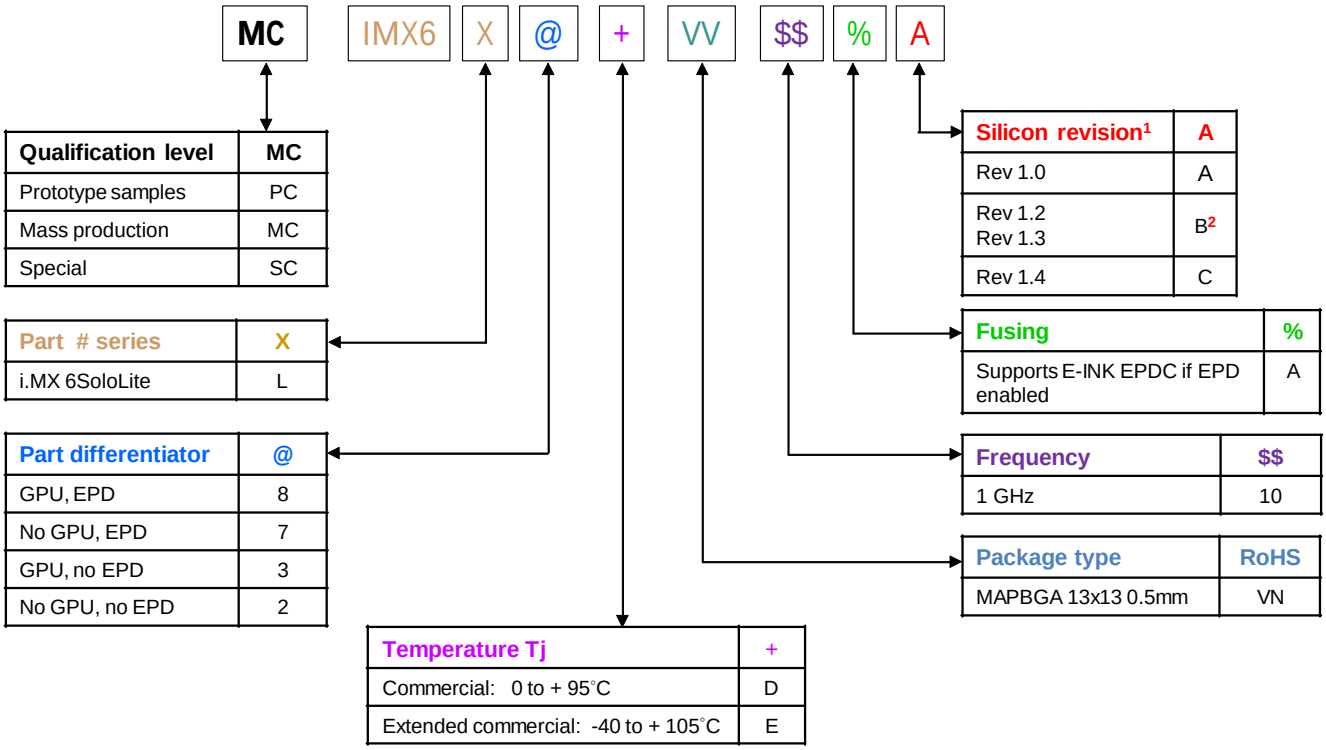
Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, LVDDR3, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + PHY (3)
Voltage - I/O	1.2V, 1.8V, 3.0V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	432-TFBGA
Supplier Device Package	432-MAPBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6l2evn10abr



1. See the nxp.com\imx6series Web page for latest information on the available silicon revision.
2. Rev 1.2 (USB_ANALOG_DIGPROG register = 0x0062_0002)
   Rev 1.3 (USB_ANALOG_DIGPROG register = 0x0062_0003)

Figure 1. Part Number Nomenclature—i.MX 6SoloLite

1.2 Features

The i.MX 6SoloLite processor is based on ARM Cortex-A9 MPCore multicore processor, which has the following features:

- ARM Cortex-A9 MPCore CPU processor (with TrustZone)
- The core configuration is symmetric, where each core includes:
  - 32 KByte L1 Instruction Cache
  - 32 KByte L1 Data Cache
  - Private Timer and Watchdog
  - Cortex-A9 NEON MPE (Media Processing Engine) co-processor

The ARM Cortex-A9 MPCore complex includes:

- General Interrupt Controller (GIC) with 128 interrupt support
- Global Timer
- Snoop Control Unit (SCU)
- 256 KB unified I/D L2 cache
- Two Master AXI (64-bit) bus interfaces output of L2 cache
- Frequency of the core (including NEON and L1 cache) as per Table 9, "Operating Ranges," on page 21

3.1 Special Signal Considerations

Table 3 lists special signal considerations for the i.MX 6SoloLite processor. The signal names are listed in alphabetical order.

The package contact assignments can be found in Section 6, "Package Information and Contact Assignments." Signal descriptions are provided in the *i.MX 6SoloLite reference manual* (IMX6SLRM).

Table 3. Special Signal Considerations

Signal Name	Remarks
XTALOSC_CLK1_P/ XTALOSC_CLK1_N	One general purpose differential high speed clock Input/output is provided. It could be used to: • To feed external reference clock to the PLLs and further to the modules inside SoC, for example as alternate reference clock for Audio interfaces, etc. • To output internal SoC clock to be used outside the SoC as either reference clock or as a functional clock for peripherals. See the i.MX 6SoloLite reference manual for details on the respective clock trees. The clock inputs/outputs are LVDS differential pairs compatible with TIA/EIA-644 standard, the maximum clock out frequency range supported is 528 MHz. Alternatively one may use single ended signal to drive XTALOSC_CLK1_P input. In this case, the corresponding XTALOSC_CLK1_N input should be tied to the constant voltage level equal 1/2 of the input signal swing. Termination should be provided in case of high frequency signals. See LVDS pad electrical specification for further details. After initialization, the XTALOSC_CLK1 input/output could be disabled (if not used). If unused, the XTALOSC_CLK1_N/P pair can remain unconnected.
DRAM_VREF	When using DRAM_VREF with DDR I/O, the nominal reference voltage must be half of the NVCC_DRAM supply. The user must tie DRAM_VREF to a precision external resistor divider. Use a 1 kΩ 0.5% resistor to GND and a 1 kΩ 0.5% resistor to NVCC_DRAM. Shunt each resistor with a closely-mounted 0.1 µF capacitor. To reduce supply current, a pair of 1.5 kΩ 0.1% resistors can be used. Using resistors with recommended tolerances ensures the ± 2% DRAM_VREF tolerance (per the DDR3 specification) is maintained when four DDR3 ICs plus the i.MX 6SoloLite are drawing current on the resistor divider. It is recommended to use regulated power supply for "big" memory configurations (more that eight devices).
JTAG_*nnnn*	The JTAG interface is summarized in Table 4. Use of external resistors is unnecessary. However, if external resistors are used, the user must ensure that the on-chip pull-up/down configuration is followed. For example, do not use an external pull down on an input that has on-chip pull-up.
	JTAG_TDO is configured with a keeper circuit such that the floating condition is eliminated if an external pull resistor is not present. An external pull resistor on JTAG_TDO is detrimental and should be avoided.
	JTAG_MODE must be externally connected to GND for normal operation. Termination to GND through an external pull-down resistor (such as 1 kΩ) is allowed. JTAG_MODE set to high configures the JTAG interface to mode compliant with IEEE1149.1 standard. JTAG_MODE set to low configures the JTAG interface for common Software debug adding all the system TAPs to the chain.
NC	These signals are No Connect (NC) and must remain unconnected by the user.
SRC_ONOFF	In normal mode may be connected to ONOFF button (de-bouncing provided at this input). Internally this pad is pulled up. A short duration (<5s) connection to GND in OFF mode causes the internal power management state machine to change the state to ON. In ON mode, a short duration connection to GND generates interrupt (intended to initiate a software controllable power down). A long duration (above ~5s) connection to GND causes "forced" OFF.
SRC_POR_B	This cold reset negative logic input resets all modules and logic in the IC.

Table 9. Operating Ranges (continued)

Parameter Description	Symbol	Min	Typ	Max[1]	Unit	Comment
GPIO supplies[6]	NVCC33_IO	2.8	3.0	3.3	V	Worst case, assuming all SOC I/O operating at 1.8V. NVCC33_IO must always be greater than NVCC18_IO.
	NVCC18_IO	1.62	1.8	1.98	V	—
	NVCC_1P2V	1.14	1.2	1.3	V	—
Junction temperature	T_J	0	—	95	°C	Commercial See *i.MX 6SoloLite Product Lifetime Usage Estimates Application Note*, AN4726, for information on product lifetime (power-on years) for this processor.
Junction temperature	T_J	-40	—	105	—	Extended commercial See *i.MX 6SoloLite Product Lifetime Usage Estimates Application Note*, AN4726, for information on product lifetime (power-on years) for this processor.

1 Applying the maximum voltage results in maximum power consumption and heat generation. NXP recommends a voltage set point = (Vmin + the supply tolerance). This results in an optimized power/speed ratio.

2 VDD_ARM_IN and VDD_SOC_IN must be at least 125 mV higher than the LDO Output Set Point for correct voltage regulation.

3 VDD_SOC_CAP and VDD_PU_CAP must be equal.

4 VDD_SOC and VDD_PU output voltage must be set to this rule: VDD_ARM - VDD_SOC / VDD_PU < 50mV.

5 While setting VDD_SNVS_IN voltage with respect to Charging Currents and RTC, refer to Hardware Development Guide for i.MX 6Dual, 6Quad, 6Solo, 6DualLite Families of Applications Processors (IMX6DQ6SDLHDG).

6 All digital I/O supplies (NVCC_xxxx) must be powered under normal conditions whether the associated I/O pins are in use or not, and associated I/O pins need to have a pull-up or pull-down resistor applied to limit any floating gate current.

4.1.4 External Clock Sources

Each i.MX 6SoloLite processor has two external input system clocks: a low frequency (RTC_XTALI) and a high frequency (XTALI).

The RTC_XTALI is used for low-frequency functions. It supplies the clock for wake-up circuit, power-down real time clock operation, and slow system and watchdog counters. The clock input can be connected to either an external oscillator or a crystal using the internal oscillator amplifier. Additionally, there is an internal ring oscillator, which can substitute the RTC_XTALI, in case accuracy is not important.

The system clock input XTALI is used to generate the main system clock. It supplies the PLLs and other peripherals. The system clock input can be connected to either an external oscillator or a crystal using the internal oscillator amplifier.

NOTE

The internal RTC oscillator does not provide an accurate frequency and is affected by process, voltage, and temperature variations. NXP strongly recommends using an external crystal as the RTC_XTALI reference. If the internal oscillator is used instead, careful consideration must be given to the timing implications on all of the SoC modules dependent on this clock.

Table 10 shows the interface frequency requirements.

Table 10. External Input Clock Frequency

Parameter Description	Symbol	Min	Typ	Max	Unit
RTC_XTALI Oscillator[1, 2]	f_{ckil}	—	32.768[(see 3)]/32.0	—	kHz
XTALI Oscillator[4, 2]	f_{xtal}	—	24	—	MHz

1 External oscillator or a crystal with internal oscillator amplifier.

2 The required frequency stability of this clock source is application dependent. For recommendations, see Hardware Development Guide for i.MX 6Dual, 6Quad, 6Solo, 6DualLite Families of Applications Processors (IMX6DQ6SDLHDG).

3 Recommended nominal frequency 32.768 kHz.

4 External oscillator or a fundamental frequency crystal with internal oscillator amplifier.

The typical values shown in Table 10 are required for use with NXP BSPs to ensure precise time keeping and USB operation. For RTC_XTALI operation, two clock sources are available:

- On-chip 40 kHz ring oscillator: This clock source has the following characteristics:
  - Approximately 25 µA more Idd than crystal oscillator
  - Approximately ±50% tolerance
  - No external component required
  - Starts up quicker than 32 kHz crystal oscillator
- External crystal oscillator with on-chip support circuit
  - At power up, ring oscillator is utilized. After crystal oscillator is stable, the clock circuit switches over to the crystal oscillator automatically.
  - Higher accuracy than ring oscillator
  - If no external crystal is present, then the ring oscillator is utilized

The decision to choose a clock source should be taken based on real-time clock use and precision time-out.

4.1.5 Maximum Supply Currents

The Power Virus numbers shown in Table 11 represent a use case designed specifically to show the maximum current consumption possible. All cores are running at the defined maximum frequency and are limited to L1 cache accesses only to ensure no pipeline stalls. Although a valid condition, it would have a very limited practical use case, if at all, and be limited to an extremely low duty cycle unless the intention was to specifically show the worst case power consumption.

The NXP power management IC, MMPF0100xxxx, which is targeted for the i.MX 6 series processor family, supports the power consumption shown in Table 11, however a robust thermal design is required for the increased system power dissipation.

See the *i.MX 6SoloLite Power Consumption Measurement Application Note* (AN4580) for more details on typical power consumption under various use case definitions.

Table 21. DVGPIO I/O DC Parameters

Parameter	Symbol	Test Conditions	Min	Max	Unit
High-level output voltage[1]	Voh	Ioh = -0.1 mA (DSE[2] = 001, 010) Ioh = -1 mA (DSE = 011, 100, 101, 110, 111)	OVDD – 0.15	—	V
Low-level output voltage[1]	Vol	Iol = 0.1 mA (DSE[2] = 001, 010) Iol = 1mA (DSE = 011, 100, 101, 110, 111)	—	0.15	V
High-Level DC input voltage [1, 3]	Vih	—	0.7 × OVDD	OVDD	V
Low-Level DC input voltage [1, 3]	Vil	—	0	0.3 × OVDD	V
Input Hysteresis	Vhys	OVDD = 1.8 V OVDD = 3.3 V	0.25	—	V
Schmitt trigger VT+, [3, 4]	VT+	—	0.5 × OVDD	—	V
Schmitt trigger VT–, [3, 4]	VT–	—	—	0.5 × OVDD	V
Input current (no pull-up/down)	Iin	Vin = OVDD or 0	-1.25	1.25	µA
Input current (22 kΩ pull-up)	Iin	Vin = 0 V Vin = OVDD	—	212 1	µA
Input current (47 kΩ pull-up)	Iin	Vin = 0 V Vin = OVDD	—	100 1	µA
Input current (100 kΩ pull-up)	Iin	Vin = 0 V Vin= OVDD	—	48 1	µA
Input current (100 kΩ pull-down)	Iin	Vin = 0 V Vin = OVDD	—	1 48	µA
Keeper circuit resistance	Rkeep	Vin = 0.3 x OVDD Vin = 0.7 x OVDD	105	205	kΩ

1 Overshoot and undershoot conditions (transitions above OVDD and below GND) on switching pads must be held below 0.6 V, and the duration of the overshoot/undershoot must not exceed 10% of the system clock cycle. Overshoot/ undershoot must be controlled through printed circuit board layout, transmission line impedance matching, signal line termination, or other methods. Non-compliance to this specification may affect device reliability or cause permanent damage to the device.

2 DSE is the Drive Strength Field setting in the associated IOMUX control register.

3 To maintain a valid level, the transition edge of the input must sustain a constant slew rate (monotonic) from the current DC level through to the target DC level, Vil or Vih. Monotonic input transition time is from 0.1 ns to 1 s.

4 Hysteresis of 250 mV is guaranteed over all operating conditions when hysteresis is enabled.

4.6.3 DDR I/O DC Parameters

The DDR I/O pads support LPDDR2 and DDR3 operational modes.

4.6.3.1 LPDDR2 Mode I/O DC Parameters

The parameters in Table 22 are guaranteed per the operating ranges in Table 9, unless otherwise noted. For details on supported DDR memory configurations, see Section 4.9.4, “Multi-Mode DDR Controller (MMDC)”.

4.7.2 DDR I/O AC Parameters

Table 26 shows the AC parameters for DDR I/O operating in LPDDR2 mode. For details on supported DDR memory configurations, see Section 4.9.4, "Multi-Mode DDR Controller (MMDC)".

Table 26. DDR I/O LPDDR2 Mode AC Parameters[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
AC input logic high	Vih(ac)	—	Vref + 0.22	—	OVDD	V
AC input logic low	Vil(ac)	—	0	—	Vref – 0.22	V
AC differential input high voltage[2]	Vidh(ac)	—	0.44	—	—	V
AC differential input low voltage	Vidl(ac)	—	—	—	0.44	V
Input AC differential cross point voltage[3]	Vix(ac)	Relative to Vref	-0.12	—	0.12	V
Over/undershoot peak	Vpeak	—	—	—	0.35	V
Over/undershoot area (above OVDD or below OVSS)	Varea	400 MHz	—	—	0.3	V-ns
Single output slew rate, measured between Vol (ac) and Voh (ac)	tsr	50 Ω to Vref. 5 pF load. Drive impedance = 4 0 Ω ±30%	1.5	—	3.5	V/ns
		50 Ω to Vref. 5pF load. Drive impedance = 60 Ω ±30%	1	—	2.5	
Skew between pad rise/fall asymmetry + skew caused by SSN	t_{SKD}	clk = 400 MHz	—	—	0.1	ns

1 Note that the JEDEC LPDDR2 specification (JESD209_2B) supersedes any specification in this document.

2 Vid(ac) specifies the input differential voltage |Vtr – Vcp| required for switching, where Vtr is the "true" input signal and Vcp is the "complementary" input signal. The Minimum value is equal to Vih(ac) – Vil(ac).

3 The typical value of Vix(ac) is expected to be about 0.5 × OVDD. and Vix(ac) is expected to track variation of OVDD. Vix(ac) indicates the voltage at which differential input signal must cross.

Table 27 shows the AC parameters for DDR I/O operating in DDR3 mode.

Table 27. DDR I/O DDR3 Mode AC Parameters[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
AC input logic high	Vih(ac)	—	Vref + 0.175	—	OVDD	V
AC input logic low	Vil(ac)	—	0	—	Vref – 0.175	V
AC differential input voltage[2]	Vid(ac)	—	0.35	—	—	V
Input AC differential cross point voltage[3]	Vix(ac)	Relative to Vref	Vref – 0.15	—	Vref + 0.15	V
Over/undershoot peak	Vpeak	—	—	—	0.4	V
Over/undershoot area (above OVDD or below OVSS)	Varea	400 MHz	—	—	0.5	V-ns

4.9.3.2 General EIM Timing-Synchronous Mode

Figure 10, Figure 11, and Table 34 specify the timings related to the EIM module. All EIM output control signals may be asserted and deasserted by an internal clock synchronized to the BCLK rising edge according to corresponding assertion/negation control fields.

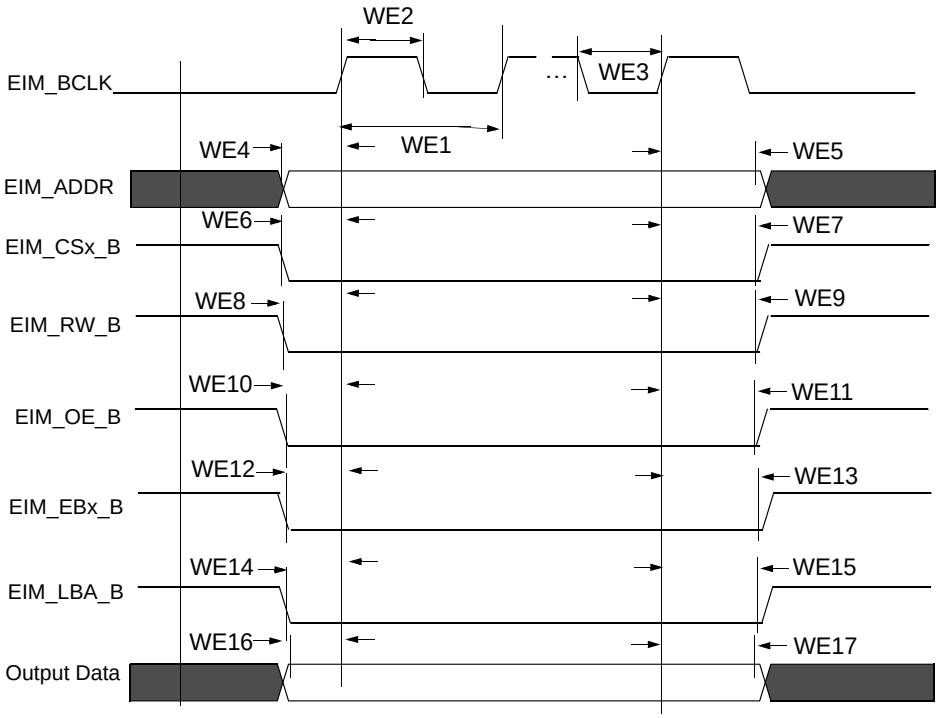


Figure 10. EIM Output Timing Diagram

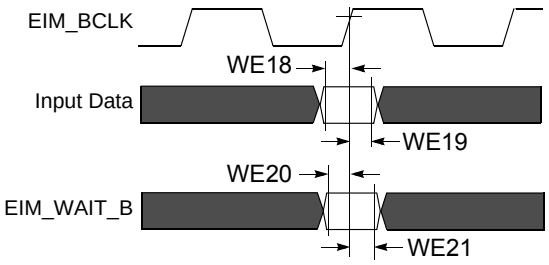


Figure 11. EIM Input Timing Diagram

4.9.3.3 Examples of EIM Synchronous Accesses

Table 34. EIM Bus Timing Parameters

ID	Parameter	Min[1]	Max[1]	Unit
WE1	EIM_BCLK cycle time[2]	t × (k+1)	—	ns
WE2	EIM_BCLK high level width	0.4 × t × (k+1)	—	ns
WE3	EIM_BCLK low level width	0.4 × t × (k+1)	—	ns
WE4	Clock rise to address valid	-0.5 × t × (k+1) -1.25	-0.5 × t × (k+1) +2.25	ns

Figure 12 to Figure 15 provide few examples of basic EIM accesses to external memory devices with the timing parameters mentioned previously for specific control parameters settings.

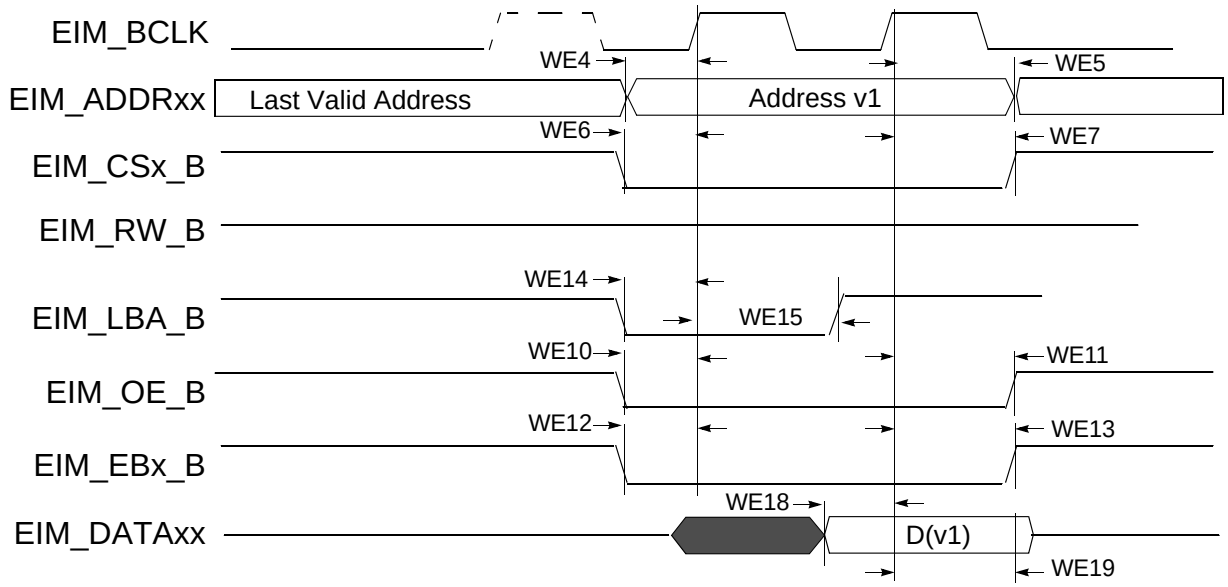


Figure 12. Synchronous Memory Read Access, WSC=1

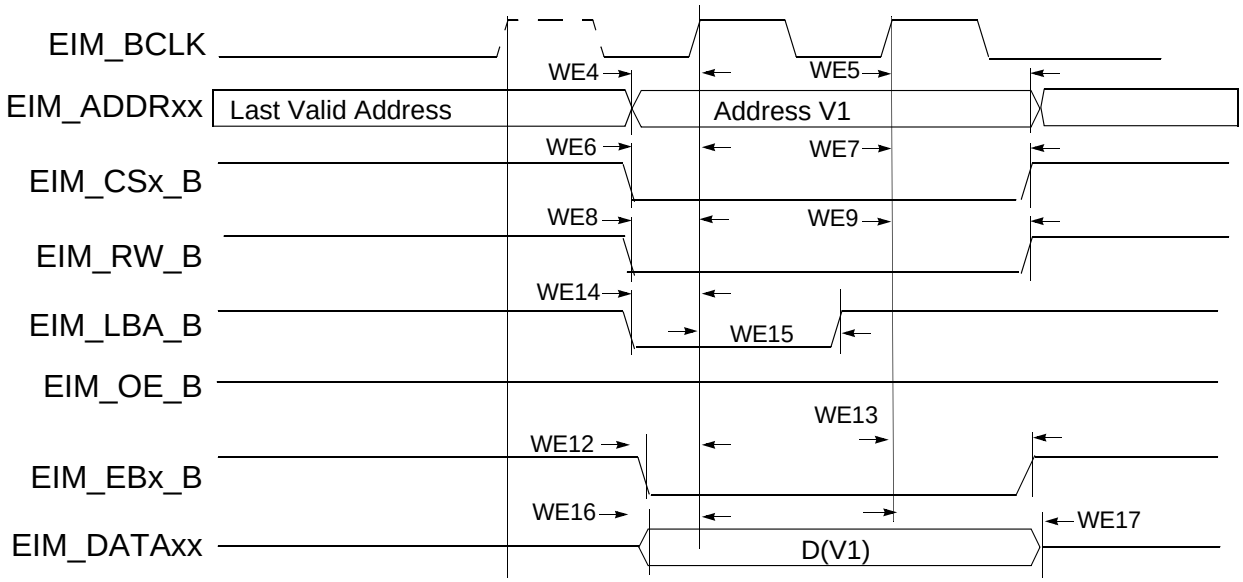


Figure 13. Synchronous Memory, Write Access, WSC=1, WBEA=0, and WADVN=0

4.10.4.3 SDR50/SDR104 AC Timing Parameters

Figure 29 depicts the timing of SDR50/SDR104, and Table 43 lists the SDR50/SDR104 timing characteristics.

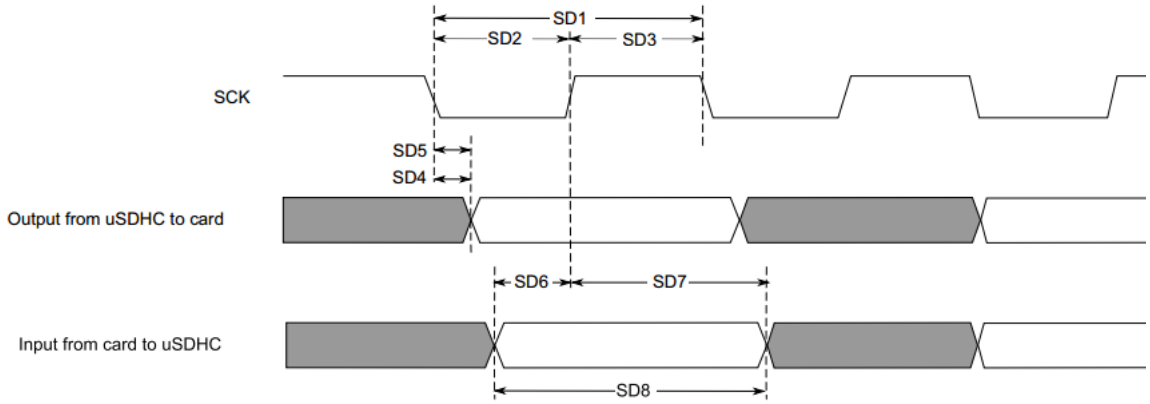


Figure 29. SDR50/SDR104 Timing Diagram

Table 43. SDR50/SDR104 Interface Timing Parameters

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency Period	t_{CLK}	4.8	—	ns
SD2	Clock Low Time	t_{CL}	$0.46 \times t_{CLK}$	$0.54 \times t_{CLK}$	ns
SD3	Clock High Time	t_{CH}	$0.46 \times t_{CLK}$	$0.54 \times t_{CLK}$	ns
uSDHC Output/Card Inputs SD_CMD, SD_DATAx in SDR50 (Reference to CLK)					
SD4	uSDHC Output Delay	t_{OD}	–3	1	ns
uSDHC Output/Card Inputs SD_CMD, SD_DATAx in SDR104 (Reference to CLK)					
SD5	uSDHC Output Delay[1]	t_{OD}	–1.6	0.74	ns
uSDHC Input/Card Outputs SD_CMD, SD_DATAx in SDR50 (Reference to CLK)					
SD6	uSDHC Input Setup Time	t_{ISU}	2.5	—	ns
SD7	uSDHC Input Hold Time	t_{IH}	1.5	—	ns
uSDHC Input/Card Outputs SD_CMD, SD_DATAx in SDR104 (Reference to CLK)[2]					
SD8	Card Output Data Window	t_{ODW}	$0.5 \times t_{CLK}$	—	ns

1 If using KEY_COL1, KEY_ROW1, KEY_COL2 and KEY_ROW2 for SD3_DATA4–SD3_DATA7, note the difference in timing: t_{od} minimum is -1.1 and t_{od} maximum is 1.5.

2 Data window in SDR100 mode is variable.

Table 54. SSI Receiver Timing with External Clock

ID	Parameter	Min	Max	Unit
External Clock Operation				
SS22	AUDx_TXC/AUDx_RXC clock period	81.4	—	ns
SS23	AUDx_TXC/AUDx_RXC clock high period	36	—	ns
SS24	AUDx_TXC/AUDx_RXC clock rise time	—	6.0	ns
SS25	AUDx_TXC/AUDx_RXC clock low period	36	—	ns
SS26	AUDx_TXC/AUDx_RXC clock fall time	—	6.0	ns
SS28	AUDx_RXC high to AUDx_TXFS (bl) high	–10	15.0	ns
SS30	AUDx_RXC high to AUDx_TXFS (bl) low	10	—	ns
SS32	AUDx_RXC high to AUDx_TXFS (wl) high	–10	15.0	ns
SS34	AUDx_RXC high to AUDx_TXFS (wl) low	10	—	ns
SS35	AUDx_TXC/AUDx_RXC External AUDx_TXFS rise time	—	6.0	ns
SS36	AUDx_TXC/AUDx_RXC External AUDx_TXFS fall time	—	6.0	ns
SS40	AUDx_RXD setup time before AUDx_RXC low	10	—	ns
SS41	AUDx_RXD hold time after AUDx_RXC low	2	—	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TXC/RXC=0) and a non-inverted frame sync (TXFS/RXFS=0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal TXC/RXC and/or the frame sync TXFS/RXFS shown in the tables and in the figures.
- All timings are on AUDMUX Pads when SSI is being used for data transfer.
- The terms, WL and BL, refer to Word Length(WL) and Bit Length(BL).
- For internal Frame Sync operation using external clock, the FS timing is same as that of TXD (for example, during AC97 mode of operation).

UART IrDA Mode Receiver

Figure 47 depicts the UART IrDA mode receive timing, with 8 data bit/1 stop bit format. Table 59 lists the receive timing characteristics.

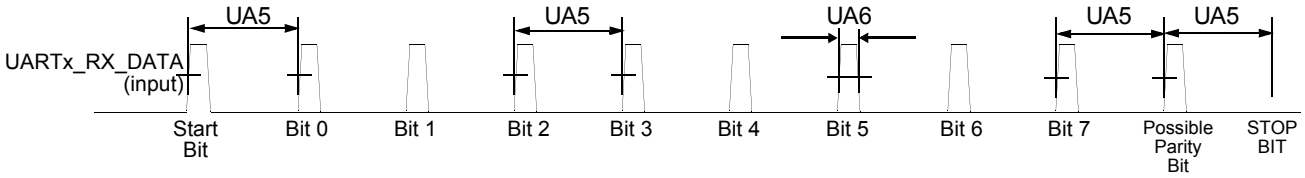


Figure 47. UART IrDA Mode Receive Timing Diagram

Table 59. IrDA Mode Receive Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA5	Receive Bit Time[1] in IrDA mode	t_{RIRbit}	$1/F_{baud\_rate}$[2] – $1/(16 \times F_{baud\_rate})$	$1/F_{baud\_rate} + 1/(16 \times F_{baud\_rate})$	—
UA6	Receive IR Pulse Duration	$t_{RIRpulse}$	1.41 µs	$(5/16) \times (1/F_{baud\_rate})$	—

1 The UART receiver can tolerate $1/(16 \times F_{baud\_rate})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16 \times F_{baud\_rate})$.

2 F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

4.10.13 USB HSIC Timing Parameters

This section describes the electrical information of the USB HSIC port.

NOTE

HSIC is the DDR signal, the following timing parameters are for both rising and falling edge.

4.10.13.1 Transmit Timing Parameters

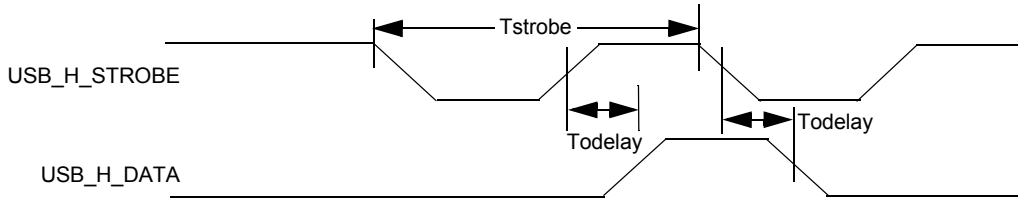


Figure 48. USB HSIC Transmit Timing Diagram

Table 60. USB HSIC Transmit Timing Parameters

Name	Parameter	Min	Max	Unit	Comment
Tstrobe	Strobe period	4.166	4.167	ns	—
Todelay	Data output delay time	550	1350	ps	Measured at 50% point
Tslew	Strobe/data rising/falling time	0.7	2	V/ns	Averaged from 30% – 70% points

4.10.13.2 Receive Timing Parameters

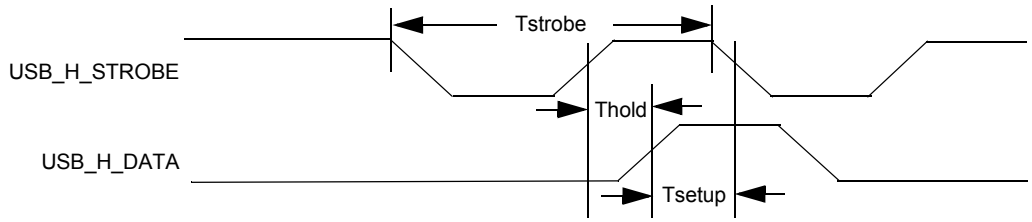


Figure 49. USB HSIC Receive Timing Diagram

Table 61. USB HSIC Receive Timing Parameters[1]

Name	Parameter	Min	Max	Unit	Comment
Tstrobe	Strobe period	4.166	4.167	ns	—
Thold	Data hold time	300	—	ps	Measured at 50% point
Tsetup	Data setup time	365	—	ps	Measured at 50% point
Tslew	Strobe/data rising/falling time	0.7	2	V/ns	Averaged from 30% – 70% points

1 The timings in the table are guaranteed when:
—AC I/O voltage is between 0.9x to 1x of the I/O supply
—DDR_SEL configuration bits of the I/O are set to (10)b

4.10.14 USB PHY Parameters

This section describes the USB-OTG PHY and the USB Host port PHY parameters.
The USB PHY meets the electrical compliance requirements defined in the Universal Serial Bus Revision 2.0 OTG, USB Host with the amendments below (On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification is not applicable to Host port).

- USB ENGINEERING CHANGE NOTICE
  - Title: 5V Short Circuit Withstand Requirement Change
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- Errata for USB Revision 2.0 April 27, 2000 as of 12/7/2000
- USB ENGINEERING CHANGE NOTICE
  - Title: Pull-up/Pull-down resistors
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- USB ENGINEERING CHANGE NOTICE
  - Title: Suspend Current Limit Changes
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- USB ENGINEERING CHANGE NOTICE
  - Title: USB 2.0 Phase Locked SOFs
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification
  - Revision 2.0 plus errata and ecn June 4, 2010

- Battery Charging Specification (available from USB-IF)
  - Revision 1.2, December 7, 2010
  - Portable device only.

Table 66. 13 x 13 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group[1]	Ball Type	Out of Reset Condition[2]			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value[3]
EPDC_SDCE1	A10	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO1_GPIO[28]	Input	Keeper
EPDC_SDCE2	B9	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO1_GPIO[29]	Input	Keeper
EPDC_SDCE3	A9	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO1_GPIO[30]	Input	Keeper
EPDC_SDCLK	B10	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO1_GPIO[23]	Input	Keeper
EPDC_SDLE	B8	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO1_GPIO[24]	Input	Keeper
EPDC_SDOE	E7	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO1_GPIO[25]	Input	Keeper
EPDC_SDSHR	F7	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO1_GPIO[26]	Input	Keeper
EPDC_VCOM0	C7	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[3]	Input	Keeper
EPDC_VCOM1	D7	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[4]	Input	Keeper
FEC_CRS_DV	AC9	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO4_GPIO[25]	Input	Keeper
FEC_MDC	AA7	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO4_GPIO[23]	Input	Keeper
FEC_MDIO	AB7	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO4_GPIO[20]	Input	Keeper
FEC_REF_CLK	W10	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO4_GPIO[26]	Input	Keeper
FEC_RX_ER	AD9	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO4_GPIO[19]	Input	Keeper
FEC_RXD0	AA10	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO4_GPIO[17]	Input	Keeper
FEC_RXD1	AC10	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO4_GPIO[18]	Input	Keeper
FEC_TX_CLK	AC8	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO4_GPIO[21]	Input	Keeper
FEC_TX_EN	AD10	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO4_GPIO[22]	Input	Keeper
FEC_TXD0	Y10	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO4_GPIO[24]	Input	Keeper
FEC_TXD1	W11	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO4_GPIO[16]	Input	Keeper
HSIC_DAT	AA6	NVCC_1P2V	DDR	—	USB_H_DATA	Input	PD (100K)
HSIC_STROBE	AB6	NVCC_1P25	DDR	—	USB_H_STROBE	Input	PD (100K)

Table 66. 13 x 13 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group[1]	Ball Type	Out of Reset Condition[2]			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value[3]
I2C1_SCL	AC13	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[12]	Input	Keeper
I2C1_SDA	AD13	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[13]	Input	Keeper
I2C2_SCL	E18	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[14]	Input	Keeper
I2C2_SDA	D18	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[15]	Input	Keeper
JTAG_MOD	Y14	NVCC33_IO	GPIO	ALT5	JTAG_MODE	—	PU (100K)
JTAG_TCK	AA14	NVCC33_IO	GPIO	ALT5	JTAG_TCK	—	PU (47K)
JTAG_TDI	W14	NVCC33_IO	GPIO	ALT5	JTAG_TDI	—	PU (47K)
JTAG_TDO	W15	NVCC33_IO	GPIO	ALT5	JTAG_TDO	—	Keeper
JTAG_TMS	Y15	NVCC33_IO	GPIO	ALT5	JTAG_TMS	—	PU (47K)
JTAG_TRSTB	AA15	NVCC33_IO	GPIO	ALT5	JTAG_TRSTB	—	PU (47K)
KEY_COL0	G23	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[24]	Input	Keeper
KEY_COL1	F23	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[26]	Input	Keeper
KEY_COL2	E23	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[28]	Input	Keeper
KEY_COL3	E22	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[30]	Input	Keeper
KEY_COL4	E20	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO4_GPIO[0]	Input	Keeper
KEY_COL5	D24	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO4_GPIO[2]	Input	Keeper
KEY_COL6	D22	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO4_GPIO[4]	Input	Keeper
KEY_COL7	C23	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO4_GPIO[6]	Input	Keeper
KEY_ROW0	G24	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[25]	Input	Keeper
KEY_ROW1	F24	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[27]	Input	Keeper
KEY_ROW2	E24	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[29]	Input	Keeper
KEY_ROW3	E21	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[31]	Input	Keeper
KEY_ROW4	E19	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO4_GPIO[1]	Input	Keeper
KEY_ROW5	D23	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO4_GPIO[3]	Input	Keeper

Table 66. 13 x 13 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group[1]	Ball Type	Out of Reset Condition[2]			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value[3]
LCD_DAT5	U21	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[25]	Input	Keeper
LCD_DAT6	U23	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[26]	Input	Keeper
LCD_DAT7	U24	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[27]	Input	Keeper
LCD_DAT8	T23	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[28]	Input	Keeper
LCD_DAT9	T24	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[29]	Input	Keeper
LCD_ENABLE	J24	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[16]	Input	Keeper
LCD_HSYNC	H23	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[17]	Input	Keeper
LCD_RESET	H24	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[19]	Input	Keeper
LCD_VSYNC	J23	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[18]	Input	Keeper
ONOFF	W18	VDD_SNVS_IN	GPIO		SRC_ONOFF	Input	PU (100K)
PMIC_ON_REQ	AD15	VDD_SNVS_IN	GPIO	ALT0	SNVS_PMIC_ON_REQ	Output	Open Drain with PU (100K)
PMIC_STBY_REQ	AD16	VDD_SNVS_IN	GPIO	ALT0	CCM_PMIC_STBY_REQ	Output	0
POR_B	AC16	VDD_SNVS_IN	GPIO	ALT0	SRC_POR_B	Input	PU (100K)
PWM1	Y7	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[23]	Input	Keeper
REF_CLK_24M	AC14	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[21]	Input	Keeper
REF_CLK_32K	AD14	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[22]	Input	Keeper
RTC_XTALI	AB19	VDD_SNVS_CAP	—	—	RTC_XTALI	—	—
RTC_XTALO	AA19	VDD_SNVS_CAP	—	—	RTC_XTALO	—	—
SD1_CLK	B20	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO5_GPIO[15]	Input	Keeper
SD1_CMD	B21	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO5_GPIO[14]	Input	Keeper
SD1_DAT0	B23	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO5_GPIO[11]	Input	Keeper
SD1_DAT1	A23	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO5_GPIO[8]	Input	Keeper
SD1_DAT2	C22	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO5_GPIO[13]	Input	Keeper

Table 68. 13 x 13 mm, 0.5 mm Pitch Ball Map (continued)

	1	2	3	4	5	6	7	8
A	GND	DRAM_SDQS3_B	DRAM_D24	GND	DRAM_D27	DRAM_D29	GND	DRAM_D31
B	DRAM_D14	DRAM_D15	DRAM_SDQS3	DRAM_D25	DRAM_D26	DRAM_D28	DRAM_D30	EPDC_SDLE
C	DRAM_D12	DRAM_D13	DRAM_DQM3	**NC**	**NC**	GND	EPDC_VCOM0	**NC**
D	GND	GND	DRAM_D11	**NC**	**NC**	DRAM_RESET	EPDC_VCOM1	**NC**
E	DRAM_D9	DRAM_D8	DRAM_D10	DRAM_SDODT1	GND	NVCC_DRAM	EPDC_SDOE	**NC**
F	DRAM_SDQS1	DRAM_SDQS1_B	**NC**	**NC**	**NC**	**NC**	EPDC_SDSHR	**NC**
G	GND	DRAM_DQM1	**NC**	**NC**	**NC**	**NC**	NVCC_DRAM	GND
H	DRAM_SDBA2	ZQPAD	GND	DRAM_A7	DRAM_A13	NVCC_DRAM	GND	**NC**
J	DRAM_SDBA0	DRAM_A10	DRAM_A8	DRAM_A9	GND	NVCC_DRAM	VDD_SOC_CAP	VDD_SOC_CAP
K	GND	DRAM_A15	**NC**	**NC**	**NC**	**NC**	VDD_SOC_CAP	VDD_SOC_CAP
L	DRAM_SDCLK_0	DRAM_CS1	**NC**	**NC**	**NC**	**NC**	GND	**NC**
M	DRAM_SDCLK_0_B	DRAM_SDCKE1	DRAM_A5	DRAM_A6	GND	NVCC_DRAM_2P5	GND	GND
N	DRAM_RAS	DRAM_CS0	GND	DRAM_A4	DRAM_VREF	NVCC_DRAM	GND	GND
P	DRAM_CAS	SDCKE0	**NC**	**NC**	**NC**	**NC**	NVCC_DRAM	**NC**
R	GND	DRAM_A14	**NC**	**NC**	**NC**	**NC**	VDD_PU_CAP	VDD_PU_CAP
T	DRAM_SDBA1	DRAM_A11	DRAM_A2	DRAM_A3	GND	NVCC_DRAM	VDD_PU_CAP	VDD_PU_CAP
U	DRAM_SDWE	DRAM_A12	GND	DRAM_A0	DRAM_A1	NVCC_DRAM	GND	**NC**
V	GND	DRAM_DQM0	**NC**	**NC**	**NC**	**NC**	NVCC_DRAM	GND
W	DRAM_SDQS0_B	DRAM_SDQS0	**NC**	**NC**	**NC**	**NC**	NVCC_1P2	**NC**
Y	DRAM_D6	DRAM_D7	DRAM_D5	DRAM_SDODT0	GND	NVCC_DRAM	PWM1	**NC**
AA	GND	GND	DRAM_D4	**NC**	**NC**	HSIC_DAT	FEC_MDC	**NC**
AB	DRAM_D3	DRAM_D2	DRAM_DQM2	**NC**	**NC**	HSIC_STROBE	FEC_MDIO	**NC**
AC	DRAM_D1	DRAM_D0	DRAm_SDQS2	DRAM_D22	DRAM_D21	DRAM_D19	DRAM_D17	FEC_TX_CLK
AD	GND	DRAM_SDQS2_B	DRAM_D23	GND	DRAM_D20	DRAM_D18	GND	DRAM_D16

7 Revision History

Table 70 provides a history for revision 4 of this data sheet.

Table 70. i.MX 6SoloLite Data Sheet Document Revision History

Rev. Number	Date	Substantive Change(s)
5	9/2017	• Figure 1, "Part Number Nomenclature—i.MX 6SoloLite" Updates to the Silicon Revision column to include Rev. 1.4, C. • Table 1, "Example Orderable Part Numbers" Added "C" suffix part numbers and descriptions. • Section 4.8.2, "DDR I/O Output Buffer Impedance" Cross-reference change from JEDEC standards to MMDC section. • Table 42, "eMMC4.4/4.41 Interface Timing Parameters," Corrected SD3 Minimum from 2.6 to 1.7 ns. • Table 42, "eMMC4.4/4.41 Interface Timing Parameters," Added footnote related to Clock duty Cycle range. • Figure 30, "HS200 Mode Timing Diagram" Updated figure to remove extraneous ID callouts.

(*Revision History table continued on next page*)

Table 70. i.MX 6SoloLite Data Sheet Document Revision History (continued)

Rev. Number	Date	Substantive Change(s)
Rev. 3	02/2014	• Section 1.2,Feature description for: - Camera sensors: Added to Parallel Camera port “and up to 66 MHz peak”. - Miscellaneous IPs and interfaces; Changed from: “Three I2S/SSI/AC97 supported,” to “SSI block is capable of supporting audio sample frequencies up to 192 kHZ stereo inputs and outputs with I2S mode.” • Table 2, Modules List: UART1–5, Brief Description; Changed bullet about programmable baud rate to “up to 5 MHz.” • Table 2, Modules List: uSDHC1–4, Brief Description; Changed bullet about Fully compliant with SD command/response to include “and SDXC cards up to 2TB.” • Table 9, operating range for GPIO supplies: Added NVCC_1P2V min/typ/max values for LPDDR2, DDR3L, DDR3. • Section 4.1.4, External Clock Sources; added Note, “The internal oscillator may run high …” • Table 11, Maximum Supply currents: Added row; NVCC_LVDS2P5. • Section 4.2.1, Power-Up Sequence: reworded third bulleted item regarding POR control. • Section 4.2.1, Power-Up Sequence: removed Note. • Section 4.5.1, OSC24K, first paragraph corrected ‘*powered from*’ signal from NVCC_1P2 to NVCC_1P2V. • Section 4.5.2, OSC32K, Changed second paragraph and added CAUTION. • Table 31 Reset Timing Parameters, changed Unit from XTALI cycle to XTALOSC_RTC_XTALI cycle. • Section 4.5.2, External Interface Module; enhanced wording to first paragraph to describe operating frequency for data transfers, and to explain register settings are valid for entire range of frequencies. • Table 34, EIM Bus Timing Parameters; reworded footnotes for clarity.
Rev. 3.0	02/2014	• Table 45, DDR3 Write Cycle; changed footnote 3, outputs from “DDR_VREF” to “DRAM_VREF”. • Figure 25, LPDDR2 Command and Address Timing Diagram; changed signal name from “DRAM_CAS_B” to “DRAM_ADDRxx”. • Table 47, LPDDR2 Timing Parameters; changed footnote 2, outputs from “DDR_VREF” to “DRAM_VREF”. • Table 48, LPDDR2 Write Cycle; changed footnote 3, outputs from “DDR_VREF” to “DRAM_VREF”. • Table 49, LPDDR2 Read Cycle; changed footnote 3, outputs from “DDR_VREF” to “DRAM_VREF”. • Table 65, 13x13mm Supplies Contact Assignment; changed Supply Rail Name “DDR_VREF” to “DRAM_VREF”. • Table 65, 13x13mm Supplies Contact Assignment; changed ZQPAD ball position from “AE17” to “H2”. • Table 68, 13x13mm Functional Contact Assignment; Changed the following signals to include active-low “_B” in the Default Function column: DRAM_CAS_B; DRAM_CS0_B; DRAM_CS1_B; DRAM_RAS_B; DRAM_RESET_B. • Table 68, 13x13mm Functional Contact Assignment; Changed the Ball Name of DRAM_WE_B to DRAM_SDWE. • Table 68, 13 x 13 mm, 0.5 mm Pitch Ball Map; Y19, changed from “ON/OFF” to “NVCC_PLL. • Table 68, 13 x 13 mm, 0.5 mm Pitch Ball Map; W18, changed from “TEST_MODE” to “ON/OFF”. • Table 68, 13 x 13 mm, 0.5 mm Pitch Ball Map; U15, changed from “NVCC_PLL” to “TEST_MODE”. • Table 68, 13 x 13 mm, 0.5 mm Pitch Ball Map; U11 & U10, changed from “NHVCC_3V3” to “NVCC33_IO”.
Rev. 2.2	8/2013	Substantive Changes are as follows: • Section 1.2, “Features,” corrected value of OCRAM from 256KB to 128KB: The SoC-level memory system consists of the following additional components: — Boot ROM, including HAB (96 KB) — Internal multimedia / shared, fast access RAM (OCRAM, 128 KB) • Removed parenthetical statement (input slope <= 5 ns) from Table 31, “Reset Timing Parameters” CC1: Duration of POR_B to be qualified as valid. The parenthetical statement was a typographical error and is not a specification requirement for this device.

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Document Number: IMX6SLCEC
Rev. 5
10/2017