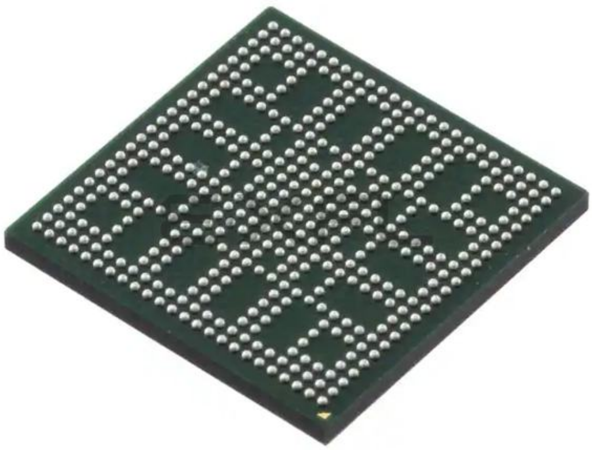

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, LVDDR3, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + PHY (3)
Voltage - I/O	1.2V, 1.8V, 3.0V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	432-TFBGA
Supplier Device Package	432-MAPBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6l2evn10acr

MC IMX6 X @ + VV $$ % A

Qualification level	MC
Prototype samples	PC
Mass production	MC
Special	SC

Part # series	X
i.MX 6SoloLite	L

Part differentiator	@
GPU, EPD	8
No GPU, EPD	7
GPU, no EPD	3
No GPU, no EPD	2

Temperature Tj	+
Commercial: 0 to + 95°C	D
Extended commercial: -40 to + 105°C	E

Silicon revision[1]	A
Rev 1.0	A
Rev 1.2 Rev 1.3	B[2]
Rev 1.4	C

Fusing	%
Supports E-INK EPDC if EPD enabled	A

Frequency	$$
1 GHz	10

Package type	RoHS
MAPBGA 13x13 0.5mm	VN

1. See the nxp.com\imx6series Web page for latest information on the available silicon revision.
2. Rev 1.2 (USB_ANALOG_DIGPROG register = 0x0062_0002)
   Rev 1.3 (USB_ANALOG_DIGPROG register = 0x0062_0003)

Figure 1. Part Number Nomenclature—i.MX 6SoloLite

1.2 Features

The i.MX 6SoloLite processor is based on ARM Cortex-A9 MPCore multicore processor, which has the following features:

- ARM Cortex-A9 MPCore CPU processor (with TrustZone)
- The core configuration is symmetric, where each core includes:
  — 32 KByte L1 Instruction Cache
  — 32 KByte L1 Data Cache
  — Private Timer and Watchdog
  — Cortex-A9 NEON MPE (Media Processing Engine) co-processor

The ARM Cortex-A9 MPCore complex includes:

- General Interrupt Controller (GIC) with 128 interrupt support
- Global Timer
- Snoop Control Unit (SCU)
- 256 KB unified I/D L2 cache
- Two Master AXI (64-bit) bus interfaces output of L2 cache
- Frequency of the core (including NEON and L1 cache) as per Table 9, "Operating Ranges," on page 21

2 Architectural Overview

The following subsections provide an architectural overview of the i.MX 6SoloLite processor system.

2.1 Block Diagram

Figure 2 shows the functional modules in the i.MX 6SoloLite processor system.

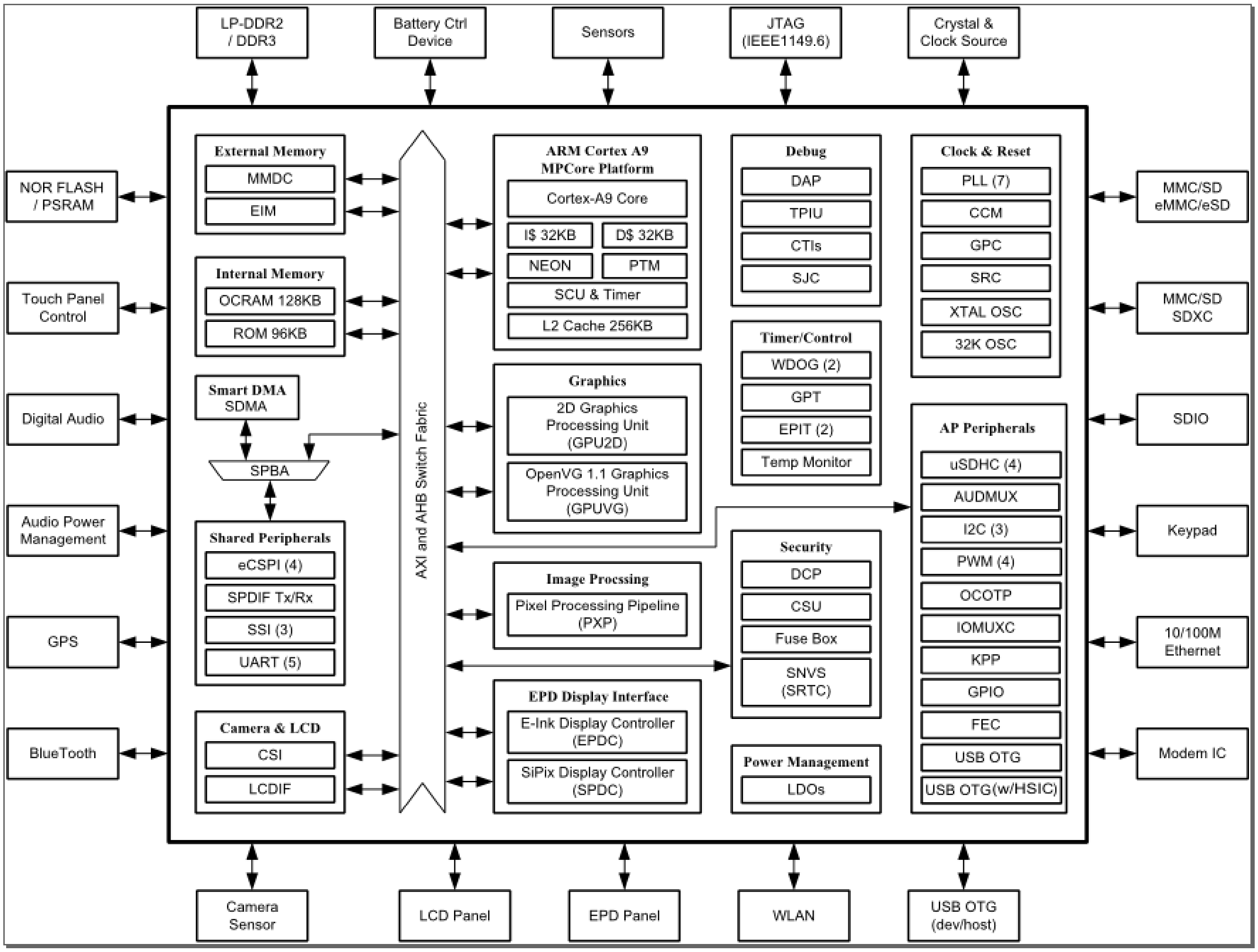

Figure 2. i.MX 6SoloLite System Block Diagram

NOTE

The numbers in brackets indicate number of module instances. For example, PWM (4) indicates four separate PWM peripherals.

Table 2. i.MX 6SoloLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
PXP	PiXel Processing Pipeline	Display Peripherals	A high-performance pixel processor capable of 1 pixel/clock performance for combined operations, such as color-space conversion, alpha blending, gamma-mapping, and rotation. The PXP isenhanced with features specifically for gray scale applications. In addition, the PXP supports traditional pixel/frame processing paths for still-image and video processing applications, allowing it to interface with either of the integrated EPD controllers.
RAM 128 KB	Internal RAM	Internal Memory	Internal RAM, which is accessed through OCRAM memory controller.
RNGB	Random Number Generator	Security	Random number generating module.
ROM 96KB	Boot ROM	Internal Memory	Supports secure and regular Boot Modes. Includes read protection on 4K region for content protection.
ROMCP	ROM Controller with Patch	Data Path	ROM Controller with ROM Patch support.
SDMA	Smart Direct Memory Access	System Control Peripherals	The SDMA is multi-channel flexible DMA engine. It helps in maximizing system performance by off-loading the various cores in dynamic data routing. It has the following features: • Powered by a 16-bit Instruction-Set micro-RISC engine • Multi-channel DMA supporting up to 32 time-division multiplexed DMA channels • 48 events with total flexibility to trigger any combination of channels • Memory accesses including linear, FIFO, and 2D addressing • Shared peripherals between ARM and SDMA • Very fast Context-Software switching with 2-level priority based preemptive multi-tasking • DMA units with auto-flush and prefetch capability • Flexible address management for DMA transfers (increment, decrement, and no address changes on source and destination address) • DMA ports can handle unit-directional and bi-directional flows (copy mode) • Up to 8-word buffer for configurable burst transfers • Support of byte-swapping and CRC calculations • Library of Scripts and API is available
SJC	System JTAG Controller	System Control Peripherals	The SJC provides JTAG interface, which complies with JTAG TAP standards, to internal logic. The i.MX 6SoloLite processor uses JTAG port for production, testing, and system debugging. In addition, the SJC provides BSR (Boundary Scan Register) standard support, which complies with IEEE1149.1 and IEEE1149.6 standards. The JTAG port must be accessible during platform initial laboratory bring-up, for manufacturing tests and troubleshooting, as well as for software debugging by authorized entities. The i.MX 6SoloLite SJC incorporates three security modes for protecting against unauthorized accesses. Modes are selected through eFUSE configuration.
SNVS	Secure Non-Volatile Storage	Security	Secure Non-Volatile Storage, including Secure Real Time Clock, Security State Machine, Master Key Control, and Violation/Tamper Detection and reporting.
SPDIF	Sony Phillips Digital Interface	Multimedia Peripherals	A standard audio file transfer format, developed jointly by the Sony and Phillips corporations. Has Transmitter and Receiver functionality.

Table 9. Operating Ranges (continued)

Parameter Description	Symbol	Min	Typ	Max[1]	Unit	Comment
GPIO supplies[6]	NVCC33_IO	2.8	3.0	3.3	V	Worst case, assuming all SOC I/O operating at 1.8V. NVCC33_IO must always be greater than NVCC18_IO.
	NVCC18_IO	1.62	1.8	1.98	V	—
	NVCC_1P2V	1.14	1.2	1.3	V	—
Junction temperature	T_J	0	—	95	°C	Commercial See *i.MX 6SoloLite Product Lifetime Usage Estimates Application Note*, AN4726, for information on product lifetime (power-on years) for this processor.
Junction temperature	T_J	-40	—	105	—	Extended commercial See *i.MX 6SoloLite Product Lifetime Usage Estimates Application Note*, AN4726, for information on product lifetime (power-on years) for this processor.

1 Applying the maximum voltage results in maximum power consumption and heat generation. NXP recommends a voltage set point = (Vmin + the supply tolerance). This results in an optimized power/speed ratio.

2 VDD_ARM_IN and VDD_SOC_IN must be at least 125 mV higher than the LDO Output Set Point for correct voltage regulation.

3 VDD_SOC_CAP and VDD_PU_CAP must be equal.

4 VDD_SOC and VDD_PU output voltage must be set to this rule: VDD_ARM - VDD_SOC / VDD_PU < 50mV.

5 While setting VDD_SNVS_IN voltage with respect to Charging Currents and RTC, refer to Hardware Development Guide for i.MX 6Dual, 6Quad, 6Solo, 6DualLite Families of Applications Processors (IMX6DQ6SDLHDG).

6 All digital I/O supplies (NVCC_xxxx) must be powered under normal conditions whether the associated I/O pins are in use or not, and associated I/O pins need to have a pull-up or pull-down resistor applied to limit any floating gate current.

4.1.4 External Clock Sources

Each i.MX 6SoloLite processor has two external input system clocks: a low frequency (RTC_XTALI) and a high frequency (XTALI).

The RTC_XTALI is used for low-frequency functions. It supplies the clock for wake-up circuit, power-down real time clock operation, and slow system and watchdog counters. The clock input can be connected to either an external oscillator or a crystal using the internal oscillator amplifier. Additionally, there is an internal ring oscillator, which can substitute the RTC_XTALI, in case accuracy is not important.

The system clock input XTALI is used to generate the main system clock. It supplies the PLLs and other peripherals. The system clock input can be connected to either an external oscillator or a crystal using the internal oscillator amplifier.

NOTE

The internal RTC oscillator does not provide an accurate frequency and is affected by process, voltage, and temperature variations. NXP strongly recommends using an external crystal as the RTC_XTALI reference. If the internal oscillator is used instead, careful consideration must be given to the timing implications on all of the SoC modules dependent on this clock.

CAUTION

The internal RTC oscillator does not provide an accurate frequency and is affected by process, voltage and temperature variations. NXP strongly recommends using an external crystal as the RTC_XTALI reference. If the internal oscillator is used instead, careful consideration must be given to the timing implications on all of the SoC modules dependent on this clock.

The OSC32k runs from VDD_SNVS_CAP, which comes from the VDD_HIGH_IN/VDD_SNVS_IN power mux.

Table 19. OSC32K Main Characteristics

Parameter	Min	Typ	Max	Comments
Fosc	—	32.768 kHz	—	This frequency is nominal and determined mainly by the crystal selected. 32.0 K would work as well.
Current consumption	—	4 µA	—	The typical value shown is only for the oscillator, driven by an external crystal. If the internal ring oscillator is used instead of an external crystal, then approximately 25 µA should be added to this value.
Bias resistor	—	14 MΩ	—	This the integrated bias resistor that sets the amplifier into a highgain state. Any leakage through the ESD network, external board leakage, or even a scope probe that is significant relative to this value will debias the amp. The debiasing will result in low gain, and will impact the circuit's ability to start up and maintain oscillations.
Target Crystal Properties				
Cload	—	10 pF	—	Usually crystals can be purchased tuned for different Cloads. This Cload value is typically 1/2 of the capacitances realized on the PCB on either side of the quartz. A higher Cload will decrease oscillation margin, but increases current oscillating through the crystal.
ESR	—	50 kΩ	—	Equivalent series resistance of the crystal. Choosing a crystal with a higher value will decrease the oscillating margin.

4.6 I/O DC Parameters

This section includes the DC parameters of the following I/O types:

- Dual Voltage General Purpose I/O cell set (DVGPIO)
- Double Data Rate I/O (DDR) for LPDDR2 and DDR3 modes

NOTE

The term OVDD in this section refers to the associated supply rail of an input or output.

4.7.1 General Purpose I/O AC Parameters

The I/O AC parameters for GPIO in slow and fast modes are presented in the Table 24 and Table 25, respectively. Note that the fast or slow I/O behavior is determined by the appropriate control bits in the IOMUXC control registers.

Table 24. General Purpose I/O AC Parameters 1.8 V Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Pad Transition Times, rise/fall (Max Drive, ipp_dse=111)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	2.72/2.79 1.51/1.54	ns
Output Pad Transition Times, rise/fall (High Drive, ipp_dse=101)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	3.20/3.36 1.96/2.07	
Output Pad Transition Times, rise/fall (Medium Drive, ipp_dse=100)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	3.64/3.88 2.27/2.53	
Output Pad Transition Times, rise/fall (Low Drive. ipp_dse=011)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	4.32/4.50 3.16/3.17	
Input Transition Times[1]	trm	—	—	—	25	ns

[1] Hysteresis mode is recommended for inputs with transition times greater than 25 ns.

Table 25. General Purpose I/O AC Parameters 3.3 V Mode

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Pad Transition Times, rise/fall (Max Drive, ipp_dse=101)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	1.70/1.79 1.06/1.15	ns
Output Pad Transition Times, rise/fall (High Drive, ipp_dse=011)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	2.35/2.43 1.74/1.77	
Output Pad Transition Times, rise/fall (Medium Drive, ipp_dse=010)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	3.13/3.29 2.46/2.60	
Output Pad Transition Times, rise/fall (Low Drive. ipp_dse=001)	tr, tf	15 pF Cload, slow slew rate 15 pF Cload, fast slew rate	—	—	5.14/5.57 4.77/5.15	
Input Transition Times[1]	trm	—	—	—	25	ns

[1] Hysteresis mode is recommended for inputs with transition times greater than 25 ns.

Table 34. EIM Bus Timing Parameters (continued)

ID	Parameter	Min[1]	Max[1]	Unit
WE5	Clock rise to address invalid	$0.5 \times t \times (k+1) -1.25$	$0.5 \times t \times (k+1) +2.25$	ns
WE6	Clock rise to EIM_CSx_B valid	$-0.5 \times t \times (k+1) -1.25$	$-0.5 \times t \times (k+1) +2.25$	ns
WE7	Clock rise to EIM_CSx_B invalid	$0.5 \times t \times (k+1) -1.25$	$0.5 \times t \times (k+1) +2.25$	ns
WE8	Clock rise to EIM_RW_B valid	$-0.5 \times t \times (k+1) -1.25$	$-0.5 \times t \times (k+1) +2.25$	ns
WE9	Clock rise to EIM_RW_B invalid	$0.5 \times t \times (k+1) -1.25$	$0.5 \times t \times (k+1) +2.25$	ns
WE10	Clock rise to EIM_OE_B valid	$-0.5 \times t \times (k+1) -1.25$	$-0.5 \times t \times (k+1) +2.25$	ns
WE11	Clock rise to EIM_OE_B invalid	$0.5 \times t \times (k+1) -1.25$	$0.5 \times t \times (k+1) +2.25$	ns
WE12	Clock rise to EIM_EBx_B valid	$0.5 \times t \times (k+1) -1.25$	$-0.5 \times t \times (k+1) +2.25$	ns
WE13	Clock rise to EIM_EBx_B invalid	$0.5 \times t \times (k+1) -1.25$	$0.5 \times t \times (k+1) +2.25$	ns
WE14	Clock rise to EIM_LBA_B valid	$-0.5 \times t \times (k+1) -1.25$	$-0.5 \times t \times (k+1) +2.25$	ns
WE15	Clock rise to EIM_LBA_B invalid	$0.5 \times t \times (k+1) -1.25$	$0.5 \times t \times (k+1) +2.25$	ns
WE16	Clock rise to output data valid	$-0.5 \times t \times (k+1) -1.25$	$-0.5 \times t \times (k+1) +2.25$	ns
WE17	Clock rise to output data invalid	$0.5 \times t \times (k+1) -1.25$	$0.5 \times t \times (k+1) +2.25$	ns
WE18	Input data setup time to clock rise	2.3	—	ns
WE19	Input data hold time from clock rise	2	—	ns
WE20	EIM_WAIT_B setup time to clock rise	2	—	ns
WE21	EIM_WAIT_B hold time from clock rise	2	—	ns

[1] k represents register setting BCD value

[2] t is clock period (1/Freq). For 104 MHz, t = 9.165 ns

Table 39. ECSPI Master Mode Timing Parameters (continued)

ID	Parameter	Symbol	Min	Max	Unit
CS6	ECSPIx_SSx Lag Time (CS hold time)	t_{HCS}	Half ECSPI_SCLK period - 2	—	ns
CS7	ECSPIx_MOSI Propagation Delay (C_{LOAD} = 20 pF)	t_{PDmosi}	-0.5	2	ns
CS8	ECSPIx_MISO Setup Time • Slow group[1] • Fast group[2]	t_{Smiso}	— 14 12	—	ns
CS9	ECSPIx_MISO Hold Time	t_{Hmiso}	0	—	ns
CS10	ECSPIx_RDY to ECSPIx_SSx Time[4]	t_{SDRY}	5	—	ns

1 ECSPI slow group includes:
ECSPI2/EPDC_SDLE, ECSPI3/EPDC_D9, ECSPI4/EPDC_D1

2 ECSPI fast group includes:
ECSPI1/LCD_DATA01, ECSPI1/ECSPI1_MISO, ECSPI2/LCD_DATA10, ECSPI2/ECSPI2_MISO, ECSPI3/AUDx_TXC, ECSPI3/SD2_DAT1, ECSPI4/KEY_ROW1, ECSPI4/FEC_RX_DV

3 See specific I/O AC parameters Section 4.7, "I/O AC Parameters."

4 ECSPIx_RDY is sampled internally by ipg_clk and is asynchronous to all other eCSPI signals.

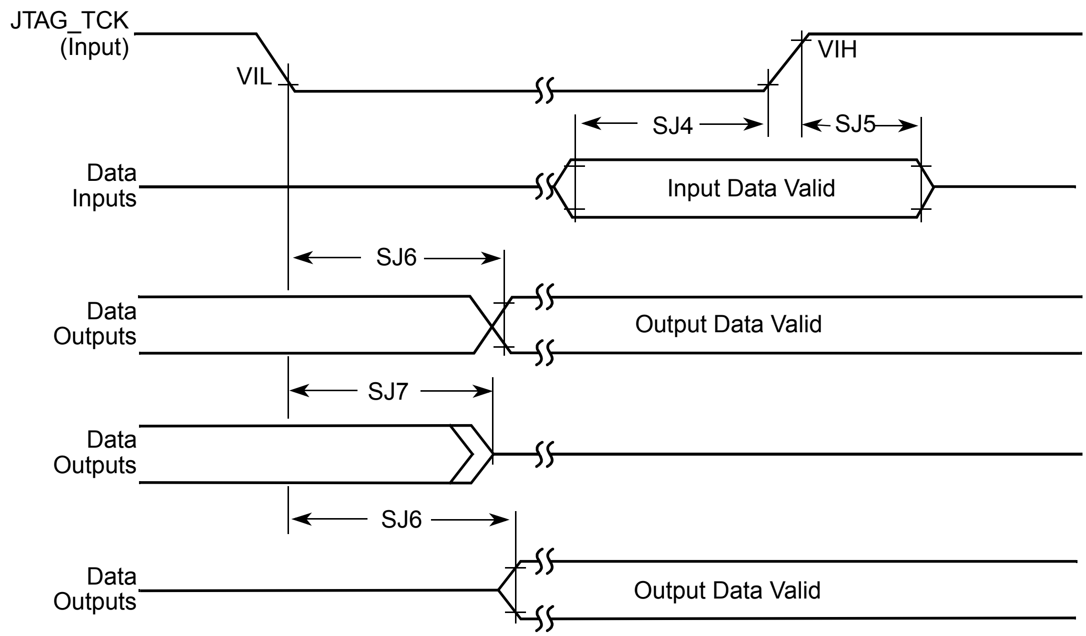

Figure 35. Boundary Scan (JTAG) Timing Diagram

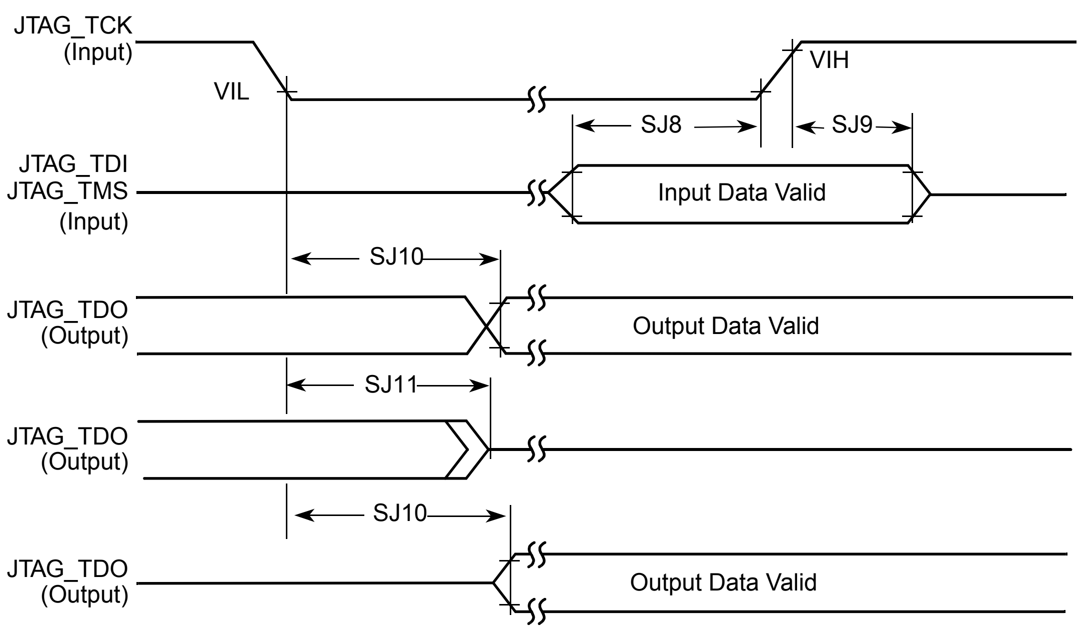

Figure 36. Test Access Port Timing Diagram

4.10.12 UART I/O Configuration and Timing Parameters

4.10.12.1 UART RS-232 I/O Configuration in Different Modes

The i.MX 6SoloLite UART interfaces can serve both as DTE or DCE device. This can be configured by the DCEDTE control bit (default 0 – DCE mode). Table 55 shows the UART I/O configuration based on the enabled mode.

Table 55. UART I/O Configuration vs. Mode

Port	DTE Mode		DCE Mode	
	Direction	Description	Direction	Description
UART_RTS_B	Output	RTS from DTE to DCE	Input	RTS from DTE to DCE
UART_CTS_B	Input	CTS from DCE to DTE	Output	CTS from DCE to DTE
UART_DTR_B	Output	DTR from DTE to DCE	Input	DTR from DTE to DCE
UART_DSR_B	Input	DSR from DCE to DTE	Output	DSR from DCE to DTE
UART_DCD_B	Input	DCD from DCE to DTE	Output	DCD from DCE to DTE
UART_RI_B	Input	RING from DCE to DTE	Output	RING from DCE to DTE
UART_TX_DATA	Input	Serial data from DCE to DTE	Output	Serial data from DCE to DTE
UART_RX_DATA	Output	Serial data from DTE to DCE	Input	Serial data from DTE to DCE

4.10.12.2 UART RS-232 Serial Mode Timing

The following sections describe the electrical information of the UART module in the RS-232 mode.

4.10.12.2.1 UART Transmitter

Figure 44 depicts the transmit timing of UART in the RS-232 serial mode, with 8 data bit/1 stop bit format. Table 56 lists the UART RS-232 serial mode transmit timing characteristics.

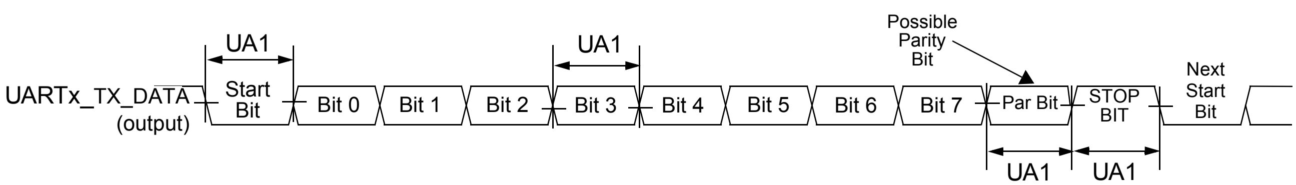

Figure 44. UART RS-232 Serial Mode Transmit Timing Diagram

Table 56. RS-232 Serial Mode Transmit Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA1	Transmit Bit Time	t_{Tbit}	$1/F_{baud\_rate}$[1] – T_{ref_clk}[2]	$1/F_{baud\_rate} + T_{ref\_clk}$	—

[1] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

[2] T_{ref_clk}: The period of UART reference clock *ref_clk* (*ipg_perclk* after RFDIV divider).

4.10.12.2.2 UART Receiver

Figure 45 depicts the RS-232 serial mode receive timing with 8 data bit/1 stop bit format. Table 57 lists serial mode receive timing characteristics.

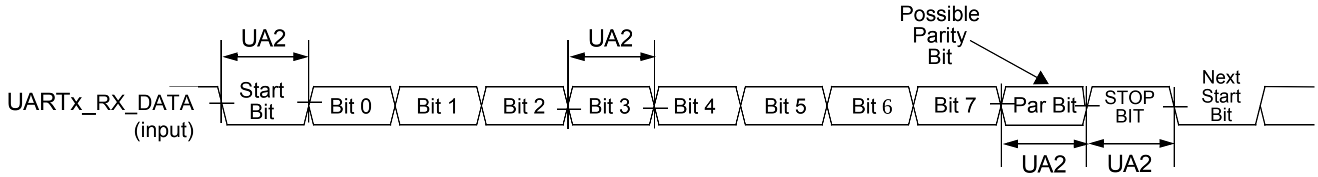

Figure 45. UART RS-232 Serial Mode Receive Timing Diagram

Table 57. RS-232 Serial Mode Receive Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA2	Receive Bit Time[1]	t_{Rbit}	$1/F_{baud\_rate}$[2] $- 1/(16 \times F_{baud\_rate})$	$1/F_{baud\_rate} + 1/(16 \times F_{baud\_rate})$	—

[1] The UART receiver can tolerate $1/(16 \times F_{baud\_rate})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16 \times F_{baud\_rate})$.

[2] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

4.10.12.2.3 UART IrDA Mode Timing

The following subsections give the UART transmit and receive timings in IrDA mode.

UART IrDA Mode Transmitter

Figure 46 depicts the UART IrDA mode transmit timing, with 8 data bit/1 stop bit format. Table 58 lists the transmit timing characteristics.

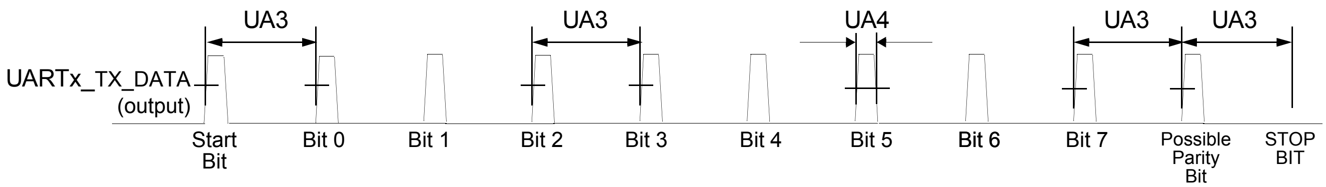

Figure 46. UART IrDA Mode Transmit Timing Diagram

Table 58. IrDA Mode Transmit Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA3	Transmit Bit Time in IrDA mode	t_{TIRbit}	$1/F_{baud\_rate}$[1] $- T_{ref\_clk}$[2]	$1/F_{baud\_rate} + T_{ref\_clk}$	—
UA4	Transmit IR Pulse Duration	$t_{TIRpulse}$	$(3/16) \times (1/F_{baud\_rate}) - T_{ref\_clk}$	$(3/16) \times (1/F_{baud\_rate}) + T_{ref\_clk}$	—

[1] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

[2] T_{ref_clk}: The period of UART reference clock *ref_clk* (*ipg_perclk* after RFDIV divider).

UART IrDA Mode Receiver

Figure 47 depicts the UART IrDA mode receive timing, with 8 data bit/1 stop bit format. Table 59 lists the receive timing characteristics.

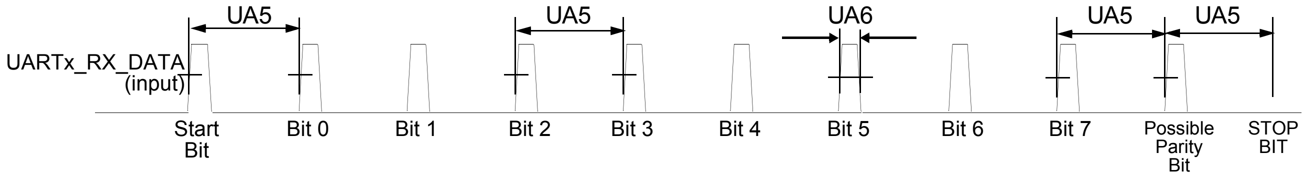

Figure 47. UART IrDA Mode Receive Timing Diagram

Table 59. IrDA Mode Receive Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
UA5	Receive Bit Time[1] in IrDA mode	t_{RIRbit}	$1/F_{baud\_rate}$[2] – $1/(16 \times F_{baud\_rate})$	$1/F_{baud\_rate} + 1/(16 \times F_{baud\_rate})$	—
UA6	Receive IR Pulse Duration	$t_{RIRpulse}$	1.41 µs	$(5/16) \times (1/F_{baud\_rate})$	—

[1] The UART receiver can tolerate $1/(16 \times F_{baud\_rate})$ tolerance in each bit. But accumulation tolerance in one frame must not exceed $3/(16 \times F_{baud\_rate})$.

[2] F_{baud_rate}: Baud rate frequency. The maximum baud rate the UART can support is (*ipg_perclk* frequency)/16.

4.10.13 USB HSIC Timing Parameters

This section describes the electrical information of the USB HSIC port.

NOTE

HSIC is the DDR signal, the following timing parameters are for both rising and falling edge.

4.10.13.1 Transmit Timing Parameters

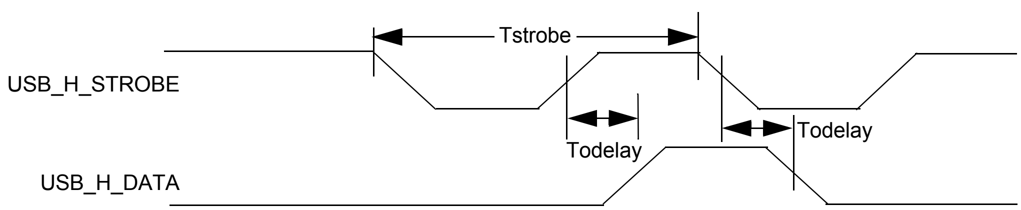

Figure 48. USB HSIC Transmit Timing Diagram

Table 60. USB HSIC Transmit Timing Parameters

Name	Parameter	Min	Max	Unit	Comment
Tstrobe	Strobe period	4.166	4.167	ns	—
Todelay	Data output delay time	550	1350	ps	Measured at 50% point
Tslew	Strobe/data rising/falling time	0.7	2	V/ns	Averaged from 30% – 70% points

4.10.13.2 Receive Timing Parameters

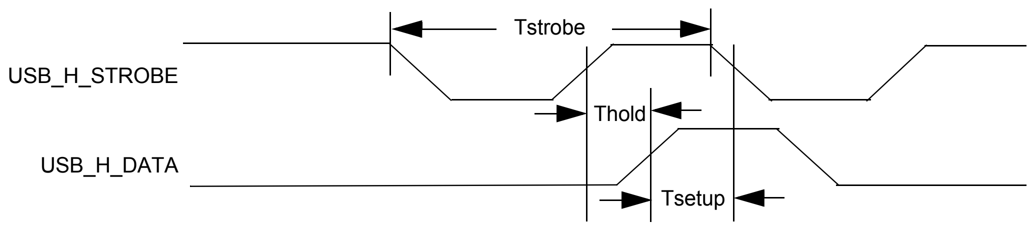

Figure 49. USB HSIC Receive Timing Diagram

Table 61. USB HSIC Receive Timing Parameters[1]

Name	Parameter	Min	Max	Unit	Comment
Tstrobe	Strobe period	4.166	4.167	ns	—
Thold	Data hold time	300	—	ps	Measured at 50% point
Tsetup	Data setup time	365	—	ps	Measured at 50% point
Tslew	Strobe/data rising/falling time	0.7	2	V/ns	Averaged from 30% – 70% points

[1] The timings in the table are guaranteed when:
—AC I/O voltage is between 0.9x to 1x of the I/O supply
—DDR_SEL configuration bits of the I/O are set to (10)b

4.10.14 USB PHY Parameters

This section describes the USB-OTG PHY and the USB Host port PHY parameters.

The USB PHY meets the electrical compliance requirements defined in the Universal Serial Bus Revision 2.0 OTG, USB Host with the amendments below (On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification is not applicable to Host port).

- USB ENGINEERING CHANGE NOTICE
  - Title: 5V Short Circuit Withstand Requirement Change
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- Errata for USB Revision 2.0 April 27, 2000 as of 12/7/2000
- USB ENGINEERING CHANGE NOTICE
  - Title: Pull-up/Pull-down resistors
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- USB ENGINEERING CHANGE NOTICE
  - Title: Suspend Current Limit Changes
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- USB ENGINEERING CHANGE NOTICE
  - Title: USB 2.0 Phase Locked SOFs
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification
  - Revision 2.0 plus errata and ecn June 4, 2010

- Battery Charging Specification (available from USB-IF)
  - Revision 1.2, December 7, 2010
  - Portable device only.

Table 64 shows the 13 x 13 mm BGA package details.

Table 64. 13 x 13, 0.5 mm BGA Package Details

Parameter	Symbol	Common Dimensions		
		Minimum	Normal	Maximum
Total Thickness	A	0.88	—	1.1
Stand Off	A1	0.16	—	0.26
Substrate Thickness	A2	0.26 REF		
Mold Thickness	A3	0.54 REF		
Body Size	D	13 BSC		
	E	13 SC		
Ball Diameter	—	0.3		
Ball Opening	—	0.275		
Ball Width	b	0.27	—	0.37
Ball Pitch	e	0.5 BSC		
Ball Count	n	432	—	—
Edge Ball Center to Center	D1	11.5 BSC		
	E1	11.5 BSC		
Body Center to Contact Ball	SD	0.25 BSC		
	SE	0.25 BSC		
Package Edge Tolerance	aaa	0.1		
Mold Flatness	bbb	0.1		
Coplanarity	ddd	0.08		
Ball Offset (Package)	eee	0.15		
Ball Offset (Ball)	fff	0.05		

B

Table 65. 13 x 13 mm Supplies Contact Assignment (continued)

Supply Rail Name	Ball(s) Position(s)	Remark
VDD_SNVS_IN	AC20	Primary Supply, for the SNVS Regulator
VDD_SOC_CAP	J7, J8, J9, K7, K8, K9, N18, P18, R18	Secondary Supply for the SoC and PU (internal regulator output—requires capacitor if internal regulator is used)
VDD_SOC_IN	J10, J11, K10, K11, R16, R17, T16, T17, T18	Primary Supply, for the SoC and PU Regulators
VDD_USB_CAP	U14	Secondary Supply for the 3V Domain (USBPHY, MLPBPHY, eFuse),internal regulator output, requires capacitor if internal regulator is used.
USB_OTG1_VBUS	AA18	—
USB_OTG2_VBUS	AD18	—
ZQPAD	H2	Connect ZQPAD to an external 240 ohm 1% resistor to GND. This is a reference used during DRAM output buffer driver calibration.
NC	C4, C5, C8, C9, C12, C13, C16, C17, C20, C21, D4, D5, D8, D9, D12, D13, D16, D17, D20, D21, E8, E9, E12, E13, E16, E17, F3, F4, F5, F6, F8, F9, F12, F13, F16, F17, F19, F20, F21, F22, G3, G4, G5, G6, G19, G20, G21, G22, H8, H9, H12, H13, H16, H17, K3, K4, K5, K6, K19, K20, K21, K22, L3, L4, L5, L6, L8, L17, L19, L20, L21, L22, P3, P4, P5, P6, P8, P17, P19, P20, P21, P22, R3, R4, R5, R6, R19, R20, R21, R22, U8, U9, U12, U13, U16, U17, V3, V4, V5, V6, V19, V20, V21, V22, W3, W4, W5, W6, W8, W9, W12, W13, W16, W17, W19, W20, W21, W22, Y8, Y9, Y12, Y13, Y16,Y17, AA4, AA5, AA8, AA9, AA12, AA13, AA16, AA17, AA20, AA21, AB4, AB5, AB8, AB9, AB12, AB13, AB16, AB17 AB20, AB21	No Connections.

Table 66 displays an alpha-sorted list of the signal assignments including power rails. The table also includes out of reset pad state.

Table 66. 13 x 13 mm Functional Contact Assignments

Ball Name	Ball	Power Group[1]	Ball Type	Out of Reset Condition[2]			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value[3]
AUD_MCLK	H19	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO1_GPIO[6]	Input	Keeper
AUD_RXC	J21	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO1_GPIO[1]	Input	Keeper
AUD_RXD	J20	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO1_GPIO[2]	Input	Keeper

Table 66. 13 x 13 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group[1]	Ball Type	Out of Reset Condition[2]			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value[3]
DRAM_D17	AC7	NVCC_DRAM	DDR	ALT0	DRAM_DATA17	Input	PU (100K)
DRAM_D18	AD6	NVCC_DRAM	DDR	ALT0	DRAM_DATA18	Input	PU (100K)
DRAM_D19	AC6	NVCC_DRAM	DDR	ALT0	DRAM_DATA19	Input	PU (100K)
DRAM_D2	AB2	NVCC_DRAM	DDR	ALT0	DRAM_DATA02	Input	PU (100K)
DRAM_D20	AD5	NVCC_DRAM	DDR	ALT0	DRAM_DATA20	Input	PU (100K)
DRAM_D21	AC5	NVCC_DRAM	DDR	ALT0	DRAM_DATA21	Input	PU (100K)
DRAM_D22	AC4	NVCC_DRAM	DDR	ALT0	DRAM_DATA22	Input	PU (100K)
DRAM_D23	AD3	NVCC_DRAM	DDR	ALT0	DRAM_DATA23	Input	PU (100K)
DRAM_D24	A3	NVCC_DRAM	DDR	ALT0	DRAM_DATA24	Input	PU (100K)
DRAM_D25	B4	NVCC_DRAM	DDR	ALT0	DRAM_DATA25	Input	PU (100K)
DRAM_D26	B5	NVCC_DRAM	DDR	ALT0	DRAM_DATA26	Input	PU (100K)
DRAM_D27	A5	NVCC_DRAM	DDR	ALT0	DRAM_DATA27	Input	PU (100K)
DRAM_D28	B6	NVCC_DRAM	DDR	ALT0	DRAM_DATA28	Input	PU (100K)
DRAM_D29	A6	NVCC_DRAM	DDR	ALT0	DRAM_DATA29	Input	PU (100K)
DRAM_D3	AB1	NVCC_DRAM	DDR	ALT0	DRAM_DATA03	Input	PU (100K)
DRAM_D30	B7	NVCC_DRAM	DDR	ALT0	DRAM_DATA30	Input	PU (100K)
DRAM_D31	A8	NVCC_DRAM	DDR	ALT0	DRAM_DATA31	Input	PU (100K)
DRAM_D4	AA3	NVCC_DRAM	DDR	ALT0	DRAM_DATA04	Input	PU (100K)
DRAM_D5	Y3	NVCC_DRAM	DDR	ALT0	DRAM_DATA05	Input	PU (100K)
DRAM_D6	Y1	NVCC_DRAM	DDR	ALT0	DRAM_DATA06	Input	PU (100K)
DRAM_D7	Y2	NVCC_DRAM	DDR	ALT0	DRAM_DATA07	Input	PU (100K)
DRAM_D8	E2	NVCC_DRAM	DDR	ALT0	DRAM_DATA08	Input	PU (100K)
DRAM_D9	E1	NVCC_DRAM	DDR	ALT0	DRAM_DATA09	Input	PU (100K)
DRAM_DQM0	V2	NVCC_DRAM	DDR	ALT0	DRAM_DQM0	Output	0
DRAM_DQM1	G2	NVCC_DRAM	DDR	ALT0	DRAM_DQM1	Output	0
DRAM_DQM2	AB3	NVCC_DRAM	DDR	ALT0	DRAM_DQM2	Output	0
DRAM_DQM3	C3	NVCC_DRAM	DDR	ALT0	DRAM_DQM3	Output	0
DRAM_RAS_B	N1	NVCC_DRAM	DDR	ALT0	DRAM_RAS_B	Output	0
DRAM_RESET_B	D6	NVCC_DRAM	DDR	ALT0	DRAM_RESET_B	Output	0
DRAM_SDBA0	J1	NVCC_DRAM	DDR	ALT0	DRAM_SDBA0	Output	0
DRAM_SDBA1	T1	NVCC_DRAM	DDR	ALT0	DRAM_SDBA1	Output	0
DRAM_SDBA2	H1	NVCC_DRAM	DDR	ALT0	DRAM_SDBA2	Output	0
DRAM_SDCKE0	P2	NVCC_DRAM	DDR	ALT0	DRAM_SDCKE0	Output	0
DRAM_SDCKE1	M2	NVCC_DRAM	DDR	ALT0	DRAM_SDCKE1	Output	0
DRAM_SDCLK_0	L1	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDCLK0_P	Output	0
DRAM_SDCLK_0_B	M1	NVCC_DRAM	DDRCLK	—	DRAM_SDCLK0_N	—	—
DRAM_SDODT0	Y4	NVCC_DRAM	DDR	ALT0	DRAM_ODT0	Output	0
DRAM_SDODT1	E4	NVCC_DRAM	DDR	ALT0	DRAM_ODT1	Output	0
DRAM_SDQS0	W2	NVCC_DRAM	DDRCLK	ALT0	DRAM_SDQS0_P	Input	Hi-Z

Table 66. 13 x 13 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group[1]	Ball Type	Out of Reset Condition[2]			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value[3]
KEY_ROW6	C24	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO4_GPIO[5]	Input	Keeper
KEY_ROW7	B24	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO4_GPIO[7]	Input	Keeper
LCD_CLK	T22	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[15]	Input	Keeper
LCD_DAT0	Y24	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[20]	Input	Keeper
LCD_DAT1	W23	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[21]	Input	Keeper
LCD_DAT10	R23	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[30]	Input	Keeper
LCD_DAT11	R24	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[31]	Input	Keeper
LCD_DAT12	P23	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[0]	Input	Keeper
LCD_DAT13	P24	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[1]	Input	Keeper
LCD_DAT14	N21	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[2]	Input	Keeper
LCD_DAT15	N23	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[3]	Input	Keeper
LCD_DAT16	N24	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[4]	Input	Keeper
LCD_DAT17	M22	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[5]	Input	Keeper
LCD_DAT18	M23	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[6]	Input	Keeper
LCD_DAT19	M24	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[7]	Input	Keeper
LCD_DAT2	W24	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[22]	Input	Keeper
LCD_DAT20	L23	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[8]	Input	Keeper
LCD_DAT21	L24	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[9]	Input	Keeper
LCD_DAT22	K23	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[10]	Input	Keeper
LCD_DAT23	K24	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[11]	Input	Keeper
LCD_DAT3	V23	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[23]	Input	Keeper
LCD_DAT4	V24	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[24]	Input	Keeper

Table 66. 13 x 13 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group[1]	Ball Type	Out of Reset Condition[2]			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value[3]
LCD_DAT5	U21	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[25]	Input	Keeper
LCD_DAT6	U23	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[26]	Input	Keeper
LCD_DAT7	U24	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[27]	Input	Keeper
LCD_DAT8	T23	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[28]	Input	Keeper
LCD_DAT9	T24	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[29]	Input	Keeper
LCD_ENABLE	J24	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[16]	Input	Keeper
LCD_HSYNC	H23	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[17]	Input	Keeper
LCD_RESET	H24	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[19]	Input	Keeper
LCD_VSYNC	J23	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[18]	Input	Keeper
ONOFF	W18	VDD_SNVS_IN	GPIO		SRC_ONOFF	Input	PU (100K)
PMIC_ON_REQ	AD15	VDD_SNVS_IN	GPIO	ALT0	SNVS_PMIC_ON_REQ	Output	Open Drain with PU (100K)
PMIC_STBY_REQ	AD16	VDD_SNVS_IN	GPIO	ALT0	CCM_PMIC_STBY_REQ	Output	0
POR_B	AC16	VDD_SNVS_IN	GPIO	ALT0	SRC_POR_B	Input	PU (100K)
PWM1	Y7	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[23]	Input	Keeper
REF_CLK_24M	AC14	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[21]	Input	Keeper
REF_CLK_32K	AD14	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[22]	Input	Keeper
RTC_XTALI	AB19	VDD_SNVS_CAP	—	—	RTC_XTALI	—	—
RTC_XTALO	AA19	VDD_SNVS_CAP	—	—	RTC_XTALO	—	—
SD1_CLK	B20	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO5_GPIO[15]	Input	Keeper
SD1_CMD	B21	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO5_GPIO[14]	Input	Keeper
SD1_DAT0	B23	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO5_GPIO[11]	Input	Keeper
SD1_DAT1	A23	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO5_GPIO[8]	Input	Keeper
SD1_DAT2	C22	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO5_GPIO[13]	Input	Keeper

Table 70. i.MX 6SoloLite Data Sheet Document Revision History (continued)

Rev. Number	Date	Substantive Change(s)
4 *Continued*	11/2016	• Section 4.2.2, "Power-Down Sequence," Replaced contents of section with sentence: "There are no special requirements on the power-down sequence other than …". • Section 4.5.2, "OSC32K": Removed text regarding coin cell from third paragraph and removed second NOTE about third party coin cell manufacturer. • Section 4.6, "I/O DC Parameters": Removed second bullet regarding single voltage GPIO cell set. • Section 4.6.1, "XTALI and RTC_XTALI (Clock Inputs) DC Parameters" Added NOTE after table.Table 20, "XTALI and RTC_XTALI DC Parameters": – Added parameter rows: Input capacitance; XTALI input leakage; and DC input current. – Added new footnote, "This voltage specification…" • Section 4.6.3, "*Single Voltage General Purpose I/O (GPIO) DC Parameters"* removed section. • Section 4.8, "Output Buffer Impedance Parameters": Removed second bullet "Single voltage General Purpose I/O cell set …". • Table 28, "DVGPIO Output Buffer Average Impedance (OVDD 1.8 V)": Changed all Typical values. • Table 29, "DVGPIO Output Buffer Average Impedance (OVDD 3.3 V)": Changed all Typical values. • Section 4.8.2, "*Single Voltage GPIO Output Buffer Impedance*": removed section. • Table 34, "EIM Bus Timing Parameters, Updates throughout table to include min/max values. • Table 35, "EIM Asynchronous Timing Parameters Table Relative Chip Select, Updates throughout table to include min/max values. • Section 4.9.4, "Multi-Mode DDR Controller (MMDC)," created this new section. • Removed: Section 4.9.5, "DDR SDRAM Specific Parameters (DDR3 and LPDDR2)," Section 4.9.5.1, "DDR3 Parameters," and Section 4.9.5.2, "LPDDR2 Parameters." • Table 37, "CSI Gated Clock Mode Timing Parameters," – Parameter P5 reduced (improved) from 10ns to 7.5 ns. – Parameter P6 reduced (improved) from 10ns to 7.5 ns. – Parameter P7 corrected to 66 MHz (no functional change). • Table 38, "CSI Ungated Clock Mode Timing Parameters," – Parameter P4 reduced (improved) from 10ns to 7.5 ns. – Parameter P5 reduced (improved) from 10ns to 7.5 ns. – Parameter P6 corrected to 66 MHz (no functional change). • Section 4.10.3.1, "ECSPI Master Mode Timing," Added new NOTE under Figure 25. • Section 4.10.3.2, "ECSPI Slave Mode Timing," Added new NOTE under Figure 26. • Section 4.10.4.3, "SDR50/SDR104 AC Timing Parameters," Figure 29 updated to correct SD5. • Table 43, "SDR50/SDR104 Interface Timing Parameters," – SD2, changed minimum value to "0.46", and changed maximum value to "0.54". – SD3, changed minimum value to "0.46", and changed maximum value to "0.54". – SD2 (parameter Clock High Time), parameter name corrected to SD3. – SD5, changed maximum value to "0.74". • Section 4.10.5, "HS200 Mode Timing Parameters," Added this new section. • Section 4.10.14, "USB PHY Parameters," Added new text to second paragraph "USB Host with the amendments below…" • Table 63, "Interfaces Allocation During Boot USDHC-1–USDHC-4 row, replaced existing text with "Refer to the table "SD/MMC…" • Table 65, "13 x 13 mm Supplies Contact Assignment," – GPANAIO: changed remark from "Analog pad" to "Analog output for NXP use…" – ZQPAD: changed remark to "Connect ZQPAD to…" • Table 66, "13 x 13 mm Functional Contact Assignments," DRAM_SDCLK_0, corrected "Input" to "Output" and Value to "0". • Section 6.2.2, "13 x 13 mm Ground, Power, Sense, Not Connected, and Reference Contact Assignments," Added new text "For most of the signals…" after Table 66. • Table 68, "13 x 13 mm, 0.5 mm Pitch Ball Map," ball AD6 name corrected to "DRAM_D18".