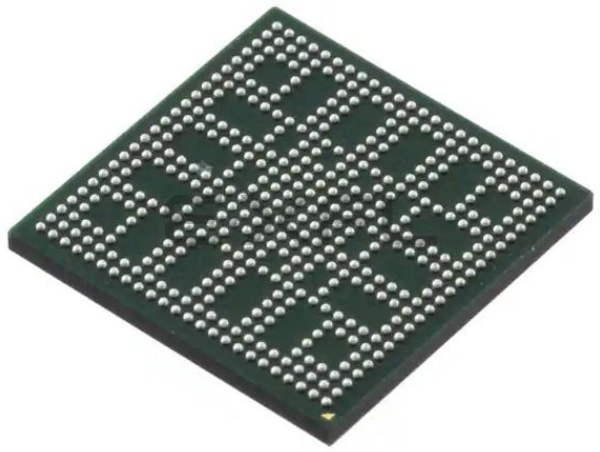

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, LVDDR3, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + PHY (3)
Voltage - I/O	1.2V, 1.8V, 3.0V
Operating Temperature	0°C ~ 95°C (TJ)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	432-TFBGA
Supplier Device Package	432-MAPBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6l3dvn10ac

NOTE

The actual feature set depends on the part numbers as described in Table 1, "Example Orderable Part Numbers," on page 3. Functions, such as 2D hardware graphics acceleration or E Ink may not be enabled for specific part numbers.

1.3 Updated Signal Naming Convention

The signal names of the i.MX6 series of products have been standardized to better align the signal names within the family and across the documentation. Some of the benefits of these changes are as follows:

- The names are unique within the scope of an SoC and within the series of products
- Searches will return all occurrences of the named signal
- The names are consistent between i.MX 6 series products implementing the same modules
- The module instance is incorporated into the signal name

This change applies only to signal names. The original ball names have been preserved to prevent the need to change schematics, BSDL models, IBIS models, and so on.

Throughout this document, the updated signal names are used except where referenced as a ball name (such as the Functional Contact Assignments table, Ball Map table, and so on). A master list of the signal name changes is in the document, *IMX 6 Series Signal Name Mapping* (EB792). This list can be used to map the signal names used in older documentation to the new standardized naming conventions.

3 Modules List

The i.MX 6SoloLite processor contains a variety of digital and analog modules. Table 2 describes these modules in alphabetical order.

Table 2. i.MX 6SoloLite Modules List

Block Mnemonic	Block Name	Subsystem	Brief Description
128x8 Fuse Box	Electrical Fuse Array	Security	Electrical Fuse Array. Enables to setup Boot Modes, Security Levels, Security Keys, and many other system parameters. The i.MX 6SoloLite processor consists of 2-128x8-bit fuse box accessible through OCOTP_CTRL interface.
ARM	ARM Platform	ARM	The ARM Cortex-A9 platform consists of a Cortex-A9 core version r2p10 and associated sub-blocks, including Level 2 Cache Controller, SCU (Snoop Control Unit), GIC (General Interrupt Controller), private timers, Watchdog, and CoreSight debug modules.
AUDMUX	Digital Audio Mux	Multimedia Peripherals	The AUDMUX is a programmable interconnect for voice, audio, and synchronous data routing between host serial interfaces (for example, SSI1, SSI2, and SSI3) and peripheral serial interfaces (audio and voice codecs). The AUDMUX has seven ports with identical functionality and programming models. A desired connectivity is achieved by configuring two or more AUDMUX ports.
CCM GPC SRC	Clock Control Module, General Power Controller, System Reset Controller	Clocks, Resets, and Power Control	These modules are responsible for clock and reset distribution in the system, and also for the system power management.
CSU	Central Security Unit	Security	The Central Security Unit (CSU) is responsible for setting comprehensive security policy within the i.MX 6SoloLite platform. The Security Control Registers (SCR) of the CSU are set during boot time by the HAB and are locked to prevent further writing.
CTI-1 CTI-2 CTI-3 CTI-4 CTI-5	Cross Trigger Interfaces	Debug / Trace	Cross Trigger Interfaces allows cross-triggering based on inputs from masters attached to CTIs. The CTI module is internal to the Cortex-A9 Core Platform.
CTM	Cross Trigger Matrix	Debug / Trace	Cross Trigger Matrix IP is used to route triggering events between CTIs. The CTM module is internal to the Cortex-A9 Core Platform.
DAP	Debug Access Port	System Control Peripherals	The DAP provides real-time access for the debugger without halting the core to: • System memory and peripheral registers • All debug configuration registers The DAP also provides debugger access to JTAG scan chains. The DAP module is internal to the Cortex-A9 Core Platform.
DCP	Data co-processor	Security	This module provides support for general encryption and hashing functions typically used for security functions. Because its basic job is moving data from memory to memory, it also incorporates a memory-copy (memcopy) function for both debugging and as a more efficient method of copying data between memory blocks than the DMA-based approach.

Table 2. i.MX 6SoloLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
eCSPI-1 eCSPI-2 eCSPI-3 eCSPI-4	Configurable SPI	Connectivity Peripherals	Full-duplex enhanced Synchronous Serial Interface. It is configurable to support Master/Slave modes, four chip selects to support multiple peripherals.
EIM	NOR-Flash /PSRAM interface	Connectivity Peripherals	The EIM NOR-FLASH / PSRAM provides: • Support 16-bit (in muxed IO mode only) PSRAM memories (sync and async operating modes), at slow frequency • Support 16-bit (in muxed IO mode only) NOR-Flash memories, at slow frequency • Multiple chip selects
EPDC	Electrophoretic Display Controller	Peripherals	The EPDC is a feature-rich, low power, and high-performance direct-drive, active matrix EPD controller. It is specifically designed to drive E Ink EPD panels, supporting a wide variety of TFT backplanes.
EPIT-1 EPIT-2	Enhanced Periodic Interrupt Timer	Timer Peripherals	Each EPIT is a 32-bit “set and forget” timer that starts counting after the EPIT is enabled by software. It is capable of providing precise interrupts at regular intervals with minimal processor intervention. It has a 12-bit prescaler for division of input clock frequency to get the required time setting for the interrupts to occur, and counter value can be programmed on the fly.
FEC	Fast Ethernet Controller	Connectivity Peripherals	The Ethernet Media Access Controller (MAC) is designed to support 10 and 100 Mbps Ethernet/IEEE 802.3 networks. An external transceiver interface and transceiver function are required to complete the interface to the media.
GPIO-1 GPIO-2 GPIO-3 GPIO-4 GPIO-5	General Purpose I/O Modules	System Control Peripherals	Used for general purpose input/output to external ICs. Each GPIO module supports 32 bits of I/O.
GPT	General Purpose Timer	Timer Peripherals	Each GPT is a 32-bit “free-running” or “set and forget” mode timer with programmable prescaler and compare and capture register. A timer counter value can be captured using an external event and can be configured to trigger a capture event on either the leading or trailing edges of an input pulse. When the timer is configured to operate in “set and forget” mode, it is capable of providing precise interrupts at regular intervals with minimal processor intervention. The counter has output compare logic to provide the status and interrupt at comparison. This timer can be configured to run either on an external clock or on an internal clock.
GPU2Dv2	Graphics Processing Unit-2D, ver 2	Multimedia Peripherals	The GPU2Dv2 provides hardware acceleration for 2D graphics algorithms, such as Bit BLT, stretch BLT, and many other 2D functions.
GPUVGv2	Vector Graphics Processing Unit, ver2	Multimedia Peripherals	OpenVG graphics accelerator provides OpenVG 1.1 support as well as other accelerations, including Real-time hardware curve tesselation of lines, quadratic and cubic Bezier curves, 16x Line Anti-aliasing, and various Vector Drawing functions.
I^2C-1 I^2C-2 I^2C-3	I^2C Interface	Connectivity Peripherals	I^2C provide serial interface for external devices. Data rates of up to 400 kbps are supported.

Table 2. i.MX 6SoloLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
PXP	PiXel Processing Pipeline	Display Peripherals	A high-performance pixel processor capable of 1 pixel/clock performance for combined operations, such as color-space conversion, alpha blending, gamma-mapping, and rotation. The PXP isenhanced with features specifically for gray scale applications. In addition, the PXP supports traditional pixel/frame processing paths for still-image and video processing applications, allowing it to interface with either of the integrated EPD controllers.
RAM 128 KB	Internal RAM	Internal Memory	Internal RAM, which is accessed through OCRAM memory controller.
RNGB	Random Number Generator	Security	Random number generating module.
ROM 96KB	Boot ROM	Internal Memory	Supports secure and regular Boot Modes. Includes read protection on 4K region for content protection.
ROMCP	ROM Controller with Patch	Data Path	ROM Controller with ROM Patch support.
SDMA	Smart Direct Memory Access	System Control Peripherals	The SDMA is multi-channel flexible DMA engine. It helps in maximizing system performance by off-loading the various cores in dynamic data routing. It has the following features: • Powered by a 16-bit Instruction-Set micro-RISC engine • Multi-channel DMA supporting up to 32 time-division multiplexed DMA channels • 48 events with total flexibility to trigger any combination of channels • Memory accesses including linear, FIFO, and 2D addressing • Shared peripherals between ARM and SDMA • Very fast Context-Software switching with 2-level priority based preemptive multi-tasking • DMA units with auto-flush and prefetch capability • Flexible address management for DMA transfers (increment, decrement, and no address changes on source and destination address) • DMA ports can handle unit-directional and bi-directional flows (copy mode) • Up to 8-word buffer for configurable burst transfers • Support of byte-swapping and CRC calculations • Library of Scripts and API is available
SJC	System JTAG Controller	System Control Peripherals	The SJC provides JTAG interface, which complies with JTAG TAP standards, to internal logic. The i.MX 6SoloLite processor uses JTAG port for production, testing, and system debugging. In addition, the SJC provides BSR (Boundary Scan Register) standard support, which complies with IEEE1149.1 and IEEE1149.6 standards. The JTAG port must be accessible during platform initial laboratory bring-up, for manufacturing tests and troubleshooting, as well as for software debugging by authorized entities. The i.MX 6SoloLite SJC incorporates three security modes for protecting against unauthorized accesses. Modes are selected through eFUSE configuration.
SNVS	Secure Non-Volatile Storage	Security	Secure Non-Volatile Storage, including Secure Real Time Clock, Security State Machine, Master Key Control, and Violation/Tamper Detection and reporting.
SPDIF	Sony Phillips Digital Interface	Multimedia Peripherals	A standard audio file transfer format, developed jointly by the Sony and Phillips corporations. Has Transmitter and Receiver functionality.

Table 3. Special Signal Considerations (continued)

Signal Name	Remarks
RTC_XTALI/ RTC_XTALO	If the user wishes to configure RTC_XTALI and RTC_XTALO as an RTC oscillator, a 32.768 kHz crystal (≤100 kΩ ESR, 10 pF load) should be connected between RTC_XTALI and RTC_XTALO. Keep in mind the capacitors implemented on either side of the crystal are about twice the crystal load capacitor. To hit the exact oscillation frequency, the board capacitors need to be reduced to account for board and chip parasitics. The integrated oscillation amplifier is self biasing, but relatively weak. Care must be taken to limit parasitic leakage from RTC_XTALI and RTC_XTALO to either power or ground (>100 MΩ). This will debias the amplifier and cause a reduction of startup margin. Typically RTC_XTALI and RTC_XTALO should bias to approximately 0.5 V. If it is desired to feed an external low frequency clock into RTC_XTALI, the RTC_XTALO pin must remain unconnected or driven with a complimentary signal. The logic level of this forcing clock should not exceed VDD_SNVS_CAP level and the frequency should be <100 kHz under typical conditions. In the case when a high accuracy real time clock is not required, the system may use an internal low frequency ring oscillator. It is recommended to connect RTC_XTALI to GND and leave RTC_XTALO unconnected.
TEST_MODE	TEST_MODE is for NXP factory use. This signal is internally connected to an on-chip pull-down device. The user must either leave this signal unconnected or tie it to GND.
XTALI/XTALO	• A 24.0 MHz crystal must be connected between XTALI and XTALO. The level and frequency must be <32 MHz under typical conditions. • The crystal must be rated for a maximum drive level of 250 μW. An ESR (equivalent series resistance) of typically 80 Ω is recommended. NXP BSP (board support package) software requires 24 MHz on XTALI/XTALO. • The crystal can be eliminated if an external 24 MHz oscillator is available in the system. In this case, XTALI must be directly driven by the external oscillator and XTALO remains unconnected. The XTALI signal level must swing from ~0.8 x NVCC_PLL_OUT to ~0.2 V. • This clock is used as a reference for USB, so there are strict frequency tolerance and jitter requirements. • See the XTALOSC chapter and relevant interface specifications chapters of the i.MX 6SoloLite reference manual (IMX6SLRM), for details.
ZQPAD	DRAM calibration resistor 240 Ω 1% used as reference during DRAM output buffer driver calibration should be connected between this pad and GND.

Table 4. JTAG Controller Interface Summary

JTAG	I/O Type	On-Chip Termination
JTAG_TCK	Input	47 kΩ pull-up
JTAG_TMS	Input	47 kΩ pull-up
JTAG_TDI	Input	47 kΩ pull-up
JTAG_TDO	3-state output	Keeper
JTAG_TRST_B	Input	47 kΩ pull-up
JTAG_MODE	Input	100 kΩ pull-up

3.2 Recommended Connections for Unused Analog Interfaces

Table 5 shows the recommended connections for unused analog interfaces.

Table 5. Recommended Connections for Unused Analog Interfaces

Module	Pad Name	Recommendations if Unused?
XTALOSC	XTALOSC_CLK1_N, XTALOSC_CLK1_P	Leave unconnected
USB	USB_OTGx_DN, USB_OTGx_DP, USB_OTGx_VBUS, USB_OTG_CHD_B	Leave unconnected

4 Electrical Characteristics

This section provides the device and module-level electrical characteristics for the i.MX 6SoloLite.

4.1 Chip-Level Conditions

This section provides the device-level electrical characteristics for the IC. See Table 6 for a quick reference to the individual tables and sections.

Table 6. i.MX 6SoloLite Chip-Level Conditions

For these characteristics, …	Topic appears …
Absolute Maximum Ratings	on page 18
BGA Case 2240 Package Thermal Resistance	on page 19
Operating Ranges	on page 21
External Clock Sources	on page 23
Maximum Supply Currents	on page 24
Low Power Mode Supply Currents	on page 25
USB PHY Current Consumption	on page 26

4.1.1 Absolute Maximum Ratings

CAUTION

Stresses beyond those listed under Table 7 may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the Table 9, "Operating Ranges" or subsequent parameters tables is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 7 provides the absolute maximum operating ratings.

Table 9. Operating Ranges (continued)

Parameter Description	Symbol	Min	Typ	Max[1]	Unit	Comment
GPIO supplies[6]	NVCC33_IO	2.8	3.0	3.3	V	Worst case, assuming all SOC I/O operating at 1.8V. NVCC33_IO must always be greater than NVCC18_IO.
	NVCC18_IO	1.62	1.8	1.98	V	—
	NVCC_1P2V	1.14	1.2	1.3	V	—
Junction temperature	T_J	0	—	95	°C	Commercial See *i.MX 6SoloLite Product Lifetime Usage Estimates Application Note*, AN4726, for information on product lifetime (power-on years) for this processor.
Junction temperature	T_J	-40	—	105	—	Extended commercial See *i.MX 6SoloLite Product Lifetime Usage Estimates Application Note*, AN4726, for information on product lifetime (power-on years) for this processor.

1 Applying the maximum voltage results in maximum power consumption and heat generation. NXP recommends a voltage set point = (Vmin + the supply tolerance). This results in an optimized power/speed ratio.

2 VDD_ARM_IN and VDD_SOC_IN must be at least 125 mV higher than the LDO Output Set Point for correct voltage regulation.

3 VDD_SOC_CAP and VDD_PU_CAP must be equal.

4 VDD_SOC and VDD_PU output voltage must be set to this rule: VDD_ARM - VDD_SOC / VDD_PU < 50mV.

5 While setting VDD_SNVS_IN voltage with respect to Charging Currents and RTC, refer to Hardware Development Guide for i.MX 6Dual, 6Quad, 6Solo, 6DualLite Families of Applications Processors (IMX6DQ6SDLHDG).

6 All digital I/O supplies (NVCC_xxxx) must be powered under normal conditions whether the associated I/O pins are in use or not, and associated I/O pins need to have a pull-up or pull-down resistor applied to limit any floating gate current.

4.1.4 External Clock Sources

Each i.MX 6SoloLite processor has two external input system clocks: a low frequency (RTC_XTALI) and a high frequency (XTALI).

The RTC_XTALI is used for low-frequency functions. It supplies the clock for wake-up circuit, power-down real time clock operation, and slow system and watchdog counters. The clock input can be connected to either an external oscillator or a crystal using the internal oscillator amplifier. Additionally, there is an internal ring oscillator, which can substitute the RTC_XTALI, in case accuracy is not important.

The system clock input XTALI is used to generate the main system clock. It supplies the PLLs and other peripherals. The system clock input can be connected to either an external oscillator or a crystal using the internal oscillator amplifier.

NOTE

The internal RTC oscillator does not provide an accurate frequency and is affected by process, voltage, and temperature variations. NXP strongly recommends using an external crystal as the RTC_XTALI reference. If the internal oscillator is used instead, careful consideration must be given to the timing implications on all of the SoC modules dependent on this clock.

Table 11. Maximum Supply Currents

Power Line	Conditions	Max Current	Unit
VDD_ARM_IN	1 GHz ARM clock based on Power Virus operation	1100	mA
VDD_SOC_IN	1 GHz ARM clock	650	mA
VDD_PU_IN	1 GHz ARM clock	150	mA
VDD_HIGH_IN	—	30[1]	mA
VDD_SNVS_IN	—	250[2]	µA
USB_OTG1_VBUS USB_OTG2_VBUS	—	25[3]	mA
Primary Interface (IO) Supplies			
NVCC_DRAM	—	(see[4])	
NVCC33_IO	N=156	Use maximum IO Equation[5]	
NVCC18_IO	N=156	Use maximum IO Equation[5]	
NVCC_1P2V	N=2	Use maximum IO Equation[5]	mA
MISC			
DRAM_VREF	—	1	mA

1 The actual maximum current drawn from VDD_HIGH_IN will be as shown plus any additional current drawn from the VDD_HIGH_CAP outputs, depending upon actual application configuration (for example, NVCC_DRAM_2P5 supplies).

2 The maximum VDD_SNVS_IN current may be higher depending on specific operating configurations, such as BOOT_MODE[1:0] not equal to 00, or use of the Tamper feature. During initial power on, VDD_SNVS_IN can draw up to 1 mA, if available. VDD_SNVS_CAP charge time will increase if less than 1 mA is available.

3 This is the maximum current per active USB physical interface.

4 The DRAM power consumption is dependent on several factors, such as external signal termination. DRAM power calculators are typically available from the memory vendors. They take in account factors, such as signal termination.
See the i.MX 6SoloLite Power Consumption Measurement Application Note or examples of DRAM power consumption during specific use case scenarios.

5 General equation for estimated, maximum power consumption of an IO power supply:

Imax = N x C x V x (0.5 x F)

Where:

N—Number of IO pins supplied by the power line

C—Equivalent external capacitive load

V—IO voltage

(0.5 xF)—Data change rate. Up to 0.5 of the clock rate (F)

In this equation, Imax is in Amps, C in Farads, V in Volts, and F in Hertz.

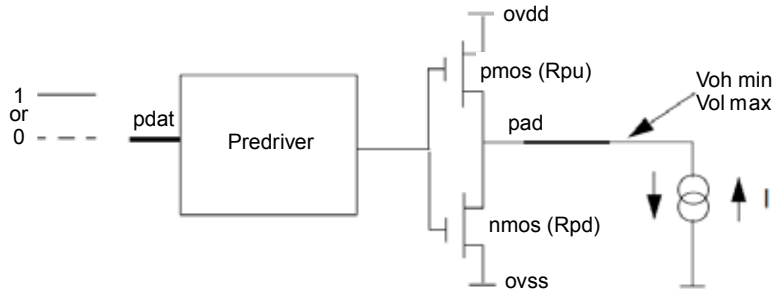

Figure 4. Circuit for Parameters Voh and Vol for I/O Cells

4.6.1 XTALI and RTC_XTALI (Clock Inputs) DC Parameters

Table 20 shows the DC parameters for the clock inputs.

Table 20. XTALI and RTC_XTALI DC Parameters

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
XTALI high-level DC input voltage	Vih	—	0.8 x NVCC_PLL_OUT	—	NVCC_PLL_ OUT	V
XTALI low-level DC input voltage	Vil	—	0	—	0.2V	V
RTC_XTALI high-level DC input voltage	Vih	—	0.8	—	1.1[1]	V
RTC_XTALI low-level DC input voltage	Vil	—	0	—	0.2V	V
Input capacitance	C_{IN}	Simulated data	—	5	—	pF
XTALI input leakage at startup	$I_{XTALI\_STARTUP}$	Power-on startup for 0.15 msec with a driven 24 MHz RTC clock @1.1 V. [2]	—	—	600	µA
DC input current	I_{XTALI_DC}	—	—	—	2.5	µA

[1] This voltage specification must not be exceeded and, as such, is an absolute maximum specification.

[2] This current draw is present even if an external clock source directly drives XTALI.

NOTE

The Vil and Vih specifications only apply when an external clock source is used. If a crystal is used, Vil and Vih do not apply.

4.6.2 Dual Voltage General Purpose IO Cell Set (DVGPIO) DC Parameters

Table 21 shows DC parameters for GPIO pads. The parameters in Table 21 are guaranteed per the operating ranges in Table 9, unless otherwise noted.

4.7.2 DDR I/O AC Parameters

Table 26 shows the AC parameters for DDR I/O operating in LPDDR2 mode. For details on supported DDR memory configurations, see Section 4.9.4, "Multi-Mode DDR Controller (MMDC)".

Table 26. DDR I/O LPDDR2 Mode AC Parameters[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
AC input logic high	Vih(ac)	—	Vref + 0.22	—	OVDD	V
AC input logic low	Vil(ac)	—	0	—	Vref – 0.22	V
AC differential input high voltage[2]	Vidh(ac)	—	0.44	—	—	V
AC differential input low voltage	Vidl(ac)	—	—	—	0.44	V
Input AC differential cross point voltage[3]	Vix(ac)	Relative to Vref	-0.12	—	0.12	V
Over/undershoot peak	Vpeak	—	—	—	0.35	V
Over/undershoot area (above OVDD or below OVSS)	Varea	400 MHz	—	—	0.3	V-ns
Single output slew rate, measured between Vol (ac) and Voh (ac)	tsr	50 Ω to Vref. 5 pF load. Drive impedance = 4 0 Ω ±30%	1.5	—	3.5	V/ns
		50 Ω to Vref. 5pF load. Drive impedance = 60 Ω ±30%	1	—	2.5	
Skew between pad rise/fall asymmetry + skew caused by SSN	t_{SKD}	clk = 400 MHz	—	—	0.1	ns

1 Note that the JEDEC LPDDR2 specification (JESD209_2B) supersedes any specification in this document.

2 Vid(ac) specifies the input differential voltage |Vtr – Vcp| required for switching, where Vtr is the "true" input signal and Vcp is the "complementary" input signal. The Minimum value is equal to Vih(ac) – Vil(ac).

3 The typical value of Vix(ac) is expected to be about 0.5 × OVDD. and Vix(ac) is expected to track variation of OVDD. Vix(ac) indicates the voltage at which differential input signal must cross.

Table 27 shows the AC parameters for DDR I/O operating in DDR3 mode.

Table 27. DDR I/O DDR3 Mode AC Parameters[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
AC input logic high	Vih(ac)	—	Vref + 0.175	—	OVDD	V
AC input logic low	Vil(ac)	—	0	—	Vref – 0.175	V
AC differential input voltage[2]	Vid(ac)	—	0.35	—	—	V
Input AC differential cross point voltage[3]	Vix(ac)	Relative to Vref	Vref – 0.15	—	Vref + 0.15	V
Over/undershoot peak	Vpeak	—	—	—	0.4	V
Over/undershoot area (above OVDD or below OVSS)	Varea	400 MHz	—	—	0.5	V-ns

Table 27. DDR I/O DDR3 Mode AC Parameters[1] (continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Single output slew rate, measured between Vol (ac) and Voh (ac)	tsr	Driver impedance = 34 Ω	2.5	—	5	V/ns
Skew between pad rise/fall asymmetry + skew caused by SSN	t_{SKD}	clk = 400 MHz	—	—	0.1	ns

1 Note that the JEDEC JESD79_3C specification supersedes any specification in this document.

2 Vid(ac) specifies the input differential voltage |Vtr-Vcp| required for switching, where Vtr is the “true” input signal and Vcp is the “complementary” input signal. The Minimum value is equal to Vih(ac) – Vil(ac).

3 The typical value of Vix(ac) is expected to be about 0.5 × OVDD. and Vix(ac) is expected to track variation of OVDD. Vix(ac) indicates the voltage at which differential input signal must cross.

4.8 Output Buffer Impedance Parameters

This section defines the I/O impedance parameters of the i.MX 6SoloLite processor for the following I/O types:

- Dual Voltage General Purpose I/O cell set (DVGPIO)
- Double Data Rate I/O (DDR) for LPDDR2, and DDR3 modes

NOTE

GPIO and DDR I/O output driver impedance is measured with “long” transmission line of impedance Ztl attached to I/O pad and incident wave launched into transmission line. Rpu/Rpd and Ztl form a voltage divider that defines specific voltage of incident wave relative to OVDD. Output driver impedance is calculated from this voltage divider (see Figure 7).

Table 34. EIM Bus Timing Parameters (continued)

ID	Parameter	Min[1]	Max[1]	Unit
WE5	Clock rise to address invalid	0.5 × t × (k+1) -1.25	0.5 × t × (k+1) +2.25	ns
WE6	Clock rise to EIM_CSx_B valid	-0.5 × t × (k+1) -1.25	-0.5 × t × (k+1) +2.25	ns
WE7	Clock rise to EIM_CSx_B invalid	0.5 × t × (k+1) -1.25	0.5 × t × (k+1) +2.25	ns
WE8	Clock rise to EIM_RW_B valid	-0.5 × t × (k+1) -1.25	-0.5 × t × (k+1) +2.25	ns
WE9	Clock rise to EIM_RW_B invalid	0.5 × t × (k+1) -1.25	0.5 × t × (k+1) +2.25	ns
WE10	Clock rise to EIM_OE_B valid	-0.5 × t × (k+1) -1.25	-0.5 × t × (k+1) +2.25	ns
WE11	Clock rise to EIM_OE_B invalid	0.5 × t × (k+1) -1.25	0.5 × t × (k+1) +2.25	ns
WE12	Clock rise to EIM_EBx_B valid	0.5 × t × (k+1) -1.25	-0.5 × t × (k+1) +2.25	ns
WE13	Clock rise to EIM_EBx_B invalid	0.5 × t × (k+1) -1.25	0.5 × t × (k+1) +2.25	ns
WE14	Clock rise to EIM_LBA_B valid	-0.5 × t × (k+1) -1.25	-0.5 × t × (k+1) +2.25	ns
WE15	Clock rise to EIM_LBA_B invalid	0.5 × t × (k+1) -1.25	0.5 × t × (k+1) +2.25	ns
WE16	Clock rise to output data valid	-0.5 × t × (k+1) -1.25	-0.5 × t × (k+1) +2.25	ns
WE17	Clock rise to output data invalid	0.5 × t × (k+1) -1.25	0.5 × t × (k+1) +2.25	ns
WE18	Input data setup time to clock rise	2.3	—	ns
WE19	Input data hold time from clock rise	2	—	ns
WE20	EIM_WAIT_B setup time to clock rise	2	—	ns
WE21	EIM_WAIT_B hold time from clock rise	2	—	ns

1 k represents register setting BCD value

2 t is clock period (1/Freq). For 104 MHz, t = 9.165 ns

4.10.7 I²C Module Timing Parameters

This section describes the timing parameters of the I²C module. Figure 32 depicts the timing of I²C module, and Table 46 lists the I²C module timing characteristics.

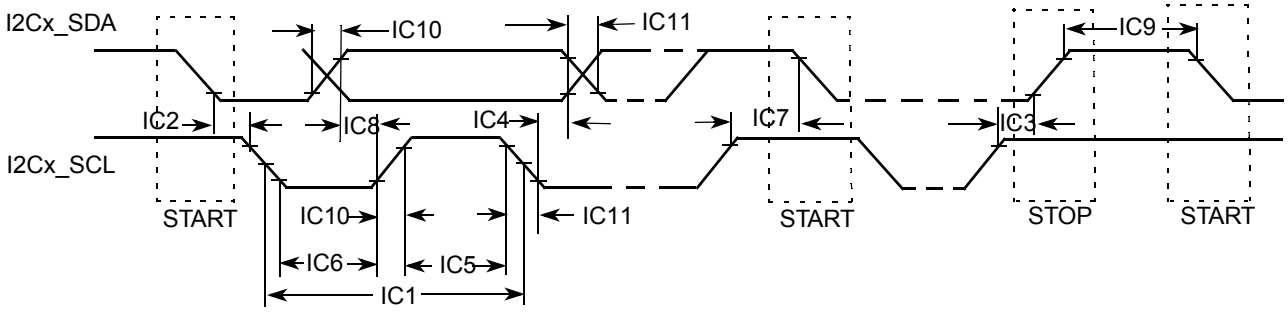

Figure 32. I²C Bus Timing Diagram

Table 46. I²C Module Timing Parameters

ID	Parameter	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
IC1	I2Cx_SCL cycle time	10	—	2.5	—	µs
IC2	Hold time (repeated) START condition	4.0	—	0.6	—	µs
IC3	Set-up time for STOP condition	4.0	—	0.6	—	µs
IC4	Data hold time	0[1]	3.45[2]	0[1]	0.9[2]	µs
IC5	HIGH Period of I2Cx_SCL	4.0	—	0.6	—	µs
IC6	LOW Period of the I2Cx_SCL	4.7	—	1.3	—	µs
IC7	Set-up time for a repeated START condition	4.7	—	0.6	—	µs
IC8	Data set-up time	250	—	100[3]	—	ns
IC9	Bus free time between a STOP and START condition	4.7	—	1.3	—	µs
IC10	Rise time of both I2Cx_SDA and I2Cx_SCL signals	—	1000	$20 + 0.1C_b$[4]	300	ns
IC11	Fall time of both I2Cx_SDA and I2Cx_SCL signals	—	300	$20 + 0.1C_b$[4]	300	ns
IC12	Capacitive load for each bus line (C_b)	—	400	—	400	pF

1 A device must internally provide a hold time of at least 300 ns for I2Cx_SDA signal in order to bridge the undefined region of the falling edge of I2Cx_SCL.

2 The maximum hold time has only to be met if the device does not stretch the LOW period (ID no IC5) of the I2Cx_SCL signal.

3 A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement of Set-up time (ID No IC7) of 250 ns must be met. This automatically is the case if the device does not stretch the LOW period of the I2Cx_SCL signal. If such a device does stretch the LOW period of the I2Cx_SCL signal, it must output the next data bit to the I2Cx_SDA line max_rise_time (IC9) + data_setup_time (IC7) = 1000 + 250 = 1250 ns (according to the Standard-mode I2C-bus specification) before the I2Cx_SCL line is released.

4 C_b = total capacitance of one bus line in pF.

Table 51. SSI Transmitter Timing with Internal Clock

ID	Parameter	Min	Max	Unit
Internal Clock Operation				
SS1	AUDx_TXC/AUDx_RXC clock period	81.4	—	ns
SS2	AUDx_TXC/AUDx_RXC clock high period	36.0	—	ns
SS4	AUDx_TXC/AUDx_RXC clock low period	36.0	—	ns
SS6	AUDx_TXC high to AUDx_TXFS (bl) high	—	15.0	ns
SS8	AUDx_TXC high to AUDx_TXFS (bl) low	—	15.0	ns
SS10	AUDx_TXC high to AUDx_TXFS (wl) high	—	15.0	ns
SS12	AUDx_TXC high to AUDx_TXFS (wl) low	—	15.0	ns
SS14	AUDx_TXC/AUDx_RXC Internal AUDx_TXFS rise time	—	6.0	ns
SS15	AUDx_TXC/AUDx_RXC Internal AUDx_TXFS fall time	—	6.0	ns
SS16	AUDx_TXC high to AUDx_TXD valid from high impedance	—	15.0	ns
SS17	AUDx_TXC high to AUDx_TXD high/low	—	15.0	ns
SS18	AUDx_TXC high to AUDx_TXD high impedance	—	15.0	ns
Synchronous Internal Clock Operation				
SS42	AUDx_RXD setup before AUDx_TXC falling	10.0	—	ns
SS43	AUDx_RXD hold after AUDx_TXC falling	0.0	—	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TXC/RXC = 0) and a non-inverted frame sync (TXFS/RXFS = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal TXC/RXC and/or the frame sync TXFS/RXFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is used for data transfer.
- The terms, WL and BL, refer to Word Length(WL) and Bit Length(BL).
- For internal Frame Sync operation using external clock, the FS timing is same as that of TXD (for example, during AC97 mode of operation).

4.10.11.3 SSI Transmitter Timing with External Clock

Figure 42 depicts the SSI transmitter external clock timing and Table 53 lists the timing parameters for the transmitter timing with the external clock.

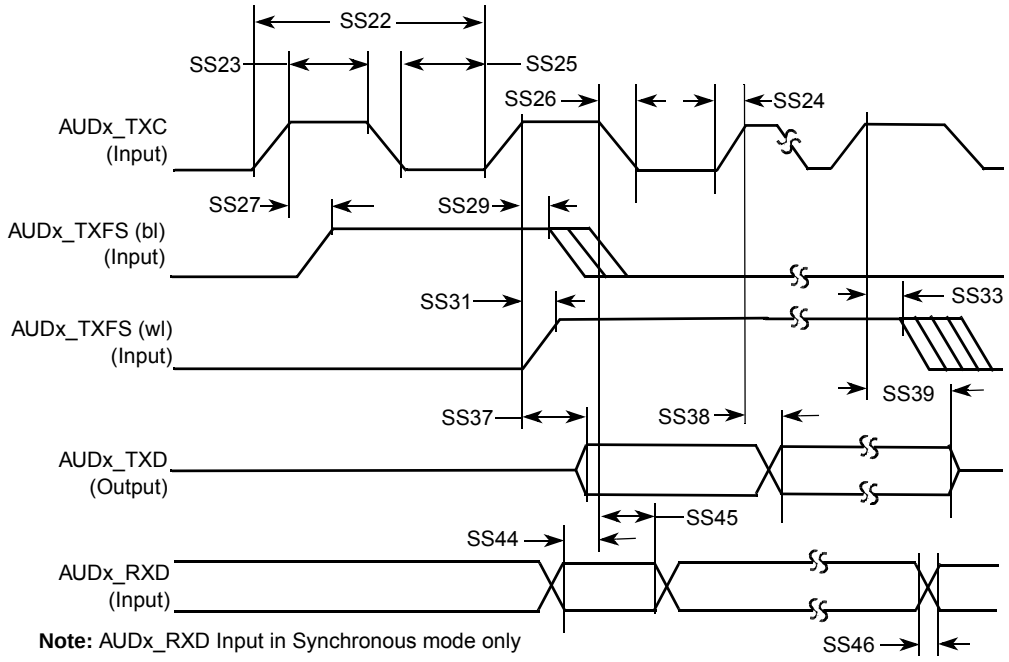

Figure 42. SSI Transmitter External Clock Timing Diagram

Table 53. SSI Transmitter with External Clock Timing Parameters

ID	Parameter	Min	Max	Unit
External Clock Operation				
SS22	AUDx_TXC/AUDx_RXC clock period	81.4	—	ns
SS23	AUDx_TXC/AUDx_RXC clock high period	36.0	—	ns
SS24	AUDx_TXC/AUDx_RXC clock rise time	—	6.0	ns
SS25	AUDx_TXC/AUDx_RXC clock low period	36.0	—	ns
SS26	AUDx_TXC/AUDx_RXC clock fall time	—	6.0	ns
SS27	AUDx_TXC high to AUDx_TXFS (bl) high	–10.0	15.0	ns
SS29	AUDx_TXC high to AUDx_TXFS (bl) low	10.0	—	ns
SS31	AUDx_TXC high to AUDx_TXFS (wl) high	–10.0	15.0	ns
SS33	AUDx_TXC high to AUDx_TXFS (wl) low	10.0	—	ns
SS37	AUDx_TXC high to AUDx_TXD valid from high impedance	—	15.0	ns
SS38	AUDx_TXC high to AUDx_TXD high/low	—	15.0	ns
SS39	AUDx_TXC high to AUDx_TXD high impedance	—	15.0	ns

4.10.13.2 Receive Timing Parameters

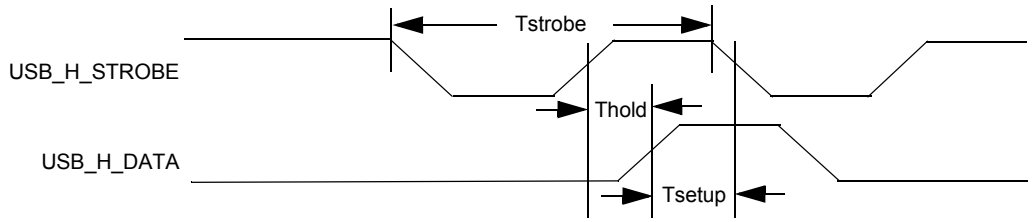

Figure 49. USB HSIC Receive Timing Diagram

Table 61. USB HSIC Receive Timing Parameters[1]

Name	Parameter	Min	Max	Unit	Comment
Tstrobe	Strobe period	4.166	4.167	ns	—
Thold	Data hold time	300	—	ps	Measured at 50% point
Tsetup	Data setup time	365	—	ps	Measured at 50% point
Tslew	Strobe/data rising/falling time	0.7	2	V/ns	Averaged from 30% – 70% points

1 The timings in the table are guaranteed when:
—AC I/O voltage is between 0.9x to 1x of the I/O supply
—DDR_SEL configuration bits of the I/O are set to (10)b

4.10.14 USB PHY Parameters

This section describes the USB-OTG PHY and the USB Host port PHY parameters.
The USB PHY meets the electrical compliance requirements defined in the Universal Serial Bus Revision 2.0 OTG, USB Host with the amendments below (On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification is not applicable to Host port).

- USB ENGINEERING CHANGE NOTICE
  - Title: 5V Short Circuit Withstand Requirement Change
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- Errata for USB Revision 2.0 April 27, 2000 as of 12/7/2000
- USB ENGINEERING CHANGE NOTICE
  - Title: Pull-up/Pull-down resistors
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- USB ENGINEERING CHANGE NOTICE
  - Title: Suspend Current Limit Changes
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- USB ENGINEERING CHANGE NOTICE
  - Title: USB 2.0 Phase Locked SOFs
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification
  - Revision 2.0 plus errata and ecn June 4, 2010

Table 66. 13 x 13 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group[1]	Ball Type	Out of Reset Condition[2]			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value[3]
KEY_ROW6	C24	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO4_GPIO[5]	Input	Keeper
KEY_ROW7	B24	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO4_GPIO[7]	Input	Keeper
LCD_CLK	T22	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[15]	Input	Keeper
LCD_DAT0	Y24	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[20]	Input	Keeper
LCD_DAT1	W23	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[21]	Input	Keeper
LCD_DAT10	R23	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[30]	Input	Keeper
LCD_DAT11	R24	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[31]	Input	Keeper
LCD_DAT12	P23	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[0]	Input	Keeper
LCD_DAT13	P24	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[1]	Input	Keeper
LCD_DAT14	N21	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[2]	Input	Keeper
LCD_DAT15	N23	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[3]	Input	Keeper
LCD_DAT16	N24	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[4]	Input	Keeper
LCD_DAT17	M22	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[5]	Input	Keeper
LCD_DAT18	M23	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[6]	Input	Keeper
LCD_DAT19	M24	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[7]	Input	Keeper
LCD_DAT2	W24	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[22]	Input	Keeper
LCD_DAT20	L23	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[8]	Input	Keeper
LCD_DAT21	L24	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[9]	Input	Keeper
LCD_DAT22	K23	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[10]	Input	Keeper
LCD_DAT23	K24	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[11]	Input	Keeper
LCD_DAT3	V23	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[23]	Input	Keeper
LCD_DAT4	V24	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[24]	Input	Keeper

Table 66. 13 x 13 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group[1]	Ball Type	Out of Reset Condition[2]			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value[3]
TAMPER	Y18	VDD_SNVS_IN	GPIO	ALT0	SNVS_TAMPER	Input	—
TEST_MODE	U15	VDD_SNVS_IN	GPIO	ALT0	TEST_MODE	Input	—
UART1_RXD	B19	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[16]	Input	Keeper
UART1_TXD	D19	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[17]	Input	Keeper
USB_OTG_CHD_B	AC22	VDD_USB_CAP	ANALOG	—	USB_OTG_CHD_B	—	—
USB_OTG1_DN	AD19	VDD_USB_CAP	ANALOG	—	USB_OTG1_DN	—	—
USB_OTG1_DP	AC19	VDD_USB_CAP	ANALOG	—	USB_OTG1_DP	—	—
USB_OTG2_DN	AD17	VDD_USB_CAP	ANALOG	—	USB_OTG2_DN	—	—
USB_OTG2_DP	AC17	VDD_USB_CAP	ANALOG	—	USB_OTG2_DP	—	—
WDOG_B	F18	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[18]	Input	Keeper
XTALI	AD21	NVCC_PLL	ANALOG	—	XTALI	—	—
XTALO	AC21	NVCC_PLL	ANALOG	—	XTALO	—	—
ZQPAD	H2	NVCC_DRAM	ZQPAD	—	DRAM_ZQPAD	Input	Hi-Z

1 All balls marked Power Group NVCC33_IO or NVCC18_IO are dual-voltage IOs. The user supplies NVCC33_IO and NVCC18_IO. In the IOMUX for each ball, the user selects either 3.3 V or 1.8 V operation using the LVE field in the Pad Control Register for each ball.

2 The state immediately after reset and before ROM firmware or software has executed.

3 Variance of the pull-up and pull-down strengths are shown in the tables as follows:

- Table 21, "DVGPIO I/O DC Parameters," on page 33
- Table 22, "LPDDR2 I/O DC Electrical Parameters," on page 34
- Table 23, "DDR3 I/O DC Electrical Parameters," on page 34

For most of the signals, the state during reset is same as the state after reset, given in the *Out of Reset Condition* column of Table 66. However, there are some signals for which the state during reset is different from the state after reset. These signals along with their state during reset are given in Table 67.

Table 67. Signals with Differing Before Reset and After Reset States

Ball name	Before Reset State	
	Input/Output	Value
EIM_A16	**Input**	PD (100k)
EIM_A17	**Input**	PD (100k)
EIM_A18	**Input**	PD (100k)
EIM_A19	**Input**	PD (100k)
EIM_A20	**Input**	PD (100k)
EIM_A21	**Input**	PD (100k)

Table 68. 13 x 13 mm, 0.5 mm Pitch Ball Map (continued)

	1	2	3	4	5	6	7	8
A	GND	DRAM_SDQS3_B	DRAM_D24	GND	DRAM_D27	DRAM_D29	GND	DRAM_D31
B	DRAM_D14	DRAM_D15	DRAM_SDQS3	DRAM_D25	DRAM_D26	DRAM_D28	DRAM_D30	EPDC_SDLE
C	DRAM_D12	DRAM_D13	DRAM_DQM3	**NC**	**NC**	GND	EPDC_VCOM0	**NC**
D	GND	GND	DRAM_D11	**NC**	**NC**	DRAM_RESET	EPDC_VCOM1	**NC**
E	DRAM_D9	DRAM_D8	DRAM_D10	DRAM_SDODT1	GND	NVCC_DRAM	EPDC_SDOE	**NC**
F	DRAM_SDQS1	DRAM_SDQS1_B	**NC**	**NC**	**NC**	**NC**	EPDC_SDSHR	**NC**
G	GND	DRAM_DQM1	**NC**	**NC**	**NC**	**NC**	NVCC_DRAM	GND
H	DRAM_SDBA2	ZQPAD	GND	DRAM_A7	DRAM_A13	NVCC_DRAM	GND	**NC**
J	DRAM_SDBA0	DRAM_A10	DRAM_A8	DRAM_A9	GND	NVCC_DRAM	VDD_SOC_CAP	VDD_SOC_CAP
K	GND	DRAM_A15	**NC**	**NC**	**NC**	**NC**	VDD_SOC_CAP	VDD_SOC_CAP
L	DRAM_SDCLK_0	DRAM_CS1	**NC**	**NC**	**NC**	**NC**	GND	**NC**
M	DRAM_SDCLK_0_B	DRAM_SDCKE1	DRAM_A5	DRAM_A6	GND	NVCC_DRAM_2P5	GND	GND
N	DRAM_RAS	DRAM_CS0	GND	DRAM_A4	DRAM_VREF	NVCC_DRAM	GND	GND
P	DRAM_CAS	SDCKE0	**NC**	**NC**	**NC**	**NC**	NVCC_DRAM	**NC**
R	GND	DRAM_A14	**NC**	**NC**	**NC**	**NC**	VDD_PU_CAP	VDD_PU_CAP
T	DRAM_SDBA1	DRAM_A11	DRAM_A2	DRAM_A3	GND	NVCC_DRAM	VDD_PU_CAP	VDD_PU_CAP
U	DRAM_SDWE	DRAM_A12	GND	DRAM_A0	DRAM_A1	NVCC_DRAM	GND	**NC**
V	GND	DRAM_DQM0	**NC**	**NC**	**NC**	**NC**	NVCC_DRAM	GND
W	DRAM_SDQS0_B	DRAM_SDQS0	**NC**	**NC**	**NC**	**NC**	NVCC_1P2	**NC**
Y	DRAM_D6	DRAM_D7	DRAM_D5	DRAM_SDODT0	GND	NVCC_DRAM	PWM1	**NC**
AA	GND	GND	DRAM_D4	**NC**	**NC**	HSIC_DAT	FEC_MDC	**NC**
AB	DRAM_D3	DRAM_D2	DRAM_DQM2	**NC**	**NC**	HSIC_STROBE	FEC_MDIO	**NC**
AC	DRAM_D1	DRAM_D0	DRAm_SDQS2	DRAM_D22	DRAM_D21	DRAM_D19	DRAM_D17	FEC_TX_CLK
AD	GND	DRAM_SDQS2_B	DRAM_D23	GND	DRAM_D20	DRAM_D18	GND	DRAM_D16

7 Revision History

Table 70 provides a history for revision 4 of this data sheet.

Table 70. i.MX 6SoloLite Data Sheet Document Revision History

Rev. Number	Date	Substantive Change(s)
5	9/2017	• Figure 1, "Part Number Nomenclature—i.MX 6SoloLite" Updates to the Silicon Revision column to include Rev. 1.4, C. • Table 1, "Example Orderable Part Numbers" Added "C" suffix part numbers and descriptions. • Section 4.8.2, "DDR I/O Output Buffer Impedance" Cross-reference change from JEDEC standards to MMDC section. • Table 42, "eMMC4.4/4.41 Interface Timing Parameters," Corrected SD3 Minimum from 2.6 to 1.7 ns. • Table 42, "eMMC4.4/4.41 Interface Timing Parameters," Added footnote related to Clock duty Cycle range. • Figure 30, "HS200 Mode Timing Diagram" Updated figure to remove extraneous ID callouts.

(*Revision History table continued on next page*)