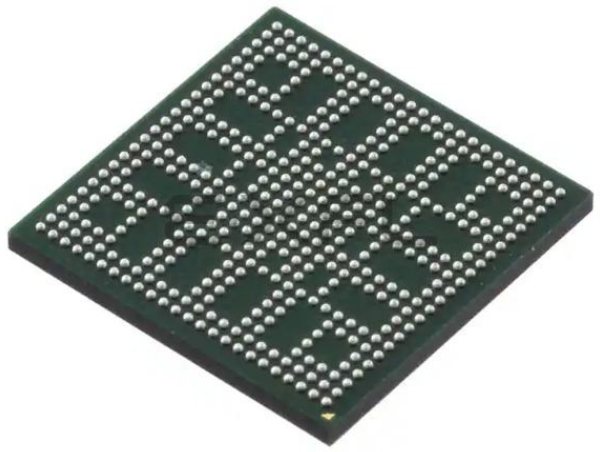

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, LVDDR3, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + PHY (3)
Voltage - I/O	1.2V, 1.8V, 3.0V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	432-TFBGA
Supplier Device Package	432-MAPBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6l3evn10ac

NOTE

The actual feature set depends on the part numbers as described in Table 1, "Example Orderable Part Numbers," on page 3. Functions, such as 2D hardware graphics acceleration or E Ink may not be enabled for specific part numbers.

1.3 Updated Signal Naming Convention

The signal names of the i.MX6 series of products have been standardized to better align the signal names within the family and across the documentation. Some of the benefits of these changes are as follows:

- The names are unique within the scope of an SoC and within the series of products
- Searches will return all occurrences of the named signal
- The names are consistent between i.MX 6 series products implementing the same modules
- The module instance is incorporated into the signal name

This change applies only to signal names. The original ball names have been preserved to prevent the need to change schematics, BSDL models, IBIS models, and so on.

Throughout this document, the updated signal names are used except where referenced as a ball name (such as the Functional Contact Assignments table, Ball Map table, and so on). A master list of the signal name changes is in the document, *IMX 6 Series Signal Name Mapping* (EB792). This list can be used to map the signal names used in older documentation to the new standardized naming conventions.

Table 2. i.MX 6SoloLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
eCSPI-1 eCSPI-2 eCSPI-3 eCSPI-4	Configurable SPI	Connectivity Peripherals	Full-duplex enhanced Synchronous Serial Interface. It is configurable to support Master/Slave modes, four chip selects to support multiple peripherals.
EIM	NOR-Flash /PSRAM interface	Connectivity Peripherals	The EIM NOR-FLASH / PSRAM provides: • Support 16-bit (in muxed IO mode only) PSRAM memories (sync and async operating modes), at slow frequency • Support 16-bit (in muxed IO mode only) NOR-Flash memories, at slow frequency • Multiple chip selects
EPDC	Electrophoretic Display Controller	Peripherals	The EPDC is a feature-rich, low power, and high-performance direct-drive, active matrix EPD controller. It is specifically designed to drive E Ink EPD panels, supporting a wide variety of TFT backplanes.
EPIT-1 EPIT-2	Enhanced Periodic Interrupt Timer	Timer Peripherals	Each EPIT is a 32-bit “set and forget” timer that starts counting after the EPIT is enabled by software. It is capable of providing precise interrupts at regular intervals with minimal processor intervention. It has a 12-bit prescaler for division of input clock frequency to get the required time setting for the interrupts to occur, and counter value can be programmed on the fly.
FEC	Fast Ethernet Controller	Connectivity Peripherals	The Ethernet Media Access Controller (MAC) is designed to support 10 and 100 Mbps Ethernet/IEEE 802.3 networks. An external transceiver interface and transceiver function are required to complete the interface to the media.
GPIO-1 GPIO-2 GPIO-3 GPIO-4 GPIO-5	General Purpose I/O Modules	System Control Peripherals	Used for general purpose input/output to external ICs. Each GPIO module supports 32 bits of I/O.
GPT	General Purpose Timer	Timer Peripherals	Each GPT is a 32-bit “free-running” or “set and forget” mode timer with programmable prescaler and compare and capture register. A timer counter value can be captured using an external event and can be configured to trigger a capture event on either the leading or trailing edges of an input pulse. When the timer is configured to operate in “set and forget” mode, it is capable of providing precise interrupts at regular intervals with minimal processor intervention. The counter has output compare logic to provide the status and interrupt at comparison. This timer can be configured to run either on an external clock or on an internal clock.
GPU2Dv2	Graphics Processing Unit-2D, ver 2	Multimedia Peripherals	The GPU2Dv2 provides hardware acceleration for 2D graphics algorithms, such as Bit BLT, stretch BLT, and many other 2D functions.
GPUVGv2	Vector Graphics Processing Unit, ver2	Multimedia Peripherals	OpenVG graphics accelerator provides OpenVG 1.1 support as well as other accelerations, including Real-time hardware curve tesselation of lines, quadratic and cubic Bezier curves, 16x Line Anti-aliasing, and various Vector Drawing functions.
I^2C-1 I^2C-2 I^2C-3	I^2C Interface	Connectivity Peripherals	I^2C provide serial interface for external devices. Data rates of up to 400 kbps are supported.

Table 9 provides the operating ranges of the i.MX 6SoloLite processor. For details on the chip's power structure, see the “Power Management Unit (PMU)” chapter of the *i.MX 6SoloLite Reference Manual* (IMX6SLRM).

Table 9. Operating Ranges

Parameter Description	Symbol	Min	Typ	Max[1]	Unit	Comment
Run mode: LDO enabled	VDD_ARM_IN	1.375[2]	—	1.5	V	LDO output set at 1.250V minimum for operation up to 996 MHz
		1.275[2]	—	1.5	V	LDO output set at 1.150V minimum for operation up to 792 MHz
		1.075[2]	—	1.5	V	LDO output set at 0.95V minimum for operation up to 396 MHz
		1.075[2]	—	1.5	V	LDO output set at 0.950V minimum for operation up to 192 MHz
		1.050[2]	—	1.5	V	LDO output set at 0.9250V minimum for operation up to 24 MHz
	VDD_SOC_IN[3] VDD_PU_IN	1.275[2,4]	—	1.5	V	VDD_SOC and VDD_PU LDO outputs (VDD_SOC_CAP and VDD_PU_CAP) require 1.15 V minimum
Run mode: LDO bypassed	VDD_ARM_IN	1.250	—	1.3	V	LDO bypassed for operation up to 996 MHz
		1.150	—	1.3	V	LDO bypassed for operation up to 792 MHz
		0.950	—	1.3	V	LDO bypassed for operation up to 396 MHz
		0.950	—	1.3	V	LDO bypassed for operation up to 192 MHz
		0.925	—	1.3	V	LDO bypassed for operation up to 24 MHz
	VDD_SOC_IN[3] VDD_PU_IN	1.15[4]	—	1.3	V	—
Standby/DSM Mode	VDD_ARM_IN	0.9	—	1.3	V	See Table 12, "Stop Mode Current and Power Consumption," on page 25.
	VDD_SOC_IN VDD_PU_IN	0.9	—	1.3	V	
VDDHIGH internal Regulator	VDD_HIGH_IN[5]	2.8	—	3.3	V	Must match the range of voltages that the rechargeable backup battery supports.
Backup battery supply range	VDD_SNVS_IN[5]	2.7	—	3.6	V	Should be supplied from the same supply as VDD_HIGH_IN if the system does not require keeping real time and other data on OFF state.
USB supply voltages	USB_OTG1_VBUS USB_OTG2_VBUS	4.4	—	5.25	V	—
DDR I/O supply	NVCC_DRAM	1.14	1.2	1.3	V	LPDDR2
		1.425	1.5	1.575	V	DDR3
	NVCC_DRAM_2P5	2.5	2.5	2.75	V	—

NOTE

For customers beginning new designs with the i.MX 6SoloLite and the PF0100 PMIC, it is recommended to use the F3 OTP option instead of the F1 OTP option and the F4 OTP option instead of the F2 OTP option.

4.2.2 Power-Down Sequence

There are no special requirements on the power-down sequence other than the VDD_SNVS_IN supply should be the last to turn off.

4.2.3 Power Supplies Usage

All I/O pins should not be externally driven while the I/O power supply for the pin (NVCC_xxx) is OFF. This can cause internal latch-up and malfunctions due to reverse current flows. For information about I/O power supply of each pin, see “Power Group” column of Table 66, "13 x 13 mm Functional Contact Assignments," on page 86.

4.3 Integrated LDO Voltage Regulator Parameters

Various internal supplies can be powered ON from internal LDO voltage regulators. All the supply pins named *_CAP must be connected to external capacitors. The onboard LDOs are intended for internal use only and should not be used to power any external circuitry. See the i.MX 6SoloLite reference manual for details on the power tree scheme recommended operation.

NOTE

The *_CAP signals should not be powered externally. These signals are intended for internal LDO or LDO bypass operation only.

4.3.1 Digital Regulators (LDO_ARM, LDO_PU, LDO_SOC)

There are three digital LDO regulators (“Digital”, because of the logic loads that they drive, not because of their construction). The advantages of the regulators are to reduce the input supply variation because of their input supply ripple rejection and their on die trimming. This translates into more voltage for the die producing higher operating frequencies. These regulators have three basic modes.

- Bypass. The regulation FET is switched fully on passing the external voltage, DCDC_LOW, to the load unaltered. The analog part of the regulator is powered down in this state, removing any loss other than the IR drop through the power grid and FET.
- Power Gate. The regulation FET is switched fully off limiting the current draw from the supply. The analog part of the regulator is powered down here limiting the power consumption.
- Analog regulation mode. The regulation FET is controlled such that the output voltage of the regulator equals the programmed target voltage. The target voltage is fully programmable in 25 mV steps.

For additional information, see the i.MX 6SoloLite reference manual.

Table 21. DVGPIO I/O DC Parameters

Parameter	Symbol	Test Conditions	Min	Max	Unit
High-level output voltage[1]	Voh	Ioh = -0.1 mA (DSE[2] = 001, 010) Ioh = -1 mA (DSE = 011, 100, 101, 110, 111)	OVDD – 0.15	—	V
Low-level output voltage[1]	Vol	Iol = 0.1 mA (DSE[2] = 001, 010) Iol = 1mA (DSE = 011, 100, 101, 110, 111)	—	0.15	V
High-Level DC input voltage [1, 3]	Vih	—	0.7 × OVDD	OVDD	V
Low-Level DC input voltage [1, 3]	Vil	—	0	0.3 × OVDD	V
Input Hysteresis	Vhys	OVDD = 1.8 V OVDD = 3.3 V	0.25	—	V
Schmitt trigger VT+, [3, 4]	VT+	—	0.5 × OVDD	—	V
Schmitt trigger VT–, [3, 4]	VT–	—	—	0.5 × OVDD	V
Input current (no pull-up/down)	Iin	Vin = OVDD or 0	-1.25	1.25	µA
Input current (22 kΩ pull-up)	Iin	Vin = 0 V Vin = OVDD	—	212 1	µA
Input current (47 kΩ pull-up)	Iin	Vin = 0 V Vin = OVDD	—	100 1	µA
Input current (100 kΩ pull-up)	Iin	Vin = 0 V Vin= OVDD	—	48 1	µA
Input current (100 kΩ pull-down)	Iin	Vin = 0 V Vin = OVDD	—	1 48	µA
Keeper circuit resistance	Rkeep	Vin = 0.3 x OVDD Vin = 0.7 x OVDD	105	205	kΩ

1 Overshoot and undershoot conditions (transitions above OVDD and below GND) on switching pads must be held below 0.6 V, and the duration of the overshoot/undershoot must not exceed 10% of the system clock cycle. Overshoot/ undershoot must be controlled through printed circuit board layout, transmission line impedance matching, signal line termination, or other methods. Non-compliance to this specification may affect device reliability or cause permanent damage to the device.

2 DSE is the Drive Strength Field setting in the associated IOMUX control register.

3 To maintain a valid level, the transition edge of the input must sustain a constant slew rate (monotonic) from the current DC level through to the target DC level, Vil or Vih. Monotonic input transition time is from 0.1 ns to 1 s.

4 Hysteresis of 250 mV is guaranteed over all operating conditions when hysteresis is enabled.

4.6.3 DDR I/O DC Parameters

The DDR I/O pads support LPDDR2 and DDR3 operational modes.

4.6.3.1 LPDDR2 Mode I/O DC Parameters

The parameters in Table 22 are guaranteed per the operating ranges in Table 9, unless otherwise noted. For details on supported DDR memory configurations, see Section 4.9.4, “Multi-Mode DDR Controller (MMDC)”.

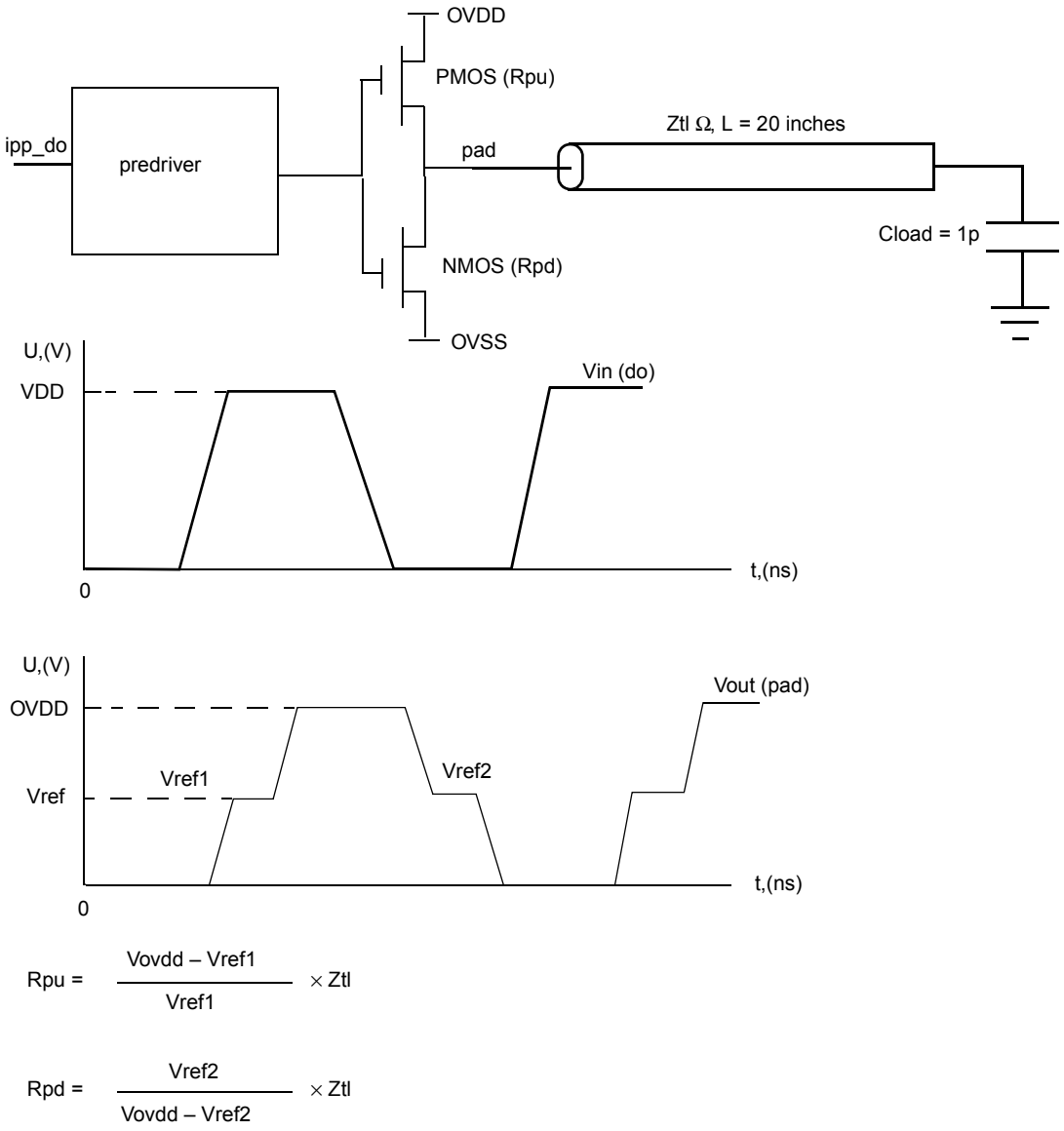

Figure 7. Impedance Matching Load for Measurement

4.8.1 Dual Voltage GPIO Output Buffer Impedance

Table 28 shows the GPIO output buffer impedance (OVDD 1.8 V).

Table 28. DVGPIO Output Buffer Average Impedance (OVDD 1.8 V)

Parameter	Symbol	Drive Strength (ipp_dse)	Typ Value	Unit
Output Driver Impedance	Rdrv	001 010 011 100 101 110 111	262 134 88 62 51 43 37	Ω

4.9.3.2 General EIM Timing-Synchronous Mode

Figure 10, Figure 11, and Table 34 specify the timings related to the EIM module. All EIM output control signals may be asserted and deasserted by an internal clock synchronized to the BCLK rising edge according to corresponding assertion/negation control fields.

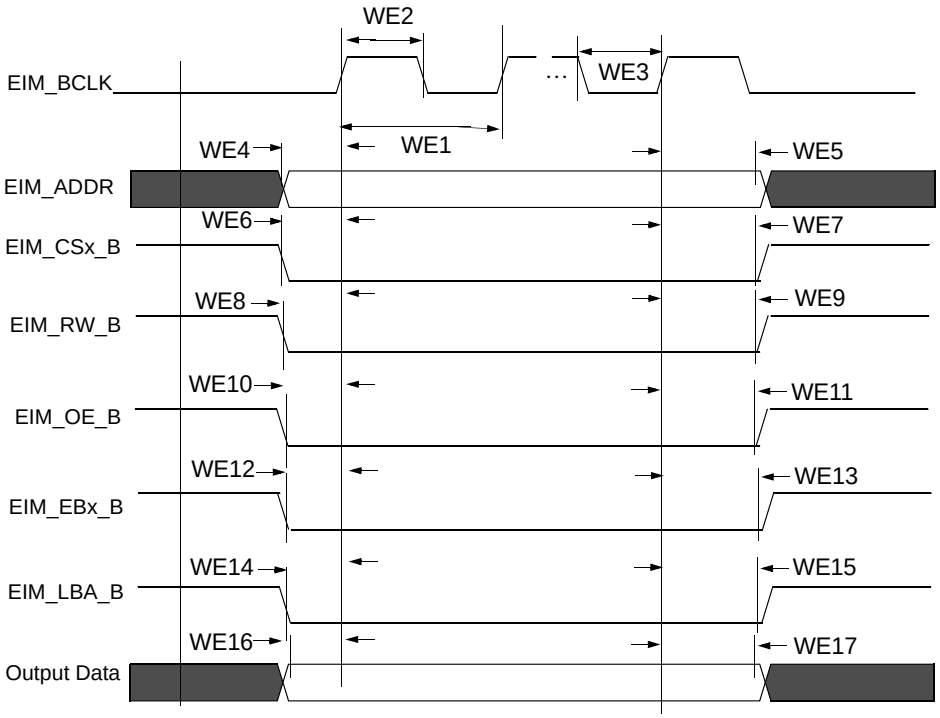

Figure 10. EIM Output Timing Diagram

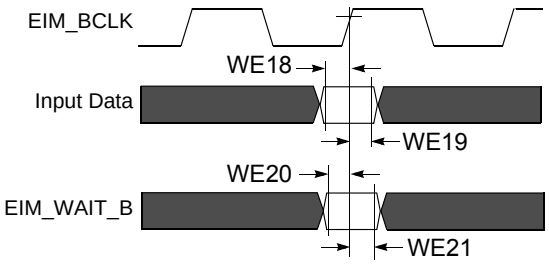

Figure 11. EIM Input Timing Diagram

4.9.3.3 Examples of EIM Synchronous Accesses

Table 34. EIM Bus Timing Parameters

ID	Parameter	Min[1]	Max[1]	Unit
WE1	EIM_BCLK cycle time[2]	t × (k+1)	—	ns
WE2	EIM_BCLK high level width	0.4 × t × (k+1)	—	ns
WE3	EIM_BCLK low level width	0.4 × t × (k+1)	—	ns
WE4	Clock rise to address valid	-0.5 × t × (k+1) -1.25	-0.5 × t × (k+1) +2.25	ns

Figure 12 to Figure 15 provide few examples of basic EIM accesses to external memory devices with the timing parameters mentioned previously for specific control parameters settings.

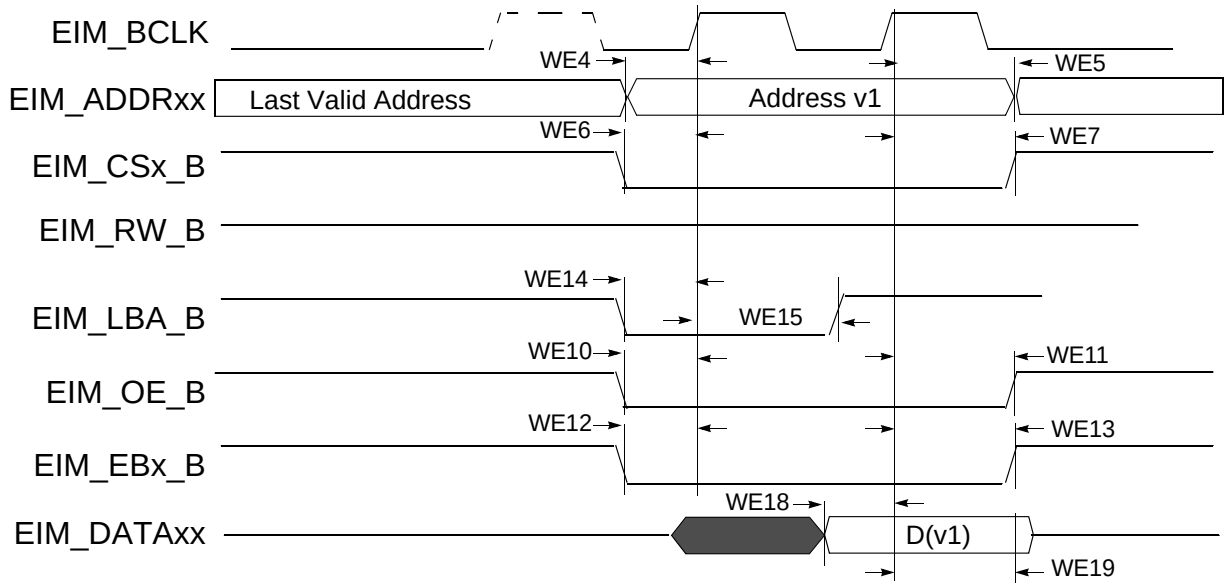

Figure 12. Synchronous Memory Read Access, WSC=1

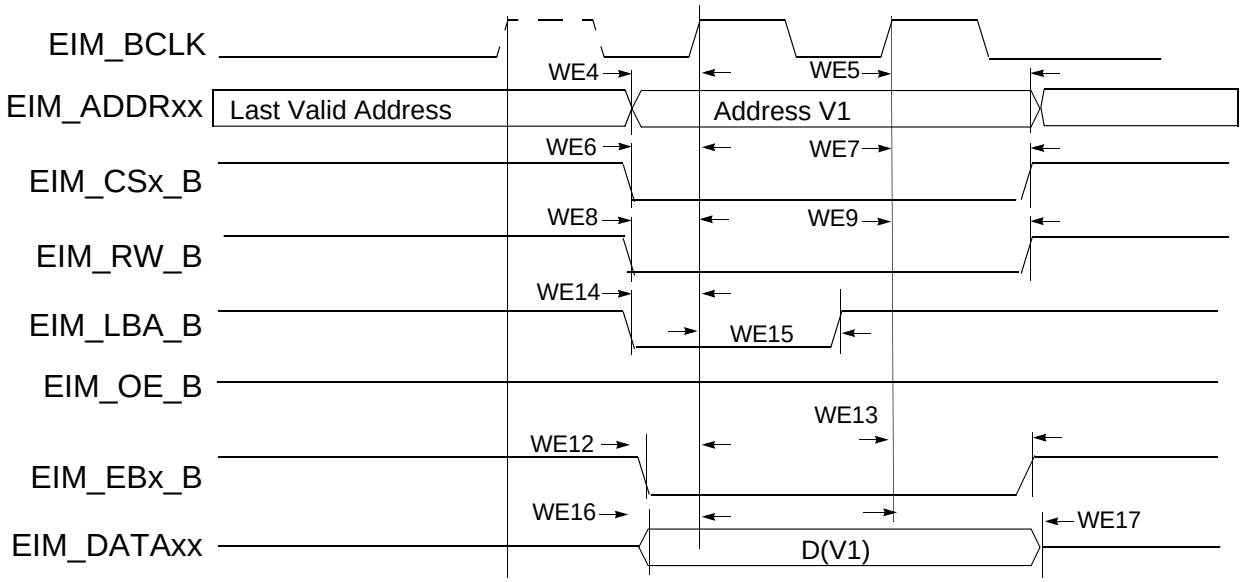

Figure 13. Synchronous Memory, Write Access, WSC=1, WBEA=0, and WADVN=0

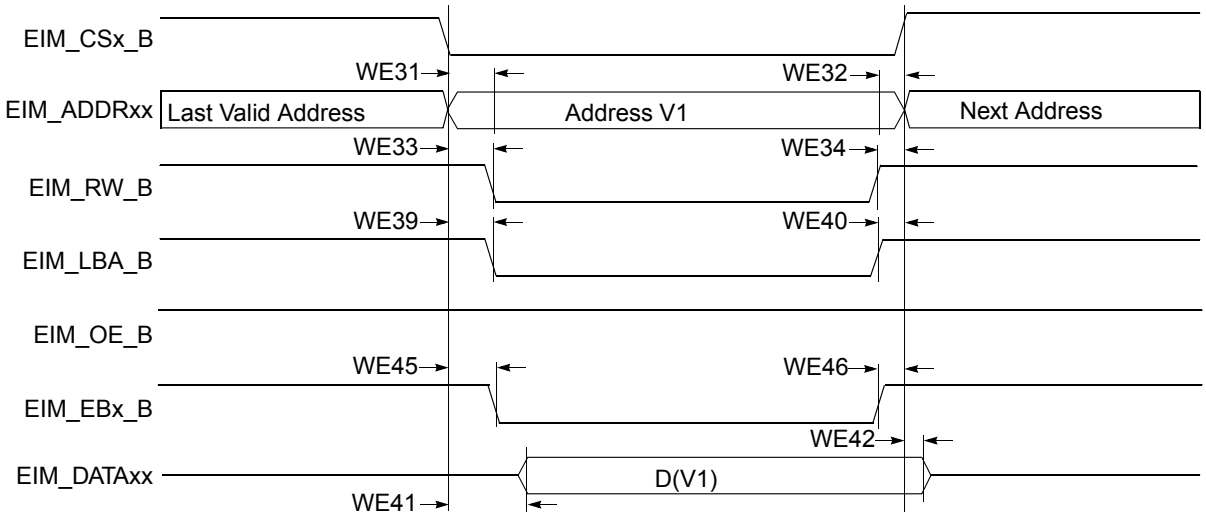

Figure 18. Asynchronous Memory Write Access

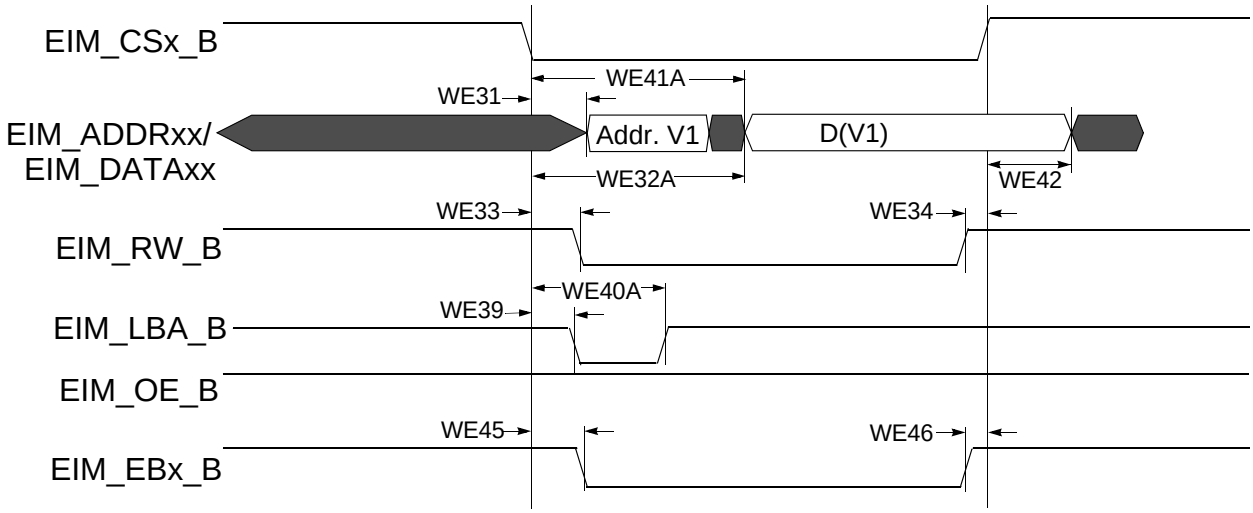

Figure 19. Asynchronous A/D Muxed Write Access

4.10.6.1 RMII Mode Timing Parameters

In RMII mode, FEC_TX_CLK is used as the REF_CLK which is a 50 MHz ±50 ppm continuous reference clock. FEC_RX_DV is used as the CRS_DV in RMII, and other signals under RMII mode include FEC_TX_EN, FEC_TX_DATA[1:0], FEC_RX_DATA[1:0] and optional FEC_RX_ER.

The RMII mode timing parameters are shown in Figure 31 and Table 45.

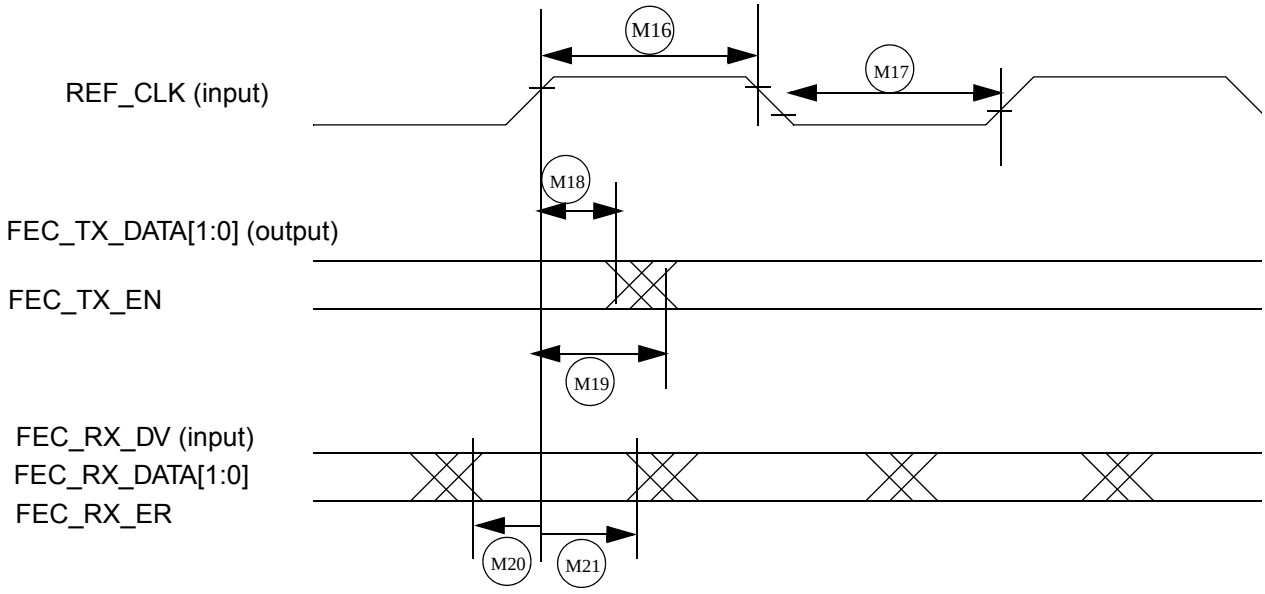

Figure 31. RMII Mode Signal Timing Diagram

Table 45. RMII Signal Timing Parameters

No.	Characteristics[1]	Min	Max	Unit
M16	REF_CLK(FEC_TX_CLK) pulse width high	35%	65%	REF_CLK period
M17	REF_CLK(FEC_TX_CLK) pulse width low	35%	65%	REF_CLK period
M18	REF_CLK to FEC_TX_DATA[1:0], FEC_TX_EN invalid	2	—	ns
M19	REF_CLK to FEC_TX_DATA[1:0], FEC_TX_EN valid	—	16	ns
M20	FEC_RX_DATA[1:0], CRS_DV(FEC_RX_DV), FEC_RX_ER to REF_CLK setup	4	—	ns
M21	REF_CLK to FEC_RX_DATA[1:0], FEC_RX_DV, FEC_RX_ER hold	2	—	ns

1 Test conditions: 25pF on each output signal.

4.10.8 Pulse Width Modulator (PWM) Timing Parameters

This section describes the electrical information of the PWM. The PWM can be programmed to select one of three clock signals as its source frequency. The selected clock signal is passed through a prescaler before being input to the counter. The output is available at the pulse-width modulator output (PWMx_OUT) external pin (see external signals table in the i.MX 6SoloLite reference manual for PWM pin assignments).

Figure 33 depicts the timing of the PWM, and Table 47 lists the PWM timing parameters.

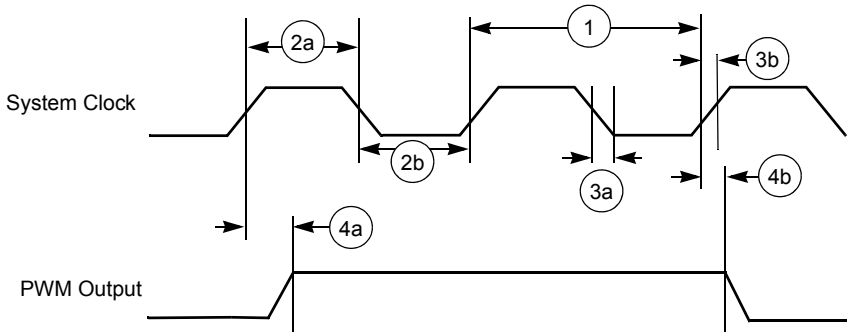

Figure 33. PWM Timing Diagram

Table 47. PWM Output Timing Parameters

Reference Number	Parameter	Min	Max	Unit
1	System CLK frequency[1]	0	ipg_clk	MHz
2a	Clock high time	12.29	—	ns
2b	Clock low time	9.91	—	ns

1 CL of PWMx_OUT = 30 pF

4.10.9 SCAN JTAG Controller (SJC) Timing Parameters

Figure 34 depicts the SJC test clock input timing. Figure 35 depicts the SJC boundary scan timing. Figure 36 depicts the SJC test access port. Signal parameters are listed in Table 48.

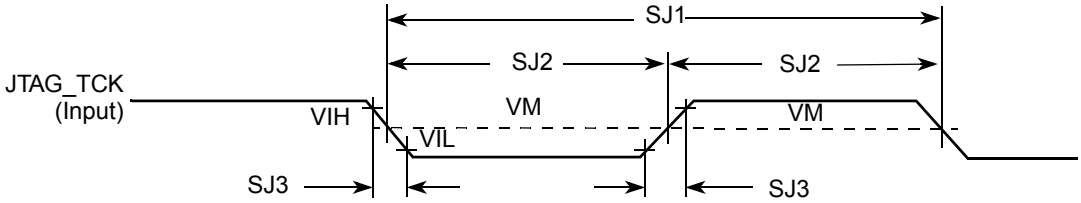

Figure 34. Test Clock Input Timing Diagram

Table 51. SSI Transmitter Timing with Internal Clock

ID	Parameter	Min	Max	Unit
Internal Clock Operation				
SS1	AUDx_TXC/AUDx_RXC clock period	81.4	—	ns
SS2	AUDx_TXC/AUDx_RXC clock high period	36.0	—	ns
SS4	AUDx_TXC/AUDx_RXC clock low period	36.0	—	ns
SS6	AUDx_TXC high to AUDx_TXFS (bl) high	—	15.0	ns
SS8	AUDx_TXC high to AUDx_TXFS (bl) low	—	15.0	ns
SS10	AUDx_TXC high to AUDx_TXFS (wl) high	—	15.0	ns
SS12	AUDx_TXC high to AUDx_TXFS (wl) low	—	15.0	ns
SS14	AUDx_TXC/AUDx_RXC Internal AUDx_TXFS rise time	—	6.0	ns
SS15	AUDx_TXC/AUDx_RXC Internal AUDx_TXFS fall time	—	6.0	ns
SS16	AUDx_TXC high to AUDx_TXD valid from high impedance	—	15.0	ns
SS17	AUDx_TXC high to AUDx_TXD high/low	—	15.0	ns
SS18	AUDx_TXC high to AUDx_TXD high impedance	—	15.0	ns
Synchronous Internal Clock Operation				
SS42	AUDx_RXD setup before AUDx_TXC falling	10.0	—	ns
SS43	AUDx_RXD hold after AUDx_TXC falling	0.0	—	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TXC/RXC = 0) and a non-inverted frame sync (TXFS/RXFS = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal TXC/RXC and/or the frame sync TXFS/RXFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is used for data transfer.
- The terms, WL and BL, refer to Word Length(WL) and Bit Length(BL).
- For internal Frame Sync operation using external clock, the FS timing is same as that of TXD (for example, during AC97 mode of operation).

4.10.11.3 SSI Transmitter Timing with External Clock

Figure 42 depicts the SSI transmitter external clock timing and Table 53 lists the timing parameters for the transmitter timing with the external clock.

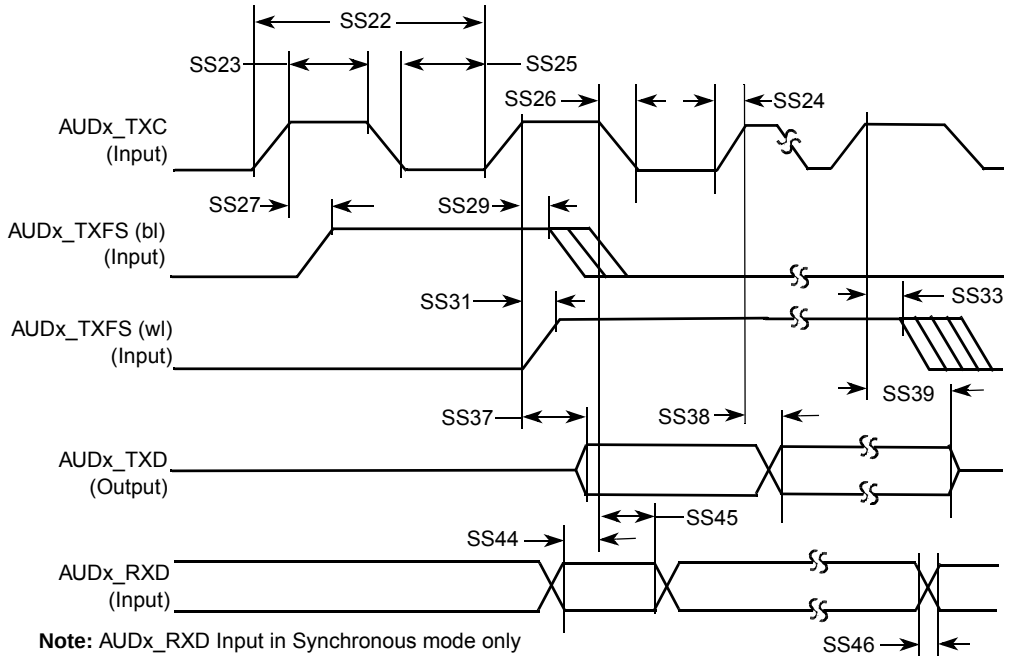

Figure 42. SSI Transmitter External Clock Timing Diagram

Table 53. SSI Transmitter with External Clock Timing Parameters

ID	Parameter	Min	Max	Unit
External Clock Operation				
SS22	AUDx_TXC/AUDx_RXC clock period	81.4	—	ns
SS23	AUDx_TXC/AUDx_RXC clock high period	36.0	—	ns
SS24	AUDx_TXC/AUDx_RXC clock rise time	—	6.0	ns
SS25	AUDx_TXC/AUDx_RXC clock low period	36.0	—	ns
SS26	AUDx_TXC/AUDx_RXC clock fall time	—	6.0	ns
SS27	AUDx_TXC high to AUDx_TXFS (bl) high	–10.0	15.0	ns
SS29	AUDx_TXC high to AUDx_TXFS (bl) low	10.0	—	ns
SS31	AUDx_TXC high to AUDx_TXFS (wl) high	–10.0	15.0	ns
SS33	AUDx_TXC high to AUDx_TXFS (wl) low	10.0	—	ns
SS37	AUDx_TXC high to AUDx_TXD valid from high impedance	—	15.0	ns
SS38	AUDx_TXC high to AUDx_TXD high/low	—	15.0	ns
SS39	AUDx_TXC high to AUDx_TXD high impedance	—	15.0	ns

4.10.13.2 Receive Timing Parameters

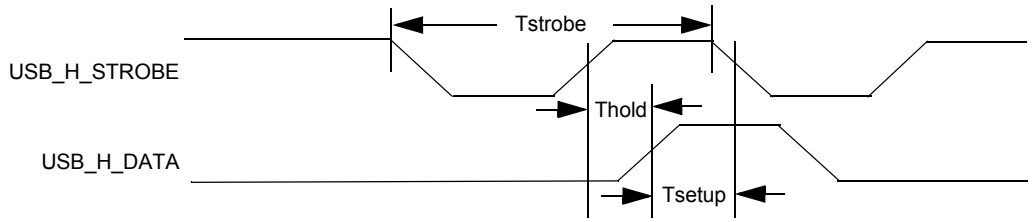

Figure 49. USB HSIC Receive Timing Diagram

Table 61. USB HSIC Receive Timing Parameters[1]

Name	Parameter	Min	Max	Unit	Comment
Tstrobe	Strobe period	4.166	4.167	ns	—
Thold	Data hold time	300	—	ps	Measured at 50% point
Tsetup	Data setup time	365	—	ps	Measured at 50% point
Tslew	Strobe/data rising/falling time	0.7	2	V/ns	Averaged from 30% – 70% points

1 The timings in the table are guaranteed when:
—AC I/O voltage is between 0.9x to 1x of the I/O supply
—DDR_SEL configuration bits of the I/O are set to (10)b

4.10.14 USB PHY Parameters

This section describes the USB-OTG PHY and the USB Host port PHY parameters.
The USB PHY meets the electrical compliance requirements defined in the Universal Serial Bus Revision 2.0 OTG, USB Host with the amendments below (On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification is not applicable to Host port).

- USB ENGINEERING CHANGE NOTICE
  - Title: 5V Short Circuit Withstand Requirement Change
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- Errata for USB Revision 2.0 April 27, 2000 as of 12/7/2000
- USB ENGINEERING CHANGE NOTICE
  - Title: Pull-up/Pull-down resistors
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- USB ENGINEERING CHANGE NOTICE
  - Title: Suspend Current Limit Changes
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- USB ENGINEERING CHANGE NOTICE
  - Title: USB 2.0 Phase Locked SOFs
  - Applies to: Universal Serial Bus Specification, Revision 2.0
- On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification
  - Revision 2.0 plus errata and ecn June 4, 2010

- Battery Charging Specification (available from USB-IF)
  - Revision 1.2, December 7, 2010
  - Portable device only.

Table 63. Interfaces Allocation During Boot (continued)

Interface	IP Instance	Allocated Ball Names During Boot	Comment
I2C	I2C-2	I2C2_SCL, I2C2_SDA	—
I2C	I2C-3	AUD_RXFS, AUD_RXC	—
USB	USB_OTG1_PHY	USB_OTG1_DP USB_OTG1_DN USB_OTG1_VBUS USB_OTG1_CHD_B USB_OTG1_DP USB_OTG1_DN USB_OTG1_VBUS	—

6 Package Information and Contact Assignments

This section includes the contact assignment information and mechanical package drawing.

6.1 Updated Signal Naming Convention

The signal names of the i.MX6 series of products have been standardized to better align the signal names within the family and across the documentation. Some of the benefits of these changes are as follows:

- The names are unique within the scope of an SoC and within the series of products
- Searches will return all occurrences of the named signal
- The names are consistent between i.MX 6 series products implementing the same modules
- The module instance is incorporated into the signal name

This change applies only to signal names. The original ball names have been preserved to prevent the need to change schematics, BSDL models, IBIS models, and so on.

Throughout this document, the updated signal names are used except where referenced as a ball name (such as the Functional Contact Assignments table, Ball Map table, and so on). A master list of the signal name changes is in the document, *IMX 6 Series Signal Name Mapping* (EB792). This list can be used to map the signal names used in older documentation to the new standardized naming conventions.

Table 66. 13 x 13 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group[1]	Ball Type	Out of Reset Condition[2]			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value[3]
EPDC_D15	A13	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO1_GPIO[22]	Input	Keeper
EPDC_D2	B17	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO1_GPIO[9]	Input	Keeper
EPDC_D3	A16	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO1_GPIO[10]	Input	Keeper
EPDC_D4	B16	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO1_GPIO[11]	Input	Keeper
EPDC_D5	A15	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO1_GPIO[12]	Input	Keeper
EPDC_D6	B15	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO1_GPIO[13]	Input	Keeper
EPDC_D7	C15	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO1_GPIO[14]	Input	Keeper
EPDC_D8	D15	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO1_GPIO[15]	Input	Keeper
EPDC_D9	F15	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO1_GPIO[16]	Input	Keeper
EPDC_GDCLK	A12	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO1_GPIO[31]	Input	Keeper
EPDC_GDOE	B13	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[0]	Input	Keeper
EPDC_GDRL	B12	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[1]	Input	Keeper
EPDC_GDSP	A11	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[2]	Input	Keeper
EPDC_PWRCOM	B11	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[11]	Input	Keeper
EPDC_PWRCTRL0	D11	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[7]	Input	Keeper
EPDC_PWRCTRL1	E11	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[8]	Input	Keeper
EPDC_PWRCTRL2	F11	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[9]	Input	Keeper
EPDC_PWRCTRL3	G12	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[10]	Input	Keeper
EPDC_PWRINT	F10	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[12]	Input	Keeper
EPDC_PWRSTAT	E10	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[13]	Input	Keeper
EPDC_PWRWAKEUP	D10	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[14]	Input	Keeper
EPDC_SDCE0	C11	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO1_GPIO[27]	Input	Keeper

Table 66. 13 x 13 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group[1]	Ball Type	Out of Reset Condition[2]			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value[3]
LCD_DAT5	U21	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[25]	Input	Keeper
LCD_DAT6	U23	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[26]	Input	Keeper
LCD_DAT7	U24	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[27]	Input	Keeper
LCD_DAT8	T23	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[28]	Input	Keeper
LCD_DAT9	T24	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[29]	Input	Keeper
LCD_ENABLE	J24	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[16]	Input	Keeper
LCD_HSYNC	H23	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[17]	Input	Keeper
LCD_RESET	H24	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[19]	Input	Keeper
LCD_VSYNC	J23	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[18]	Input	Keeper
ONOFF	W18	VDD_SNVS_IN	GPIO		SRC_ONOFF	Input	PU (100K)
PMIC_ON_REQ	AD15	VDD_SNVS_IN	GPIO	ALT0	SNVS_PMIC_ON_REQ	Output	Open Drain with PU (100K)
PMIC_STBY_REQ	AD16	VDD_SNVS_IN	GPIO	ALT0	CCM_PMIC_STBY_REQ	Output	0
POR_B	AC16	VDD_SNVS_IN	GPIO	ALT0	SRC_POR_B	Input	PU (100K)
PWM1	Y7	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[23]	Input	Keeper
REF_CLK_24M	AC14	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[21]	Input	Keeper
REF_CLK_32K	AD14	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[22]	Input	Keeper
RTC_XTALI	AB19	VDD_SNVS_CAP	—	—	RTC_XTALI	—	—
RTC_XTALO	AA19	VDD_SNVS_CAP	—	—	RTC_XTALO	—	—
SD1_CLK	B20	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO5_GPIO[15]	Input	Keeper
SD1_CMD	B21	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO5_GPIO[14]	Input	Keeper
SD1_DAT0	B23	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO5_GPIO[11]	Input	Keeper
SD1_DAT1	A23	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO5_GPIO[8]	Input	Keeper
SD1_DAT2	C22	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO5_GPIO[13]	Input	Keeper

Table 70. i.MX 6SoloLite Data Sheet Document Revision History (continued)

Rev. Number	Date	Substantive Change(s)
4	11/2016	• Changed throughout: – Changed terminology from “floating” to “not connected.” – Removed references to DDR3 • Section 1, “Introduction,” *i.MX 6SoloLite processor features*” Removed “low voltage DDR3” from second paragraph. • Table 1, "Example Orderable Part Numbers": Added new footnote to Speed Grade heading. – Removed paragraph about selecting the right data sheet. – Removed silicon revision 1 part numbers ending in “AA”. • Figure 1, "Part Number Nomenclature—i.MX 6SoloLite": Added to Silicon revision block Rev 1.3 and associated footnote. • Section 1.2, “Features,” added new bullet under Expansion cards, “4-bit or 8-bit…” • Table 2, "i.MX 6SoloLite Modules List": UART1–5, UART Interface row: – Changed bullet about programmable baud rate to “up to 5 Mbps.” – Added new bullet at top: “Conforms to the SD Host Controller…” – Added version “4.5” to MMCS specifications listed in second bullet “Fully compliant with MMC…” – Added new bullet “4-bit or 8-bit transfer mode…” • Table 3, "Special Signal Considerations," Content changes in the following rows: – XTALOSC_CLK1_P/ XTALOSC_CLK1_N: changed “floating” to “unconnected”. – NC: changed “floating” to “remain unconnected”. – SRC_POR_B: removed second sentence “May be used…” – RTC_XTALI/ RTC_XTALO: changed “floating” to “unconnected”. – RTC_XTALI/ RTC_XTALO: changed “keep RTC_XTALO floating” to “leave RTC_XTALO unconnected”. – TEST_MODE: changed “float this signal” to “leave this signal unconnected”. – XTALI/ XTALO: changed “floated” to “remains unconnected”. – Separated paragraphs with bullets. • Table 5, "Recommended Connections for Unused Analog Interfaces": changed “Float” to “Leave unconnected” in both lines. • Section 4.1.1, “Absolute Maximum Ratings”: Added new CAUTION text. • Table 7, "Absolute Maximum Ratings,": – Updated the maximum voltage specifications to an increased of 100 mV. – NVCC_DRAM maximum value changed to 1.975 V. – Added footnote regarding NVCC_DRAM maximum voltage allowance. – Added row to Vin/Vout supply voltage, separating DDR pins and non-DDR pins and included footnote regarding maximum voltage allowance. • Section 4.1.2.1, “BGA Case 2240 Package Thermal Resistance” Added NOTE “Per JEDEC JESD51-2…”. • Table 9, "Operating Ranges," Changed within rows: – Backup battery supply range, minimum reduced (improved) from “2.8” to “2.7”. – Backup battery supply range, maximum increased (improved) from “3.3” to “3.6” – Removed from the GPIO supplies row; NVCC_1P2V row for DDR3L • Section 4.1.5, “Maximum Supply Currents,” Paragraph 3: changed “AN4715” to “AN4580”. • Section 4.2.1, “Power-Up Sequence,” Removed reference to external SRC_POR_B: – Bullet 3: Removed “If the external” and final sentence “In the absence of…” – Removed bullet 4. – Added third NOTE: “For customers starting new designs…” *Continued on next page*

Table 70. i.MX 6SoloLite Data Sheet Document Revision History (continued)

Rev. Number	Date	Substantive Change(s)
4 *Continued*	11/2016	• Section 4.2.2, “Power-Down Sequence,” Replaced contents of section with sentence: “There are no special requirements on the power-down sequence other than …”. • Section 4.5.2, “OSC32K”: Removed text regarding coin cell from third paragraph and removed second NOTE about third party coin cell manufacturer. • Section 4.6, “I/O DC Parameters”: Removed second bullet regarding single voltage GPIO cell set. • Section 4.6.1, “XTALI and RTC_XTALI (Clock Inputs) DC Parameters” Added NOTE after table.Table 20, "XTALI and RTC_XTALI DC Parameters”: – Added parameter rows: Input capacitance; XTALI input leakage; and DC input current. – Added new footnote, “This voltage specification…” • Section 4.6.3, “*Single Voltage General Purpose I/O (GPIO) DC Parameters”* removed section. • Section 4.8, “Output Buffer Impedance Parameters”: Removed second bullet “Single voltage General Purpose I/O cell set …”. • Table 28, "DVGPIO Output Buffer Average Impedance (OVDD 1.8 V)”: Changed all Typical values. • Table 29, "DVGPIO Output Buffer Average Impedance (OVDD 3.3 V)”: Changed all Typical values. • Section 4.8.2, “*Single Voltage GPIO Output Buffer Impedance*”: removed section. • Table 34, "EIM Bus Timing Parameters, Updates throughout table to include min/max values. • Table 35, "EIM Asynchronous Timing Parameters Table Relative Chip Select, Updates throughout table to include min/max values. • Section 4.9.4, “Multi-Mode DDR Controller (MMDC),” created this new section. • Removed: Section 4.9.5, “DDR SDRAM Specific Parameters (DDR3 and LPDDR2),” Section 4.9.5.1, “DDR3 Parameters,” and Section 4.9.5.2, “LPDDR2 Parameters.” • Table 37, "CSI Gated Clock Mode Timing Parameters,” – Parameter P5 reduced (improved) from 10ns to 7.5 ns. – Parameter P6 reduced (improved) from 10ns to 7.5 ns. – Parameter P7 corrected to 66 MHz (no functional change). • Table 38, "CSI Ungated Clock Mode Timing Parameters,” – Parameter P4 reduced (improved) from 10ns to 7.5 ns. – Parameter P5 reduced (improved) from 10ns to 7.5 ns. – Parameter P6 corrected to 66 MHz (no functional change). • Section 4.10.3.1, “ECSPI Master Mode Timing,” Added new NOTE under Figure 25. • Section 4.10.3.2, “ECSPI Slave Mode Timing,” Added new NOTE under Figure 26. • Section 4.10.4.3, “SDR50/SDR104 AC Timing Parameters,” Figure 29 updated to correct SD5. • Table 43, "SDR50/SDR104 Interface Timing Parameters,” – SD2, changed minimum value to “0.46”, and changed maximum value to “0.54”. – SD3, changed minimum value to “0.46”, and changed maximum value to “0.54”. – SD2 (parameter Clock High Time), parameter name corrected to SD3. – SD5, changed maximum value to “0.74”. • Section 4.10.5, “HS200 Mode Timing Parameters,” Added this new section. • Section 4.10.14, “USB PHY Parameters,” Added new text to second paragraph “USB Host with the amendments below…” • Table 63, "Interfaces Allocation During Boot USDHC-1–USDHC-4 row, replaced existing text with “Refer to the table “SD/MMC…” • Table 65, "13 x 13 mm Supplies Contact Assignment,” – GPANAIO: changed remark from “Analog pad” to “Analog output for NXP use…” – ZQPAD: changed remark to “Connect ZQPAD to…” • Table 66, "13 x 13 mm Functional Contact Assignments,” DRAM_SDCLK_0, corrected “Input” to “Output” and Value to “0”. • Section 6.2.2, “13 x 13 mm Ground, Power, Sense, Not Connected, and Reference Contact Assignments,” Added new text “For most of the signals…” after Table 66. • Table 68, "13 x 13 mm, 0.5 mm Pitch Ball Map,” ball AD6 name corrected to “DRAM_D18”.