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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1GHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	DDR3, LPDDR2
Graphics Acceleration	Yes
Display & Interface Controllers	LCD
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + PHY (2), USB 2.0 OTG + PHY (1)
Voltage - I/O	1.2V, 1.8V, 3V
Operating Temperature	0°C ~ 95°C (TJ)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	432-TFBGA
Supplier Device Package	432-MAPBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6l7dvn10ac

Table 2. i.MX 6SoloLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
IOMUXC	IOMUX Control	System Control Peripherals	This module enables flexible IO multiplexing. Each IO pad has default and several alternate functions. The alternate functions are software configurable.
KPP	Key Pad Port	Connectivity Peripherals	KPP Supports 8 x 8 external key pad matrix. KPP features are: • Open drain design • Glitch suppression circuit design • Multiple keys detection • Standby key press detection
LCDIF	LCD Interface	Multimedia Peripherals	The LCDIF provides display data for external LCD panels from simple text-only displays to WVGA, 16/18/24 bpp color TFT panels. The LCDIF supports all of these different interfaces by providing fully programmable functionality and sharing register space, FIFOs, and ALU resources at the same time. The LCDIF supports RGB (DOTCLK) modes as well as system mode including both VSYNC and WSYNC modes.
MMDC	DDR Controller	Connectivity Peripherals	DDR Controller has the following features: • Support 16/32-bit DDR3-800 or LPDDR2-800 • Supports up to 2 GByte DDR memory space
OCOTP_ CTRL	OTP Controller	Security	The On-Chip OTP controller (OCOTP_CTRL) provides an interface for reading, programming, and/or overriding identification and control information stored in on-chip fuse elements. The module supports electrically-programmable poly fuses (eFUSEs). The OCOTP_CTRL also provides a set of volatile software-accessible signals that can be used for software control of hardware elements, not requiring non-volatility. The OCOTP_CTRL provides the primary user-visible mechanism for interfacing with on-chip fuse elements. Among the uses for the fuses are unique chip identifiers, mask revision numbers, cryptographic keys, JTAG secure mode, boot characteristics, and various control signals, requiring permanent non-volatility.
OCRAM	On-Chip Memory Controller	Data Path	The On-Chip Memory controller (OCRAM) module is designed as an interface between system's AXI bus and internal (on-chip) SRAM memory module. In i.MX 6SoloLite processor, the OCRAM is used for controlling the 128 KB multimedia RAM through a 64-bit AXI bus.
OCRAM_L2	On-Chip Memory Controller for L2 Cache	Data Path	The On-Chip Memory controller for L2 cache (OCRAM_L2) module is designed as an interface between system's AXI bus and internal (on-chip) L2 cache memory module during boot mode.
OSC 32 kHz	OSC 32 kHz	Clocking	Generates 32.768 kHz clock from external crystal.
PMU	Power Management functions	Data Path	Integrated power management unit. Used to provide power to various SoC domains.
PWM-1 PWM-2 PWM-3 PWM-4	Pulse Width Modulation	Connectivity Peripherals	The pulse-width modulator (PWM) has a 16-bit counter and is optimized to generate sound from stored sample audio images and it can also generate tones. It uses 16-bit resolution and a 4x16 data FIFO to generate sound.

Table 3. Special Signal Considerations (continued)

Signal Name	Remarks
RTC_XTALI/ RTC_XTALO	If the user wishes to configure RTC_XTALI and RTC_XTALO as an RTC oscillator, a 32.768 kHz crystal (≤100 kΩ ESR, 10 pF load) should be connected between RTC_XTALI and RTC_XTALO. Keep in mind the capacitors implemented on either side of the crystal are about twice the crystal load capacitor. To hit the exact oscillation frequency, the board capacitors need to be reduced to account for board and chip parasitics. The integrated oscillation amplifier is self biasing, but relatively weak. Care must be taken to limit parasitic leakage from RTC_XTALI and RTC_XTALO to either power or ground (>100 MΩ). This will debias the amplifier and cause a reduction of startup margin. Typically RTC_XTALI and RTC_XTALO should bias to approximately 0.5 V. If it is desired to feed an external low frequency clock into RTC_XTALI, the RTC_XTALO pin must remain unconnected or driven with a complimentary signal. The logic level of this forcing clock should not exceed VDD_SNVS_CAP level and the frequency should be <100 kHz under typical conditions. In the case when a high accuracy real time clock is not required, the system may use an internal low frequency ring oscillator. It is recommended to connect RTC_XTALI to GND and leave RTC_XTALO unconnected.
TEST_MODE	TEST_MODE is for NXP factory use. This signal is internally connected to an on-chip pull-down device. The user must either leave this signal unconnected or tie it to GND.
XTALI/XTALO	• A 24.0 MHz crystal must be connected between XTALI and XTALO. The level and frequency must be <32 MHz under typical conditions. • The crystal must be rated for a maximum drive level of 250 μW. An ESR (equivalent series resistance) of typically 80 Ω is recommended. NXP BSP (board support package) software requires 24 MHz on XTALI/XTALO. • The crystal can be eliminated if an external 24 MHz oscillator is available in the system. In this case, XTALI must be directly driven by the external oscillator and XTALO remains unconnected. The XTALI signal level must swing from ~0.8 x NVCC_PLL_OUT to ~0.2 V. • This clock is used as a reference for USB, so there are strict frequency tolerance and jitter requirements. • See the XTALOSC chapter and relevant interface specifications chapters of the i.MX 6SoloLite reference manual (IMX6SLRM), for details.
ZQPAD	DRAM calibration resistor 240 Ω 1% used as reference during DRAM output buffer driver calibration should be connected between this pad and GND.

Table 4. JTAG Controller Interface Summary

JTAG	I/O Type	On-Chip Termination
JTAG_TCK	Input	47 kΩ pull-up
JTAG_TMS	Input	47 kΩ pull-up
JTAG_TDI	Input	47 kΩ pull-up
JTAG_TDO	3-state output	Keeper
JTAG_TRST_B	Input	47 kΩ pull-up
JTAG_MODE	Input	100 kΩ pull-up

3.2 Recommended Connections for Unused Analog Interfaces

Table 5 shows the recommended connections for unused analog interfaces.

Table 5. Recommended Connections for Unused Analog Interfaces

Module	Pad Name	Recommendations if Unused?
XTALOSC	XTALOSC_CLK1_N, XTALOSC_CLK1_P	Leave unconnected
USB	USB_OTGx_DN, USB_OTGx_DP, USB_OTGx_VBUS, USB_OTG_CHD_B	Leave unconnected

4 Electrical Characteristics

This section provides the device and module-level electrical characteristics for the i.MX 6SoloLite.

4.1 Chip-Level Conditions

This section provides the device-level electrical characteristics for the IC. See Table 6 for a quick reference to the individual tables and sections.

Table 6. i.MX 6SoloLite Chip-Level Conditions

For these characteristics, …	Topic appears …
Absolute Maximum Ratings	on page 18
BGA Case 2240 Package Thermal Resistance	on page 19
Operating Ranges	on page 21
External Clock Sources	on page 23
Maximum Supply Currents	on page 24
Low Power Mode Supply Currents	on page 25
USB PHY Current Consumption	on page 26

4.1.1 Absolute Maximum Ratings

CAUTION

Stresses beyond those listed under Table 7 may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the Table 9, "Operating Ranges" or subsequent parameters tables is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 7 provides the absolute maximum operating ratings.

For information on external capacitor requirements for this regulator, see the Hardware Development Guide for i.MX 6SoloLite Applications Processors (IMX6SLHDG).

For additional information, see the i.MX 6SoloLite reference manual.

4.4 PLL's Electrical Characteristics

4.4.1 Audio/Video PLL's Electrical Parameters

Table 14. Audio/Video PLL's Electrical Parameters

Parameter	Value
Clock output range	650 MHz ~1.3 GHz
Reference clock	24 MHz
Lock time	<11250 reference cycles (450 μs)

4.4.2 528 MHz PLL

Table 15. 528 MHz PLL's Electrical Parameters

Parameter	Value
Clock output range	528 MHz PLL output
Reference clock	24 MHz
Lock time	<11250 reference cycles (15 μs)

4.4.3 Ethernet PLL

Table 16. Ethernet PLL's Electrical Parameters

Parameter	Value
Clock output range	500 MHz
Reference clock	24 MHz
Lock time	<11250 reference cycles (450 μs)

4.9.1 Reset Timings Parameters

Figure 8 shows the reset timing and Table 31 lists the timing parameters.

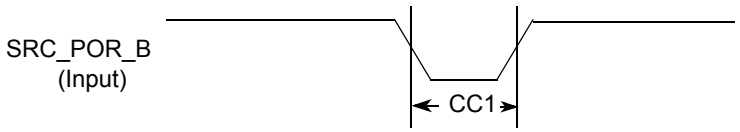

Figure 8. Reset Timing Diagram

Table 31. Reset Timing Parameters

ID	Parameter	Min	Max	Unit
CC1	Duration of POR_B to be qualified as valid.	1	—	XTALOSC_RTC_XTALI

4.9.2 WDOG Reset Timing Parameters

Figure 9 shows the WDOG reset timing and Table 32 lists the timing parameters.

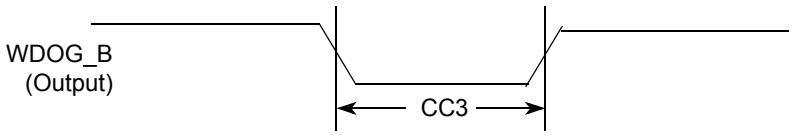

Figure 9. WDOG_B Timing Diagram

Table 32. WDOG_B Timing Parameters

ID	Parameter	Min	Max	Unit
CC3	Duration of WDOG_B Assertion	1	—	RTC_XTALI cycle

NOTE

RTC_XTALI is approximately 32 kHz. RTC_XTALI cycle is one period or approximately 30 µs.

NOTE

WDOG_B output signals (for each one of the Watchdog modules) do not have dedicated bins, but are muxed out through the IOMUX. See the IOMUX manual for detailed information.

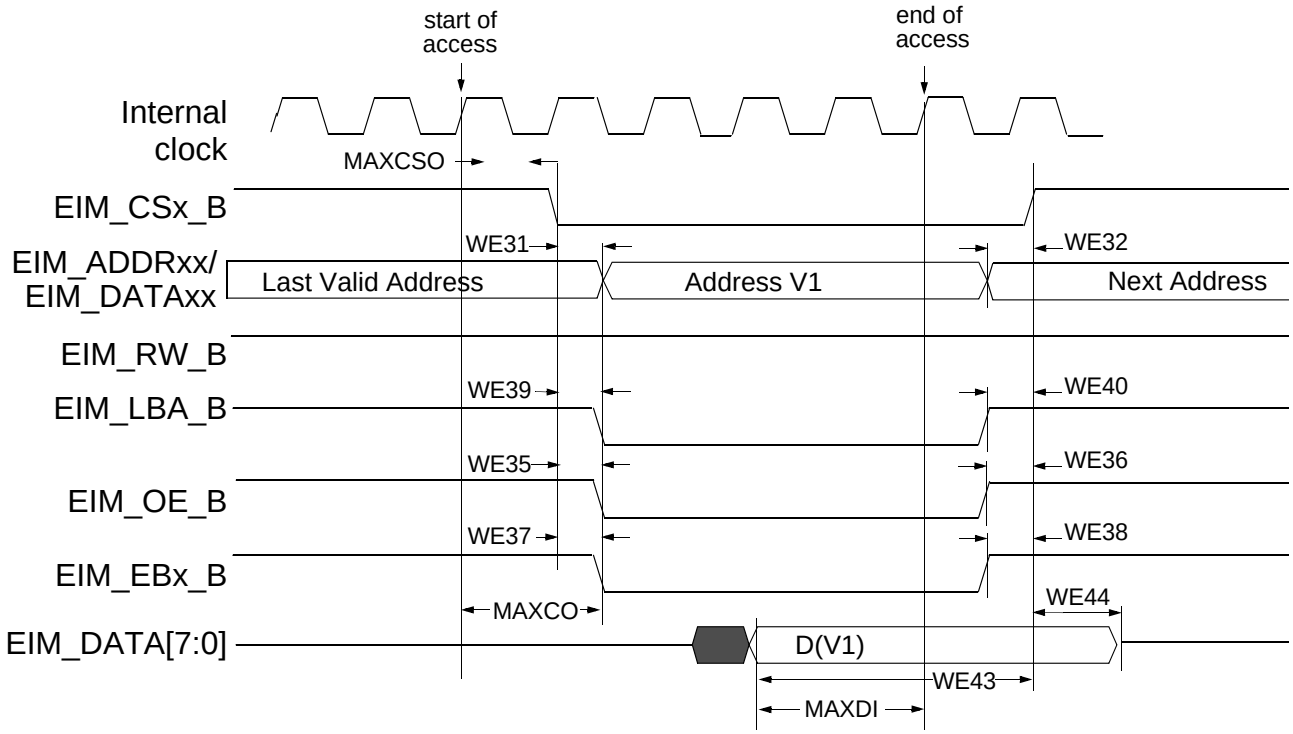

Figure 16. Asynchronous Memory Read Access (RWSC = 5)

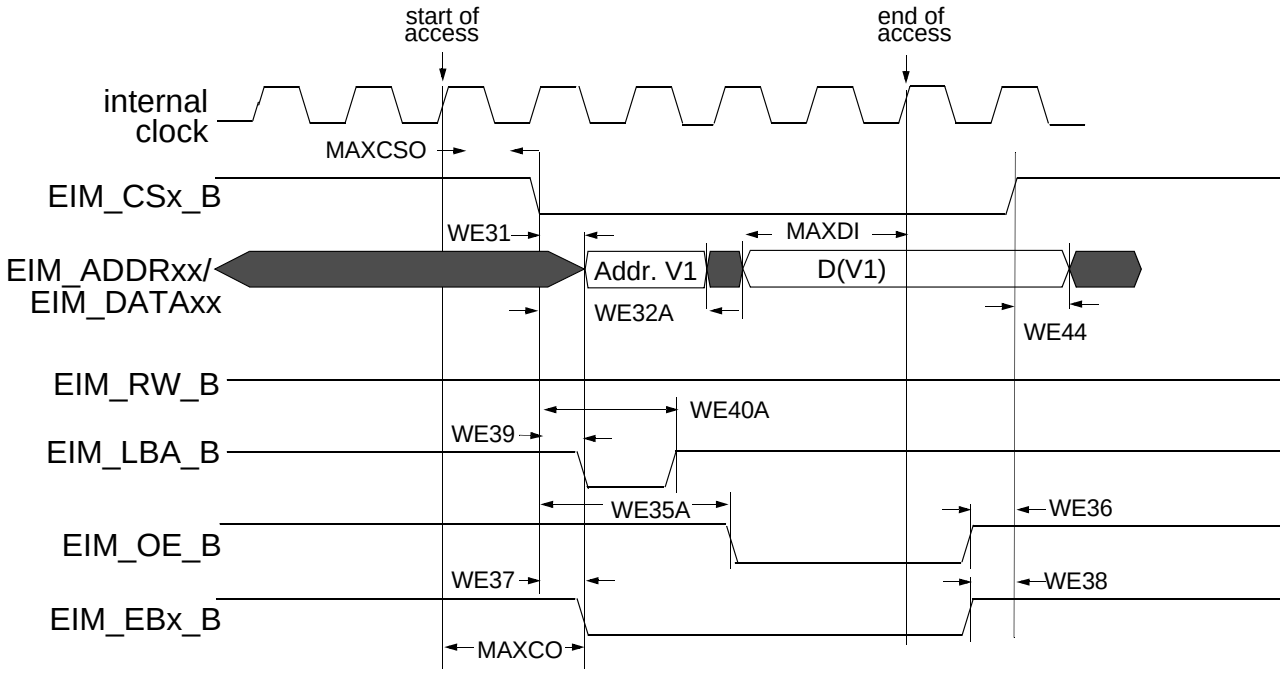

Figure 17. Asynchronous A/D Muxed Read Access (RWSC = 5)

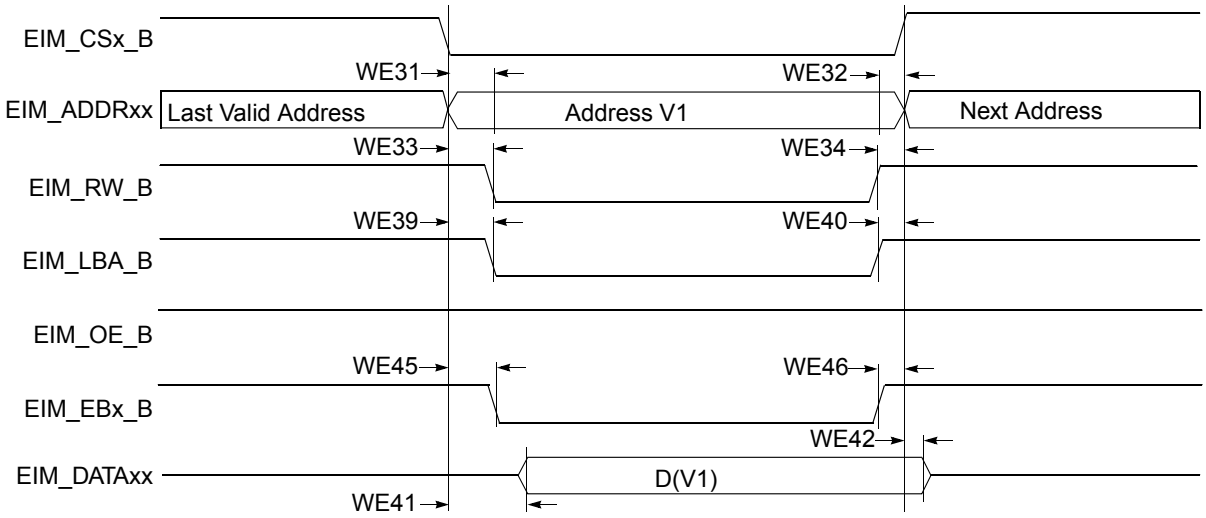

Figure 18. Asynchronous Memory Write Access

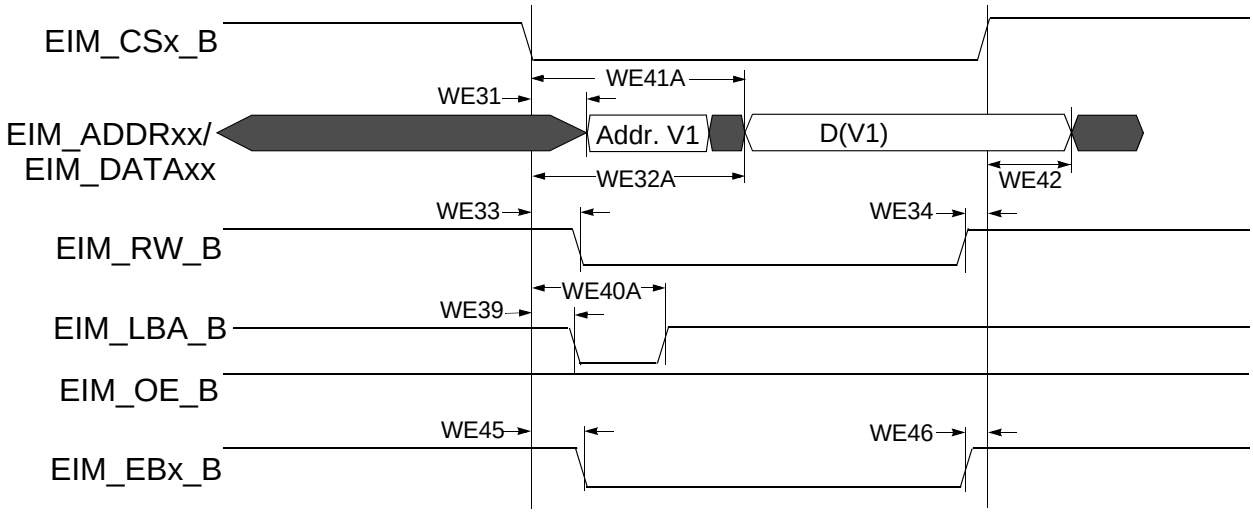

Figure 19. Asynchronous A/D Muxed Write Access

Table 35. EIM Asynchronous Timing Parameters Table Relative Chip Select (continued)

Reference Number	Parameter	Determination by Synchronous measured parameters[1]	Min	Max	Unit
MAXCO	Output maximum delay from internal driving EIM_ADDRxx/control flip-flops to chip outputs.	10	—	10	ns
MAXCSO	Output maximum delay from internal chip selects driving flip-flops to EIM_CSx_B out.	10	—	10	ns
MAXDI	EIM_DATAxx MAXIMUM delay from chip input data to its internal flip-flop	5	—	5	ns
WE43	Input Data Valid to EIM_CSx_B Invalid	MAXCO-MAXCSO+MAXDI	MAXCO-MAXCSO+MAXDI	—	ns
WE44	EIM_CSx_B Invalid to Input Data Invalid	0	0	—	ns
WE45	EIM_CSx_B Valid to EIM_EBx_B Valid (Write access)	WE12-WE6+(WBEA-WCSA)×t	-3.5+(WBEA-WCSA)×t	3.5+(WBEA-WCSA)×t	ns
WE46	EIM_EBx_B Invalid to EIM_CSx_B Invalid (Write access)	WE7-WE13+(WBEN-WCSN)×t	-3.5+(WBEN-WCSN)×t	3.5+(WBEN-WCSN)×t	ns
MAXDTI	Maximum delay from EIM_DTACK_B input to its internal flip-flop + 2 cycles for synchronization	10	—	10	ns
WE47	EIM_DTACK_B Active to EIM_CSx_B Invalid	MAXCO-MAXCSO+MAXDTI	MAXCO-MAXCSO+MAXDTI	—	ns
WE48	EIM_CSx_B Invalid to EIM_DTACK_B invalid	0	0	—	ns

1 For more information on configuration parameters mentioned in this table, see the i.MX 6SoloLite reference manual.

2 CSA means register setting for WCSA when in write operations or RCSA when in read operations.

3 CSN means register setting for WCSN when in write operations or RCSN when in read operations.

4 t means clock period from axi_clk frequency.

5 ADVA means register setting for WADVA when in write operations or RADVA when in read operations.

6 ADVN means register setting for WADVN when in write operations or RADVN when in read operations.

7 BE Assertion. This bit field determines when BE signal is asserted during read cycles.

Table 37. CSI Gated Clock Mode Timing Parameters (continued)

ID	Parameter	Symbol	Min	Max	Units
P4	CSI DATA hold time	tDh	1.2	—	ns
P5	CSI pixel clock high time	tCLKh	7.5	—	ns
P6	CSI pixel clock low time	tCLKl	7.5	—	ns
P7	CSI pixel clock frequency	fCLK	—	66	MHz

4.10.2.0.2 Ungated Clock Mode Timing

Figure 24 shows the ungated clock mode timings of CSI, and Table 38 describes the timing parameters (P1–P6) that are shown in the figure. In ungated mode the CSI_VSYNC and CSI_PIXCLK signals are used, and the CSI_HSYNC signal is ignored.

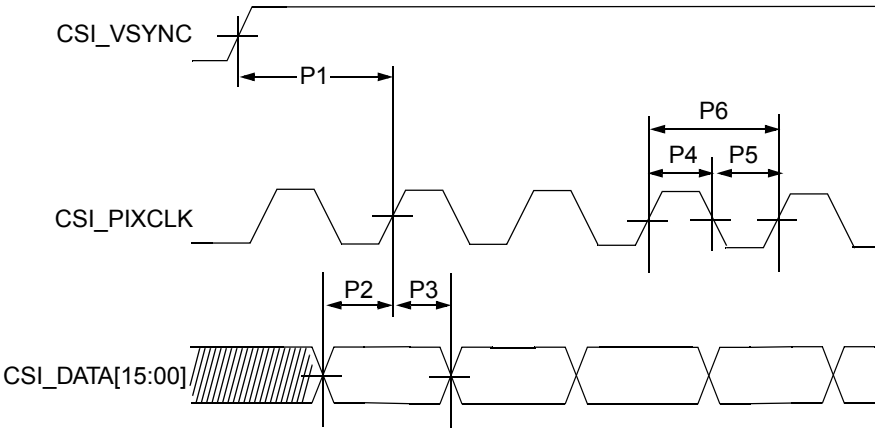

Figure 24. CSI Ungated Clock Mode—Sensor Data at Falling Edge, Latch Data at Rising Edge

Table 38. CSI Ungated Clock Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Units
P1	CSI_VSYNC to pixel clock time	tVSYNC	67.5	—	ns
P2	CSI DATA setup time	tDsu	2.5	—	ns
P3	CSI DATA hold time	tDh	1.2	—	ns
P4	CSI pixel clock high time	tCLKh	7.5	—	ns
P5	CSI pixel clock low time	tCLKl	7.5	—	ns
P6	CSI pixel clock frequency	fCLK	—	66	MHz

The CSI enables the chip to connect directly to external CMOS image sensors, which are classified as dumb or smart as follows:

- Dumb sensors only support traditional sensor timing (vertical sync (VSYNC) and horizontal sync (HSYNC)) and output-only Bayer and statistics data.
- Smart sensors support CCIR656 video decoder formats and perform additional processing of the image (for example, image compression, image pre-filtering, and various data output formats).

4.10.3.2 ECSPI Slave Mode Timing

Figure 26 depicts the timing of ECSPI in slave mode and Table 40 lists the ECSPI slave mode timing characteristics.

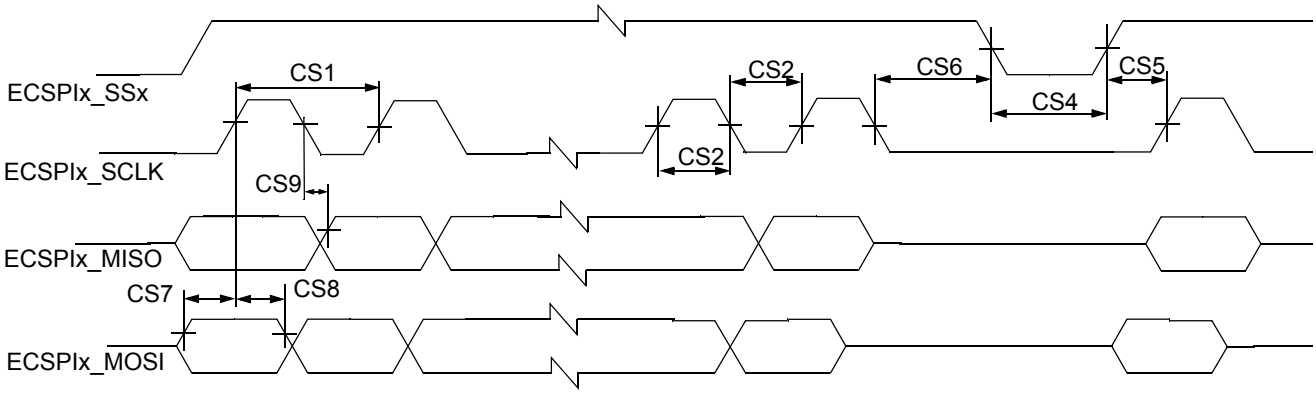

Figure 26. ECSPI Slave Mode Timing Diagram

NOTE

ECSPIx_MISO is always driven (not tri-stated) between actual data transmissions. This limits the ECSPI to be connected between a single master and a single slave.

Table 40. ECSPI Slave Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	ECSPIx_SCLK Cycle Time–Read ECSPIx_SCLK Cycle Time–Write	t_{clk}	40 15	—	ns
CS2	ECSPIx_SCLK High or Low Time–Read ECSPIx_SCLK High or Low Time–Write	t_{SW}	20 7	—	ns
CS4	ECSPIx_SSx pulse width	t_{CSLH}	Half SCLK period	—	ns
CS5	ECSPIx_SSx Lead Time (CS setup time)	t_{SCS}	5	—	ns
CS6	ECSPIx_SSx Lag Time (CS hold time)	t_{HCS}	5	—	ns
CS7	ECSPIx_MOSI Setup Time	t_{Smosi}	4	—	ns
CS8	ECSPIx_MOSI Hold Time	t_{Hmosi}	4	—	ns
CS9	ECSPIx_MISO Propagation Delay (C_{LOAD} = 20 pF)	t_{PDmiso}	4	17	ns

4.10.6.1 RMII Mode Timing Parameters

In RMII mode, FEC_TX_CLK is used as the REF_CLK which is a 50 MHz ±50 ppm continuous reference clock. FEC_RX_DV is used as the CRS_DV in RMII, and other signals under RMII mode include FEC_TX_EN, FEC_TX_DATA[1:0], FEC_RX_DATA[1:0] and optional FEC_RX_ER.

The RMII mode timing parameters are shown in Figure 31 and Table 45.

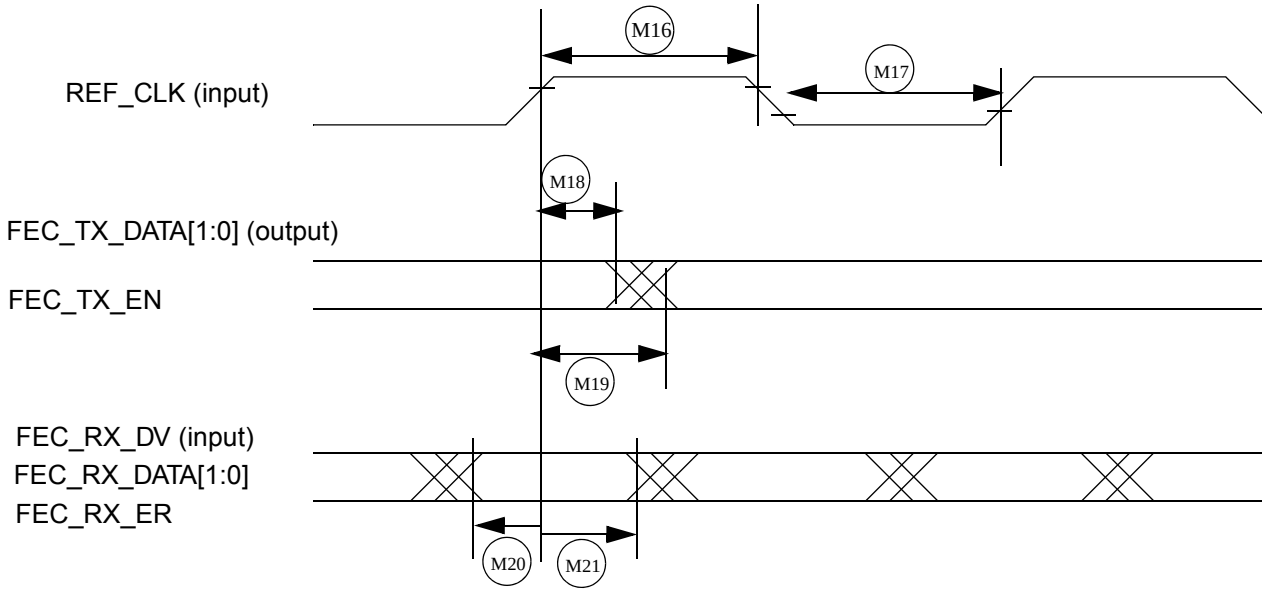

Figure 31. RMII Mode Signal Timing Diagram

Table 45. RMII Signal Timing Parameters

No.	Characteristics[1]	Min	Max	Unit
M16	REF_CLK(FEC_TX_CLK) pulse width high	35%	65%	REF_CLK period
M17	REF_CLK(FEC_TX_CLK) pulse width low	35%	65%	REF_CLK period
M18	REF_CLK to FEC_TX_DATA[1:0], FEC_TX_EN invalid	2	—	ns
M19	REF_CLK to FEC_TX_DATA[1:0], FEC_TX_EN valid	—	16	ns
M20	FEC_RX_DATA[1:0], CRS_DV(FEC_RX_DV), FEC_RX_ER to REF_CLK setup	4	—	ns
M21	REF_CLK to FEC_RX_DATA[1:0], FEC_RX_DV, FEC_RX_ER hold	2	—	ns

1 Test conditions: 25pF on each output signal.

4.10.7 I²C Module Timing Parameters

This section describes the timing parameters of the I²C module. Figure 32 depicts the timing of I²C module, and Table 46 lists the I²C module timing characteristics.

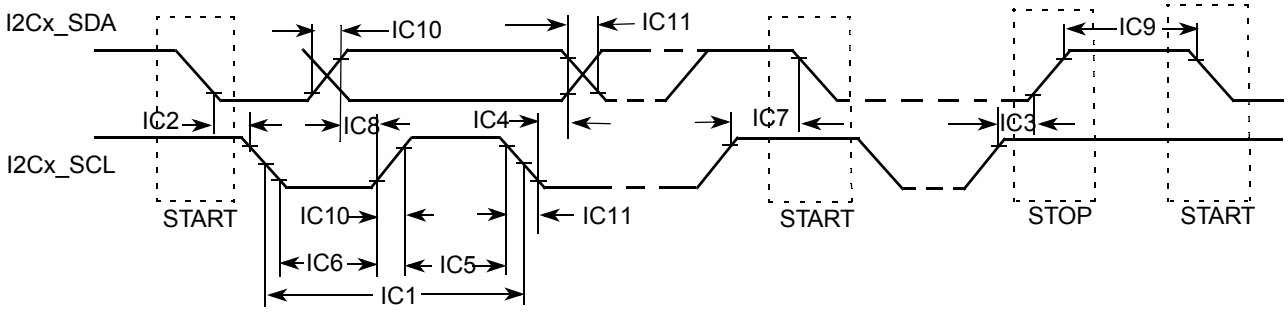

Figure 32. I²C Bus Timing Diagram

Table 46. I²C Module Timing Parameters

ID	Parameter	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
IC1	I2Cx_SCL cycle time	10	—	2.5	—	µs
IC2	Hold time (repeated) START condition	4.0	—	0.6	—	µs
IC3	Set-up time for STOP condition	4.0	—	0.6	—	µs
IC4	Data hold time	0[1]	3.45[2]	0[1]	0.9[2]	µs
IC5	HIGH Period of I2Cx_SCL	4.0	—	0.6	—	µs
IC6	LOW Period of the I2Cx_SCL	4.7	—	1.3	—	µs
IC7	Set-up time for a repeated START condition	4.7	—	0.6	—	µs
IC8	Data set-up time	250	—	100[3]	—	ns
IC9	Bus free time between a STOP and START condition	4.7	—	1.3	—	µs
IC10	Rise time of both I2Cx_SDA and I2Cx_SCL signals	—	1000	$20 + 0.1C_b$[4]	300	ns
IC11	Fall time of both I2Cx_SDA and I2Cx_SCL signals	—	300	$20 + 0.1C_b$[4]	300	ns
IC12	Capacitive load for each bus line (C_b)	—	400	—	400	pF

1 A device must internally provide a hold time of at least 300 ns for I2Cx_SDA signal in order to bridge the undefined region of the falling edge of I2Cx_SCL.

2 The maximum hold time has only to be met if the device does not stretch the LOW period (ID no IC5) of the I2Cx_SCL signal.

3 A Fast-mode I2C-bus device can be used in a Standard-mode I2C-bus system, but the requirement of Set-up time (ID No IC7) of 250 ns must be met. This automatically is the case if the device does not stretch the LOW period of the I2Cx_SCL signal. If such a device does stretch the LOW period of the I2Cx_SCL signal, it must output the next data bit to the I2Cx_SDA line max_rise_time (IC9) + data_setup_time (IC7) = 1000 + 250 = 1250 ns (according to the Standard-mode I2C-bus specification) before the I2Cx_SCL line is released.

4 C_b = total capacitance of one bus line in pF.

4.10.8 Pulse Width Modulator (PWM) Timing Parameters

This section describes the electrical information of the PWM. The PWM can be programmed to select one of three clock signals as its source frequency. The selected clock signal is passed through a prescaler before being input to the counter. The output is available at the pulse-width modulator output (PWMx_OUT) external pin (see external signals table in the i.MX 6SoloLite reference manual for PWM pin assignments).

Figure 33 depicts the timing of the PWM, and Table 47 lists the PWM timing parameters.

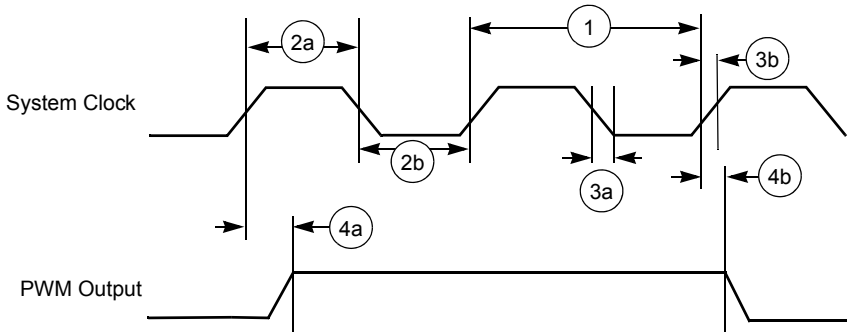

Figure 33. PWM Timing Diagram

Table 47. PWM Output Timing Parameters

Reference Number	Parameter	Min	Max	Unit
1	System CLK frequency[1]	0	ipg_clk	MHz
2a	Clock high time	12.29	—	ns
2b	Clock low time	9.91	—	ns

1 CL of PWMx_OUT = 30 pF

4.10.9 SCAN JTAG Controller (SJC) Timing Parameters

Figure 34 depicts the SJC test clock input timing. Figure 35 depicts the SJC boundary scan timing. Figure 36 depicts the SJC test access port. Signal parameters are listed in Table 48.

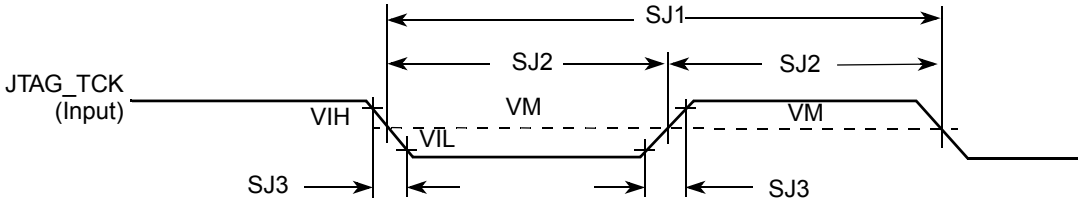

Figure 34. Test Clock Input Timing Diagram

Table 53. SSI Transmitter with External Clock Timing Parameters (continued)

ID	Parameter	Min	Max	Unit
Synchronous External Clock Operation				
SS44	AUDx_RXD setup before AUDx_TXC falling	10.0	—	ns
SS45	AUDx_RXD hold after AUDx_TXC falling	2.0	—	ns
SS46	AUDx_RXD rise/fall time	—	6.0	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TXC/RXC = 0) and a non-inverted frame sync (TXFS/RXFS = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal TXC/RXC and/or the frame sync TXFS/RXFS shown in the tables and in the figures.
- All timings are on AUDMUX Pads when SSI is used for data transfer.
- The terms WL and BL refer to Word Length (WL) and Bit Length (BL).
- For internal Frame Sync operation using external clock, the FS timing is same as that of TXD (for example, during AC97 mode of operation).

4.10.11.4 SSI Receiver Timing with External Clock

Figure 43 depicts the SSI receiver external clock timing and Table 54 lists the timing parameters for the receiver timing with the external clock.

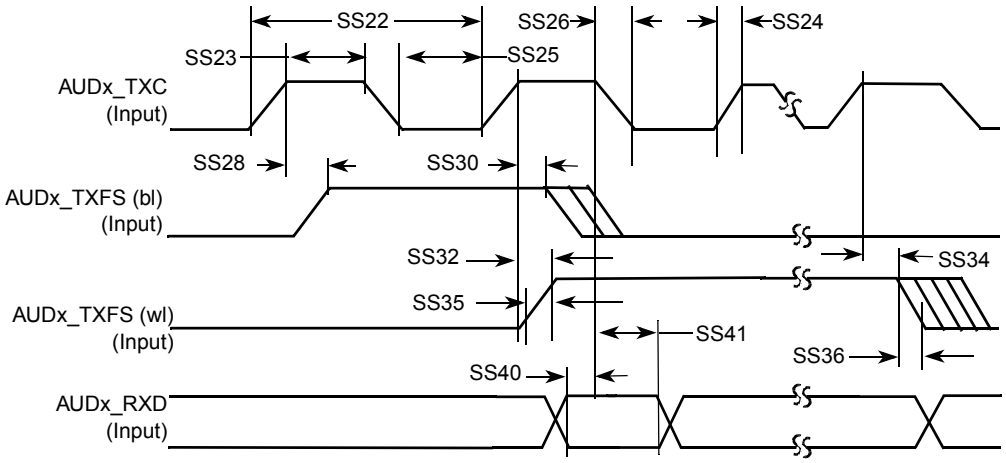

Figure 43. SSI Receiver External Clock Timing Diagram

Table 66. 13 x 13 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group[1]	Ball Type	Out of Reset Condition[2]			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value[3]
EPDC_D15	A13	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO1_GPIO[22]	Input	Keeper
EPDC_D2	B17	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO1_GPIO[9]	Input	Keeper
EPDC_D3	A16	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO1_GPIO[10]	Input	Keeper
EPDC_D4	B16	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO1_GPIO[11]	Input	Keeper
EPDC_D5	A15	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO1_GPIO[12]	Input	Keeper
EPDC_D6	B15	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO1_GPIO[13]	Input	Keeper
EPDC_D7	C15	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO1_GPIO[14]	Input	Keeper
EPDC_D8	D15	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO1_GPIO[15]	Input	Keeper
EPDC_D9	F15	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO1_GPIO[16]	Input	Keeper
EPDC_GDCLK	A12	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO1_GPIO[31]	Input	Keeper
EPDC_GDOE	B13	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[0]	Input	Keeper
EPDC_GDRL	B12	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[1]	Input	Keeper
EPDC_GDSP	A11	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[2]	Input	Keeper
EPDC_PWRCOM	B11	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[11]	Input	Keeper
EPDC_PWRCTRL0	D11	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[7]	Input	Keeper
EPDC_PWRCTRL1	E11	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[8]	Input	Keeper
EPDC_PWRCTRL2	F11	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[9]	Input	Keeper
EPDC_PWRCTRL3	G12	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[10]	Input	Keeper
EPDC_PWRINT	F10	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[12]	Input	Keeper
EPDC_PWRSTAT	E10	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[13]	Input	Keeper
EPDC_PWRWAKEUP	D10	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO2_GPIO[14]	Input	Keeper
EPDC_SDCE0	C11	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO1_GPIO[27]	Input	Keeper

Table 67. Signals with Differing Before Reset and After Reset States (continued)

Ball name	Before Reset State	
	Input/Output	Value
EIM_A22	**Input**	PD (100k)
EIM_A23	**Input**	PD (100k)
EIM_A24	**Input**	PD (100k)
EIM_EB0	**Input**	PD (100k)
EIM_EB1	**Input**	PD (100k)
EIM_LBA	**Input**	PD (100k)
EIM_RW	**Input**	PD (100k)
EIM_GPIO19	**Input**	PD (100k)
EIM_GPIO17	**Input**	PD (100k)
KEY_COL0	**Input**	PD (100k)

6.2.3 13 x 13 mm, 0.5 mm Pitch Ball Map

Table 68 shows the MAPBGA 13 x 13 mm, 0.5 mm pitch ball map.

Table 68. 13 x 13 mm, 0.5 mm Pitch Ball Map

	17	18	19	20	21	22	23	24
A	EPDC_D1	EPDC_D0	SD1_DAT7	SD1_DAT6	SD1_DAT5	SD1_DAT4	SD1_DAT1	GND
B	EPDC_D2	EPDC_BDR1	UART1_RXD	SD1_CLK	SD1_CMD	SD1_DAT3	SD1_DAT0	KEY_ROW7
C	NC	EPDC_BDR0	GND	NC	NC	SD1_DAT2	KEY_COL7	KEY_ROW6
D	NC	I2C2_SDA	UART1_TXD	NC	NC	KEY_COL6	KEY_ROW5	KEY_COL5
E	NC	I2C2_SCL	KEY_ROW4	KEY_COL4	KEY_ROW3	KEY_COL3	KEY_COL2	KEY_ROW2
F	NC	WDOG_B	NC	NC	NC	NC	KEY_COL1	KEY_ROW1
G	GND	GND	NC	NC	NC	NC	KEY_COL0	KEY_ROW0
H	NC	GND	AUD_MCLK	AUD_TXC	AUD_TXFS	GND	LCD_HSYNC	LCD_RESET
J	VDD_ARM_CAP	VDD_ARM_CAP	AUD_RXFS	AUD_RXD	AUD_RXC	AUD_TXD	LCD_VSYNC	LCD_ENABLE
K	VDD_ARM_CAP	VDD_ARM_CAP	NC	NC	NC	NC	LCD_DAT22	LCD_DAT23
L	NC	NVCC33_IO	NC	NC	NC	NC	LCD_DAT20	LCD_DAT21
M	GND	NVCC33_IO	ECSPI1_MISO	NVCC18_IO	ECSPI1_SS0	LCD_DAT17	LCD_DAT18	LCD_DAT19
N	GND	VDD_SOC_CAP	ECSPI1_SCLK	ECSPI1_MOSI	LCD_DAT14	GND	LCD_DAT15	LCD_DAT16
P	NC	VDD_SOC_CAP	NC	NC	NC	NC	LCD_DAT12	LCD_DAT13
R	VDD_SOC_IN	VDD_SOC_CAP	NC	NC	NC	NC	LCD_DAT10	LCD_DAT11
T	VDD_SOC_IN	VDD_SOC_IN	NVCC33_IO	ECSPI2_MISO	ECSPI_SS0	LCD_CLK	LCD_DAT8	LCD_DAT9
U	NC	GND	ECSPI2_SCLK	ECSPI2_MOSI	LCD_DAT5	GND	LCD_DAT6	LCD_DAT7
V	GND_KELVIN	GND	NC	NC	NC	NC	LCD_DAT3	LCD_DAT4
W	NC	ONOFF	NC	NC	NC	NC	LCD_DAT1	LCD_DAT2
Y	NC	TAMPER	NVCC_PLL	SD2_DAT5	SD2_DAT6	SD2_DAT7	SD2_RST	LCD_DAT0
AA	NC	USB_OTG1_VBUS	RTC_XTALO	NC	NC	SD2_DAT2	SD2_DAT3	SD2_DAT4
AB	NC	GND	RTC_XTALI	NC	NC	SD2_DAt0	SD2_DAT1	SD2_CMD
AC	USB_OTG2_DP	GND	USB_OTG1_DP	VDD_SNVS_IN	XTALO	USB_OTG_CHD_B	CLK1_P	SD2_CLK
AD	USB_OTG2_DN	USB_OTG2_VBUS	USB_OTG1_DN	VDD_SNVS_CAP	XTALI	GPANAIO	CLK1_N	GND

Table 68. 13 x 13 mm, 0.5 mm Pitch Ball Map (continued)

	9	10	11	12	13	14	15	16
A	EPDC_SDCE3	EPDC_SDCE1	EPDC_GDSP	EPDC_GDCLK	EPDC_D15	EPDC_D14	EPDC_D5	EPDC_D3
B	EPDC_SDCE2	EPDC_SDCLK	EPDC_PRWCOM	EPDC_GDRL	EPDC_GDOE	EPDC_D13	EPDC_D6	EPDC_D4
C	**NC**	GND	EPDC_SDCE0	**NC**	**NC**	GND	EPDC_D7	**NC**
D	**NC**	EPDC_PWRWAKEUP	EPDC_PWRCTRL0	**NC**	**NC**	EPDC_D12	EPDC_D8	**NC**
E	**NC**	EPDC_PWRSTAT	EPDC_PWRCTRL1	**NC**	**NC**	NVCC18_IO	NVCC18_IO	**NC**
F	**NC**	EPDC_PWRINT	EPDC_PWRCTRL2	**NC**	**NC**	EPDC_D11	EPDC_D9	**NC**
G	GND	GND	GND	EPDC_PWRCTRL3	GND	GND	GND	EPDC_D10
H	**NC**	NVCC33_IO	NVCC33_IO	**NC**	**NC**	NVCC33_IO	NVCC33_IO	**NC**
J	VDD_SOC_CAP	VDD_SOC_IN	VDD_SOC_IN	VDD_ARM_IN	VDD_ARM_IN	VDD_ARM_IN	VDD_ARM_CAP	VDD_ARM_CAP
K	VDD_SOC_CAP	VDD_SOC_IN	VDD_SOC_IN	VDD_ARM_IN	VDD_ARM_IN	VDD_ARM_IN	VDD_ARM_CAP	VDD_ARM_CAP
L	GND	GND	GND	GND	GND	GND	GND	GND
M	GND	GND	GND	GND	GND	GND	GND	GND
N	GND	GND	GND	GND	GND	GND	GND	GND
P	GND	GND	GND	GND	GND	GND	GND	GND
R	VDD_PU_CAP	VDD_PU_IN	VDD_PU_IN	VDD_HIGH_IN	VDD_HIGH_IN	VDD_HIGH_CAP	VDD_HIGH_CAP	VDD_SOC_IN
T	VDD_PU_CAP	VDD_PU_IN	VDD_PU_IN	VDD_HIGH_IN	VDD_HIGH_IN	VDD_HIGH_CAP	VDD_HIGH_CAP	VDD_SOC_IN
U	**NC**	NVCC33_IO	NVCC33_IO	**NC**	**NC**	VDD_USB_CAP	TEST_MODE	**NC**
V	GND	GND	GND	GND	GND	GND	GND	GND
W	**NC**	FEC_REF_CLK	FEC_TXD1	**NC**	**NC**	JTAG_TDI	JTAG_TDO	**NC**
Y	**NC**	FEC_TXD0	NVCC18_IO	**NC**	**NC**	JTAG_MOD	JTAG_TMS	**NC**
AA	**NC**	FEC_RXD0	SD3_CMD	**NC**	**NC**	JTAG_TCK	JTAG_TRSTB	**NC**
AB	**NC**	GND	SD3_CLk	**NC**	**NC**	GND	BOOT_MODE1	**NC**
AC	FEC_CRS_DV	FEC_RXD1	SD3_DAT0	SD3_DAT2	I2C1_SCL	REF_CLK_24M	BOOT_MODE0	POR_B
AD	FEC_RX_ER	FEC_TX_EN	SD3_DAT1	SD3_DAT3	I2C1_SDA	REF_CLK_32K	PMIC_ON_REQ	PMIC_STBY_REQ

Table 68. 13 x 13 mm, 0.5 mm Pitch Ball Map (continued)

	1	2	3	4	5	6	7	8
A	GND	DRAM_SDQS3_B	DRAM_D24	GND	DRAM_D27	DRAM_D29	GND	DRAM_D31
B	DRAM_D14	DRAM_D15	DRAM_SDQS3	DRAM_D25	DRAM_D26	DRAM_D28	DRAM_D30	EPDC_SDLE
C	DRAM_D12	DRAM_D13	DRAM_DQM3	**NC**	**NC**	GND	EPDC_VCOM0	**NC**
D	GND	GND	DRAM_D11	**NC**	**NC**	DRAM_RESET	EPDC_VCOM1	**NC**
E	DRAM_D9	DRAM_D8	DRAM_D10	DRAM_SDODT1	GND	NVCC_DRAM	EPDC_SDOE	**NC**
F	DRAM_SDQS1	DRAM_SDQS1_B	**NC**	**NC**	**NC**	**NC**	EPDC_SDSHR	**NC**
G	GND	DRAM_DQM1	**NC**	**NC**	**NC**	**NC**	NVCC_DRAM	GND
H	DRAM_SDBA2	ZQPAD	GND	DRAM_A7	DRAM_A13	NVCC_DRAM	GND	**NC**
J	DRAM_SDBA0	DRAM_A10	DRAM_A8	DRAM_A9	GND	NVCC_DRAM	VDD_SOC_CAP	VDD_SOC_CAP
K	GND	DRAM_A15	**NC**	**NC**	**NC**	**NC**	VDD_SOC_CAP	VDD_SOC_CAP
L	DRAM_SDCLK_0	DRAM_CS1	**NC**	**NC**	**NC**	**NC**	GND	**NC**
M	DRAM_SDCLK_0_B	DRAM_SDCKE1	DRAM_A5	DRAM_A6	GND	NVCC_DRAM_2P5	GND	GND
N	DRAM_RAS	DRAM_CS0	GND	DRAM_A4	DRAM_VREF	NVCC_DRAM	GND	GND
P	DRAM_CAS	SDCKE0	**NC**	**NC**	**NC**	**NC**	NVCC_DRAM	**NC**
R	GND	DRAM_A14	**NC**	**NC**	**NC**	**NC**	VDD_PU_CAP	VDD_PU_CAP
T	DRAM_SDBA1	DRAM_A11	DRAM_A2	DRAM_A3	GND	NVCC_DRAM	VDD_PU_CAP	VDD_PU_CAP
U	DRAM_SDWE	DRAM_A12	GND	DRAM_A0	DRAM_A1	NVCC_DRAM	GND	**NC**
V	GND	DRAM_DQM0	**NC**	**NC**	**NC**	**NC**	NVCC_DRAM	GND
W	DRAM_SDQS0_B	DRAM_SDQS0	**NC**	**NC**	**NC**	**NC**	NVCC_1P2	**NC**
Y	DRAM_D6	DRAM_D7	DRAM_D5	DRAM_SDODT0	GND	NVCC_DRAM	PWM1	**NC**
AA	GND	GND	DRAM_D4	**NC**	**NC**	HSIC_DAT	FEC_MDC	**NC**
AB	DRAM_D3	DRAM_D2	DRAM_DQM2	**NC**	**NC**	HSIC_STROBE	FEC_MDIO	**NC**
AC	DRAM_D1	DRAM_D0	DRAm_SDQS2	DRAM_D22	DRAM_D21	DRAM_D19	DRAM_D17	FEC_TX_CLK
AD	GND	DRAM_SDQS2_B	DRAM_D23	GND	DRAM_D20	DRAM_D18	GND	DRAM_D16

Table 70. i.MX 6SoloLite Data Sheet Document Revision History (continued)

Rev. Number	Date	Substantive Change(s)
4 *Continued*	11/2016	• Section 4.2.2, “Power-Down Sequence,” Replaced contents of section with sentence: “There are no special requirements on the power-down sequence other than …”. • Section 4.5.2, “OSC32K”: Removed text regarding coin cell from third paragraph and removed second NOTE about third party coin cell manufacturer. • Section 4.6, “I/O DC Parameters”: Removed second bullet regarding single voltage GPIO cell set. • Section 4.6.1, “XTALI and RTC_XTALI (Clock Inputs) DC Parameters” Added NOTE after table.Table 20, "XTALI and RTC_XTALI DC Parameters”: – Added parameter rows: Input capacitance; XTALI input leakage; and DC input current. – Added new footnote, “This voltage specification…” • Section 4.6.3, “*Single Voltage General Purpose I/O (GPIO) DC Parameters”* removed section. • Section 4.8, “Output Buffer Impedance Parameters”: Removed second bullet “Single voltage General Purpose I/O cell set …”. • Table 28, "DVGPIO Output Buffer Average Impedance (OVDD 1.8 V)”: Changed all Typical values. • Table 29, "DVGPIO Output Buffer Average Impedance (OVDD 3.3 V)”: Changed all Typical values. • Section 4.8.2, “*Single Voltage GPIO Output Buffer Impedance*”: removed section. • Table 34, "EIM Bus Timing Parameters, Updates throughout table to include min/max values. • Table 35, "EIM Asynchronous Timing Parameters Table Relative Chip Select, Updates throughout table to include min/max values. • Section 4.9.4, “Multi-Mode DDR Controller (MMDC),” created this new section. • Removed: Section 4.9.5, “DDR SDRAM Specific Parameters (DDR3 and LPDDR2),” Section 4.9.5.1, “DDR3 Parameters,” and Section 4.9.5.2, “LPDDR2 Parameters.” • Table 37, "CSI Gated Clock Mode Timing Parameters,” – Parameter P5 reduced (improved) from 10ns to 7.5 ns. – Parameter P6 reduced (improved) from 10ns to 7.5 ns. – Parameter P7 corrected to 66 MHz (no functional change). • Table 38, "CSI Ungated Clock Mode Timing Parameters,” – Parameter P4 reduced (improved) from 10ns to 7.5 ns. – Parameter P5 reduced (improved) from 10ns to 7.5 ns. – Parameter P6 corrected to 66 MHz (no functional change). • Section 4.10.3.1, “ECSPI Master Mode Timing,” Added new NOTE under Figure 25. • Section 4.10.3.2, “ECSPI Slave Mode Timing,” Added new NOTE under Figure 26. • Section 4.10.4.3, “SDR50/SDR104 AC Timing Parameters,” Figure 29 updated to correct SD5. • Table 43, "SDR50/SDR104 Interface Timing Parameters,” – SD2, changed minimum value to “0.46”, and changed maximum value to “0.54”. – SD3, changed minimum value to “0.46”, and changed maximum value to “0.54”. – SD2 (parameter Clock High Time), parameter name corrected to SD3. – SD5, changed maximum value to “0.74”. • Section 4.10.5, “HS200 Mode Timing Parameters,” Added this new section. • Section 4.10.14, “USB PHY Parameters,” Added new text to second paragraph “USB Host with the amendments below…” • Table 63, "Interfaces Allocation During Boot USDHC-1–USDHC-4 row, replaced existing text with “Refer to the table “SD/MMC…” • Table 65, "13 x 13 mm Supplies Contact Assignment,” – GPANAIO: changed remark from “Analog pad” to “Analog output for NXP use…” – ZQPAD: changed remark to “Connect ZQPAD to…” • Table 66, "13 x 13 mm Functional Contact Assignments,” DRAM_SDCLK_0, corrected “Input” to “Output” and Value to “0”. • Section 6.2.2, “13 x 13 mm Ground, Power, Sense, Not Connected, and Reference Contact Assignments,” Added new text “For most of the signals…” after Table 66. • Table 68, "13 x 13 mm, 0.5 mm Pitch Ball Map,” ball AD6 name corrected to “DRAM_D18”.