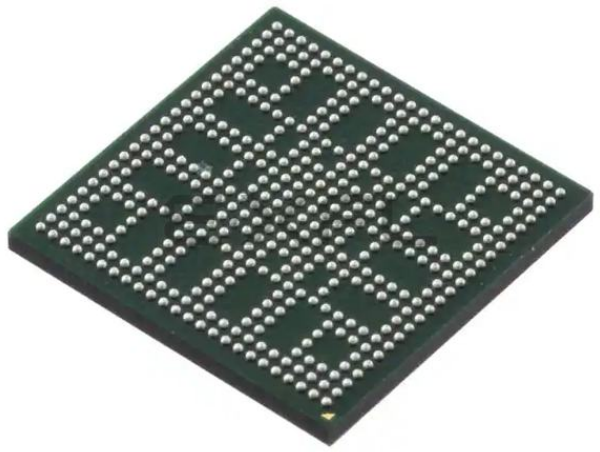

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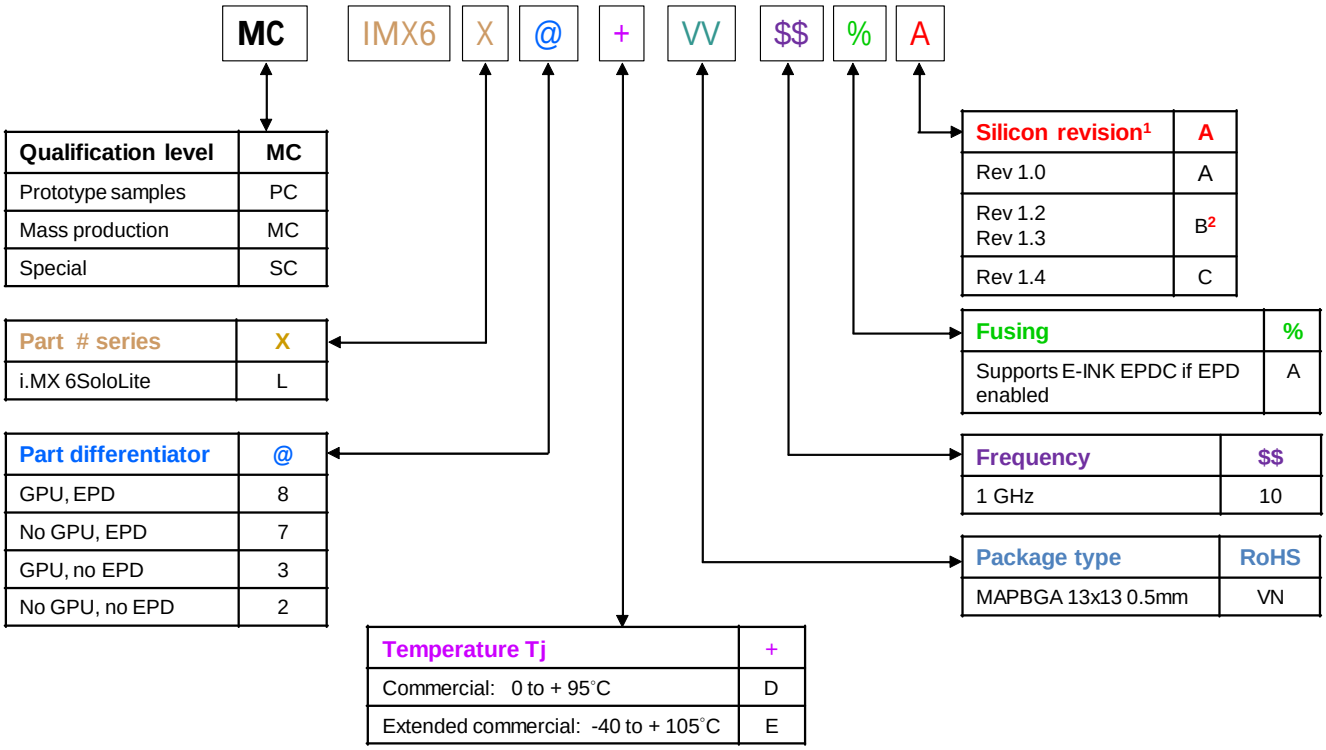
Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	1.0GHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	LPDDR2, LVDDR3, DDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + PHY (3)
Voltage - I/O	1.2V, 1.8V, 3.0V
Operating Temperature	0°C ~ 95°C (TJ)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	432-TFBGA
Supplier Device Package	432-MAPBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6l8dvn10ac



1. See the nxp.com\imx6series Web page for latest information on the available silicon revision.
2. Rev 1.2 (USB_ANALOG_DIGPROG register = 0x0062_0002)
   Rev 1.3 (USB_ANALOG_DIGPROG register = 0x0062_0003)

Figure 1. Part Number Nomenclature—i.MX 6SoloLite

1.2 Features

The i.MX 6SoloLite processor is based on ARM Cortex-A9 MPCore multicore processor, which has the following features:

- ARM Cortex-A9 MPCore CPU processor (with TrustZone)
- The core configuration is symmetric, where each core includes:
  - 32 KByte L1 Instruction Cache
  - 32 KByte L1 Data Cache
  - Private Timer and Watchdog
  - Cortex-A9 NEON MPE (Media Processing Engine) co-processor

The ARM Cortex-A9 MPCore complex includes:

- General Interrupt Controller (GIC) with 128 interrupt support
- Global Timer
- Snoop Control Unit (SCU)
- 256 KB unified I/D L2 cache
- Two Master AXI (64-bit) bus interfaces output of L2 cache
- Frequency of the core (including NEON and L1 cache) as per Table 9, "Operating Ranges," on page 21

- NEON MPE coprocessor
  - SIMD Media Processing Architecture
  - NEON register file with 32x64-bit general-purpose registers
  - NEON Integer execute pipeline (ALU, Shift, MAC)
  - NEON dual, single-precision floating point execute pipeline (FADD, FMUL)
  - NEON load/store and permute pipeline

The SoC-level memory system consists of the following additional components:

  - Boot ROM, including HAB (96 KB)
  - Internal multimedia / shared, fast access RAM (OCRAM, 128 KB)
- External memory interfaces:
  - 16-bit, and 32-bit DDR3-800, and LPDDR2-800 channels
  - 16/32-bit NOR Flash.
  - 16/32-bit PSRAM, Cellular RAM (32 bits or less)

Each i.MX 6SoloLite processor enables the following interfaces to external devices (some of them are muxed and not available simultaneously):

- Displays—Total of three interfaces are available.
  - LCD, 24-bit display port, up to 225 Mpixels/sec (for example, WUXGA at 60 Hz)
  - EPDC, color, and monochrome E Ink, up to 1650 x 2332 resolution and 5-bit grayscale
- Camera sensors:
  - Parallel Camera port (up to 16-bit and up to 66 MHz peak)
- Expansion cards:
  - Four MMC/SD/SDIO card ports all supporting:
    - 1-bit or 4-bit transfer mode specifications for SD and SDIO cards up to UHS-I SDR-104 mode (104 MB/s max)
    - 1-bit, 4-bit, or 8-bit transfer mode specifications for MMC cards up to 52 MHz in both SDR and DDR modes (104 MB/s max)
    - 4-bit or 8-bit transfer mode specifications for eMMC chips up to 200 MHz in HS200 mode (200 MB/s max)
- USB:
  - Two High Speed (HS) USB 2.0 OTG (Up to 480 Mbps), with integrated HS USB Phy
  - One USB 2.0 (480 Mbps) hosts:
    - One HS hosts with integrated HS-IC USB (High Speed Inter-Chip USB) Phy
- Miscellaneous IPs and interfaces:
  - SSI block—capable of supporting audio sample frequencies up to 192 kHz stereo inputs and outputs with I^2S mode
  - Five UARTs, up to 5.0 Mbps each:
    - Providing RS232 interface
    - Supporting 9-bit RS485 multidrop mode

  - One of the five UARTs (UART1) supports 8-wire while others four supports 4-wire. This is due to the SoC IOMUX limitation, since all UART IPs are identical.
- Four eCSPI (Enhanced CSPI)
- Three I^2C, supporting 400 kbps
- Ethernet Controller, 10/100 Mbps
- Four Pulse Width Modulators (PWM)
- System JTAG Controller (SJC)
- GPIO with interrupt capabilities
- 8x8 Key Pad Port (KPP)
- Sony Philips Digital Interface (SPDIF), Rx and Tx
- Two Watchdog timers (WDOG)
- Audio MUX (AUDMUX)

The i.MX 6SoloLite processor integrates advanced power management unit and controllers:

- Provide PMU, including LDO supplies, for on-chip resources
- Use Temperature Sensor for monitoring the die temperature
- Support DVFS techniques for low power modes
- Use Software State Retention and Power Gating for ARM and MPE
- Support various levels of system power modes
- Use flexible clock gating control scheme

The i.MX 6SoloLite processor uses dedicated hardware accelerators to meet the targeted multimedia performance. The use of hardware accelerators is a key factor in obtaining high performance at low power consumption numbers, while having the CPU core relatively free for performing other tasks.

The i.MX 6SoloLite processor incorporates the following hardware accelerators:

- GPU2Dv2—2D Graphics Processing Unit (BitBlt).
- GPUVG—OpenVG 1.1 Graphics Processing Unit.
- PXP—PiXel Processing Pipeline. Off loading key pixel processing operations are required to support the EPD display applications.

Security functions are enabled and accelerated by the following hardware:

- ARM TrustZone including the TZ architecture (separation of interrupts, memory mapping, and so on.)
- SJC—System JTAG Controller. Protecting JTAG from debug port attacks by regulating or blocking the access to the system debug features.
- SNVS—Secure Non-Volatile Storage, including Secure Real Time Clock.
- CSU—Central Security Unit. Enhancement for the IC Identification Module (IIM). Will be configured during boot and by eFUSEs and will determine the security level operation mode as well as the TZ policy.
- A-HAB—Advanced High Assurance Boot—HABv4 with the new embedded enhancements: SHA-256, 2048-bit RSA key, version control mechanism, warm boot, CSU, and TZ initialization.

Table 2. i.MX 6SoloLite Modules List (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
uSDHC-1 uSDHC-2 uSDHC-2 uSDHC-4	SD/MMC and SDXC Enhanced Multi-Media Card / Secure Digital Host Controller	Connectivity Peripherals	i.MX 6SoloLite specific SoC characteristics: All four MMC/SD/SDIO controller IPs are identical and are based on the uSDHC IP. They are: • Conforms to the SD Host Controller Standard Specification version 3.0. • Fully compliant with MMC command/response sets and Physical Layer as defined in the Multimedia Card System Specification, v4.2/4.3/4.4/4.41/4.5 including high-capacity (size > 2 GB) cards HC MMC. Hardware reset as specified for eMMC cards is supported at ports 3 and 4 only. • Fully compliant with SD command/response sets and Physical Layer as defined in the SD Memory Card Specifications, v3.0 including high-capacity SDHC cards up to 32 GB and SDXC cards up to 2 TB. • Fully compliant with SDIO command/response sets and interrupt/read-wait mode as defined in the SDIO Card Specification, Part E1, v1.10 • Fully compliant with SD Card Specification, Part A2, SD Host Controller Standard Specification, v2.00 All four ports support: • 1-bit or 4-bit transfer mode specifications for SD and SDIO cards up to UHS-I SDR104 mode (104 MB/s max) • 1-bit, 4-bit, or 8-bit transfer mode specifications for MMC cards up to 52 MHz in both SDR and DDR modes (104 MB/s max) • 4-bit or 8-bit transfer mode specifications for eMMC chips up to 200 MHz in HS200 mode (200 MB/s max) However, the SoC level integration and I/O muxing logic restrict the functionality to the following: • Instances 1 and 2 are primarily intended to serve as external slots or interfaces to on-board SDIO devices. These ports are equipped with “Card detection” and “Write Protection” pads and do not support hardware reset. • All ports can work with 1.8 V and 3.3 V cards. There are two completely independent I/O power domains for Ports 1 and 2 in four bit configuration (SD interface). Port 3 is placed in an independent power domain and port 4 shares its power domain with other interfaces.
WDOG-1	Watchdog	Timer Peripherals	The Watchdog Timer supports two comparison points during each counting period. Each of the comparison points is configurable to evoke an interrupt to the ARM core, and a second point evokes an external event on the WDOG line.
WDOG-2 (TZ)	Watchdog (TrustZone)	Timer Peripherals	The TrustZone Watchdog (TZ WDOG) timer module protects against TrustZone starvation by providing a method of escaping normal mode and forcing a switch to the TZ mode. TZ starvation is a situation where the normal OS prevents switching to the TZ mode. Such situation is undesirable as it can compromise the system’s security. Once the TZ WDOG module is activated, it must be serviced by TZ software on a periodic basis. If servicing does not take place, the timer times out. Upon a time-out, the TZ WDOG asserts a TZ mapped interrupt that forces switching to the TZ mode. If it is still not served, the TZ WDOG asserts a security violation signal to the CSU. The TZ WDOG module cannot be programmed or deactivated by a normal mode Software.
XTALOSC	Crystal Oscillator I/F	Clocking	The XTALOSC module enables connectivity to external crystal oscillator device. In a typical application use-case, it is used for 24 MHz oscillator.

Table 9 provides the operating ranges of the i.MX 6SoloLite processor. For details on the chip's power structure, see the “Power Management Unit (PMU)” chapter of the *i.MX 6SoloLite Reference Manual* (IMX6SLRM).

Table 9. Operating Ranges

Parameter Description	Symbol	Min	Typ	Max[1]	Unit	Comment
Run mode: LDO enabled	VDD_ARM_IN	1.375[2]	—	1.5	V	LDO output set at 1.250V minimum for operation up to 996 MHz
		1.275[2]	—	1.5	V	LDO output set at 1.150V minimum for operation up to 792 MHz
		1.075[2]	—	1.5	V	LDO output set at 0.95V minimum for operation up to 396 MHz
		1.075[2]	—	1.5	V	LDO output set at 0.950V minimum for operation up to 192 MHz
		1.050[2]	—	1.5	V	LDO output set at 0.9250V minimum for operation up to 24 MHz
	VDD_SOC_IN[3] VDD_PU_IN	1.275[2,4]	—	1.5	V	VDD_SOC and VDD_PU LDO outputs (VDD_SOC_CAP and VDD_PU_CAP) require 1.15 V minimum
Run mode: LDO bypassed	VDD_ARM_IN	1.250	—	1.3	V	LDO bypassed for operation up to 996 MHz
		1.150	—	1.3	V	LDO bypassed for operation up to 792 MHz
		0.950	—	1.3	V	LDO bypassed for operation up to 396 MHz
		0.950	—	1.3	V	LDO bypassed for operation up to 192 MHz
		0.925	—	1.3	V	LDO bypassed for operation up to 24 MHz
	VDD_SOC_IN[3] VDD_PU_IN	1.15[4]	—	1.3	V	—
Standby/DSM Mode	VDD_ARM_IN	0.9	—	1.3	V	See Table 12, "Stop Mode Current and Power Consumption," on page 25.
	VDD_SOC_IN VDD_PU_IN	0.9	—	1.3	V	
VDDHIGH internal Regulator	VDD_HIGH_IN[5]	2.8	—	3.3	V	Must match the range of voltages that the rechargeable backup battery supports.
Backup battery supply range	VDD_SNVS_IN[5]	2.7	—	3.6	V	Should be supplied from the same supply as VDD_HIGH_IN if the system does not require keeping real time and other data on OFF state.
USB supply voltages	USB_OTG1_VBUS USB_OTG2_VBUS	4.4	—	5.25	V	—
DDR I/O supply	NVCC_DRAM	1.14	1.2	1.3	V	LPDDR2
		1.425	1.5	1.575	V	DDR3
	NVCC_DRAM_2P5	2.5	2.5	2.75	V	—

4.1.6 Low Power Mode Supply Currents

Table 12 shows the current core consumption (not including I/O) of i.MX 6SoloLite processor in selected low power modes.

Table 12. Stop Mode Current and Power Consumption

Mode	Test Conditions	Supply	Typical[1]	Unit
WAIT	• ARM, SoC, and PU LDOs are set to 1.225 V • HIGH LDO set to 2.5 V • Clocks are gated • DDR is in self refresh • PLLs are active in bypass (24 MHz) • Supply voltages remain ON	VDD_ARM_IN (1.375 V)	4	mA
		VDD_SOC_IN (1.375 V)	7.5	
		VDD_PU_IN (1.375 V)	1.5	
		VDD_HIGH_IN(3.0 V)	9	
		Total	44.9	mW
STOP_ON	• ARM LDO set to 0.9 V • SoC and PU LDOs set to 1.225 V • HIGH LDO set to 2.5 V • PLLs disabled • DDR is in self refresh	VDD_ARM_IN (1.375 V)	2.5	mA
		VDD_SOC_IN (1.375 V)	7.5	
		VDD_PU_IN (1.375 V)	1.5	
		VDD_HIGH_IN (3.0 V)	4.5	
		Total	29.3	mW
STOP_OFF	• ARM LDO set to 0.9 V • SoC LDO set to 1.225 V • PU LDO is power gated • HIGH LDO set to 2.5 V • PLLs disabled • DDR is in self refresh	VDD_ARM_IN (1.375 V)	2.5	mA
		VDD_SOC_IN (1.375 V)	7.5	
		VDD_PU_IN (1.375 V)	0.1	
		VDD_HIGH_IN (3.0 V)	4.0	
		Total	25.9	mW
STANDBY	• ARM and PU LDOs are power gated • SoC LDO is in bypass • HIGH LDO is set to 2.5 V • PLLs are disabled • Low voltage • Well Bias ON • XTAL is enabled	VDD_ARM_IN (0.9 V)	0.1	mA
		VDD_SoC_IN (0.9 V)	1.0	
		VDD_PU_IN (0.9 V)	0.1	
		VDD_HIGH_IN (3.0 V)	3	
		Total	10.1	mW
Deep Sleep Mode (DSM)	• ARM and PU LDOs are power gated • SoC LDO is in bypass • HIGH LDO is set to 2.5 V • PLLs are disabled • Low voltage • Well Bias ON • XTAL and bandgap are disabled	VDD_ARM_IN (0.9 V)	0.1	mA
		VDD_SoC_IN (0.9 V)	0.75	
		VDD_PU_IN (0.9 V)	0.1	
		VDD_HIGH_IN (3.0 V)	0.15	
		Total	1.3	mW
SNVS Only	• VDD_SNVS_IN powered • All other supplies off • SRTC running	VDD_SNVS_IN (2.8V)	41	µA
		Total	115	µW

[1] The typical values shown here are for information only and are not guaranteed. These values are average values measured on a worst-case wafer at 25°C.

For information on external capacitor requirements for this regulator, see the Hardware Development Guide for i.MX 6SoloLite Applications Processors (IMX6SLHDG).

For additional information, see the i.MX 6SoloLite reference manual.

4.4 PLL's Electrical Characteristics

4.4.1 Audio/Video PLL's Electrical Parameters

Table 14. Audio/Video PLL's Electrical Parameters

Parameter	Value
Clock output range	650 MHz ~1.3 GHz
Reference clock	24 MHz
Lock time	<11250 reference cycles (450 μs)

4.4.2 528 MHz PLL

Table 15. 528 MHz PLL's Electrical Parameters

Parameter	Value
Clock output range	528 MHz PLL output
Reference clock	24 MHz
Lock time	<11250 reference cycles (15 μs)

4.4.3 Ethernet PLL

Table 16. Ethernet PLL's Electrical Parameters

Parameter	Value
Clock output range	500 MHz
Reference clock	24 MHz
Lock time	<11250 reference cycles (450 μs)

Table 23. DDR3 I/O DC Electrical Parameters[1] (continued)

Parameters	Symbol	Test Conditions	Min	Max	Unit
Input current (no pull-up/down)	Iin	Vin = 0 or OVDD	-2.9	2.9	μA
Pull-up/pull-down impedance mismatch	MMpupd	—	-10	10	%
240 Ω unit calibration resolution	Rres	—	—	10	Ω
Keeper circuit resistance[5]	Rkeep	—	105	175	kΩ

1 Note that the JEDEC DDR3 specification (JESD79_3D) supersedes any specification in this document.

2 OVDD – I/O power supply (1.425 V – 1.575 V for DDR3

3 Vref – DDR3 external reference voltage

4 The single-ended signals need to be within the respective limits (Vih(dc) max, Vil(dc) min) for single-ended signals as well as the limitations for overshoot and undershoot (see Table 27).

5 Use an off-chip pull resistor of 10 kΩ or less to override this keeper.

4.7 I/O AC Parameters

This section includes the AC parameters of the following I/O types:

- General Purpose I/O (GPIO)
- Dual Voltage General Purpose I/O (DVGPIO)
- Double Data Rate I/O (DDR) for LPDDR2 and DDR3 modes

The GPIO and DDR I/O load circuit and output transition time waveforms are shown in Figure 5 and Figure 6.

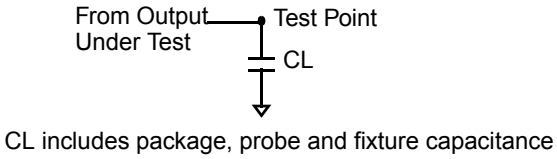


Figure 5. Load Circuit for Output

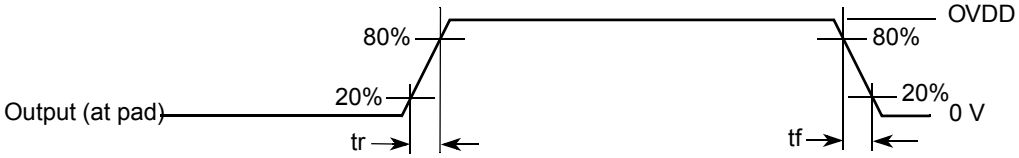


Figure 6. Output Transition Time Waveform

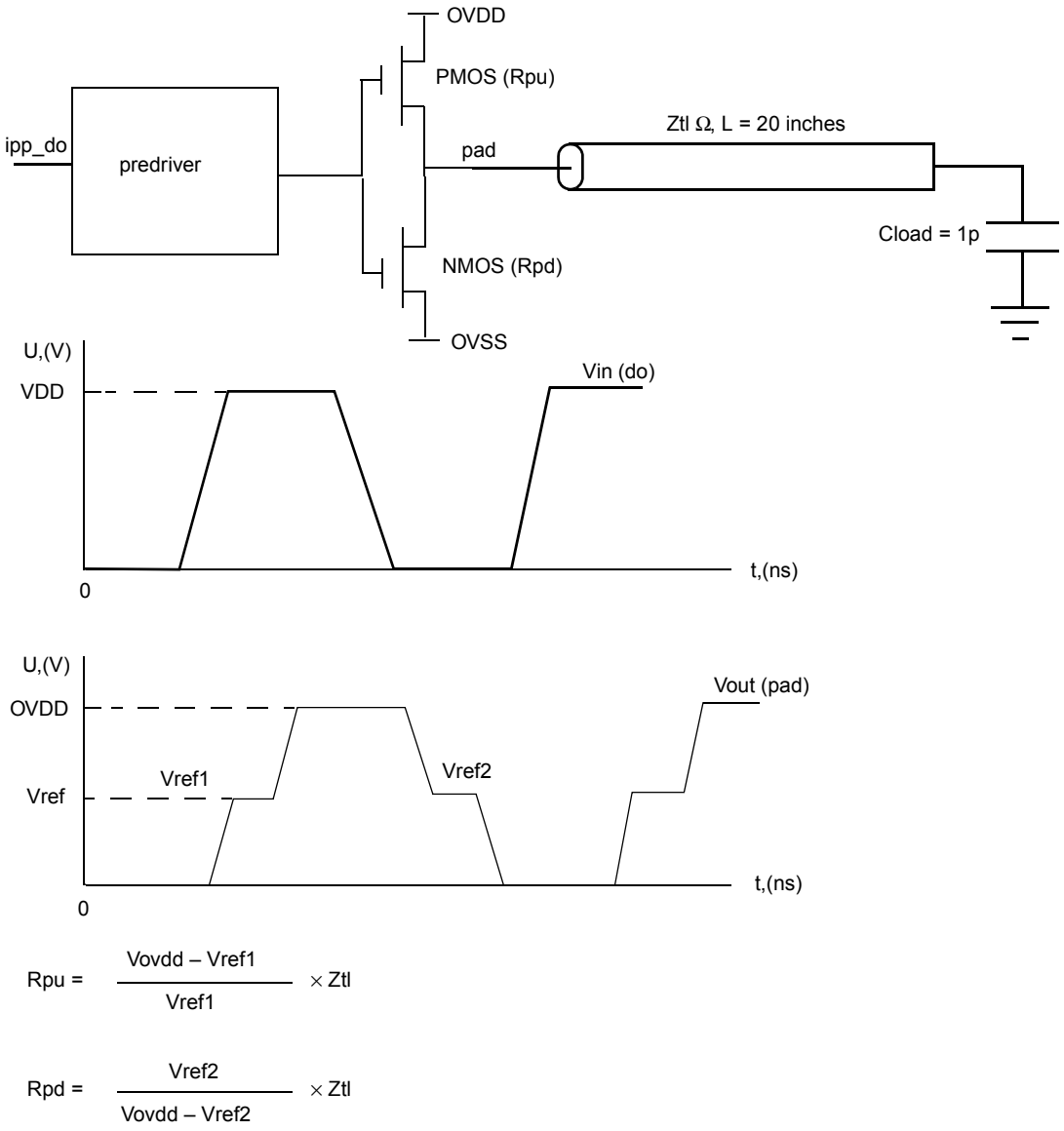


Figure 7. Impedance Matching Load for Measurement

4.8.1 Dual Voltage GPIO Output Buffer Impedance

Table 28 shows the GPIO output buffer impedance (OVDD 1.8 V).

Table 28. DVGPIO Output Buffer Average Impedance (OVDD 1.8 V)

Parameter	Symbol	Drive Strength (ipp_dse)	Typ Value	Unit
Output Driver Impedance	Rdrv	001 010 011 100 101 110 111	262 134 88 62 51 43 37	Ω

Table 35. EIM Asynchronous Timing Parameters Table Relative Chip Select (continued)

Reference Number	Parameter	Determination by Synchronous measured parameters[1]	Min	Max	Unit
MAXCO	Output maximum delay from internal driving EIM_ADDRxx/control flip-flops to chip outputs.	10	—	10	ns
MAXCSO	Output maximum delay from internal chip selects driving flip-flops to EIM_CSx_B out.	10	—	10	ns
MAXDI	EIM_DATAxx MAXIMUM delay from chip input data to its internal flip-flop	5	—	5	ns
WE43	Input Data Valid to EIM_CSx_B Invalid	MAXCO-MAXCSO+MAXDI	MAXCO-MAXCSO+MAXDI	—	ns
WE44	EIM_CSx_B Invalid to Input Data Invalid	0	0	—	ns
WE45	EIM_CSx_B Valid to EIM_EBx_B Valid (Write access)	WE12-WE6+(WBEA-WCSA)×t	-3.5+(WBEA-WCSA)×t	3.5+(WBEA-WCSA)×t	ns
WE46	EIM_EBx_B Invalid to EIM_CSx_B Invalid (Write access)	WE7-WE13+(WBEN-WCSN)×t	-3.5+(WBEN-WCSN)×t	3.5+(WBEN-WCSN)×t	ns
MAXDTI	Maximum delay from EIM_DTACK_B input to its internal flip-flop + 2 cycles for synchronization	10	—	10	ns
WE47	EIM_DTACK_B Active to EIM_CSx_B Invalid	MAXCO-MAXCSO+MAXDTI	MAXCO-MAXCSO+MAXDTI	—	ns
WE48	EIM_CSx_B Invalid to EIM_DTACK_B invalid	0	0	—	ns

1 For more information on configuration parameters mentioned in this table, see the i.MX 6SoloLite reference manual.

2 CSA means register setting for WCSA when in write operations or RCSA when in read operations.

3 CSN means register setting for WCSN when in write operations or RCSN when in read operations.

4 t means clock period from axi_clk frequency.

5 ADVA means register setting for WADVA when in write operations or RADVA when in read operations.

6 ADVN means register setting for WADVN when in write operations or RADVN when in read operations.

7 BE Assertion. This bit field determines when BE signal is asserted during read cycles.

Table 37. CSI Gated Clock Mode Timing Parameters (continued)

ID	Parameter	Symbol	Min	Max	Units
P4	CSI DATA hold time	tDh	1.2	—	ns
P5	CSI pixel clock high time	tCLKh	7.5	—	ns
P6	CSI pixel clock low time	tCLKl	7.5	—	ns
P7	CSI pixel clock frequency	fCLK	—	66	MHz

4.10.2.0.2 Ungated Clock Mode Timing

Figure 24 shows the ungated clock mode timings of CSI, and Table 38 describes the timing parameters (P1–P6) that are shown in the figure. In ungated mode the CSI_VSYNC and CSI_PIXCLK signals are used, and the CSI_HSYNC signal is ignored.

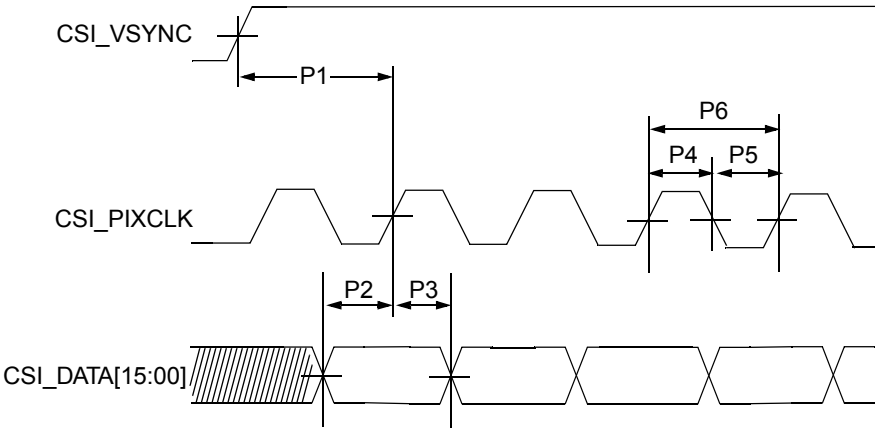


Figure 24. CSI Ungated Clock Mode—Sensor Data at Falling Edge, Latch Data at Rising Edge

Table 38. CSI Ungated Clock Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Units
P1	CSI_VSYNC to pixel clock time	tVSYNC	67.5	—	ns
P2	CSI DATA setup time	tDsu	2.5	—	ns
P3	CSI DATA hold time	tDh	1.2	—	ns
P4	CSI pixel clock high time	tCLKh	7.5	—	ns
P5	CSI pixel clock low time	tCLKl	7.5	—	ns
P6	CSI pixel clock frequency	fCLK	—	66	MHz

The CSI enables the chip to connect directly to external CMOS image sensors, which are classified as dumb or smart as follows:

- Dumb sensors only support traditional sensor timing (vertical sync (VSYNC) and horizontal sync (HSYNC)) and output-only Bayer and statistics data.
- Smart sensors support CCIR656 video decoder formats and perform additional processing of the image (for example, image compression, image pre-filtering, and various data output formats).

The following subsections describe the CSI timing in gated and ungated clock modes.

4.10.3 ECSPI Timing Parameters

This section describes the timing parameters of the ECSPI block. The ECSPI has separate timing parameters for master and slave modes.

4.10.3.1 ECSPI Master Mode Timing

Figure 25 depicts the timing of ECSPI in master mode and Table 39 lists the ECSPI master mode timing characteristics.

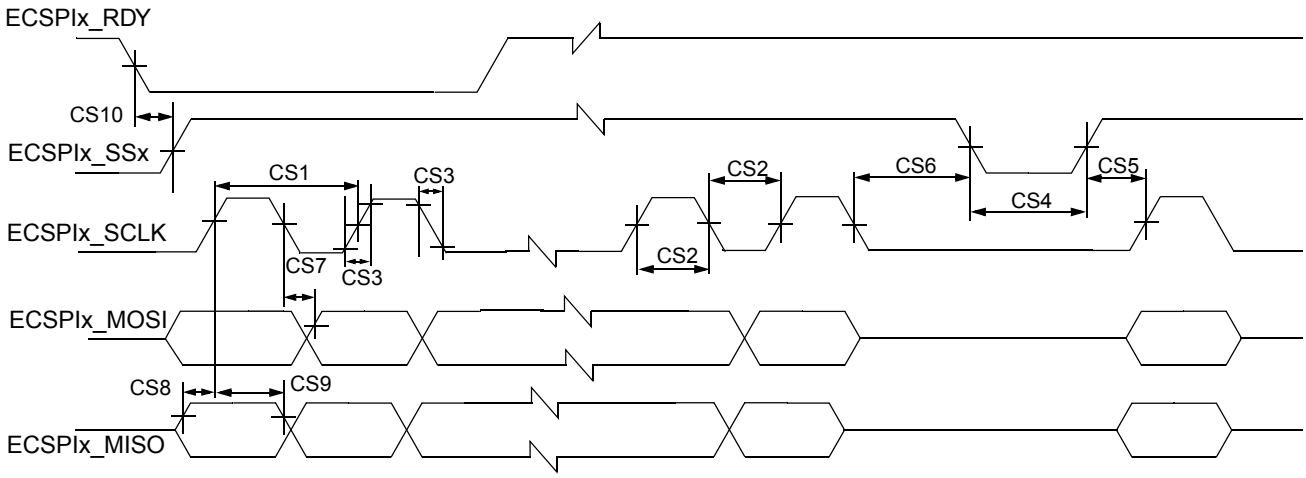


Figure 25. ECSPI Master Mode Timing Diagram

NOTE

ECSPIx_MOSI is always driven (not tri-stated) between actual data transmissions. This limits the ECSPI to be connected between a single master and a single slave.

Table 39. ECSPI Master Mode Timing Parameters

ID	Parameter	Symbol	Min	Max	Unit
CS1	ECSPIx_SCLK Cycle Time–Read • Slow group[1] • Fast group[2] ECSPIx_SCLK Cycle Time–Write	t_{clk}	 46 40 15	—	ns
CS2	ECSPIx_SCLK High or Low Time–Read • Slow group[1] • Fast group[2] ECSPIx_SCLK High or Low Time–Write	t_{SW}	 22 20 7	—	ns
CS3	ECSPIx_SCLK Rise or Fall[3]	$t_{RISE/FALL}$	—	—	ns
CS4	ECSPIx_SSx pulse width	t_{CSLH}	Half ECSPIx period	—	ns
CS5	ECSPIx_SSx Lead Time (CS setup time)	t_{SCS}	Half ECSPIx_SCLK period - 4	—	ns

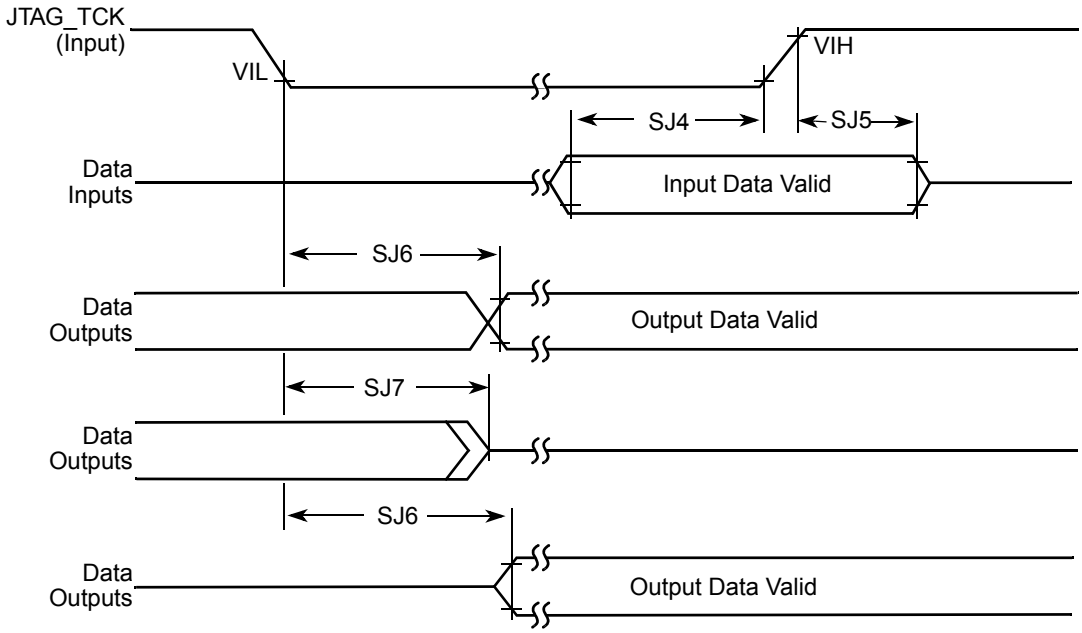


Figure 35. Boundary Scan (JTAG) Timing Diagram

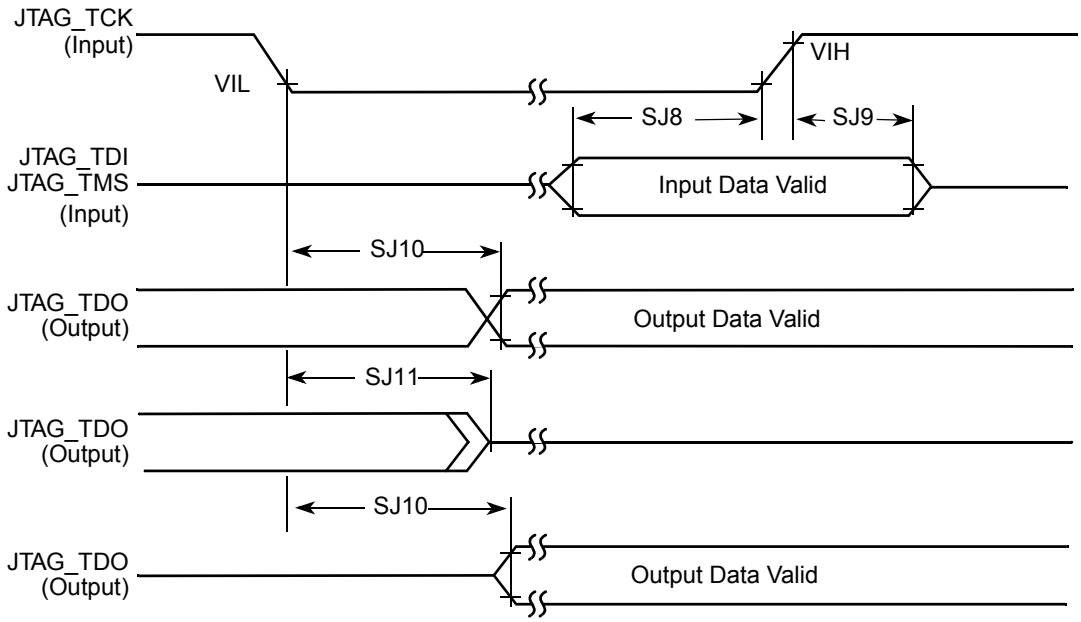


Figure 36. Test Access Port Timing Diagram

4.10.11.2 SSI Receiver Timing with Internal Clock

Figure 41 depicts the SSI receiver internal clock timing and Table 52 lists the timing parameters for the receiver timing with the internal clock.

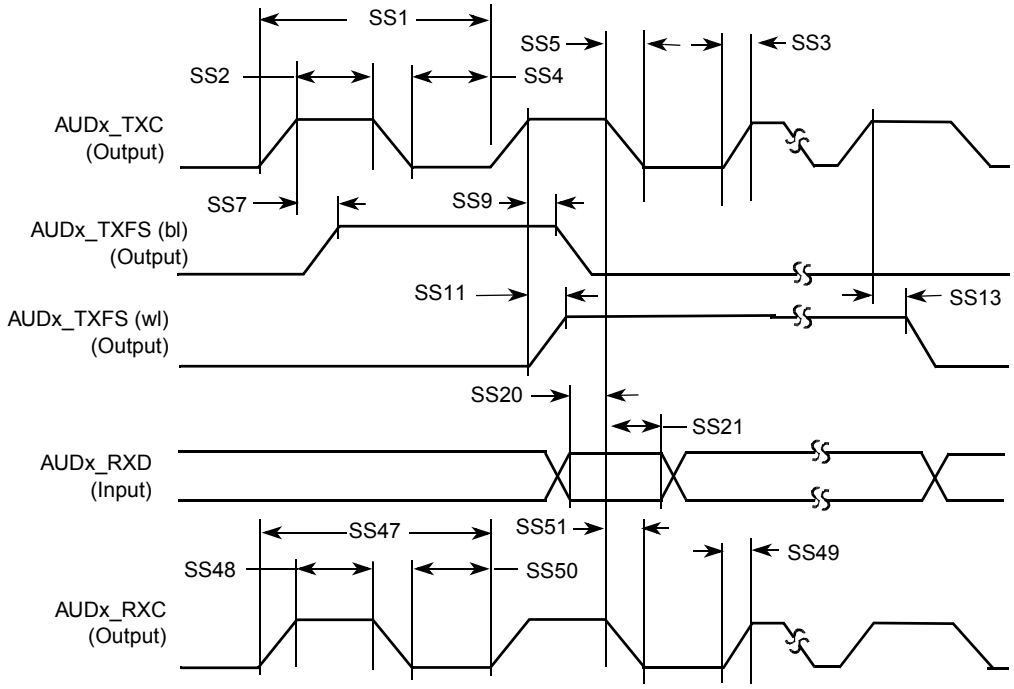


Figure 41. SSI Receiver Internal Clock Timing Diagram

Table 52. SSI Receiver with Internal Clock Timing Parameters

ID	Parameter	Min	Max	Unit
Internal Clock Operation				
SS1	AUDx_TXC/AUDx_RXC clock period	81.4	—	ns
SS2	AUDx_TXC/AUDx_RXC clock high period	36.0	—	ns
SS3	AUDx_TXC/AUDx_RXC clock rise time	—	6.0	ns
SS4	AUDx_TXC/AUDx_RXC clock low period	36.0	—	ns
SS5	AUDx_TXC/AUDx_RXC clock fall time	—	6.0	ns
SS7	AUDx_RXC high to AUDx_TXFS (bl) high	—	15.0	ns
SS9	AUDx_RXC high to AUDx_TXFS (bl) low	—	15.0	ns
SS11	AUDx_RXC high to AUDx_TXFS (wl) high	—	15.0	ns
SS13	AUDx_RXC high to AUDx_TXFS (wl) low	—	15.0	ns
SS20	AUDx_RXD setup time before AUDx_RXC low	10.0	—	ns
SS21	AUDx_RXD hold time after AUDx_RXC low	0.0	—	ns

Table 53. SSI Transmitter with External Clock Timing Parameters (continued)

ID	Parameter	Min	Max	Unit
Synchronous External Clock Operation				
SS44	AUDx_RXD setup before AUDx_TXC falling	10.0	—	ns
SS45	AUDx_RXD hold after AUDx_TXC falling	2.0	—	ns
SS46	AUDx_RXD rise/fall time	—	6.0	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TXC/RXC = 0) and a non-inverted frame sync (TXFS/RXFS = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal TXC/RXC and/or the frame sync TXFS/RXFS shown in the tables and in the figures.
- All timings are on AUDMUX Pads when SSI is used for data transfer.
- The terms WL and BL refer to Word Length (WL) and Bit Length (BL).
- For internal Frame Sync operation using external clock, the FS timing is same as that of TXD (for example, during AC97 mode of operation).

4.10.11.4 SSI Receiver Timing with External Clock

Figure 43 depicts the SSI receiver external clock timing and Table 54 lists the timing parameters for the receiver timing with the external clock.

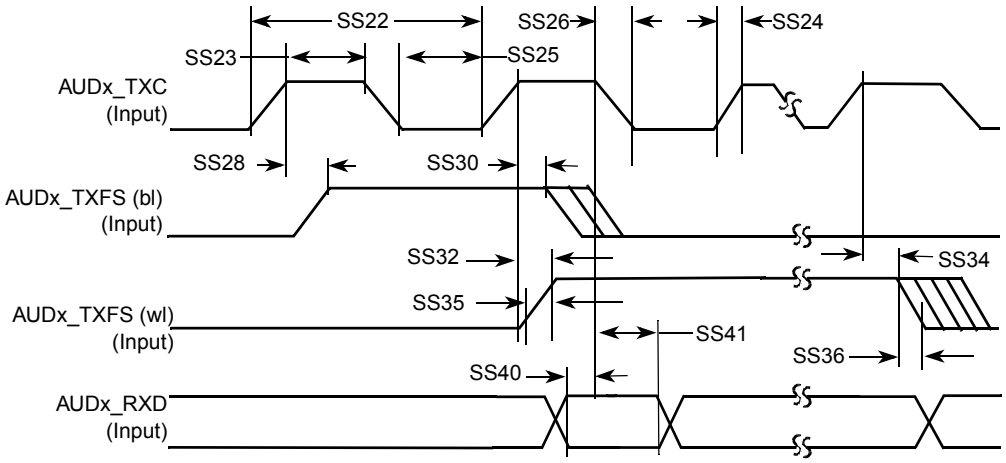


Figure 43. SSI Receiver External Clock Timing Diagram

Table 63. Interfaces Allocation During Boot (continued)

Interface	IP Instance	Allocated Ball Names During Boot	Comment
I2C	I2C-2	I2C2_SCL, I2C2_SDA	—
I2C	I2C-3	AUD_RXFS, AUD_RXC	—
USB	USB_OTG1_PHY	USB_OTG1_DP USB_OTG1_DN USB_OTG1_VBUS USB_OTG1_CHD_B USB_OTG1_DP USB_OTG1_DN USB_OTG1_VBUS	—

6 Package Information and Contact Assignments

This section includes the contact assignment information and mechanical package drawing.

6.1 Updated Signal Naming Convention

The signal names of the i.MX6 series of products have been standardized to better align the signal names within the family and across the documentation. Some of the benefits of these changes are as follows:

- The names are unique within the scope of an SoC and within the series of products
- Searches will return all occurrences of the named signal
- The names are consistent between i.MX 6 series products implementing the same modules
- The module instance is incorporated into the signal name

This change applies only to signal names. The original ball names have been preserved to prevent the need to change schematics, BSDL models, IBIS models, and so on.

Throughout this document, the updated signal names are used except where referenced as a ball name (such as the Functional Contact Assignments table, Ball Map table, and so on). A master list of the signal name changes is in the document, *IMX 6 Series Signal Name Mapping* (EB792). This list can be used to map the signal names used in older documentation to the new standardized naming conventions.

Table 66. 13 x 13 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group[1]	Ball Type	Out of Reset Condition[2]			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value[3]
I2C1_SCL	AC13	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[12]	Input	Keeper
I2C1_SDA	AD13	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[13]	Input	Keeper
I2C2_SCL	E18	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[14]	Input	Keeper
I2C2_SDA	D18	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[15]	Input	Keeper
JTAG_MOD	Y14	NVCC33_IO	GPIO	ALT5	JTAG_MODE	—	PU (100K)
JTAG_TCK	AA14	NVCC33_IO	GPIO	ALT5	JTAG_TCK	—	PU (47K)
JTAG_TDI	W14	NVCC33_IO	GPIO	ALT5	JTAG_TDI	—	PU (47K)
JTAG_TDO	W15	NVCC33_IO	GPIO	ALT5	JTAG_TDO	—	Keeper
JTAG_TMS	Y15	NVCC33_IO	GPIO	ALT5	JTAG_TMS	—	PU (47K)
JTAG_TRSTB	AA15	NVCC33_IO	GPIO	ALT5	JTAG_TRSTB	—	PU (47K)
KEY_COL0	G23	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[24]	Input	Keeper
KEY_COL1	F23	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[26]	Input	Keeper
KEY_COL2	E23	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[28]	Input	Keeper
KEY_COL3	E22	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[30]	Input	Keeper
KEY_COL4	E20	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO4_GPIO[0]	Input	Keeper
KEY_COL5	D24	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO4_GPIO[2]	Input	Keeper
KEY_COL6	D22	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO4_GPIO[4]	Input	Keeper
KEY_COL7	C23	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO4_GPIO[6]	Input	Keeper
KEY_ROW0	G24	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[25]	Input	Keeper
KEY_ROW1	F24	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[27]	Input	Keeper
KEY_ROW2	E24	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[29]	Input	Keeper
KEY_ROW3	E21	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO3_GPIO[31]	Input	Keeper
KEY_ROW4	E19	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO4_GPIO[1]	Input	Keeper
KEY_ROW5	D23	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO4_GPIO[3]	Input	Keeper

Table 66. 13 x 13 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group[1]	Ball Type	Out of Reset Condition[2]			
				Default Mode (Reset Mode)	Default Function	Input/Output	Value[3]
SD1_DAT3	B22	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO5_GPIO[6]	Input	Keeper
SD1_DAT4	A22	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO5_GPIO[12]	Input	Keeper
SD1_DAT5	A21	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO5_GPIO[9]	Input	Keeper
SD1_DAT6	A20	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO5_GPIO[7]	Input	Keeper
SD1_DAT7	A19	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO5_GPIO[10]	Input	Keeper
SD2_CLK	AC24	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO5_GPIO[5]	Input	Keeper
SD2_CMD	AB24	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO5_GPIO[4]	Input	Keeper
SD2_DAT0	AB22	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO5_GPIO[1]	Input	Keeper
SD2_DAT1	AB23	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO4_GPIO[30]	Input	Keeper
SD2_DAT2	AA22	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO5_GPIO[3]	Input	Keeper
SD2_DAT3	AA23	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO4_GPIO[28]	Input	Keeper
SD2_DAT4	AA24	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO5_GPIO[2]	Input	Keeper
SD2_DAT5	Y20	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO4_GPIO[31]	Input	Keeper
SD2_DAT6	Y21	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO4_GPIO[29]	Input	Keeper
SD2_DAT7	Y22	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO5_GPIO[0]	Input	Keeper
SD2_RST	Y23	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO4_GPIO[27]	Input	Keeper
SD3_CLK	AB11	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO5_GPIO[18]	Input	Keeper
SD3_CMD	AA11	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO5_GPIO[21]	Input	Keeper
SD3_DAT0	AC11	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO5_GPIO[19]	Input	Keeper
SD3_DAT1	AD11	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO5_GPIO[20]	Input	Keeper
SD3_DAT2	AC12	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO5_GPIO[16]	Input	Keeper
SD3_DAT3	AD12	NVCC33_IO NVCC18_IO	GPIO	ALT5	GPIO5_GPIO[17]	Input	Keeper

Table 68. 13 x 13 mm, 0.5 mm Pitch Ball Map (continued)

	1	2	3	4	5	6	7	8
A	GND	DRAM_SDQS3_B	DRAM_D24	GND	DRAM_D27	DRAM_D29	GND	DRAM_D31
B	DRAM_D14	DRAM_D15	DRAM_SDQS3	DRAM_D25	DRAM_D26	DRAM_D28	DRAM_D30	EPDC_SDLE
C	DRAM_D12	DRAM_D13	DRAM_DQM3	**NC**	**NC**	GND	EPDC_VCOM0	**NC**
D	GND	GND	DRAM_D11	**NC**	**NC**	DRAM_RESET	EPDC_VCOM1	**NC**
E	DRAM_D9	DRAM_D8	DRAM_D10	DRAM_SDODT1	GND	NVCC_DRAM	EPDC_SDOE	**NC**
F	DRAM_SDQS1	DRAM_SDQS1_B	**NC**	**NC**	**NC**	**NC**	EPDC_SDSHR	**NC**
G	GND	DRAM_DQM1	**NC**	**NC**	**NC**	**NC**	NVCC_DRAM	GND
H	DRAM_SDBA2	ZQPAD	GND	DRAM_A7	DRAM_A13	NVCC_DRAM	GND	**NC**
J	DRAM_SDBA0	DRAM_A10	DRAM_A8	DRAM_A9	GND	NVCC_DRAM	VDD_SOC_CAP	VDD_SOC_CAP
K	GND	DRAM_A15	**NC**	**NC**	**NC**	**NC**	VDD_SOC_CAP	VDD_SOC_CAP
L	DRAM_SDCLK_0	DRAM_CS1	**NC**	**NC**	**NC**	**NC**	GND	**NC**
M	DRAM_SDCLK_0_B	DRAM_SDCKE1	DRAM_A5	DRAM_A6	GND	NVCC_DRAM_2P5	GND	GND
N	DRAM_RAS	DRAM_CS0	GND	DRAM_A4	DRAM_VREF	NVCC_DRAM	GND	GND
P	DRAM_CAS	SDCKE0	**NC**	**NC**	**NC**	**NC**	NVCC_DRAM	**NC**
R	GND	DRAM_A14	**NC**	**NC**	**NC**	**NC**	VDD_PU_CAP	VDD_PU_CAP
T	DRAM_SDBA1	DRAM_A11	DRAM_A2	DRAM_A3	GND	NVCC_DRAM	VDD_PU_CAP	VDD_PU_CAP
U	DRAM_SDWE	DRAM_A12	GND	DRAM_A0	DRAM_A1	NVCC_DRAM	GND	**NC**
V	GND	DRAM_DQM0	**NC**	**NC**	**NC**	**NC**	NVCC_DRAM	GND
W	DRAM_SDQS0_B	DRAM_SDQS0	**NC**	**NC**	**NC**	**NC**	NVCC_1P2	**NC**
Y	DRAM_D6	DRAM_D7	DRAM_D5	DRAM_SDODT0	GND	NVCC_DRAM	PWM1	**NC**
AA	GND	GND	DRAM_D4	**NC**	**NC**	HSIC_DAT	FEC_MDC	**NC**
AB	DRAM_D3	DRAM_D2	DRAM_DQM2	**NC**	**NC**	HSIC_STROBE	FEC_MDIO	**NC**
AC	DRAM_D1	DRAM_D0	DRAm_SDQS2	DRAM_D22	DRAM_D21	DRAM_D19	DRAM_D17	FEC_TX_CLK
AD	GND	DRAM_SDQS2_B	DRAM_D23	GND	DRAM_D20	DRAM_D18	GND	DRAM_D16

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