Welcome to E-XFL.COM

Embedded - Microcontrollers - Application Specific: Tailored Solutions for Precision and Performance

Embedded - Microcontrollers - Application Specific represents a category of microcontrollers designed with unique features and capabilities tailored to specific application needs. Unlike general-purpose microcontrollers, application-specific microcontrollers are optimized for particular tasks, offering enhanced performance, efficiency, and functionality to meet the demands of specialized applications.

What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	SD3™ USB and Mass Storage Peripheral Controller
Core Processor	ARM9®
Program Memory Type	-
Controller Series	CYUSB
RAM Size	512K x 8
Interface	I²C, I²S, MMC/SD, SPI, UART, USB
Number of I/O	59
Voltage - Supply	1.15V ~ 1.25V
Operating Temperature	0°C ~ 70°C
Mounting Type	Surface Mount
Package / Case	131-UFBGA, WLCSP
Supplier Device Package	131-WLCSP (5.1x4.7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cyusb3023-fbxct

Contents

Power

SD3 has the following main groups of power supply domains:

- **IO_VDDQ:** This refers to a group of independent supply domains for digital I/Os. The voltage level on these supplies are 1.8 V to 3.3 V. SD3 provides six independent supply domains for digital I/Os listed as follows:
  - S0VDDQ: S0-Port (for SD/MMC) I/O Power Supply Domain
  - S1VDDQ: S1-Port (for SD/MMC) I/O Power Supply Domain
  - S2VDDQ: S2-Port (GPIO) Power Supply Domain
  - VIO4: S1-Port GPIO[53:57]/O Power Supply Domain (these pins support MMC's high nibble data line - D[7:4] on S1-Port)
  - VIO5: I2C Power Supply Domain (supports 1.2 V to 3.3 V)
  - CVDDQ: Clock Power Supply Domain
- **VDD:** This is the supply voltage for the logic core. The nominal supply voltage level is 1.2 V. This supplies the core logic circuits. The same supply must also be used for the following:
  - **AVDD**: This is the 1.2-V supply for the PLL, crystal oscillator and other core analog circuits
  - **U3TXVDDQ/U3RXVDDQ**: These are the 1.2-V supply voltages for the USB 3.0 interface.
- **VBATT/VBUS:** This is the 3.2-V to 6-V battery power supply for the USB I/O and analog circuits. This supply powers the USB transceiver through SD3's internal voltage regulator. VBATT is internally regulated to 3.3 V.

Power Modes

SD3 supports the following power modes:

- Normal mode: This is the full-functional operating mode. In this mode the internal CPU clock and the internal PLLs are enabled.

Normal operating power consumption does not exceed the sum of ICC_CORE max and ICC_USB max (see Table 9 on page 15 for current consumption specifications).

The I/O power supplies (S0VDDQ, S1VDDQ, VIO4, and VIO5) may be turned off when the corresponding interface is not in use. S2VDDQ cannot be turned off at any time if the S2-Port is used in the application.

- SD3 supports four low-power modes (see Table 6 on page 5):
  - Suspend mode with USB 3.0 PHY enabled (L1 mode)
  - Suspend mode with USB 3.0 PHY disabled (L2 mode)
  - Standby mode (L3 mode)
  - Core power-down mode (L4 mode)

Table 6. Entry and Exit Methods for Low-Power Modes

Low Power Mode	Characteristics	Methods of Entry	Methods of Exit
Suspend mode with USB 3.0 PHY Enabled (L1 mode)	■ The power consumption in this mode does not exceed ISB_1 ■ USB 3.0 PHY is enabled and is in U3 mode (one of the suspend modes defined by the USB 3.0 specification). This one block alone operates with its internal clock while all other clocks are shut down ■ All I/Os maintain their previous state ■ Power supply for the wakeup source and core power must be retained. All other power domains can be turned on/off individually ■ The states of the configuration registers, buffer memory and all internal RAM are maintained ■ All transactions must be completed before SD3 enters Suspend mode (state of outstanding transactions are not preserved) ■ The firmware resumes operation from where it was suspended (except when woken up by RESET# assertion) because the program counter does not reset	■ Firmware executing on the core can put SD3 into suspend mode. For example, on USB suspend condition, firmware may decide to put SD3 into suspend mode	■ D+ transitioning to low or high ■ D– transitioning to low or high ■ Resume condition on SSRX +/- ■ Detection of VBUS ■ Assertion of GPIO[17] ■ Assertion of RESET#

Configuration Fuse

Fuse options are available for specific usage models. Contact Cypress Applications/Marketing for details.

Digital I/Os

SD3 provides firmware controlled pull-up or pull-down resistors internally on all digital I/O pins. The pins can be pulled high through an internal 50-kΩ resistor or can be pulled low through an internal 10-kΩ resistor to prevent the pins from floating. The I/O pins may have the following states:

- Tristated (High-Z)
- Weak pull-up (through internal 50 kΩ)
- Pull down (through internal 10 kΩ)
- Hold (I/O hold its value) when in low power modes

All unused I/Os should be pulled high by using the internal pull-up resistors. All unused outputs should be left floating. All I/Os can be driven at full-strength, three-quarter strength, half-strength, or quarter-strength. These drive strengths are configured based on each interface.

EMI

SD3 meets EMI requirements outlined by FCC 15B (USA) and EN55022 (Europe) for consumer electronics. SD3 can tolerate reasonable EMI, conducted by aggressor, outlined by these specifications and continue to function as expected.

System Level ESD

SD3 has built-in ESD protection on the D+, D–, GND pins on the USB interface. The ESD protection levels provided on these ports are:

- ±2.2-KV human body model (HBM) based on JESD22-A114 Specification
- ±6-KV contact discharge and ±8-KV air gap discharge based on IEC61000-4-2 level 3A
- ±8-KV contact discharge and ±15-KV air gap discharge based on IEC61000-4-2 level 4C.

This protection ensures the device continues to function after ESD events up to the levels stated.

The SuperSpeed USB signals (SSRX+, SSRX-, SSTX+, SSTX-) and S0/S1_INS have up to ±2.2 KV HBM internal ESD protection.

Pinout for BGA

Figure 2. SD3 BGA Ball Map (Top View)

	1	2	3	4	5	6	7	8	9	10	11
A	U3VSSQ	U3RXVDDQ	SSRXM	SSRXP	SSTXP	SSTXM	AVDD	VSS	DP	DM	NC
B	VIO4	FSLC[0]	R_USB3	FSLC[1]	U3TXVDDQ	CVDDQ	AVSS	VSS	VSS	VDD	NC
C	GPIO[54]	GPIO[55]	VDD	GPIO[57]	RESET#	XTALIN	XTALOUT	R_USB2	OTG_ID	NC	VIO5
D	GPIO[50]	GPIO[51]	GPIO[52]	GPIO[53]	GPIO[56]	CLKIN_32	CLKIN	VSS	I2C_GPIO[58]	I2C_GPIO[59]	O[60]
E	GPIO[47]	VSS	S1VDDQ	GPIO[49]	GPIO[48]	FSLC[2]	NC	NC	VDD	VBATT	VBUS
F	S0VDDQ	GPIO[45]	GPIO[44]	GPIO[41]	GPIO[46]	NC	GPIO[2]	GPIO[5]	GPIO[1]	GPIO[0]	VDD
G	VSS	GPIO[42]	GPIO[43]	GPIO[30]	GPIO[25]	GPIO[22]	GPIO[21]	GPIO[15]	GPIO[4]	GPIO[3]	VSS
H	VDD	GPIO[39]	GPIO[40]	GPIO[31]	GPIO[29]	GPIO[26]	GPIO[20]	GPIO[24]	GPIO[7]	GPIO[6]	S2VDDQ
J	GPIO[38]	GPIO[36]	GPIO[37]	GPIO[34]	GPIO[28]	GPIO[16]	GPIO[19]	GPIO[14]	GPIO[9]	GPIO[8]	VDD
K	GPIO[35]	GPIO[33]	VSS	VSS	GPIO[27]	GPIO[23]	GPIO[18]	GPIO[17]	GPIO[13]	GPIO[12]	GPIO[10]
L	VSS	VSS	VSS	GPIO[32]	VDD	VSS	VDD	NC	S2VDDQ	GPIO[11]	VSS

Table 7. Pin List (continued)

Pin No.	Power Domain	I/O	Name	Description							
G3	VI02	I/O	GPIO[43]	S0_WP			S0_WP			GPIO	
F3	VI02	I/O	GPIO[44]	S0S1_INS			S0S1_INS			GPIO	
F2	VI02	I/O	GPIO[45]	MMC0_RST_OUT			GPIO			GPIO	
				8b MMC	**SD+UART**	**SD+SPI**	**SD+GPIO**	**GPIO**	**GPIO+ UART+I2S**	**SD+I2S**	**UART+ SPI+I2S**
F5	VI03	I/O	GPIO[46]	S1_SD0	S1_SD0	S1_SD0	S1_SD0	GPIO	GPIO	S1_SD0	UART_RTS
E1	VI03	I/O	GPIO[47]	S1_SD1	S1_SD1	S1_SD1	S1_SD1	GPIO	GPIO	S1_SD1	UART_CTS
E5	VI03	I/O	GPIO[48]	S1_SD2	S1_SD2	S1_SD2	S1_SD2	GPIO	GPIO	S1_SD2	UART_TX
E4	VI03	I/O	GPIO[49]	S1_SD3	S1_SD3	S1_SD3	S1_SD3	GPIO	GPIO	S1_SD3	UART_RX
D1	VI03	I/O	GPIO[50]	S1_CMD	S1_CMD	S1_CMD	S1_CMD	GPIO	I2S_CLK	S1_CMD	I2S_CLK
D2	VI03	I/O	GPIO[51]	S1_CLK	S1_CLK	S1_CLK	S1_CLK	GPIO	I2S_SD	S1_CLK	I2S_SD
D3	VI03	I/O	GPIO[52]	S1_WP	S1_WP	S1_WP	S1_WP	GPIO	I2S_WS	S1_WP	I2S_WS
D4	VIO4	I/O	GPIO[53]	S1_SD4	UART_RTS	SPI_SCK	GPIO	GPIO	UART_RTS	GPIO	SPI_SCK
C1	VIO4	I/O	GPIO[54]	S1_SD5	UART_CTS	SPI_SSN	GPIO	GPIO	UART_CTS	I2S_CLK	SPI_SSN
C2	VIO4	I/O	GPIO[55]	S1_SD6	UART_TX	SPI_MISO	GPIO	GPIO	UART_TX	I2S_SD	SPI_MISO
D5	VIO4	I/O	GPIO[56]	S1_SD7	UART_RX	SPI_MOSI	GPIO	GPIO	UART_RX	I2S_WS	SPI_MOSI
C4	VIO4	I/O	GPIO[57]	MMC1_RST_OUT	GPIO	GPIO	GPIO	GPIO	I2S_MCLK	I2S_MCLK	I2S_MCLK
C9			NC	No Connect							
A3	U3RXVDDQ	I	SSRXM	USB 3.0 SuperSpeed Receive Minus							
A4	U3RXVDDQ	I	SSRXP	USB 3.0 SuperSpeed Receive Plus							
A6	U3TXVDDQ	O	SSTXM	USB 3.0 SuperSpeed Transmit Minus							
A5	U3TXVDDQ	O	SSTXP	USB 3.0 SuperSpeed Transmit Plus							
A9	VBATT/ VBUS	I/O	D+	USB (HS/FS) Data Plus							
A10	VBATT/ VBUS	I/O	D-	USB (HS/FS) Data Minus							
A11			NC	No Connect							
B2	CVDDQ	I	FSLC[0]	FSLC[0]							
C6	AVDD	I/O	XTALIN	XTALIN							
C7	AVDD	I/O	XTALOUT	XTALOUT							
B4	CVDDQ	I	FSLC[1]	FSLC[1]							
E6	CVDDQ	I	FSLC[2]	FSLC[2]							
D7	CVDDQ	I	CLKIN	CLKIN							
D6	CVDDQ	I	CLKIN_32	CLKIN_32							
D9	VIO5	I/O	I^2C_GPIO[58]	SCL (Serial Clock) for I^2C Bus Interface							
D10	VIO5	I/O	I^2C_GPIO[59]	SDA (Serial Data) for I^2C Bus Interface							
E7			NC	No Connect							
C10			NC	No Connect							
B11			NC	No Connect							
E8			NC	No Connect							
F6			NC	No Connect							
D11	VIO5	O	O[60]	Output only							
E10		PWR	VBATT								
B10		PWR	VDD								
A1		PWR	U3VSSQ								

Table 7. Pin List (continued)

Pin No.	Power Domain	I/O	Name	Description
E11		PWR	VBUS	
D8		PWR	VSS	
H11		PWR	S2VDDQ	
E2		PWR	VSS	
L9		PWR	S2VDDQ	
G1		PWR	VSS	
F1		PWR	S0VDDQ	
G11		PWR	VSS	
E3		PWR	S1VDDQ	
L1		PWR	VSS	
B1		PWR	VIO4	
L6		PWR	VSS	
B6		PWR	CVDDQ	
B5		PWR	U3TXVDDQ	
A2		PWR	U3RXVDDQ	
C11		PWR	VIO5	
L11		PWR	VSS	
A7		PWR	AVDD	
B7		PWR	AVSS	
C3		PWR	VDD	
B8		PWR	VSS	
E9		PWR	VDD	
B9		PWR	VSS	
F11		PWR	VDD	
H1		PWR	VDD	
L7		PWR	VDD	
J11		PWR	VDD	
L5		PWR	VDD	
K4		PWR	VSS	
L3		PWR	VSS	
K3		PWR	VSS	
L2		PWR	VSS	
A8		PWR	VSS	
				Precision Resistors
C8	VBUS/VBATT	I/O	R_usb2	Precision resistor for USB 2.0 (Connect a 6.04 kΩ+/-1% resistor between this pin and GND)
B3	U3TXVDDQ	I/O	R_usb3	Precision resistor for USB 3.0 (Connect a 200 Ω+/-1% resistor between this pin and GND)

Pin Description for WLCSP

Table 8. Pin List

Pin	Power Domain	I/O	Name	Description		
				P-Port		
				GPIO		
F1	VI01	I/O	GPIO[0]	GPIO		
F2	VI01	I/O	GPIO[1]	GPIO		
G1	VI01	I/O	GPIO[2]	GPIO		
E3	VI01	I/O	GPIO[3]	GPIO		
F3	VI01	I/O	GPIO[4]	GPIO		
J1	VI01	I/O	GPIO[5]	GPIO		
G2	VI01	I/O	GPIO[6]	GPIO		
G3	VI01	I/O	GPIO[7]	GPIO		
H2	VI01	I/O	GPIO[8]	GPIO		
G4	VI01	I/O	GPIO[9]	GPIO		
J2	VI01	I/O	GPIO[10]	GPIO		
K2	VI01	I/O	GPIO[11]	GPIO		
H3	VI01	I/O	GPIO[12]	GPIO		
L2	VI01	I/O	GPIO[13]	GPIO		
H4	VI01	I/O	GPIO[14]	GPIO		
J3	VI01	I/O	GPIO[15]	GPIO		
K6	VI01	I/O	GPIO[16]	GPIO		
L3	VI01	I/O	GPIO[17]	GPIO		
H5	VI01	I/O	GPIO[18]	GPIO		
J4	VI01	I/O	GPIO[19]	GPIO		
H6	VI01	I/O	GPIO[20]	GPIO		
K5	VI01	I/O	GPIO[21]	GPIO		
J5	VI01	I/O	GPIO[22]	GPIO		
L6	VI01	I/O	GPIO[23]	GPIO		
K3	VI01	I/O	GPIO[24]	GPIO		
J6	VI01	I/O	GPIO[25]	GPIO		
K7	VI01	I/O	GPIO[26]	GPIO		
J7	VI01	I/O	GPIO[27]	GPIO		
K8	VI01	I/O	GPIO[28]	GPIO		
L8	VI01	I/O	GPIO[29]	GPIO		
L9	VI01	I/O	GPIO[30]	PMODE[0]		
J8	VI01	I/O	GPIO[31]	PMODE[1]		
K9	VI01	I/O	GPIO[32]	PMODE[2]		
K4	VI01	O	INT#	INT#		
D8	CVDDQ	I	RESET#	RESET#		
				S0-Port		
				8b MMC	**SD+GPIO**	**GPIO**
K10	VI02	I/O	GPIO[33]	S0_SD0	S0_SD0	GPIO
K11	VI02	I/O	GPIO[34]	S0_SD1	S0_SD1	GPIO
K12	VI02	I/O	GPIO[35]	S0_SD2	S0_SD2	GPIO
J9	VI02	I/O	GPIO[36]	S0_SD3	S0_SD3	GPIO
J10	VI02	I/O	GPIO[37]	S0_SD4	GPIO	GPIO
J11	VI02	I/O	GPIO[38]	S0_SD5	GPIO	GPIO
H8	VI02	I/O	GPIO[39]	S0_SD6	GPIO	GPIO
H11	VI02	I/O	GPIO[40]	S0_SD7	GPIO	GPIO
H10	VI02	I/O	GPIO[41]	S0_CMD	S0_CMD	GPIO

Table 8. Pin List (continued)

Pin	Power Domain	I/O	Name	Description							
H9	VI02	I/O	GPIO[42]	S0_CLK		S0_CLK		GPIO			
G11	VI02	I/O	GPIO[43]	S0_WP		S0_WP		GPIO			
G10	VI02	I/O	GPIO[44]	S0S1_INS		S0S1_INS		GPIO			
G9	VI02	I/O	GPIO[45]	MMC0_RST_OUT		GPIO		GPIO			
				S1-Port							
				8b MMC	**SD+UART**	**SD+SPI**	**SD+GPIO**	**GPIO**	**GPIO+UART+I2S**	**SD+I2S**	**UART+SPI+I2S**
F11	VI03	I/O	GPIO[46]	S1_SD0	S1_SD0	S1_SD0	S1_SD0	GPIO	GPIO	S1_SD0	UART_RTS
F10	VI03	I/O	GPIO[47]	S1_SD1	S1_SD1	S1_SD1	S1_SD1	GPIO	GPIO	S1_SD1	UART_CTS
E11	VI03	I/O	GPIO[48]	S1_SD2	S1_SD2	S1_SD2	S1_SD2	GPIO	GPIO	S1_SD2	UART_TX
D12	VI03	I/O	GPIO[49]	S1_SD3	S1_SD3	S1_SD3	S1_SD3	GPIO	GPIO	S1_SD3	UART_RX
D11	VI03	I/O	GPIO[50]	S1_CMD	S1_CMD	S1_CMD	S1_CMD	GPIO	I2S_CLK	S1_CMD	I2S_CLK
E10	VI03	I/O	GPIO[51]	S1_CLK	S1_CLK	S1_CLK	S1_CLK	GPIO	I2S_SD	S1_CLK	I2S_SD
E9	VI03	I/O	GPIO[52]	S1_WP	S1_WP	S1_WP	S1_WP	GPIO	I2S_WS	S1_WP	I2S_WS
D10	VI04	I/O	GPIO[53]	S1_SD4	UART_RTS	SPI_SCK	GPIO	GPIO	UART_RTS	GPIO	SPI_SCK
D9	VI04	I/O	GPIO[54]	S1_SD5	UART_CTS	SPI_SSN	GPIO	GPIO	UART_CTS	I2S_CLK	SPI_SSN
B12	VI04	I/O	GPIO[55]	S1_SD6	UART_TX	SPI_MISO	GPIO	GPIO	UART_TX	I2S_SD	SPI_MISO
C12	VI04	I/O	GPIO[56]	S1_SD7	UART_RX	SPI_MOSI	GPIO	GPIO	UART_RX	I2S_WS	SPI_MOSI
E12	VI04	I/O	GPIO[57]	MMC1_RST_OUT	GPIO	GPIO	GPIO	GPIO	I2S_MCLK	I2S_MCLK	I2S_MCLK
				U-Port							
C3	VBUS/VBATT	I	OTG_ID	USB OTG Identification							
A10	U3RXVDDQ	I	SSRXM	USB 3.0 SuperSpeed Receive Minus							
B10	U3RXVDDQ	I	SSRXP	USB 3.0 SuperSpeed Receive Plus							
A8	U3TXVDDQ	O	SSTXM	USB 3.0 SuperSpeed Transmit Minus							
B8	U3TXVDDQ	O	SSTXP	USB 3.0 SuperSpeed Transmit Plus							
A4	VBUS/VBATT	I/O	DP	USB (HS/FS) Data Plus							
A2	VBUS/VBATT	I/O	DM	USB (HS/FS) Data Minus							
B4	VBUS/VBATT	I/O	SWDP	USB (HS/FS) Switch Interface Data Plus							
B2	VBUS/VBATT	I/O	SWDM	USB (HS/FS) Switch Interface Data Minus							
				Crystal/Clocks							
A7	CVDDQ	I	FSLC[0]	Frequency Select 0							
B6	AVDD	I/O	XTALIN	Crystal Oscillator Input							
B5	AVDD	I/O	XTALOUT	Crystal Oscillator Output							
F9	CVDDQ	I	FSLC[1]	Frequency Select 1							
B7	CVDDQ	I	FSLC[2]	Frequency Select 2							
C5	CVDDQ	I	CLKIN	External Clock Input							
C6	CVDDQ	I	CLKIN_32	32.76-kHz Clock Input for Watchdog Timer							
				Other							
D6	I2C_VDDQ	I/O	I2C_GPIO[58]	SCL (Serial Clock) for I^2C Bus Interface							
D2	I2C_VDDQ	I/O	I2C_GPIO[59]	SDA (Serial Data) for I^2C Bus Interface							
F8	I2C_VDDQ	I	TDI	TDI (Test Data In) for JTAG Interface							
C2	I2C_VDDQ	O	TDO	TDO (Test Data Out) for JTAG Interface							
C1	I2C_VDDQ	O	TRST#	TRST (Test Reset) for JTAG Interface							
D5	I2C_VDDQ	O	TMS	TMS (Test Mode Select) for JTAG Interface							
D3	I2C_VDDQ	O	TCK	TCK (Test Clock) for JTAG Interface							
E8	I2C_VDDQ	O	O[60]	Charger Detect Output							
				Power							
E2		PWR	VBATT	USB Supply Voltage Input							

Table 8. Pin List (continued)

Pin	Power Domain	I/O	Name	Description
B1		PWR	VDD	
A1		PWR	VDD	
C9		PWR	U3VSSQ	GND
E1		PWR	VBUS	USB Supply Voltage Input
C4		PWR	U2PLLVSSQ	USB2 Regulator GND
H1		PWR	PVDDQ	P-Port Supply Voltage Input
K1		PWR	VSS	GND
L4		PWR	PVDDQ	P-Port Supply Voltage Input
L5		PWR	VSS	GND
L7		PWR	PVDDQ	P-Port Supply Voltage Input
L1		PWR	VSS	GND
J12		PWR	S0VDDQ	S0-Port Supply Voltage Input
H12		PWR	VSS	GND
G12		PWR	S0VDDQ	S0- Port Supply Voltage Input
C11		PWR	S1VDDQ	S1-Port Supply Voltage Input
F12		PWR	VSS	GND
B11		PWR	LVDDQ	Low Performance Peripherals Supply Voltage Input
A11		PWR	VSS	GND
A12		PWR	VSS	GND
C7		PWR	CVDDQ	Clock Supply Voltage Input
C8		PWR	U3TXVDDQ	USB3 1.2V Supply Voltage
C10		PWR	U3RXVDDQ	USB3 1.2V Supply Voltage
D4		PWR	I2C_VDDQ	I2C and JTAG Supply Voltage Input
A3		PWR	U2AFEVSSQ	GND
A5		PWR	AVDD	Analog Supply Voltage Input
A6		PWR	AVSS	Analog GND
F4		PWR	VDD	Core Supply Voltage Input
D1		PWR	VSS	GND
F5		PWR	VDD	Core Supply Voltage Input
E4		PWR	VSS	GND
F6		PWR	VDD	Core Supply Voltage Input
E5		PWR	VSS	GND
F7		PWR	VDD	Core Supply Voltage Input
E6		PWR	VSS	GND
D7		PWR	VDD	Core Supply Voltage Input
E7		PWR	VSS	GND
G6		PWR	VDD	Core Supply Voltage Input
L10		PWR	VDD	Core Supply Voltage Input
L12		PWR	VDD	Core Supply Voltage Input
H7		PWR	VSS	GND
G7		PWR	VSS	GND
L11		PWR	VSS	GND
G8		PWR	VSS	GND
G5		PWR	VSS	GND
B3	VBUS/VBATT	I/O	R_USB2	Precision Resistor for USB 2.0 (Connect a 6.04 kΩ ± 1% resistor between this pin and GND)
B9	U3TXVDDQ	I/O	R_USB3	Precision Resistor for USB 3.0 (Connect a 200Ω ± 1% resistor between this pin and GND)

AC Timing Parameters

Storage Port Timing

The S0-Port and S1-Port support the MMC Specification Version 4.4 and SD Specification Version 3.0.

Table 9 lists the timing parameters for S0-Port and S1-Port of SD3.

Table 9. S-Port Timing Parameters[3]

Parameter	Description	Min	Max	Units
MMC-20				
tSDIS CMD	Host input setup time for CMD	4.8	–	ns
tSDIS DAT	Host input setup time for DAT	4.8	–	ns
tSDIH CMD	Host input hold time for CMD	4.4	–	ns
tSDIH DAT	Host input hold time for DAT	4.4	–	ns
tSDOS CMD	Host output setup time for CMD	5	–	ns
tSDOS DAT	Host output setup time for DAT	5	–	ns
tSDOH CMD	Host output hold time for CMD	5	–	ns
tSDOH DAT	Host output hold time for DAT	5	–	ns
tSCLKR	Clock rise time	–	2	ns
tSCLKF	Clock fall time	–	2	ns
tSDCK	Clock cycle time	50	–	ns
SDFREQ	Clock frequency		20	MHz
tSDCLKOD	Clock duty cycle	40	60	%
MMC-26				
tSDIS CMD	Host input setup time for CMD	10	–	ns
tSDIS DAT	Host input setup time for DAT	10	–	ns
tSDIH CMD	Host input hold time for CMD	9	–	ns
tSDIH DAT	Host input hold time for DAT	9	–	ns
tSDOS CMD	Host output setup time for CMD	3	–	ns
tSDOS DAT	Host output setup time for DAT	3	–	ns
tSDOH CMD	Host output hold time for CMD	3	–	ns
tSDOH DAT	Host output hold time for DAT	3	–	ns
tSCLKR	Clock rise time	–	2	ns
tSCLKF	Clock fall time	–	2	ns
tSDCK	Clock cycle time	38.5	–	ns
SDFREQ	Clock frequency		26	MHz
tSDCLKOD	Clock duty cycle	40	60	%
MC-HS				
tSDIS CMD	Host input setup time for CMD	4	–	ns
tSDIS DAT	Host input setup time for DAT	4	–	ns
tSDIH CMD	Host input hold time for CMD	3	–	ns
tSDIH DAT	Host input hold time for DAT	3	–	ns
tSDOS CMD	Host output setup time for CMD	3	–	ns
tSDOS DAT	Host output setup time for DAT	3	–	ns
tSDOH CMD	Host output hold time for CMD	3	–	ns
tSDOH DAT	Host output hold time for DAT	3	–	ns
tSCLKR	Clock rise time	–	2	ns

Table 9. S-Port Timing Parameters[3] (continued)

Parameter	Description	Min	Max	Units
tSCLKF	Clock fall time	–	2	ns
tSDCK	Clock cycle time	19.2	–	ns
SDFREQ	Clock frequency	–	52	MHz
tSDCLKOD	Clock duty cycle	40	60	%
MMC-DDR52				
tSDIS CMD	Host input setup time for CMD	4	–	ns
tSDIS DAT	Host input setup time for DAT	0.56	–	ns
tSDIH CMD	Host input hold time for CMD	3	–	ns
tSDIH DAT	Host input hold time for DAT	2.58	–	ns
tSDOS CMD	Host output setup time for CMD	3	–	ns
tSDOS DAT	Host output setup time for DAT	2.5	–	ns
tSDOH CMD	Host output hold time for CMD	3	–	ns
tSDOH DAT	Host output hold time for DAT	2.5	–	ns
tSCLKR	Clock rise time	–	2	ns
tSCLKF	Clock fall time	–	2	ns
tSDCK	Clock cycle time	19.2	–	ns
SDFREQ	Clock frequency		52	MHz
tSDCLKOD	Clock duty cycle	45	55	%
SD-Default Speed (SDR12)				
tSDIS CMD	Host input setup time for CMD	24	–	ns
tSDIS DAT	Host input setup time for DAT	24	–	ns
tSDIH CMD	Host input hold time for CMD	2.5	–	ns
tSDIH DAT	Host input hold time for DAT	2.5	–	ns
tSDOS CMD	Host output setup time for CMD	5	–	ns
tSDOS DAT	Host output setup time for DAT	5	–	ns
tSDOH CMD	Host output hold time for CMD	5	–	ns
tSDOH DAT	Host output hold time for DAT	5	–	ns
tSCLKR	Clock rise time	–	2	ns
tSCLKF	Clock fall time	–	2	ns
tSDCK	Clock cycle time	40	–	ns
SDFREQ	Clock frequency		25	MHz
tSDCLKOD	Clock duty cycle	40	60	%
SD-High-Speed(SDR25)				
tSDIS CMD	Host input setup time for CMD	4	–	ns
tSDIS DAT	Host input setup time for DAT	4	–	ns
tSDIH CMD	Host input hold time for CMD	2.5	–	ns
tSDIH DAT	Host input hold time for DAT	2.5	–	ns
tSDOS CMD	Host output setup time for CMD	6	–	ns
tSDOS DAT	Host output setup time for DAT	6	–	ns
tSDOH CMD	Host output hold time for CMD	2	–	ns
tSDOH DAT	Host output hold time for DAT	2	–	ns
tSCLKR	Clock rise time	–	2	ns

Table 9. S-Port Timing Parameters[3] (continued)

Parameter	Description	Min	Max	Units
tSCLKF	Clock fall time	–	2	ns
tSDCK	Clock cycle time	20	–	ns
SDFREQ	Clock frequency	–	50	MHz
tSDCLKOD	Clock duty cycle	40	60	%
SD-SDR50				
tSDIS CMD	Host input setup time for CMD	1.5	–	ns
tSDIS DAT	Host input setup time for DAT	1.5	–	ns
tSDIH CMD	Host input hold time for CMD	2.5	–	ns
tSDIH DAT	Host input hold time for DAT	2.5	–	ns
tSDOS CMD	Host output setup time for CMD	3	–	ns
tSDOS DAT	Host output setup time for DAT	3	–	ns
tSDOH CMD	Host output hold time for CMD	0.8	–	ns
tSDOH DAT	Host output hold time for DAT	0.8	–	ns
tSCLKR	Clock rise time	–	2	ns
tSCLKF	Clock fall time	–	2	ns
tSDCK	Clock cycle time	10	–	ns
SDFREQ	Clock frequency		100	MHz
tSDCLKOD	Clock duty cycle	40	60	%
SD-DDR50				
tSDIS CMD	Host input setup time for CMD	4	–	ns
tSDIS DAT	Host input setup time for DAT	0.92	–	ns
tSDIH CMD	Host input hold time for CMD	2.5	–	ns
tSDIH DAT	Host input hold time for DAT	2.5	–	ns
tSDOS CMD	Host output setup time for CMD	6	–	ns
tSDOS DAT	Host output setup time for DAT	3	–	ns
tSDOH CMD	Host output hold time for CMD	0.8	–	ns
tSDOH DAT	Host output hold time for DAT	0.8	–	ns
tSCLKR	Clock rise time	–	2	ns
tSCLKF	Clock fall time	–	2	ns
tSDCK	Clock cycle time	20	–	ns
SDFREQ	Clock frequency		50	MHz
tSDCLKOD	Clock duty cycle	45	55	%

Note
3. All parameters guaranteed by design and validated through characterization.

I²S Timing Diagram

Figure 5. I²S Transmit Cycle

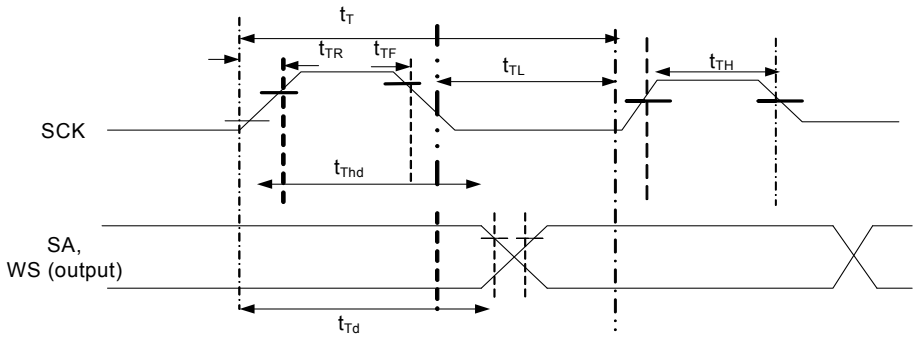


Table 11. I²S Timing Parameters[5]

Parameter	Description	Min	Max	Units
tT	I²S transmitter clock cycle	Ttr	–	ns
tTL	I²S transmitter cycle LOW period	0.35 Ttr	–	ns
tTH	I²S transmitter cycle HIGH period	0.35 Ttr	–	ns
tTR	I²S transmitter rise time	–	0.15 Ttr	ns
tTF	I²S transmitter fall time	–	0.15 Ttr	ns
tThd	I²S transmitter data hold time	0	–	ns
tTd	I²S transmitter delay time	–	0.8tT	ns
Note tT is selectable through clock gears. Max Ttr is designed for 96-kHz codec at 32 bits to be 326 ns (3.072 MHz).				

Note
5. All parameters guaranteed by design and validated through characterization.

Table 12. SPI Timing Parameters[6]

Parameter	Description	Min	Max	Units
fop	Operating frequency	0	33	MHz
tsck	Cycle time	30	–	ns
twsck	Clock high/low time	13.5	–	ns
tlead	SSN-SCK lead time	1/2 tsck[7]-5	1.5 tsck[7]+ 5	ns
tlag	Enable lag time	0.5	1.5 tsck[7]+5	ns
trf	Rise/fall time	–	8	ns
tsdd	Output SSN to valid data delay time	–	5	ns
tdv	Output data valid time	–	5	ns
tdi	Output data invalid	0	–	ns
tssnh	Minimum SSN high time	10	–	ns
tsdi	Data setup time input	8	–	ns
thoi	Data hold time input	0	–	ns
tdis	Disable data output on SSN high	0	–	ns

Notes
6. All parameters guaranteed by design and validated through characterization.
7. Depends on LAG and LEAD setting in the SPI_CONFIG register.

Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power supplied (Industrial) ..... –40 °C to +85 °C

Supply voltage to ground potential V_{DD}, A_{VDDQ} ..... 1.25 V

$S2_{VDDQ}$,$S1_{VDDQ}$, $S0_{VDDQ}$, V_{IO4}, V_{IO5} ..... 3.6 V

$U3TX_{VDDQ}$, $U3RX_{VDDQ}$ ..... 1.25 V

DC input voltage to any input pin ..... VCC + 0.3

DC voltage applied to outputs in High Z State ..... VCC + 0.3

(VCC is the corresponding I/O voltage)

Static discharge voltage ESD protection levels:

- ±2.2-KV human body model (HBM) based on JESD22-A114
- Additional ESD Protection levels on D+, D–, VBUS, GND pins U-port and GPIO pins LPP-Port
- ±6-KV contact discharge, ±8-KV air gap discharge based on IEC61000-4-2 level 3A, ±8-KV contact discharge, and ±15-KV air gap discharge based on IEC61000-4-2 level 4C

Latch-up current ..... > 200 mA

Maximum output short circuit current for all I/O configurations. (Vout = 0 V) ..... –100 mA

Operating Conditions

TA (ambient temperature under bias) Industrial ..... –40 °C to +85 °C

V_{DD}, A_{VDDQ}, $U3TX_{VDDQ}$, $U3RX_{VDDQ}$ supply voltage ..... 1.15 V to 1.25 V

V_{BATT} supply voltage ..... 3.2 V to 6 V

$S2_{VDDQ}$, $S1_{VDDQ}$, $S0_{VDDQ}$, V_{IO4}, C_{VDDQ} supply voltage ..... 1.7 V to 3.6 V

V_{IO5} supply voltage ..... 1.15 V to 3.6 V

Table 13. DC Specifications (continued)

Parameter	Description	Min	Max	Units	Notes
I_{SB1}	Total suspend current during Suspend Mode with USB 3.0 PHY enabled (L1 mode)	–	–	mA	Core current: 1.5 mA I/O current: 20 µA USB current: 2 mA For typical PVT (Typical silicon, all power supplies at their respective nominal levels at 25 °C.)
I_{SB2}	Total suspend current during Suspend Mode with USB 3.0 PHYdisabled (L2 mode)	–	–	mA	Core current: 250 µA I/O current: 20 µA USB current: 1.2 mA For typical PVT (Typical silicon, all power supplies at their respective nominal levels at 25 °C.)
I_{SB3}	Total Standby Current during Standby Mode (L3 mode)	–	–	µA	Core current: 60 µA I/O current: 20 µA USB current: 40 µA For typical PVT (Typical silicon, all power supplies at their respective nominal levels at 25 °C.)
I_{SB4}	Total Standby Current during Core Power Down Mode (L4 mode)	–	–	µA	Core current: 0 µA I/O current: 20 µA USB current: 40 µA For typical PVT (Typical silicon, all power supplies at their respective nominal levels at 25 °C.)
V_{RAMP}	Voltage Ramp Rate on Core and I/O Supplies	0.2	50	V/ms	Voltage ramp must be monotonic
V_N	Noise Level Permitted on VDD and I/O Supplies	–	100	mV	Max p-p noise level permitted on all supplies except A_{VDD}
V_{N_AVDD}	Noise Level Permitted on AVDD Supply	–	20	mV	Max p-p noise level permitted on A_{VDD}

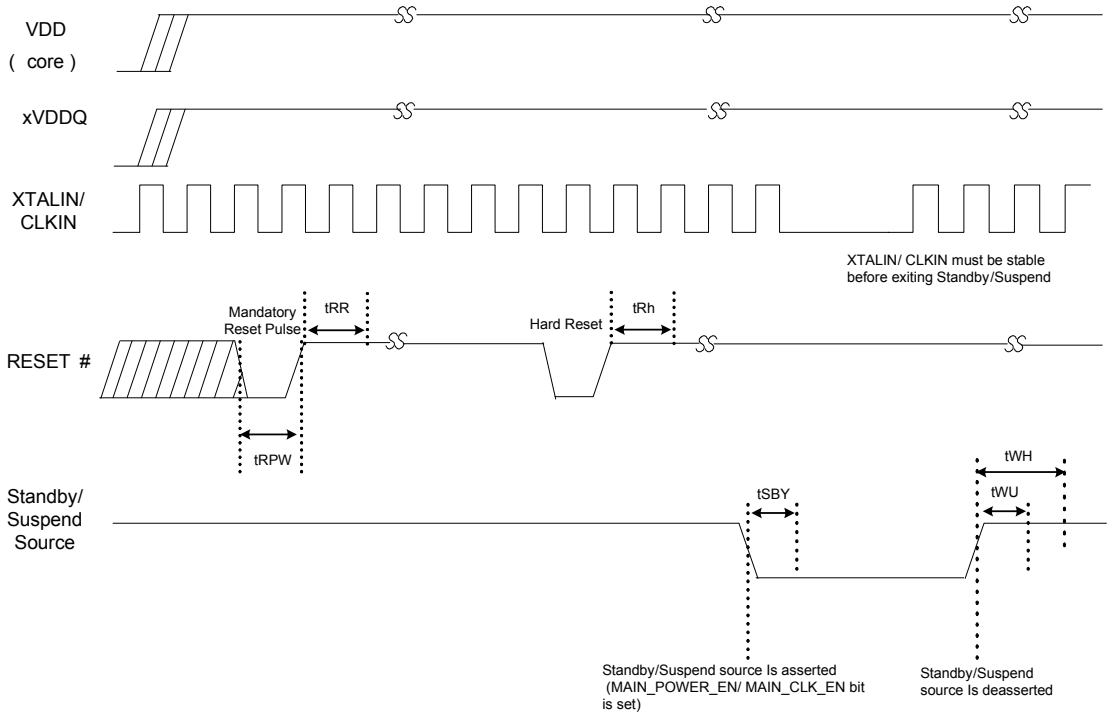
Reset Sequence

Table 14 provides the hard reset sequence requirements for SD3.

Table 14. Reset and Standby Timing Parameters

Parameter	Definition	Conditions	Min (ms)	Max (ms)
tRPW	Minimum RESET# pulse width	Clock Input	1	–
		Crystal Input	1	–
tRH	Minimum high on RESET#	–	5	–
tRR	Reset Recovery Time (after which Boot loader begins firmware download)	Clock Input	1	–
		Crystal Input	5	
tSBY	Time to enter Standby/Suspend (from the time MAIN_CLOCK_EN/ MAIN_POWER_EN bit is set)	–	–	1
tWU	Time to wakeup from standby	Clock Input	1	–
		Crystal Input	5	–
tWH	Minimum time before Standby/Suspend source may be reasserted	–	5	–

Figure 7. Reset Sequence



Acronyms

Table 16. Acronyms Used in this Document

Acronym	Description
ACA	accessory charger adaptor
BGA	ball grid array
MMC	multimedia card
PLL	phase locked loop
SD	secure digital
SDIO	secure digital input / output
SLC	single-level cell
USB	universal serial bus

Document Conventions

Units of Measure

Table 17. Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
µA	microamperes
µs	microseconds
mA	milliamperes
Mbps	Megabytes per second
MHz	mega hertz
ms	milliseconds
ns	nanoseconds
Ω	ohms
pF	pico Farad
V	volts

Errata

This document describes the errata for the SD3, CYUSB3021-BZXI. Details include errata trigger conditions, scope of impact, available workarounds, and silicon revision applicability. Compare this document to the device's datasheet for a complete functional description. Contact your local Cypress Sales Representative if you have questions.

Part Numbers Affected

Part Number	Device Characteristics
CYUSB3021-BZXI	

SD3 USB and Mass Storage Peripheral Controller Qualification Status

Product Status: Sampling

SD3 USB and Mass Storage Peripheral Controller Errata Summary

The following table defines the errata applicability to available SD3 USB and Mass Storage Peripheral Controller family devices.

Items	Part Number	Silicon Revision	Fix Status
[1]. USB Boot is Not Stable	CYUSB3021-BZXI	ES	Workaround provided Fix in Production Silicon

1. USB Boot is Not Stable

■Problem Definition

SD3 may not enumerate with the USB host (for example, a PC) and fail to boot from the USB port if, after reset, the PMODE pins are selected or configured to boot from USB.

■Parameters Affected

NA

■Trigger Condition(s)

This condition is triggered when PMODE pins are configured to boot from USB port.

■Scope of Impact

Fails to boot from USB Port

■Workaround

Select an alternate boot option, such as I2C or P-Port boot

■Fix Status

Fix in production silicon

Document History Page

Document Title: CYUSB302x, SD3™ USB and Mass Storage Peripheral Controller Document Number: 001-55190				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	2761891	VSO	09/10/09	New data sheet.
*A	2823531	OSG	12/08/2009	Added data sheet to the USB 3.0 EROS spec 001-51884. No technical updates.
*B	3080927	OSG	11/08/2010	Changed status from Advance to Preliminary Added the following sections: Power, Configuration Fuse, Digital I/Os, EMI, System Level ESD, Absolute Maximum Ratings, AC Timing Parameters, Reset Sequence. Added DC Specifications table Updated Pin List Updated block diagram Updated part number Updated package diagram
*C	3204393	OSG	03/23/2011	Added a reference to footnote 1 in Table 1.
*D	3217917	OSG	04/06/2011	Changed values of R_USB2 and R_USB3
*E	3369042	OSG	12/06/2011	Updated tRR and tRPW for crystal input Added clarification regarding I_{OZ} and I_{IX} Updated 121-ball FBGA package diagram Added clarification regarding VCC in DC Specifications table In Power Modes description, stated that S2VDDQ cannot be turned off at any time if the S2-port is used in the application Updated Absolute Maximum Ratings Added requirement for by-pass capacitor on $U3RX_{VDDQ}$ and $U3TX_{VDDQ}$ Updated I2C interface tVD:ACK parameter for 1 MHz operation. Changed datasheet status from Preliminary to Final.
*F	3649782	OSG	08/16/2012	Added note about the I2C controller support for clock stretching. Updated Clocking and Hard Reset sections. Modified V_{BUS} min value. Updated Rise/fall time max value.
*G	3848148	OSG	12/20/2012	Updated 121-ball FBGA package diagram to current revision.
*H	4016006	GSZ	06/04/2013	Updated Features. Updated Applications. Updated Logic Block Diagram. Updated Functional Overview. Updated Pin Description for BGA. Added Pinout for WLCSP. Added Pin Description for WLCSP. Updated AC Timing Parameters Updated Package Diagrams (Added Figure 9). Updated Ordering Information (Updated part numbers).
*I	4131901	GSZ	09/23/2013	Changed status to Final. Updated Package Diagrams: spec 001-62221 – Changed revision from *B to *C. Updated Ordering Information (Updated part numbers). Updated in new template. Completing Sunset Review.
*J	5460202	RAJV	10/14/2016	Added Errata. Updated package diagram (spec 001-54471 *D to *E) in Package Diagrams. Updated CY Logo, Copyright and Disclaimer.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

ARM® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Lighting & Power Control	cypress.com/powerpsoc
Memory	cypress.com/memory
PSoC	cypress.com/psoc
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless/RF	cypress.com/wireless

PSoC® Solutions

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP

Cypress Developer Community

Forums | Projects | Video | Blogs | Training | Components

Technical Support

cypress.com/support

© Cypress Semiconductor Corporation, 2009-2016. This document is the property of Cypress Semiconductor Corporation and its subsidiaries, including Spansion LLC ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. Cypress products are not designed, intended, or authorized for use as critical components in systems designed or intended for the operation of weapons, weapons systems, nuclear installations, life-support devices or systems, other medical devices or systems (including resuscitation equipment and surgical implants), pollution control or hazardous substances management, or other uses where the failure of the device or system could cause personal injury, death, or property damage ("Unintended Uses"). A critical component is any component of a device or system whose failure to perform can be reasonably expected to cause the failure of the device or system, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from or related to all Unintended Uses of Cypress products. You shall indemnify and hold Cypress harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of Cypress products.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, WICED, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit cypress.com. Other names and brands may be claimed as property of their respective owners.