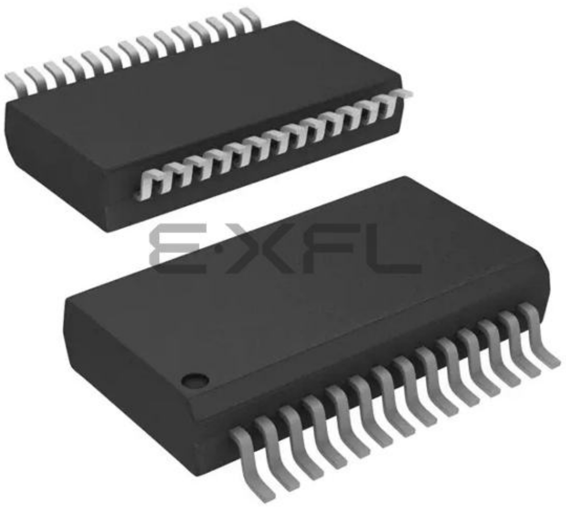

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

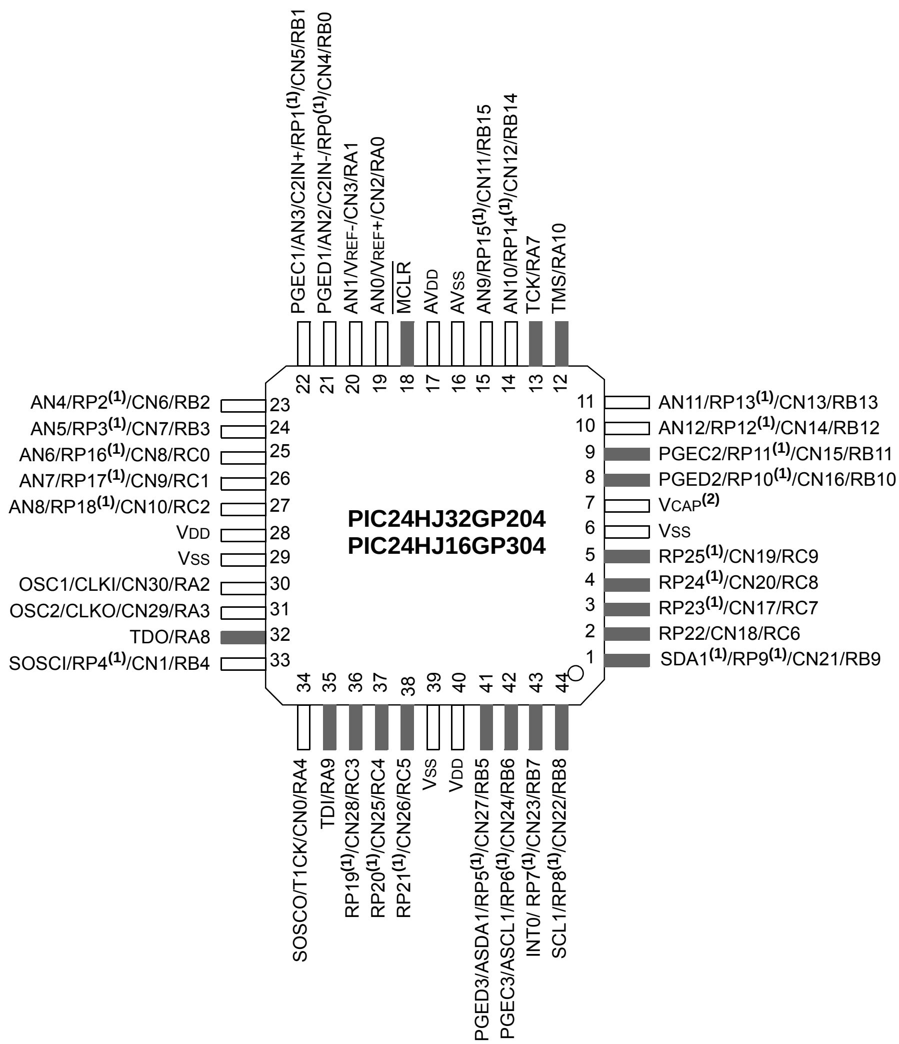
## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | PIC |
| Core Size | 16-Bit |
| Speed | 40 MIPs |
| Connectivity | I²C, IrDA, LINbus, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, POR, PWM, WDT |
| Number of I/O | 21 |
| Program Memory Size | 32KB (11K x 24) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 2K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 3.6V |
| Data Converters | A/D 10x10b/12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 28-SSOP (0.209", 5.30mm Width) |
| Supplier Device Package | 28-SSOP |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic24hj32gp202-e-ss |

## Pin Diagrams (Continued)

### 44-Pin TQFP

■ = Pins are up to 5V tolerant




**Note 1:** The RPn pins can be used by any remappable peripheral. See Table 1 for the list of available peripherals.

**2:** Refer to **Section 2.3 "CPU Logic Filter Capacitor Connection (VCAP)"** for proper connection to this pin.

## 3.3 CPU Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

| **Note:** | In the event you are not able to access the product page using the link above, enter this URL in your browser: http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en530271 |
|---|---|

### 3.3.1 KEY RESOURCES

- **Section 2. "CPU"** (DS70204)
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All related dsPIC33F/PIC24H Family Reference Manuals Sections
- Development Tools

## 4.2 Data Address Space

The CPU has a separate 16 bit wide data memory space. The data space is accessed using separate Address Generation Units (AGUs) for read and write operations. The data memory maps is shown in Figure 4-3.

All Effective Addresses (EAs) in the data memory space are 16 bits wide and point to the bytes within the data space. This arrangement gives a data space address range of 64 Kbytes or 32K words. The lower half of the data memory space (that is, when EA<15> = 0) is used for implemented memory addresses, while the upper half (EA<15> = 1) is reserved for the Program Space Visibility area (see **Section 4.6.3 "Reading Data from Program Memory Using Program Space Visibility"**).

PIC24HJ32GP202/204 and PIC24HJ16GP304 devices implement up to 2 Kbytes of data memory. Should an EA point to a location outside of this area, an all-zero word or byte will be returned.

### 4.2.1 DATA SPACE WIDTH

The data memory space is organized in byte addressable, 16 bit wide blocks. Data is aligned in data memory and registers as 16-bit words, but all data space EAs resolve to bytes. The Least Significant Bytes (LSBs) of each word have even addresses, while the Most Significant Bytes (MSBs) have odd addresses.

### 4.2.2 DATA MEMORY ORGANIZATION AND ALIGNMENT

To maintain backward compatibility with PIC® devices and improve data space memory usage efficiency, the PIC24HJ32GP202/204 and PIC24HJ16GP304 instruction set supports both word and byte operations. As a consequence of byte accessibility, all effective address calculations are internally scaled to step through word-aligned memory. For example, the core recognizes that Post-Modified Register Indirect Addressing mode [Ws++] will result in a value of Ws + 1 for byte operations and Ws + 2 for word operations.

Data byte reads will read the complete word that contains the byte, using the LSB of any EA to determine which byte to select. The selected byte is placed onto the LSB of the data path. That is, data memory and registers are organized as two parallel byte-wide entities with shared (word) address decode, but separate write lines. Data byte writes only write to the corresponding side of the array or register that matches the byte address.

All word accesses must be aligned to an even address. Misaligned word data fetches are not supported, so care must be taken when mixing byte and word operations, or when translating from 8-bit MCU code. If a misaligned read or write is attempted, an address error trap is generated. If the error occurred on a read, the instruction underway is completed. If the instruction occurred on a write, the instruction is executed but the write does not occur. In either case, a trap is then executed, allowing the system and/or user application to examine the machine state prior to execution of the address Fault.

All byte loads into any W register are loaded into the Least Significant Byte. The Most Significant Byte is not modified.

A sign-extend instruction (SE) is provided to allow users to translate 8-bit signed data to 16-bit signed values. Alternatively, for 16-bit unsigned data, user applications can clear the MSB of any W register by executing a zero-extend (ZE) instruction on the appropriate address.

### 4.2.3 SFR SPACE

The first 2 Kbytes of the Near Data Space, from 0x0000 to 0x07FF, is primarily occupied by Special Function Registers (SFRs). These are used by the PIC24HJ32GP202/204 and PIC24HJ16GP304 core and peripheral modules to control the operation of the device.

SFRs are distributed among the modules that they control, and are generally grouped together by module. Much of the SFR space contains unused addresses; these are read as '0'. A complete listing of implemented SFRs, including their addresses, is shown in Table 4-1 through Table 4-22.

| **Note:** | The actual set of peripheral features and interrupts varies by the device. Refer to the corresponding device tables and pinout diagrams for device-specific information. |
|---|---|

### 4.2.4 NEAR DATA SPACE

The 8 Kbyte area between 0x0000 and 0x1FFF is referred to as the Near Data Space. Locations in this space are directly addressable via 13-bit absolute address field within all memory direct instructions. Additionally, the whole data space is addressable using MOV instructions, which support Memory Direct Addressing mode with a 16-bit address field, or by using Indirect Addressing mode using a working register as an address pointer.

### TABLE 4-16: PORTA REGISTER MAP FOR PIC24HJ32GP202

| File Name | Addr | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TRISA | 02C0 | — | — | — | — | — | — | — | — | — | — | — | TRISA4 | TRISA3 | TRISA2 | TRISA1 | TRISA0 | 001F |
| PORTA | 02C2 | — | — | — | — | — | — | — | — | — | — | — | RA4 | RA3 | RA2 | RA1 | RA0 | xxxx |
| LATA | 02C4 | — | — | — | — | — | — | — | — | — | — | — | LATA4 | LATA3 | LATA2 | LATA1 | LATA0 | xxxx |
| ODCA | 02C6 | — | — | — | — | — | — | — | — | — | — | — | ODCA4 | ODCA3 | ODCA2 | ODCA1 | ODCA0 | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

### TABLE 4-17: PORTA REGISTER MAP FOR PIC24HJ32GP204 AND PIC24HJ16GP304

| File Name | Addr | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TRISA | 02C0 | — | — | — | — | — | TRISA10 | TRISA9 | TRISA8 | TRISA7 | — | — | TRISA4 | TRISA3 | TRISA2 | TRISA1 | TRISA0 | 001F |
| PORTA | 02C2 | — | — | — | — | — | RA10 | RA9 | RA8 | RA7 | — | — | RA4 | RA3 | RA2 | RA1 | RA0 | xxxx |
| LATA | 02C4 | — | — | — | — | — | LATA10 | LATA9 | LATA8 | LATA7 | — | — | LATA4 | LATA3 | LATA2 | LATA1 | LATA0 | xxxx |
| ODCA | 02C6 | — | — | — | — | — | ODCA10 | ODCA9 | ODCA8 | ODCA7 | — | — | ODCA4 | ODCA3 | ODCA2 | ODCA1 | ODCA0 | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

### TABLE 4-18: PORTB REGISTER MAP

| File Name | Addr | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TRISB | 02C8 | TRISB15 | TRISB14 | TRISB13 | TRISB12 | TRISB11 | TRISB10 | TRISB9 | TRISB8 | TRISB7 | TRISB6 | TRISB5 | TRISB4 | TRISB3 | TRISB2 | TRISB1 | TRISB0 | FFFF |
| PORTB | 02CA | RB15 | RB14 | RB13 | RB12 | RB11 | RB10 | RB9 | RB8 | RB7 | RB6 | RB5 | RB4 | RB3 | RB2 | RB1 | RB0 | xxxx |
| LATB | 02CC | LATB15 | LATB14 | LATB13 | LATB12 | LATB11 | LATB10 | LATB9 | LATB8 | LATB7 | LATB6 | LATB5 | LATB4 | LATB3 | LATB2 | LATB1 | LATB0 | xxxx |
| ODCB | 02CE | ODCB15 | ODCB14 | ODCB13 | ODCB12 | ODCB11 | ODCB10 | ODCB9 | ODCB8 | ODCB7 | ODCB6 | ODCB5 | ODCB4 | ODCB3 | ODCB2 | ODCB1 | ODCB0 | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal for PinHigh devices.

### TABLE 4-19: PORTC REGISTER MAP FOR PIC24HJ32GP204 AND PIC24HJ16GP304

| File Name | Addr | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TRISC | 02D0 | — | — | — | — | — | — | TRISC9 | TRISC8 | TRISC7 | TRISC6 | TRISC5 | TRISC4 | TRISC3 | TRISC2 | TRISC1 | TRISC0 | 03FF |
| PORTC | 02D2 | — | — | — | — | — | — | RC9 | RC8 | RC7 | RC6 | RC5 | RC4 | RC4 | RC2 | RC1 | RC0 | xxxx |
| LATC | 02D4 | — | — | — | — | — | — | LATC9 | LATC8 | LATC7 | LATC6 | LATC5 | LATC4 | LATC4 | LATC2 | LATC1 | LATC0 | xxxx |
| ODCC | 02D6 | — | — | — | — | — | — | ODCC9 | ODCC8 | ODCC7 | ODCC6 | ODCC5 | ODCC4 | ODCC4 | ODCC2 | ODCC1 | ODCC0 | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

### TABLE 4-20: SYSTEM CONTROL REGISTER MAP

| File Name | Addr | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RCON | 0740 | TRAPR | IOPUWR | — | — | — | — | CM | VREGS | EXTR | SWR | SWDTEN | WDTO | SLEEP | IDLE | BOR | POR | xxxx[1] |
| OSCCON | 0742 | — | COSC<2:0> | | | — | NOSC<2:0> | | | CLKLOCK | IOLOCK | LOCK | — | CF | — | LPOSCEN | OSWEN | 0300[2] |
| CLKDIV | 0744 | ROI | DOZE<2:0> | | | DOZEN | FRCDIV<2:0> | | | PLLPOST<1:0> | | — | PLLPRE<4:0> | | | | | 3040 |
| PLLFBD | 0746 | — | — | — | — | — | — | — | PLLDIV<8:0> | | | | | | | | | 0030 |
| OSCTUN | 0748 | — | — | — | — | — | — | — | — | — | — | TUN<5:0> | | | | | | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as ‘0’. Reset values are shown in hexadecimal.

**Note 1:** RCON register Reset values dependent on type of Reset.

**2:** OSCCON register Reset values dependent on the FOSC Configuration bits and by type of Reset.

### TABLE 4-21: NVM REGISTER MAP

| File Name | Addr | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| NVMCON | 0760 | WR | WREN | WRERR | — | — | — | — | — | — | ERASE | — | — | NVMOP<3:0> | | | | 0000[1] |
| NVMKEY | 0766 | — | — | — | — | — | — | — | — | NVMKEY<7:0> | | | | | | | | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as ‘0’. Reset values are shown in hexadecimal.

**Note 1:** Reset value shown is for POR only. Value on other Reset states is dependent on the state of memory write or erase operations at the time of Reset.

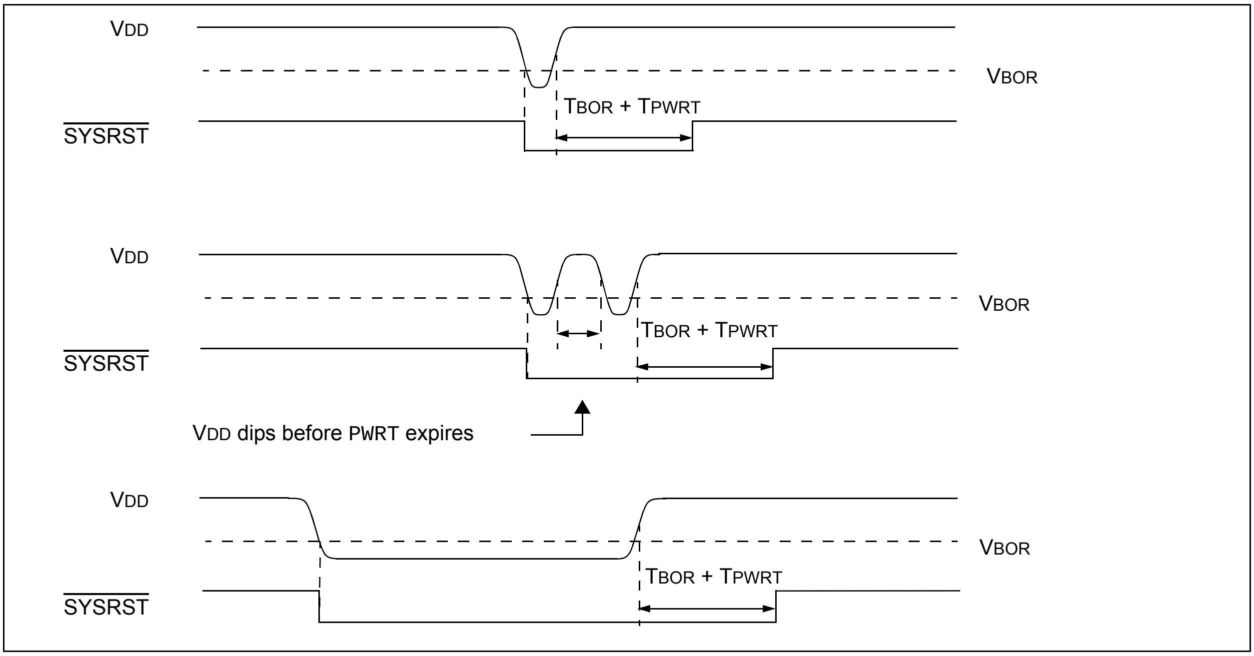
### TABLE 4-22: PMD REGISTER MAP

| File Name | Addr | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PMD1 | 0770 | — | — | T3MD | T2MD | T1MD | — | — | — | I2C1MD | — | U1MD | — | SPI1MD | — | — | AD1MD | 0000 |
| PMD2 | 0772 | IC8MD | IC7MD | — | — | — | — | IC2MD | IC1MD | — | — | — | — | — | — | OC2MD | OC1MD | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as ‘0’. Reset values are shown in hexadecimal.

**NOTES:**

**FIGURE 6-3: BROWN-OUT SITUATIONS**




## 6.5 External Reset (EXTR)

The external Reset is generated by driving the MCLR pin low. The MCLR pin is a Schmitt trigger input with an additional glitch filter. Reset pulses that are longer than the minimum pulse-width will generate a Reset. Refer to **Section 22.0 "Electrical Characteristics"** for minimum pulse-width specifications. The External Reset (MCLR) Pin (EXTR) bit in the Reset Control (RCON) register is set to indicate the MCLR Reset.

### 6.5.1 EXTERNAL SUPERVISORY CIRCUIT

Many systems have external supervisory circuits that generate reset signals to Reset multiple devices in the system. This external Reset signal can be directly connected to the MCLR pin to Reset the device when the rest of system is Reset.

### 6.5.2 INTERNAL SUPERVISORY CIRCUIT

When using the internal power supervisory circuit to Reset the device, the external reset pin (MCLR) should be tied directly or resistively to VDD. In this case, the MCLR pin will not be used to generate a Reset. The external reset pin (MCLR) does not have an internal pull-up and must not be left unconnected.

## 6.6 Software RESET Instruction (SWR)

Whenever the RESET instruction is executed, the device will assert SYSRST, placing the device in a special Reset state. This Reset state will not re-initialize the clock. The clock source in effect prior to the RESET instruction will remain. SYSRST is released at the next instruction cycle, and the reset vector fetch will commence.

The Software Reset (Instruction) Flag (SWR) bit in the Reset Control register (RCON<6>) is set to indicate the software Reset.

## 6.7 Watchdog Time-out Reset (WDTO)

Whenever a Watchdog time-out occurs, the device will asynchronously assert SYSRST. The clock source will remain unchanged. A WDT time-out during Sleep or Idle mode will wake-up the processor, but will not reset the processor.

The Watchdog Timer Time-out Flag bit (WDTO) in the Reset Control register (RCON<4>) is set to indicate the Watchdog Reset. Refer to **Section 19.4 "Watchdog Timer (WDT)"** for more information on Watchdog Reset.

## 6.8 Trap Conflict Reset

If a lower-priority hard trap occurs while a higher-priority trap is being processed, a hard trap conflict Reset occurs. The hard traps include exceptions of priority level 13 through level 15, inclusive. The address error (level 13) and oscillator error (level 14) traps fall into this category.

The Trap Reset Flag bit (TRAPR) in the Reset Control register (RCON<15>) is set to indicate the Trap Conflict Reset. Refer to **Section 7.0 "Interrupt Controller"** for more information on trap conflict Resets.

**REGISTER 10-9: RPINR21: PERIPHERAL PIN SELECT INPUT REGISTER 21**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
|---|---|---|---|---|---|---|---|
| — | — | — | SS1R<4:0> | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-5 **Unimplemented:** Read as ‘0’

bit 4-0 **SS1R<4:0>:** Assign SPI1 Slave Select Input (SS1IN) to the corresponding RPn pin
11111 = Input tied to Vss
11001 = Input tied to RP25
•
•
•
00001 = Input tied to RP1
00000 = Input tied to RP0

**REGISTER 10-10: RPOR0: PERIPHERAL PIN SELECT OUTPUT REGISTER 0**

| U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | RP1R<4:0> | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | RP0R<4:0> | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-13 **Unimplemented:** Read as ‘0’

bit 12-8 **RP1R<4:0>:** Peripheral Output Function is Assigned to RP1 Output Pin (see Table 10-2 for peripheral function numbers)

bit 7-5 **Unimplemented:** Read as ‘0’

bit 4-0 **RP0R<4:0>:** Peripheral Output Function is Assigned to RP0 Output Pin (see Table 10-2 for peripheral function numbers)

## REGISTER 12-2: T3CON CONTROL REGISTER

| R/W-0 | U-0 | R/W-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| TON(2) | — | TSIDL(1) | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | R/W-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | TGATE(2) | TCKPS<1:0>(2) | | — | — | TCS(2) | — |
| bit 7 | | | | | | | bit 0 |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15 **TON:** Timer3 On bit(2)
1 = Starts 16-bit Timer3
0 = Stops 16-bit Timer3

bit 14 **Unimplemented:** Read as ‘0’

bit 13 **TSIDL:** Stop in Idle Mode bit(1)
1 = Discontinue timer operation when device enters Idle mode
0 = Continue timer operation in Idle mode

bit 12-7 **Unimplemented:** Read as ‘0’

bit 6 **TGATE:** Timer3 Gated Time Accumulation Enable bit(2)
When TCS = 1:
This bit is ignored.
When TCS = 0:
1 = Gated time accumulation enabled
0 = Gated time accumulation disabled

bit 5-4 **TCKPS<1:0>:** Timer3 Input Clock Prescale Select bits(2)
11 = 1:256 prescale value
10 = 1:64 prescale value
01 = 1:8 prescale value
00 = 1:1 prescale value

bit 3-2 **Unimplemented:** Read as ‘0’

bit 1 **TCS:** Timer3 Clock Source Select bit(2)
1 = External clock from T3CK pin
0 = Internal clock (FOSC/2)

bit 0 **Unimplemented:** Read as ‘0’

**Note 1:** When 32-bit timer operation is enabled (T32 = 1) in the Timer Control register (T2CON<3>), the TSIDL bit must be cleared to operate the 32-bit timer in Idle mode.

**2:** When the 32-bit timer operation is enabled (T32 = 1) in the Timer Control register (T2CON<3>), these bits have no effect.

## 19.7 In-Circuit Serial Programming

PIC24HJ32GP202/204 and PIC24HJ16GP304 family microcontrollers can be serially programmed while in the end application circuit. This is done with two lines for clock and data, and three other lines for power, ground and the programming sequence. Serial programming allows customers to manufacture boards with unprogrammed devices and then program the microcontroller just before shipping the product. Serial programming also allows the most recent firmware or a custom firmware to be programmed. Refer to the *“dsPIC33F/PIC24H Flash Programming Specification”* (DS70152) document for details about In-Circuit Serial Programming™ (ICSP)™.

Any of the following three pairs of programming clock/data pins can be used:

- PGEC1 and PGED1
- PGEC2 and PGED2
- PGEC3 and PGED3

## 19.8 In-Circuit Debugger

When MPLAB® ICD 2 is selected as a debugger, the in-circuit debugging functionality is enabled. This function allows simple debugging functions when used with MPLAB IDE. Debugging functionality is controlled through the Emulation/Debug Clock (PGECx) and Emulation/Debug Data (PGEDx) pin functions.

Any of the following three pairs of debugging clock/data pins can be used:

- PGEC1 and PGED1
- PGEC2 and PGED2
- PGEC3 and PGED3

To make use of the in-circuit debugger function of the device, the design must implement ICSP connections to $\overline{\text{MCLR}}$, $V_{DD}$, $V_{SS}$ and PGECx/PGEDx pin pair. In addition, when the feature is enabled, some of the resources are not available for general use. These resources include the first 80 bytes of data RAM and two I/O pins.

**TABLE 20-1: SYMBOLS USED IN OPCODE DESCRIPTIONS**

| Field | Description |
|---|---|
| #text | Means literal defined by "text" |
| (text) | Means "content of text" |
| [text] | Means "the location addressed by text" |
| { } | Optional field or operation |
| <n:m> | Register bit field |
| .b | Byte mode selection |
| .d | Double Word mode selection |
| .S | Shadow register select |
| .w | Word mode selection (default) |
| bit4 | 4-bit bit selection field (used in word addressed instructions) ∈ {0...15} |
| C, DC, N, OV, Z | MCU Status bits: Carry, Digit Carry, Negative, Overflow, Sticky Zero |
| Expr | Absolute address, label or expression (resolved by the linker) |
| f | File register address ∈ {0x0000...0x1FFF} |
| lit1 | 1-bit unsigned literal ∈ {0,1} |
| lit4 | 4-bit unsigned literal ∈ {0...15} |
| lit5 | 5-bit unsigned literal ∈ {0...31} |
| lit8 | 8-bit unsigned literal ∈ {0...255} |
| lit10 | 10-bit unsigned literal ∈ {0...255} for Byte mode, {0:1023} for Word mode |
| lit14 | 14-bit unsigned literal ∈ {0...16384} |
| lit16 | 16-bit unsigned literal ∈ {0...65535} |
| lit23 | 23-bit unsigned literal ∈ {0...8388608}; LSB must be '0' |
| None | Field does not require an entry, may be blank |
| PC | Program Counter |
| Slit10 | 10-bit signed literal ∈ {-512...511} |
| Slit16 | 16-bit signed literal ∈ {-32768...32767} |
| Slit6 | 6-bit signed literal ∈ {-16...16} |
| Wb | Base W register ∈ {W0..W15} |
| Wd | Destination W register ∈ { Wd, [Wd], [Wd++], [Wd--], [++Wd], [--Wd] } |
| Wdo | Destination W register ∈ { Wnd, [Wnd], [Wnd++], [Wnd--], [++Wnd], [--Wnd], [Wnd+Wb] } |
| Wm,Wn | Dividend, Divisor working register pair (direct addressing) |
| Wm*Wm | Multiplicand and Multiplier working register pair for Square instructions ∈ {W4 * W4,W5 * W5,W6 * W6,W7 * W7} |
| Wn | One of 16 working registers ∈ {W0..W15} |
| Wnd | One of 16 destination working registers ∈ {W0...W15} |
| Wns | One of 16 source working registers ∈ {W0...W15} |
| WREG | W0 (working register used in file register instructions) |
| Ws | Source W register ∈ { Ws, [Ws], [Ws++], [Ws--], [++Ws], [--Ws] } |
| Wso | Source W register ∈ { Wns, [Wns], [Wns++], [Wns--], [++Wns], [--Wns], [Wns+Wb] } |

**TABLE 20-2: INSTRUCTION SET OVERVIEW (CONTINUED)**

| Base Instr # | Assembly Mnemonic | Assembly Syntax | Description | # of Words | # of Cycles | Status Flags Affected |
|---|---|---|---|---|---|---|
| 12 | BTST | `BTST f,#bit4` | Bit Test f | 1 | 1 | Z |
| | | `BTST.C Ws,#bit4` | Bit Test Ws to C | 1 | 1 | C |
| | | `BTST.Z Ws,#bit4` | Bit Test Ws to Z | 1 | 1 | Z |
| | | `BTST.C Ws,Wb` | Bit Test Ws<Wb> to C | 1 | 1 | C |
| | | `BTST.Z Ws,Wb` | Bit Test Ws<Wb> to Z | 1 | 1 | Z |
| 13 | BTSTS | `BTSTS f,#bit4` | Bit Test then Set f | 1 | 1 | Z |
| | | `BTSTS.C Ws,#bit4` | Bit Test Ws to C, then Set | 1 | 1 | C |
| | | `BTSTS.Z Ws,#bit4` | Bit Test Ws to Z, then Set | 1 | 1 | Z |
| 14 | CALL | `CALL lit23` | Call subroutine | 2 | 2 | None |
| | | `CALL Wn` | Call indirect subroutine | 1 | 2 | None |
| 15 | CLR | `CLR f` | f = 0x0000 | 1 | 1 | None |
| | | `CLR WREG` | WREG = 0x0000 | 1 | 1 | None |
| | | `CLR Ws` | Ws = 0x0000 | 1 | 1 | None |
| 16 | CLRWDT | `CLRWDT` | Clear Watchdog Timer | 1 | 1 | WDTO,Sleep |
| 17 | COM | `COM f` | f = $\overline{f}$ | 1 | 1 | N,Z |
| | | `COM f,WREG` | WREG = $\overline{f}$ | 1 | 1 | N,Z |
| | | `COM Ws,Wd` | Wd = $\overline{Ws}$ | 1 | 1 | N,Z |
| 18 | CP | `CP f` | Compare f with WREG | 1 | 1 | C,DC,N,OV,Z |
| | | `CP Wb,#lit5` | Compare Wb with lit5 | 1 | 1 | C,DC,N,OV,Z |
| | | `CP Wb,Ws` | Compare Wb with Ws (Wb – Ws) | 1 | 1 | C,DC,N,OV,Z |
| 19 | CP0 | `CP0 f` | Compare f with 0x0000 | 1 | 1 | C,DC,N,OV,Z |
| | | `CP0 Ws` | Compare Ws with 0x0000 | 1 | 1 | C,DC,N,OV,Z |
| 20 | CPB | `CPB f` | Compare f with WREG, with Borrow | 1 | 1 | C,DC,N,OV,Z |
| | | `CPB Wb,#lit5` | Compare Wb with lit5, with Borrow | 1 | 1 | C,DC,N,OV,Z |
| | | `CPB Wb,Ws` | Compare Wb with Ws, with Borrow (Wb - Ws - $\overline{C}$) | 1 | 1 | C,DC,N,OV,Z |
| 21 | CPSEQ | `CPSEQ Wb, Wn` | Compare Wb with Wn, skip if = | 1 | 1 (2 or 3) | None |
| 22 | CPSGT | `CPSGT Wb, Wn` | Compare Wb with Wn, skip if > | 1 | 1 (2 or 3) | None |
| 23 | CPSLT | `CPSLT Wb, Wn` | Compare Wb with Wn, skip if < | 1 | 1 (2 or 3) | None |
| 24 | CPSNE | `CPSNE Wb, Wn` | Compare Wb with Wn, skip if ¼ | 1 | 1 (2 or 3) | None |
| 25 | DAW | `DAW Wn` | Wn = decimal adjust Wn | 1 | 1 | C |
| 26 | DEC | `DEC f` | f = f - 1 | 1 | 1 | C,DC,N,OV,Z |
| | | `DEC f,WREG` | WREG = f - 1 | 1 | 1 | C,DC,N,OV,Z |
| | | `DEC Ws,Wd` | Wd = Ws - 1 | 1 | 1 | C,DC,N,OV,Z |
| 27 | DEC2 | `DEC2 f` | f = f - 2 | 1 | 1 | C,DC,N,OV,Z |
| | | `DEC2 f,WREG` | WREG = f - 2 | 1 | 1 | C,DC,N,OV,Z |
| | | `DEC2 Ws,Wd` | Wd = Ws - 2 | 1 | 1 | C,DC,N,OV,Z |
| 28 | DISI | `DISI #lit14` | Disable Interrupts for k instruction cycles | 1 | 1 | None |
| 29 | DIV | `DIV.S Wm,Wn` | Signed 16/16-bit Integer Divide | 1 | 18 | N,Z,C,OV |
| | | `DIV.SD Wm,Wn` | Signed 32/16-bit Integer Divide | 1 | 18 | N,Z,C,OV |
| | | `DIV.U Wm,Wn` | Unsigned 16/16-bit Integer Divide | 1 | 18 | N,Z,C,OV |
| | | `DIV.UD Wm,Wn` | Unsigned 32/16-bit Integer Divide | 1 | 18 | N,Z,C,OV |
| 30 | EXCH | `EXCH Wns,Wnd` | Swap Wns with Wnd | 1 | 1 | None |
| 31 | FBCL | `FBCL Ws,Wnd` | Find Bit Change from Left (MSb) Side | 1 | 1 | C |
| 32 | FF1L | `FF1L Ws,Wnd` | Find First One from Left (MSb) Side | 1 | 1 | C |
| 33 | FF1R | `FF1R Ws,Wnd` | Find First One from Right (LSb) Side | 1 | 1 | C |
| 34 | GOTO | `GOTO Expr` | Go to address | 2 | 2 | None |
| | | `GOTO Wn` | Go to indirect | 1 | 2 | None |

## 22.1 DC Characteristics

**TABLE 22-1: OPERATING MIPS VS. VOLTAGE**

| Characteristic | VDD Range (in Volts) | Temp Range (in °C) | Max MIPS PIC24HJ32GP202/204 and PIC24HJ16GP304 |
|---|---|---|---|
| — | VBOR-3.6V(1) | -40°C to +85°C | 40 |
| — | VBOR-3.6V(1) | -40°C to +125°C | 40 |

**Note 1:** Device is functional at VBORMIN < VDD < VDDMIN. Analog modules such as the ADC will have degraded performance. Device functionality is tested but not characterized. Refer to parameter BO10 in Table 22-11 for the minimum and maximum BOR values.

**TABLE 22-2: THERMAL OPERATING CONDITIONS**

| Rating | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Industrial Temperature Devices | | | | | |
| Operating Junction Temperature Range | $T_J$ | -40 | — | +125 | °C |
| Operating Ambient Temperature Range | $T_A$ | -40 | — | +85 | °C |
| Extended Temperature Devices | | | | | |
| Operating Junction Temperature Range | $T_J$ | -40 | — | +155 | °C |
| Operating Ambient Temperature Range | $T_A$ | -40 | — | +125 | °C |
| Power Dissipation:<br>Internal chip power dissipation:<br>$P_{INT} = V_{DD} \times (I_{DD} - \Sigma I_{OH})$<br>I/O Pin Power Dissipation:<br>$I/O = \Sigma (\{V_{DD} - V_{OH}\} \times I_{OH}) + \Sigma (V_{OL} \times I_{OL})$ | $P_D$ | $P_{INT} + P_{I/O}$ | | | W |
| Maximum Allowed Power Dissipation | $P_{DMAX}$ | $(T_J - T_A)/\theta_{JA}$ | | | W |

**TABLE 22-3: THERMAL PACKAGING CHARACTERISTICS**

| Characteristic | Symbol | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|
| Package Thermal Resistance, 44-pin QFN | $\theta_{JA}$ | 32 | — | °C/W | 1 |
| Package Thermal Resistance, 44-pin TFQP | $\theta_{JA}$ | 45 | — | °C/W | 1 |
| Package Thermal Resistance, 28-pin SPDIP | $\theta_{JA}$ | 45 | — | °C/W | 1 |
| Package Thermal Resistance, 28-pin SOIC | $\theta_{JA}$ | 50 | — | °C/W | 1 |
| Package Thermal Resistance, 28-pin SSOP | $\theta_{JA}$ | 71 | — | °C/W | 1 |
| Package Thermal Resistance, 28-pin QFN-S | $\theta_{JA}$ | 35 | — | °C/W | 1 |

**Note 1:** Junction to ambient thermal resistance, Theta-JA ($\theta_{JA}$) numbers are achieved by package simulations.

**FIGURE 22-2: EXTERNAL CLOCK TIMING**

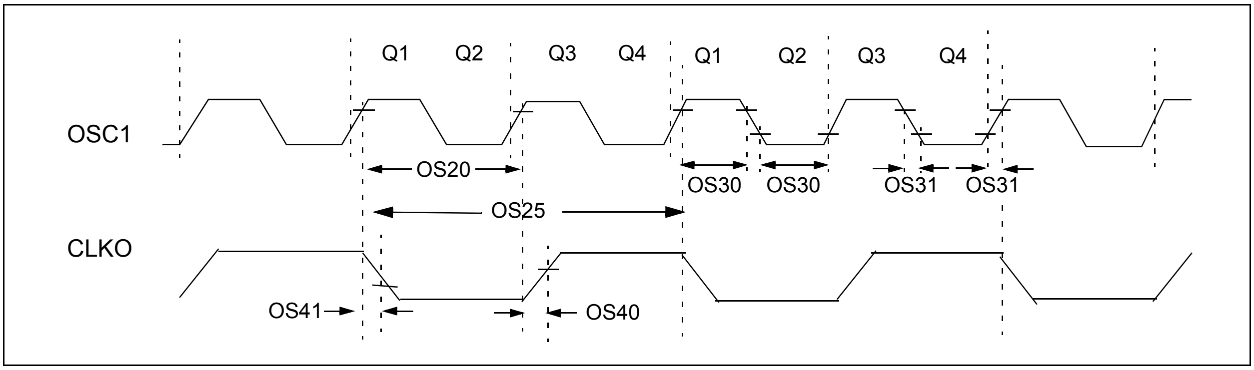



**TABLE 22-16: EXTERNAL CLOCK TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symb** | **Characteristic** | **Min** | **Typ(1)** | **Max** | **Units** | **Conditions** |
| OS10 | FIN | External CLKI Frequency (External clocks allowed only in EC and ECPLL modes)(4) | DC | — | 40 | MHz | EC |
| | | Oscillator Crystal Frequency(5) | 3.5<br>10<br> | —<br>—<br>— | 10<br>40<br>33 | MHz<br>MHz<br>kHz | XT<br>HS<br>SOSC |
| OS20 | TOSC | TOSC = 1/FOSC(4) | 12.5 | — | DC | ns | — |
| OS25 | TCY | Instruction Cycle Time(2,4) | 25 | — | DC | ns | — |
| OS30 | TosL, TosH | External Clock in (OSC1)(5) High or Low Time | 0.375 x TOSC | — | 0.625 x TOSC | ns | EC |
| OS31 | TosR, TosF | External Clock in (OSC1)(5) Rise or Fall Time | — | — | 20 | ns | EC |
| OS40 | TckR | CLKO Rise Time(3,5) | — | 5.2 | — | ns | — |
| OS41 | TckF | CLKO Fall Time(3,5) | — | 5.2 | — | ns | — |
| OS42 | GM | External Oscillator Transconductance(6) | 14 | 16 | 18 | mA/V | VDD = 3.3V<br>TA = +25ºC |

**Note 1:** Data in “Typ” column is at 3.3V, 25°C unless otherwise stated.

**2:** Instruction cycle period (TCY) equals two times the input oscillator time-base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits can result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at “min.” values with an external clock applied to the OSC1/CLKI pin. When an external clock input is used, the “max.” cycle time limit is “DC” (no clock) for all devices.

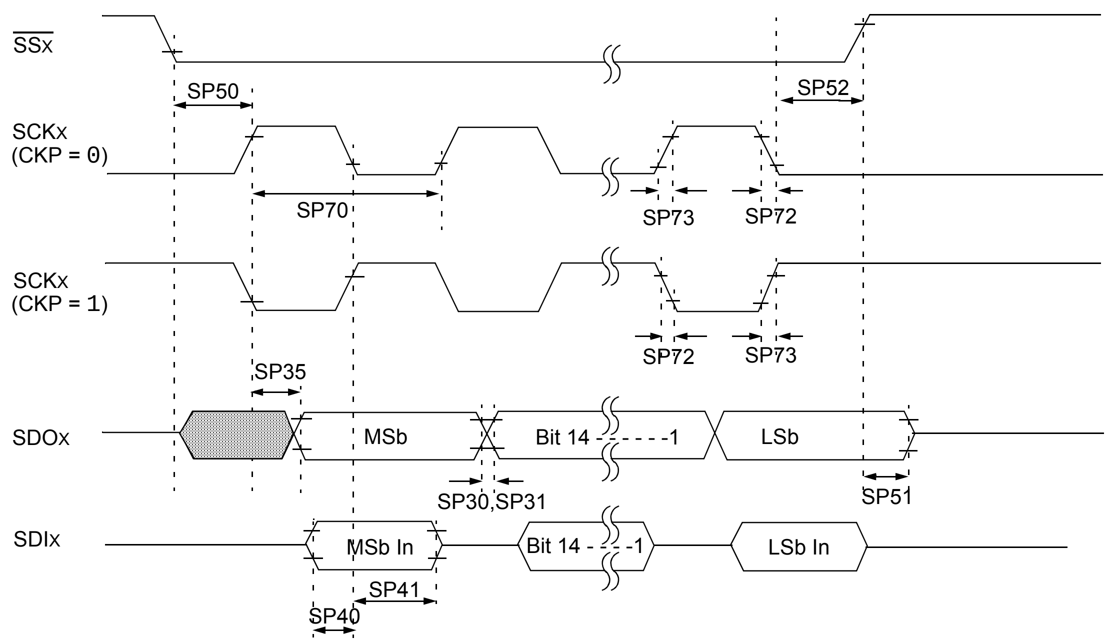
**3:** Measurements are taken in EC mode. The CLKO signal is measured on the OSC2 pin.

**4:** These parameters are characterized by similarity, but are tested in manufacturing at FIN = 40 MHz only.

**5:** These parameters are characterized by similarity, but are not tested in manufacturing.

**6:** Data for this parameter is preliminary. This parameter is characterized, but is not tested in manufacturing.

**FIGURE 22-15: SPIx SLAVE MODE (FULL-DUPLEX CKE = 0, CKP = 1, SMP = 0) TIMING CHARACTERISTICS**




**Note:** Refer to Figure 22-1 for load conditions.

**TABLE 23-10: SPIx MASTER MODE (CKE = 0) TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +150°C for High Temperature | | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic[1]** | **Min** | **Typ** | **Max** | **Units** | **Conditions** |
| HSP35 | TscH2doV, TscL2doV | SDOx Data Output Valid after SCKx Edge | — | 10 | 25 | ns | — |
| HSP40 | TdiV2scH, TdiV2scL | Setup Time of SDIx Data Input to SCKx Edge | 28 | — | — | ns | — |
| HSP41 | TscH2diL, TscL2diL | Hold Time of SDIx Data Input to SCKx Edge | 35 | — | — | ns | — |

**Note 1:** These parameters are characterized but not tested in manufacturing.

**TABLE 23-11: SPIx MODULE MASTER MODE (CKE = 1) TIMING REQUIREMENTS**

| AC CHARACTERISTICS | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +150°C for High Temperature | | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic[1]** | **Min** | **Typ** | **Max** | **Units** | **Conditions** |
| HSP35 | TscH2doV, TscL2doV | SDOx Data Output Valid after SCKx Edge | — | 10 | 25 | ns | — |
| HSP36 | TdoV2sc, TdoV2scL | SDOx Data Output Setup to First SCKx Edge | 35 | — | — | ns | — |
| HSP40 | TdiV2scH, TdiV2scL | Setup Time of SDIx Data Input to SCKx Edge | 28 | — | — | ns | — |
| HSP41 | TscH2diL, TscL2diL | Hold Time of SDIx Data Input to SCKx Edge | 35 | — | — | ns | — |

**Note 1:** These parameters are characterized but not tested in manufacturing.

### TABLE 23-12: SPIx MODULE SLAVE MODE (CKE = 0) TIMING REQUIREMENTS

| AC CHARACTERISTICS | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +150°C for High Temperature | | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic[1]** | **Min** | **Typ** | **Max** | **Units** | **Conditions** |
| HSP35 | TscH2doV,<br>TscL2doV | SDOx Data Output Valid after SCKx Edge | — | — | 35 | ns | — |
| HSP40 | TdiV2scH,<br>TdiV2scL | Setup Time of SDIx Data Input to SCKx Edge | 25 | — | — | ns | — |
| HSP41 | TscH2diL,<br>TscL2diL | Hold Time of SDIx Data Input to SCKx Edge | 25 | — | — | ns | — |
| HSP51 | TssH2doZ | $\overline{SSx}$ ↑ to SDOx Output High-Impedance | 15 | — | 55 | ns | See **Note 2** |

**Note 1:** These parameters are characterized but not tested in manufacturing.

**2:** Assumes 50 pF load on all SPIx pins.

### TABLE 23-13: SPIx MODULE SLAVE MODE (CKE = 1) TIMING REQUIREMENTS

| AC CHARACTERISTICS | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +150°C for High Temperature | | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic[1]** | **Min** | **Typ** | **Max** | **Units** | **Conditions** |
| HSP35 | TscH2doV,<br>TscL2doV | SDOx Data Output Valid after SCKx Edge | — | — | 35 | ns | — |
| HSP40 | TdiV2scH,<br>TdiV2scL | Setup Time of SDIx Data Input to SCKx Edge | 25 | — | — | ns | — |
| HSP41 | TscH2diL,<br>TscL2diL | Hold Time of SDIx Data Input to SCKx Edge | 25 | — | — | ns | — |
| HSP51 | TssH2doZ | $\overline{SSx}$ ↑ to SDOx Output High-Impedance | 15 | — | 55 | ns | See **Note 2** |
| HSP60 | TssL2doV | SDOx Data Output Valid after $\overline{SSx}$ Edge | — | — | 55 | ns | — |

**Note 1:** These parameters are characterized but not tested in manufacturing.

**2:** Assumes 50 pF load on all SPIx pins.

### TABLE 23-14: INTERNAL RC ACCURACY

| AC CHARACTERISTICS | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +150°C for Extended | | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Characteristic** | **Min** | **Typ** | **Max** | **Units** | **Conditions** | |
| | **LPRC @ 32.768 kHz[1,2]** | | | | | | |
| HF21 | LPRC | -70 | — | +70 | % | -40°C ≤ TA ≤ +150°C | VDD = 3.0-3.6V |

**Note 1:** Change of LPRC frequency as VDD changes.

**2:** LPRC accuracy impacts the Watchdog Timer Time-out Period (TWDT1). See **Section 19.4 “Watchdog Timer (WDT)”** for more information.

**FIGURE 24-5: VOL – 2x DRIVER PINS**

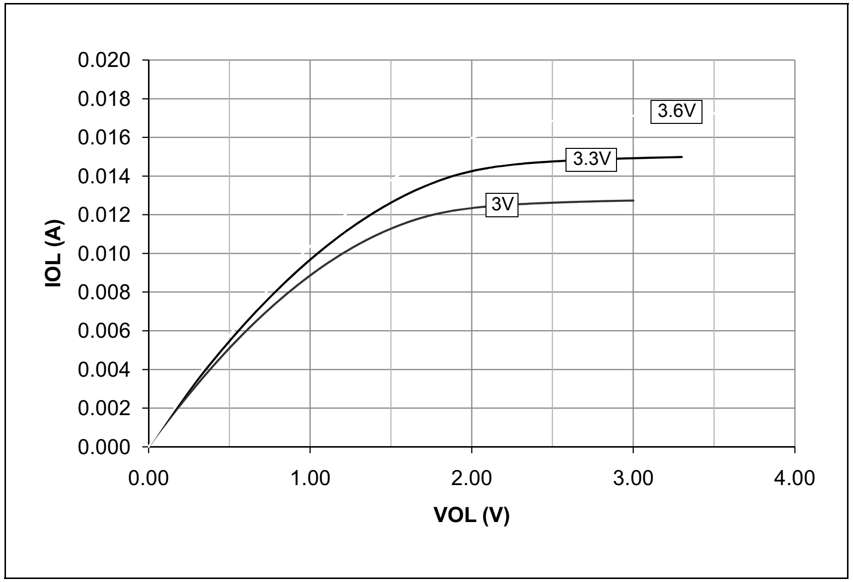



**FIGURE 24-6: VOL – 4x DRIVER PINS**

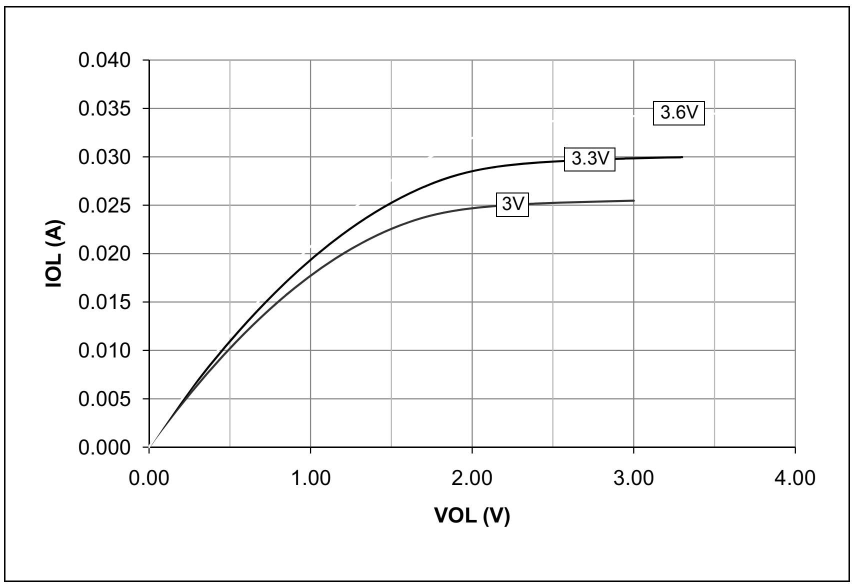



**FIGURE 24-7: VOL – 8x DRIVER PINS**

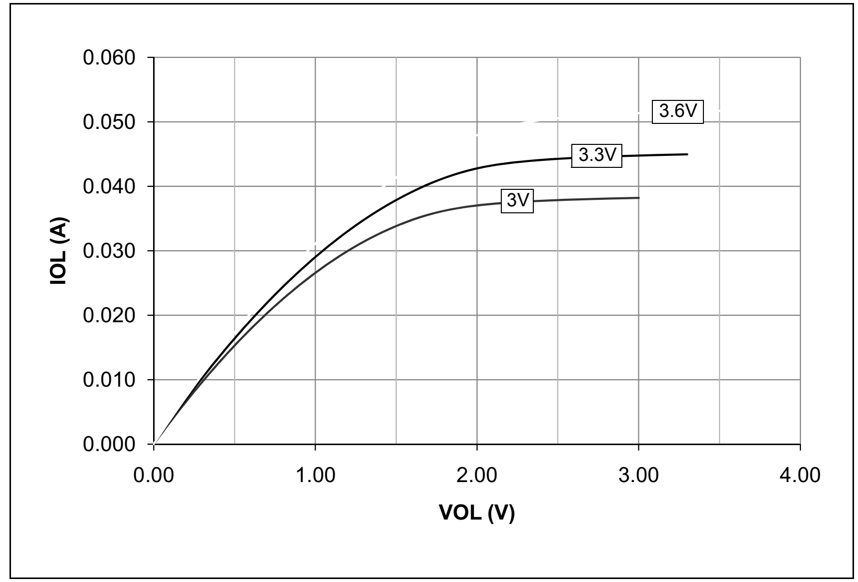
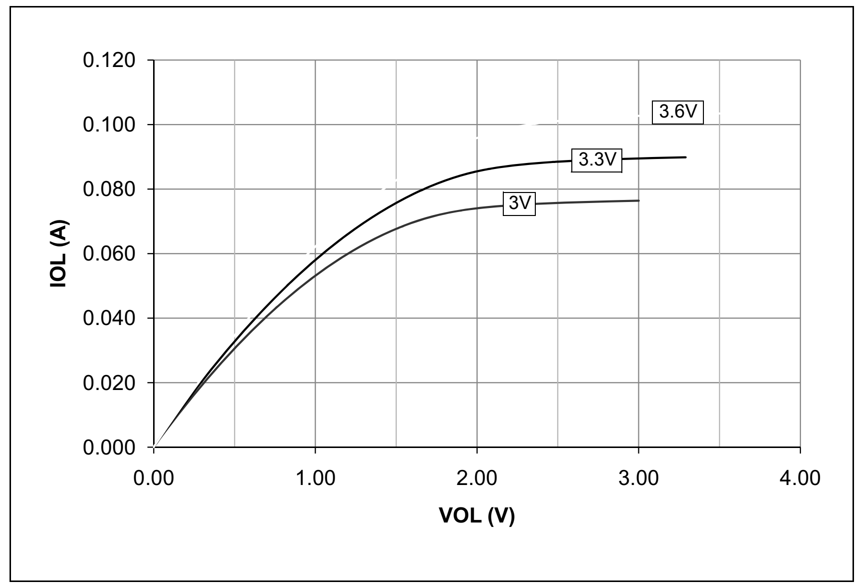



**FIGURE 24-8: VOL – 16x DRIVER PINS**

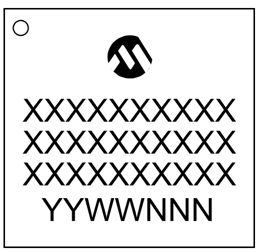


## 25.1 Package Marking Information (Continued)

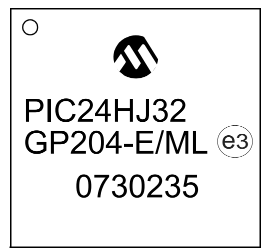
28-Lead QFN-S


Example

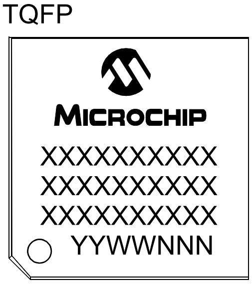

44-Lead QFN



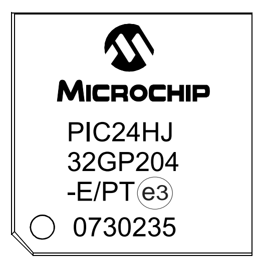

Example




44-Lead TQFP




Example




| | | |
|---|---|---|
| **Legend:** | XX...X | Customer-specific information |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week ‘01’) |
| | NNN | Alphanumeric traceability code |
| | (e3) | Pb-free JEDEC designator for Matte Tin (Sn) |
| | * | This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package. |

**Note:** If the full Microchip part number cannot be marked on one line, it is carried over to the next line, thus limiting the number of available characters for customer-specific information.

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