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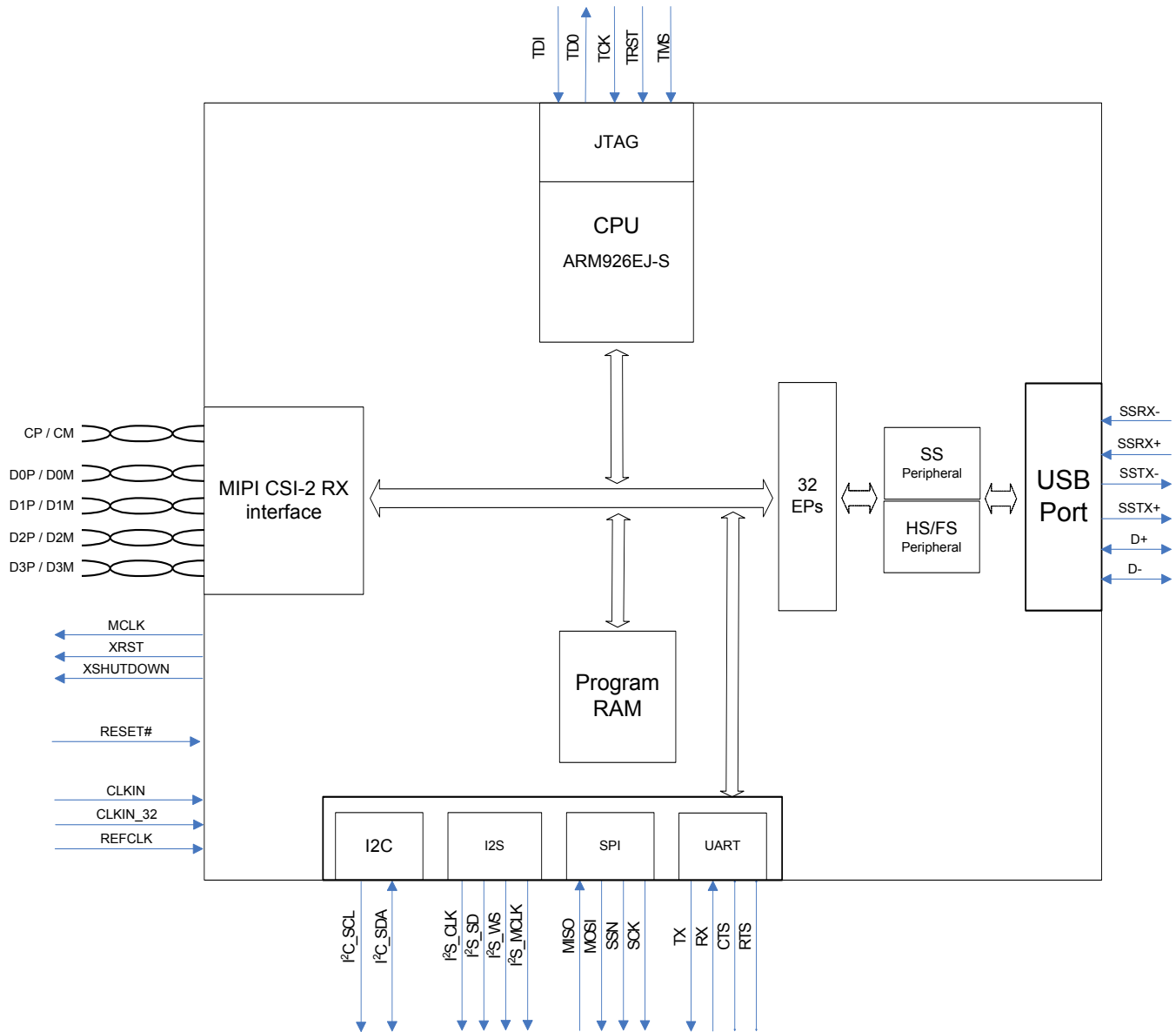
What Are [Embedded - Microcontrollers - Application Specific](#)?

Application specific microcontrollers are engineered to

Details

Product Status	Active
Applications	USB Host/Peripheral Controller
Core Processor	ARM9®
Program Memory Type	External Program Memory
Controller Series	CYUSB
RAM Size	512K x 8
Interface	GPIF, I ² C, I ² S, SPI, UART, USB
Number of I/O	12
Voltage - Supply	1.15V ~ 1.25V
Operating Temperature	0°C ~ 70°C
Mounting Type	Surface Mount
Package / Case	121-LFBGA
Supplier Device Package	121-BGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cyusb3064-bzxc

Logic Block Diagram



More Information

Cypress provides a wealth of data at www.cypress.com to help you to select the right device for your design, and to help you to quickly and effectively integrate the device into your design. For a comprehensive list of resources refer to the cypress web page for CX3 at www.cypress.com/CX3.

- Overview: [USB Portfolio](#), [USB Roadmap](#)
- USB 3.0 Product Selectors: [FX3](#), [FX3S](#), [CX3](#), [GX3](#), [HX3](#), [West Bridge Benicia](#)
- Application notes: Cypress offers a large number of USB application notes covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with CX3 are:
 - [AN75705](#) - Getting Started with EZ-USB FX3
 - [AN90369](#) - How to Interface a MIPI CSI-2 Image Sensor With EZ-USB® CX3
 - [AN75779](#) - How to Implement an Image Sensor Interface with EZ-USB® FX3™ in a USB Video Class (UVC) Framework
 - [AN76405](#) - EZ-USB FX3 Boot Options
 - [AN70707](#) - EZ-USB FX3/FX3S Hardware Design Guidelines and Schematic Checklist
 - [AN86947](#) - Optimizing USB 3.0 Throughput with EZ-USB FX3
- Code Examples:
 - [USB SuperSpeed](#)
- Technical Reference Manual (TRM):
 - [EZ-USB® CX3 Technical Reference Manual](#)

■ Knowledge Base Articles:

- [CX3 Firmware: Frequently Asked Questions - KBA91297](#)
- [CX3 Hardware: Frequently Asked Questions - KBA91295](#)
- [CX3 Application Software / USB Driver: Frequently Asked Questions - KBA91298](#)
- [Knowledge Base - Cypress Semiconductor Cage Code - KBA89258](#)

■ Development Kits:

- [Ascella - Cypress® CX3™ THine® ISP 13MP reference design kit \(RDK\)](#)
- [Denebola - USB 3.0 UVC Reference Design Kit \(RDK\)](#)

■ Models:

- [CX3 Device OrCad Schematic Symbol](#)
- [CYUSB306x - IBIS](#)

EZ-USB Software Development Kit

Cypress delivers the complete firmware stack for CX3, in order to easily integrate SuperSpeed USB into any embedded MIPI image sensor application. The [Software Development Kit \(FX3 SDK\)](#) comes with tools, drivers and application examples, which help accelerate application development. The FX3 SDK Setup includes CX3 APIs and example firmware for OmniVision OV5640 and Aptina AS0260 image sensor interface. The [eclipse plugin](#) for the FX3 SDK accelerates CX3 firmware development for any other image sensor.

Functional Overview

Cypress's EZ-USB CX3 is the next-generation bridge controller that can connect devices with the Mobile Industry Processor Interface – Camera Serial Interface 2 (MIPI CSI-2) interface to any USB 3.0 Host.

CX3 has a 4-lane CSI-2 receiver with up to 1 Gbps on each lane. It supports video data formats such as RAW8/10/12/14, YUV422 (CCIR/ITU 8/10-bit), RGB888/666/565, and user-defined 8-bit.

CX3 has integrated the USB 3.0 and USB 2.0 physical layers (PHYs) along with a 32-bit ARM926EJ-S microprocessor for powerful data processing and for building custom applications.

CX3 contains 512 KB of on-chip SRAM (see [Ordering Information on page 27](#)) for code and data. EZ-USB CX3 also provides interfaces to connect to serial peripherals such as UART, SPI, I²C, and I²S.

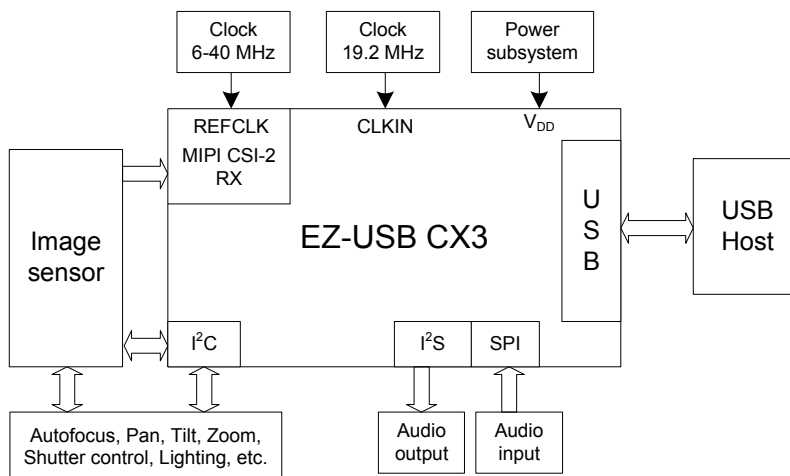
CX3 comes with application development tools. The software development kit comes with application examples for accelerating time-to-market.

CX3 complies with the USB 3.0 v1.0 specification and is also backward compatible with USB 2.0. It also complies with the MIPI CSI-2 v1.01, revision 0.04 specification dated 2nd April 2009.

Application Examples

In a typical application (see [Figure 1](#)), CX3 acts as the main processor and connects to an image sensor, an audio device, or camera control devices amongst others.

Figure 1. EZ-USB CX3 Example Application

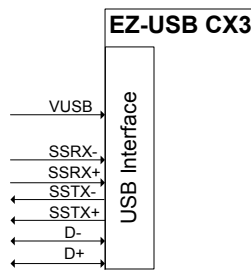


USB Interface

CX3 complies with the following specifications and supports the following features:

- Supports USB peripheral functionality compliant with USB 3.0 Specification, Revision 1.0, and is also backward compatible with the USB 2.0 Specification.
- As a peripheral, CX3 is capable of SuperSpeed, High-Speed, and Full-Speed.
- Supports up to 16 IN and 16 OUT endpoints
- Supports the USB 3.0 Streams feature
- As a USB peripheral, CX3 supports USB-attached storage (UAS), USB Video Class (UVC), and Media Transfer Protocol (MTP) USB peripheral classes. As a USB peripheral, all other device classes are supported only in pass-through mode when handled entirely by a host processor external to the device.

Figure 2. USB Interface Signals



ReNumeration

Because of CX3's soft configuration, one chip can take on the identities of multiple distinct USB devices.

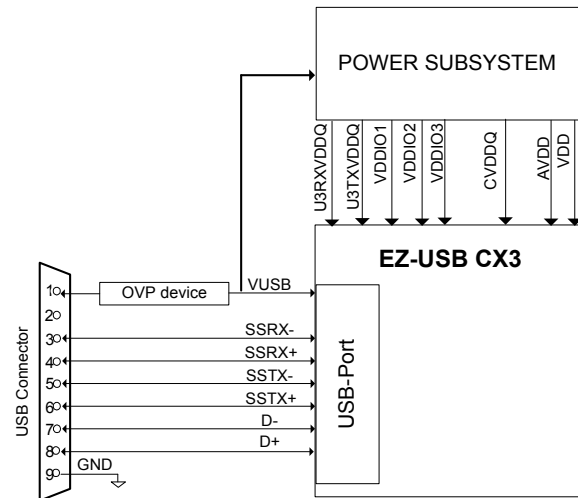
When first plugged into USB, CX3 enumerates automatically with the Cypress Vendor ID (0x04B4) and downloads the firmware and USB descriptors over the USB interface. The downloaded firmware executes an electrical disconnect and connect. CX3 enumerates again, this time as a device defined by the downloaded information. This patented two-step process, called ReNumeration, happens instantly when the device is plugged in.

VBUS Overvoltage Protection

The maximum input voltage on CX3's VUSB pin is 6 V. A charger can supply up to 9 V on VUSB. In this case, an external overvoltage protection (OVP) device is required to protect CX3 from damage on VUSB. [Figure 3](#) shows the system application diagram with an OVP device connected on VUSB. Refer to [DC Specifications on page 17](#) for the operating range of VUSB.

Note: The VBUS pin of the USB connector should be connected to the VUSB pin of CX3.

Figure 3. System Diagram with OVP Device For VUSB



MIPI CSI-2 RX Interface

The Mobile Industry Processor Interface (MIPI) association defined the Camera Serial Interface 2 (CSI-2) standard to enable image data to be sent on high-bandwidth serial lines.

CX3 implements a MIPI CSI-2 Receiver with the following features:

1. It can receive clock and data in 1, 2, 3, or 4 lanes. (CYUSB3065 part supports up to four lanes; CYUSB3064 part supports up to two lanes)
2. Up to 1 Gbps of data on each CSI lane is supported (total maximum bandwidth should not exceed 2.4 Gbps).
3. Video formats such as RAW8/10/12/14, YUV422 (CCIR/ITU 8/10-bit), RGB888/666/565, and User-Defined 8-bit are supported
4. A CCI interface (compatible with 100-kHz or 400-kHz I²C interface with 7-bit addressing) is provided to configure the sensor.
5. GPIOs are available for synchronization of external flash or lighting system with image sensors to illuminate the scene that improves the image quality by improving Signal to noise ratio.
6. GPIOs can also be used to synchronize the image sensor with external events, so that image can be captured based on external event.
7. Serial interfaces (such as I²C, I²S, SPI, UART) are available to implement camera functions such as Auto focus and Pan, Tilt, Zoom (PTZ)

Additional Outputs

In addition to the standard MIPI CSI-2 signals, the following three additional outputs are provided:

1. X_RST: this can be used to reset the image sensor
2. X_SHUTDOWN: this pin can be used to put the sensor to a standby/shutdown mode
3. MCLK: this pin can provide the clock output. It can be used only for testing the image sensor. For production, use an external clock generator as clock input for image sensors.

CPU

CX3 has an on-chip 32-bit, 200-MHz ARM926EJ-S core CPU. The core has direct access to 16 kB of Instruction Tightly Coupled Memory (TCM) and 8 kB of data TCM. The ARM926EJ-S core provides a JTAG interface for firmware debugging.

CX3 offers the following advantages:

- Integrates 512 KB of embedded SRAM for code and data and 8 kB of instruction cache and data cache.
- Implements efficient and flexible DMA connectivity between the various peripherals (such as, USB, CSI-2 Rx, I²S, SPI, and UART), requiring firmware only to configure data accesses between peripherals, which are then managed by the DMA fabric.
- Allows easy application development on industry-standard development tools for ARM926EJ-S.

Examples of the CX3 firmware are available with the Cypress EZ-USB CX3 Development Kit. Software APIs that can be ported to an external processor are available with the Cypress EZ-USB CX3 Software Development Kit.

JTAG Interface

CX3's JTAG interface has a standard five-pin interface to connect to a JTAG debugger in order to debug firmware through the CPU-core's on-chip-debug circuitry.

Industry-standard debugging tools for the ARM926EJ-S core can be used for the CX3 application development.

Other Interfaces

CX3 supports the following serial peripherals:

- UART
- I²C
- I²S
- SPI

The [CYUSB306X Pin List on page 15](#) shows the details of how these interfaces are mapped.

UART Interface

The UART interface of CX3 supports full-duplex communication. It includes the signals noted in [Table 1](#).

Table 1. UART Interface Signals

Signal	Description
TX	Output signal
RX	Input signal
CTS	Flow control
RTS	Flow control

The UART is capable of generating a range of baud rates, from 300 bps to 4608 Kbps, selectable by the firmware. If flow control is enabled, then CX3's UART only transmits data when the CTS input is asserted. In addition to this, CX3's UART asserts the RTS output signal, when it is ready to receive data.

I²C Interface

CX3's I²C interface is compatible with the I²C Bus Specification Revision 3. This I²C interface is capable of operating only as I²C master; therefore, it may be used to communicate with other I²C slave devices. For example, CX3 may boot from an EEPROM connected to the I²C interface, as a selectable boot option.

CX3's I²C Master Controller also supports multi-master mode functionality.

The power supply for the I²C interface is V_{DDIO1}, which is a separate power domain from the other serial peripherals. This gives the I²C interface the flexibility to operate at a different voltage than the other serial interfaces.

The I²C controller supports bus frequencies of 400 kHz, and 1 MHz. When V_{DDIO1} is 1.8 V, 2.5 V, or 3.3 V, the operating frequencies supported are 400 kHz and 1 MHz. The I²C controller supports the clock-stretching feature to enable slower devices to exercise flow control.

The I²C interface's SCL and SDA signals require external pull-up resistors. The pull-up resistors must be connected to V_{DDIO1}.

Note: I²C addresses with the pattern 0x000011x are used internally and no slave devices with those addresses should be connected to the bus.

I²S Interface

CX3 has an I²S port to support external audio codec devices. CX3 functions as I²S Master as transmitter only. The I²S interface consists of four signals: clock line (I2S_CLK), serial data line (I2S_SD), word select line (I2S_WS), and master system clock (I2S_MCLK). CX3 can generate the system clock as an output on I2S_MCLK or accept an external system clock input on I2S_MCLK.

The sampling frequencies supported by the I²S interface are 32 kHz, 44.1 kHz, and 48 kHz.

SPI Interface

CX3 supports an SPI Master interface on the Serial Peripherals port. The maximum operation frequency is 33 MHz.

The SPI controller supports four modes of SPI communication (see [SPI Timing Specification on page 24](#) for details on the modes) with the Start-Stop clock. This controller is a single-master controller with a single automated SSN control. It supports transaction sizes ranging from 4 bits to 32 bits.

Boot Options

CX3 can load boot images from various sources, selected by the configuration of the PMODE pins. Following are the CX3 boot options:

- Boot from USB
- Boot from I²C
- Boot from SPI (SPI devices supported are M25P16 (16 Mbit), M25P80 (8 Mbit), and M25P40 (4 Mbit)) or their equivalents

Table 2. CX3 Booting Options

PMODE[2:0] ^[1]	Boot From
F11	USB boot
F1F	I ² C, On failure, USB boot is enabled
1FF	I ² C only
0F1	SPI, On failure, USB boot is enabled

Reset

Hard Reset

A hard reset is initiated by asserting the RESET# pin on CX3. The specific reset sequence and timing requirements are detailed in [Figure 11 on page 26](#) and [Table 14 on page 26](#). All I/Os are tristated during a hard reset.

An additional reset pin called MIPI_RESET is provided that resets the MIPI CSI-2 core. It should be pulled down with a resistor for normal operation.

Soft Reset

There are two types of Soft Reset:

- CPU Reset – The CPU Program Counter is reset. Firmware does not need to be reloaded following a CPU Reset.
- Whole Device Reset – This reset is identical to Hard Reset. The firmware must be reloaded following a Whole Device Reset.

Note

1. F indicates Floating.

Clocking

CX3 requires two clocks for normal operation:

1. A 19.2-MHz clock to be connected at the CLKIN pin
2. A 6-MHz to 40-MHz clock to be connected at the REFCLK pin

Clock inputs to CX3 must meet the phase noise and jitter requirements specified in [Table 3 on page 9](#).

The input clock frequency is independent of the clock and data rate of the CX3 core or any of the device interfaces (including the CSI-2 Rx Port). The internal PLL applies the appropriate clock-multiply option depending on the input frequency.

Note: REFCLK and CLKIN must have either separate clock inputs or if the same source is used, the clock must be passed through a buffer with two outputs and then connected to the clock pins.

Table 3. CX3 Input Clock Specifications

Parameter	Description	Specification		Units
		Min	Max	
Phase noise	100-Hz offset	–	–75	dB
	1-kHz offset	–	–104	dB
	10-kHz offset	–	–120	dB
	100-kHz offset	–	–128	dB
	1-MHz offset	–	–130	dB
Maximum frequency deviation	–	–	150	ppm
Duty cycle	–	30	70	%
Overshoot	–	–	3	%
Undershoot	–	–	–3	%
Rise time/fall time	–	–	3	ns

32-kHz Watchdog Timer Clock Input

CX3 includes a watchdog timer. The watchdog timer can be used to interrupt the ARM926EJ-S core, automatically wake up the CX3 in Standby mode, and reset the ARM926EJ-S core. The watchdog timer runs a 32-kHz clock, which may be optionally supplied from an external source on a dedicated CX3 pin.

The firmware can disable the watchdog timer.

[Table 4](#) provides the requirements for the optional 32-kHz clock input

Table 4. 32-kHz Clock Input Requirements

Parameter	Min	Max	Units
Duty cycle	40	60	%
Frequency deviation	–	±200	ppm
Rise time/fall time	–	200	ns

Power

CX3 has the following power supply domains:

- **IO_VDDQ**: This is a group of independent supply domains for digital I/Os.
 - **V_{DDIO1}**: GPIO, I²C, JTAG, XRST, XSHUTDOWN and REF-CLK
 - **V_{DDIO2}**: UART and I²S (except MCLK)
 - **V_{DDIO3}**: I²S_MCLK and SPI
 - **C_{VDDQ}**: CLKIN
 - **V_{DD_MIPI}**: MIPI CSI-2 clock and data lanes
- **V_{DD}**: This is the supply voltage for the logic core. The nominal supply-voltage level is 1.2 V. This supplies the core logic circuits. The same supply must also be used for the following:
 - **A_{VDD}**: This is the 1.2-V supply for the PLL, crystal oscillator, and other core analog circuits.
 - **U3TXVDDQ/U3RXVDDQ**: These are the 1.2-V supply voltages for the USB 3.0 interface.
- **V_{USB}**: This is the 3.2-V to 6-V battery power supply for the USB I/O and analog circuits. This supply powers the USB transceiver through CX3's internal voltage regulator. V_{USB} is internally regulated to 3.3 V.

Note: The different power supplies have to be powered on or off in a specific sequence as illustrated in [Figure 4](#).

Power Modes

CX3 supports the following power modes:

- **Normal mode**: This is the full-functional operating mode. The internal CPU clock and the internal PLLs are enabled in this mode.
 - Normal operating power consumption does not exceed the sum of I_{CC} Core max and I_{CC} USB max (see [DC Specifications on page 17](#) for current consumption specifications).
 - The I/O power supplies V_{DDIO2} and V_{DDIO3} can be turned off when the corresponding interface is not in use. V_{DDIO1} should never be turned off for normal operation.
- **Low-power modes** (see [Table 5 on page 11](#)):
 - Suspend mode with USB 3.0 PHY enabled
 - Standby mode
 - Core power-down mode

Figure 4. Power-up Sequence

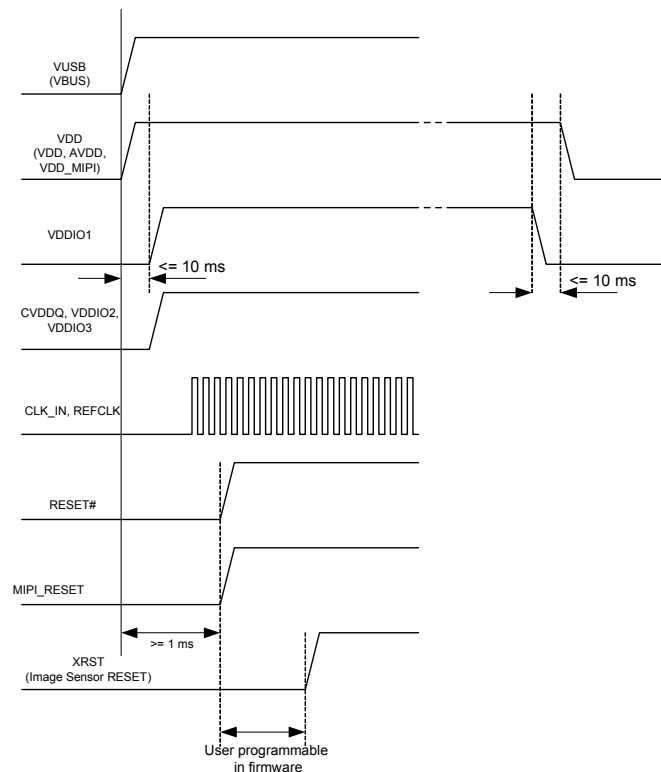


Table 5. Entry and Exit Methods for Low-Power Modes (continued)

Low-Power Mode	Characteristics	Methods of Entry	Methods of Exit
Core Power-down Mode	<ul style="list-style-type: none"> ■ The power consumption in this mode does not exceed ISB_4 ■ Core power is turned off ■ All buffer memory, configuration registers, and the program RAM do not maintain state. After exiting this mode, reload the firmware ■ In this mode, all other power domains can be turned on or off individually 	<ul style="list-style-type: none"> ■ Turn off V_{DD} 	<ul style="list-style-type: none"> ■ Reapply V_{DD} ■ Assertion of RESET#

Configuration Options

Configuration options are available for specific usage models. Contact Cypress Marketing (usb3@cypress.com) for details.

Digital I/Os

CX3 has internal firmware-controlled pull-up or pull-down resistors on all digital I/O pins. An internal 50-k Ω resistor pulls the pins high, while an internal 10-k Ω resistor pulls the pins low to prevent them from floating. The I/O pins may have the following states:

- Tristated (High-Z)
- Weak pull-up (via internal 50 k Ω)
- Pull-down (via internal 10 k Ω)
- Hold (I/O hold its value) when in low-power modes
- The JTAG TDI, TMC, and TRST# signals have fixed 50-k Ω internal pull-ups, and the TCK signal has a fixed 10-k Ω pull-down resistor.

All unused I/Os should be pulled high by using the internal pull-up resistors. All unused outputs should be left floating. All I/Os can be driven at full-strength, three-quarter strength, half-strength, or quarter-strength. These drive strengths are configured separately for each interface.

GPIOs

CX3 provides 12 pins for general purpose I/O (for example, can be used for lighting, sync-in, sync-out and so on). See [Pin Configuration on page 14](#) for pinout details.

All GPIO pins support an external load of up to 16 pF for every pin.

EMI

CX3 can meet EMI requirements outlined by FCC 15B (USA) and EN55022 (Europe) for consumer electronics at system level. CX3 can tolerate reasonable EMI, conducted by the aggressor, outlined by these specifications and continue to function as expected.

System-level ESD

CX3 has built-in ESD protection on the D+, D–, and GND pins on the USB interface. The ESD protection levels provided on these ports are:

- ± 2.2 -kV human body model (HBM) based on JESD22-A114 specification
- ± 6 -kV contact discharge and ± 8 -kV air gap discharge based on IEC61000-4-2 level 3A using external system-level protection devices
- ± 8 -kV contact discharge and ± 15 -kV air gap discharge based on IEC61000-4-2 level 4C using external system-level protection devices

This protection ensures that the device continues to function after ESD events up to the levels stated in this section.

The SSRX+, SSRX–, SSTX+, and SSTX– pins only have up to ± 2.2 -kV HBM internal ESD protection.

Pin Configuration

Figure 5. CX3 Ball Map (Top View)

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11
U3VSSQ	U3RXVDDQ	SSRXM	SSRXP	SSTXP	SSTXM	AVDD	VSS	DP	DM	GPIO[24]
B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11
VDDIO3	VSS	GPIO[23]	GPIO[21]	U3TXVDDQ	CVDDQ	AVSS	VSS	VSS	VDD	TRST#
C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	C11
SPI_SSN / GPIO[54]	SPI_MISO / GPIO[55]	VDD	GPIO[26]	RESET#	GPIO[18]	GPIO[19]	GPIO[22]	GPIO[45]	TDO	I2S_MCLK / GPIO[57]
D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11
I2S_CLK / GPIO[50]	I2S_SD / GPIO[51]	I2S_WS / GPIO[52]	SPI_SCK / GPIO[53]	SPI_MOSI / GPIO[56]	CLKIN_32	CLKIN	VSS	I2C_SCL	I2C_SDA	GPIO[17]
E1	E2	E3	E4	E5	E6	E7	E8	E9	E10	E11
UART_CTS / GPIO[47]	VSS	VDDIO2	UART_RX / GPIO[49]	UART_TX / GPIO[48]	GPIO[20]	TDI	TMS	VDD	VUSB	VSS
F1	F2	F3	F4	F5	F6	F7	F8	F9	F10	F11
DNU	REFCLK	GPIO[44]	XRST	UART_RTS / GPIO[46]	TCK	DNU	DNU	DNU	DNU	VDD
G1	G2	G3	G4	G5	G6	G7	G8	G9	G10	G11
VSS	XSHUTDOWN	MCLK	PMODE[0] / GPIO[30]	GPIO[25]	HSYNC_test	DNU	DNU	DNU	DNU	VSS
H1	H2	H3	H4	H5	H6	H7	H8	H9	H10	H11
VDD	DNU	DNU	PMODE[1] / GPIO[31]	VSYN_test	MIPI RESET	DNU	PCLK_test	DNU	DNU	VDDIO1
J1	J2	J3	J4	J5	J6	J7	J8	J9	J10	J11
DNU	DNU	DNU	DNU	MIPI_D0P	MIPI_D1P ¹	MIPI_CP	MIPI_D2P ^{1,2}	MIPI_D2N ^{1,2}	DNU	VDD
K1	K2	K3	K4	K5	K6	K7	K8	K9	K10	K11
DNU	DNU	VSS	VSS	MIPI_D0N	MIPI_D1N ¹	MIPI_CN	MIPI_D3N ^{1,2}	DNU	DNU	DNU
L1	L2	L3	L4	L5	L6	L7	L8	L9	L10	L11
VSS	VSS	VSS	PMODE[2] / GPIO[32]	VDD_MIPI	VSS	VDD	MIPI_D3P ^{1,2}	VDDIO1	DNU	VSS

1. Unused MIPI input data lanes to be connected to GND.

2. The signals MIPI_D2N, MIPI_D2P, MIPI_D3N, and MIPI_D3P are not available in the CYUSB3064 part. These pins should be left "open" in the customer board.

Legend

	Ground
	USB PHY power supply; Clock power supply
	Power supply

Table 6. CYUSB306X Pin List (continued)

CX3		
Pin#	Pin name	I/O
K7	MIPI_CN	I
J5	MIPI_D0P	I
K5	MIPI_D0N	I
J6	MIPI_D1P ¹	I
K6	MIPI_D1N ¹	I
J9	MIPI_D2N ^{1, 2}	I
J8	MIPI_D2P ^{1, 2}	I
L8	MIPI_D3P ^{1, 2}	I
K8	MIPI_D3N ^{1, 2}	I
CVDDQ Power Domain		
D7	CLKIN	I
D6	CLKIN_32	I
VDDIO1 Power Domain		
D9	I2C_SCL	I/O
D10	I2C_SDA	I/O
E7	TDI	I
C10	TDO	O
B11	TRST#	I
E8	TMS	I
F6	TCK	I
Power Domains		
E10	VUSB	PWR
A1	U3VSSQ	PWR
H11	VDDIO1	PWR
L9	VDDIO1	PWR
E3	VDDIO2	PWR
B1	VDDIO3	PWR
B6	CVDDQ	PWR
B5	U3TXVDDQ	PWR
A2	U3RXVDDQ	PWR
A7	AVDD	PWR
B7	AVSS	PWR
L5	VDD_MIPI	PWR
B10	VDD	PWR
J11	VDD	PWR
C3	VDD	PWR
E9	VDD	PWR
F11	VDD	PWR
H1	VDD	PWR

Table 6. CYUSB306X Pin List (continued)

CX3		
Pin#	Pin name	I/O
L7	VDD	PWR
D8	VSS	PWR
E2	VSS	PWR
E11	VSS	PWR
G1	VSS	PWR
A8	VSS	PWR
G11	VSS	PWR
L1	VSS	PWR
B8	VSS	PWR
L6	VSS	PWR
B2	VSS	PWR
L11	VSS	PWR
B9	VSS	PWR
K4	VSS	PWR
L3	VSS	PWR
K3	VSS	PWR
L2	VSS	PWR

1. Unused MIPI input data lanes to be connected to GND.
2. The signals MIPI_D2N, MIPI_D2P, MIPI_D3N, and MIPI_D3P are not available in the CYUSB3064 part. These pins should be left "open" in the customer board.

Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device.

Storage temperature -65 °C to +150 °C

Supply voltage to ground potential

V_{DD} , A_{VDDQ} 1.25 V

V_{DDIO1} , V_{DDIO2} , V_{DDIO3} 3.6 V

$U3TX_{VDDQ}$, $U3RX_{VDDQ}$ 1.25 V

DC input voltage to any input pin $V_{CC} + 0.3$

DC voltage applied to

outputs in high Z state

(V_{CC} is the corresponding I/O voltage) $V_{CC} + 0.3$

Maximum latch-up current 140 mA

Maximum output short-circuit current

for all I/O configurations. ($V_{OUT} = 0$ V) -100 mA

Operating Conditions

T_A (ambient temperature under bias)

Industrial -40 °C to +85 °C

V_{DD} , A_{VDDQ} , $U3TX_{VDDQ}$, $U3RX_{VDDQ}$

Supply voltage 1.15 V to 1.25 V

V_{USB} supply voltage 3.2 V to 6 V

V_{DDIO1} , V_{DDIO2} , V_{DDIO3} , C_{VDDQ}

Supply voltage 1.7 V to 3.6 V

DC Specifications

Parameter	Description	Min	Max	Units	Notes
V_{DD}	Core voltage supply	1.15	1.25	V	1.2-V typical
A_{VDD}	Analog voltage supply	1.15	1.25	V	1.2-V typical
V_{DD_MIPI}	MIPI bridge D-PHY supply voltage	1.15	1.25	V	1.2-V typical
V_{DDIO1}	I ² C, JTAG and GPIO power domain	1.7	3.6	V	1.8-, 2.5-, and 3.3-V typical
V_{DDIO2}	UART/I ² S power supply domain	1.7	3.6	V	1.8-, 2.5-, and 3.3-V typical
V_{DDIO3}	SPI/I ² S power supply domain	1.7	3.6	V	1.8-, 2.5-, and 3.3-V typical
V_{USB}	USB voltage supply	3.2	6	V	5-V typical
$U3TX_{VDDQ}$	USB 3.0 1.2-V supply	1.15	1.25	V	1.2-V typical. A 22-μF bypass capacitor is required on this power supply.
$U3RX_{VDDQ}$	USB 3.0 1.2-V supply	1.15	1.25	V	1.2-V typical. A 22-μF bypass capacitor is required on this power supply.
C_{VDDQ}	Clock voltage supply	1.7	3.6	V	1.8-, 3.3-V typical
V_{IH1}	Input HIGH voltage 1	$0.625 \times V_{CC}$	$V_{CC} + 0.3$	V	For $2.0 \text{ V} \leq V_{CC} \leq 3.6 \text{ V}$ (except USB and MIPI CSI-2 pins). V_{CC} is the corresponding I/O voltage supply.
V_{IH2}	Input HIGH voltage 2	$V_{CC} - 0.4$	$V_{CC} + 0.3$	V	For $1.7 \text{ V} \leq V_{CC} \leq 2.0 \text{ V}$ (except USB and MIPI CSI-2 pins). V_{CC} is the corresponding I/O voltage supply.
V_{IL}	Input LOW voltage	-0.3	$0.25 \times V_{CC}$	V	V_{CC} is the corresponding I/O voltage supply.
V_{OH}	Output HIGH voltage	$0.9 \times V_{CC}$	—	V	$I_{OH}(\text{max}) = -100 \mu\text{A}$ tested at quarter drive strength. V_{CC} is the corresponding I/O voltage supply.
V_{OL}	Output LOW voltage	—	$0.1 \times V_{CC}$	V	$I_{OL}(\text{min}) = +100 \mu\text{A}$ tested at quarter drive strength. V_{CC} is the corresponding I/O voltage supply.

Table 11. I²C Timing Parameters^[2] (continued)

Parameter	Description	Min	Max	Units
I²C Fast Mode Parameters				
f _{SCL}	SCL clock frequency	0	400	kHz
t _{HD:STA}	Hold time START condition	0.6	–	μs
t _{LOW}	LOW period of the SCL	1.3	–	μs
t _{HIGH}	HIGH period of the SCL	0.6	–	μs
t _{SU:STA}	Setup time for a repeated START condition	0.6	–	μs
t _{HD:DAT}	Data hold time	0	–	μs
t _{SU:DAT}	Data setup time	100	–	ns
t _r	Rise time of both SDA and SCL signals	–	300	ns
t _f	Fall time of both SDA and SCL signals	–	300	ns
t _{SU:STO}	Setup time for STOP condition	0.6	–	μs
t _{BUF}	Bus free time between a STOP and START condition	1.3	–	μs
t _{VD:DAT}	Data valid time	–	0.9	μs
t _{VD:ACK}	Data valid ACK	–	0.9	μs
t _{SP}	Pulse width of spikes that must be suppressed by input filter	0	50	ns
I²C Fast Mode Plus Parameters				
f _{SCL}	SCL clock frequency	0	1000	kHz
t _{HD:STA}	Hold time START condition	0.26	–	μs
t _{LOW}	LOW period of the SCL	0.5	–	μs
t _{HIGH}	HIGH period of the SCL	0.26	–	μs
t _{SU:STA}	Setup time for a repeated START condition	0.26	–	μs
t _{HD:DAT}	Data hold time	0	–	μs
t _{SU:DAT}	Data setup time	50	–	ns
t _r	Rise time of both SDA and SCL signals	–	120	ns
t _f	Fall time of both SDA and SCL signals	–	120	ns
t _{SU:STO}	Setup time for STOP condition	0.26	–	μs
t _{BUF}	Bus-free time between a STOP and START condition	0.5	–	μs
t _{VD:DAT}	Data valid time	–	0.45	μs
t _{VD:ACK}	Data valid ACK	–	0.55	μs
t _{SP}	Pulse width of spikes that must be suppressed by input filter	0	50	ns

I²S Timing Diagram

Figure 9. I²S Transmit Cycle

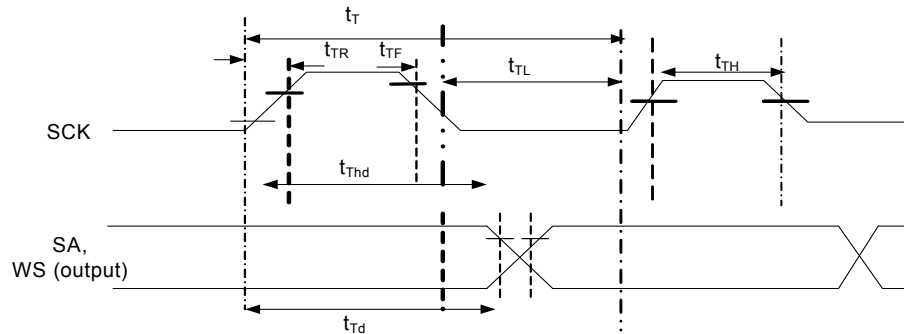


Table 12. I²S Timing Parameters^[3]

Parameter	Description	Min	Max	Units
t_T	I ² S transmitter clock cycle	t_{TR}	–	ns
t_{TL}	I ² S transmitter cycle LOW period	$0.35 t_{TR}$	–	ns
t_{TH}	I ² S transmitter cycle HIGH period	$0.35 t_{TR}$	–	ns
t_{TR}	I ² S transmitter rise time	–	$0.15 t_{TR}$	ns
t_{TF}	I ² S transmitter fall time	–	$0.15 t_{TR}$	ns
t_{Thd}	I ² S transmitter data hold time	0	–	ns
t_{Td}	I ² S transmitter delay time	–	$0.8 t_T$	ns

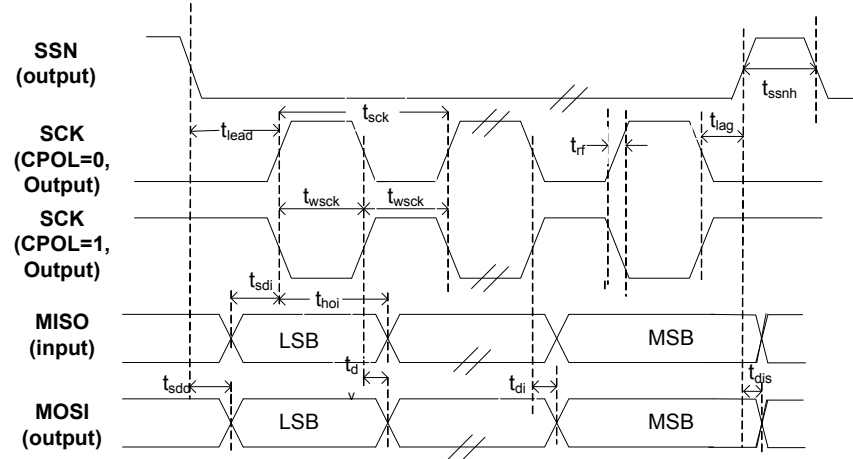
Note t_T is selectable through clock gears. Max t_{TR} is designed for 96-kHz codec at 32 bits to be 326 ns (3.072 MHz).

Note

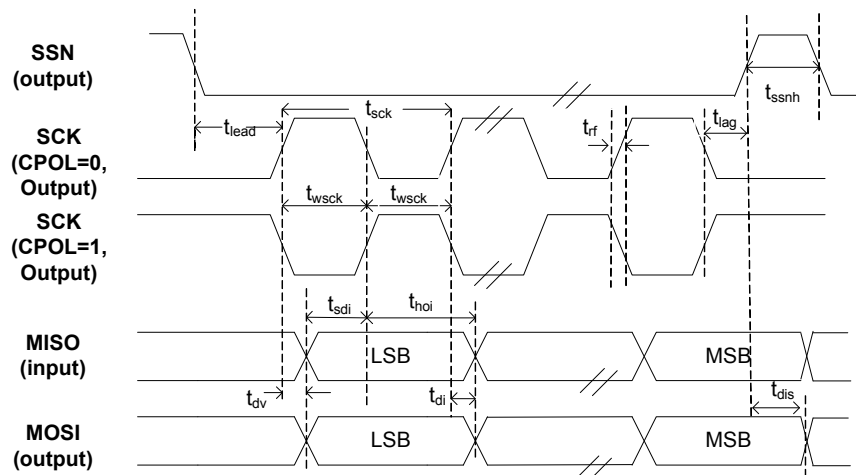
3. All parameters guaranteed by design and validated through characterization.

SPI Timing Specification

Figure 10. SPI Timing



SPI Master Timing for CPHA = 0



SPI Master Timing for CPHA = 1

Table 13. SPI Timing Parameters^[4]

Parameter	Description	Min	Max	Units
f_{op}	Operating frequency	0	33	MHz
t_{sck}	Cycle time	30	–	ns
t_{wsck}	Clock HIGH/LOW time	13.5	–	ns
t_{lead}	SSN-SCK lead time	$1/2 t_{sck}^{[5]} - 5$	$1.5 t_{sck}^{[5]} + 5$	ns
t_{lag}	Enable lag time	0.5	$1.5 t_{sck}^{[5]} + 5$	ns
t_{rf}	Rise/fall time	–	8	ns
t_{sdd}	Output SSN to valid data delay time	–	5	ns
t_{dv}	Output data valid time	–	5	ns
t_{di}	Output data invalid	0	–	ns
t_{ssnh}	Minimum SSN HIGH time	10	–	ns
t_{sdi}	Data setup time input	8	–	ns
t_{hoi}	Data hold time input	0	–	ns
t_{dis}	Disable data output on SSN HIGH	0	–	ns

Notes

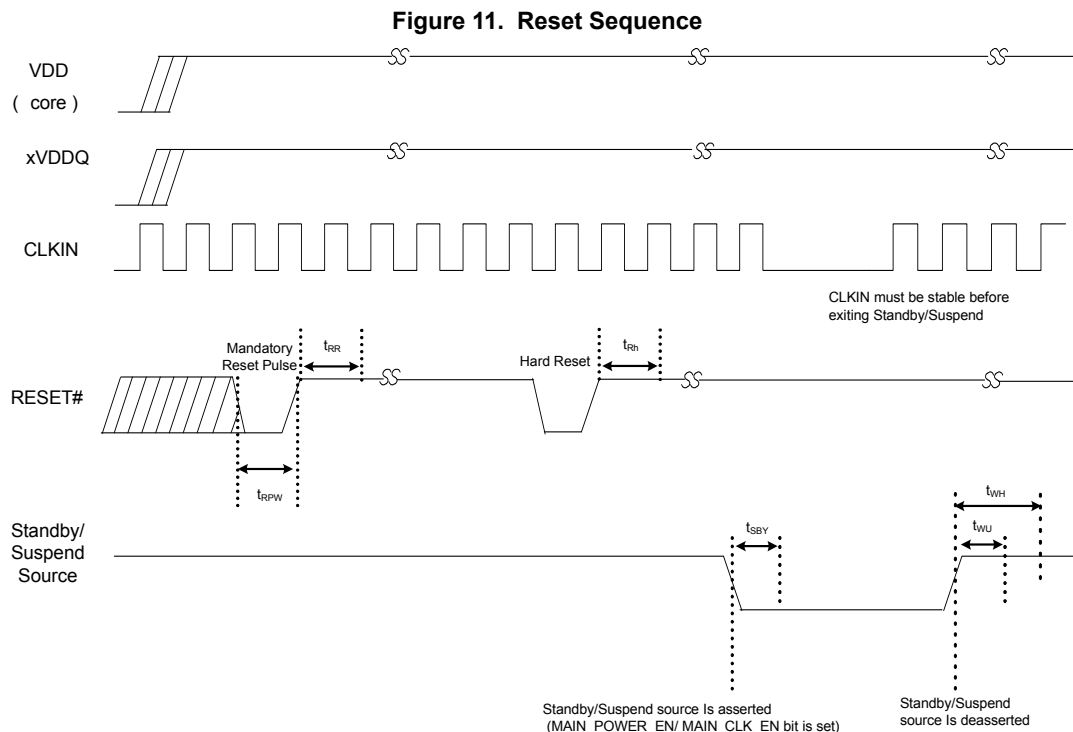
4. All parameters guaranteed by design and validated through characterization.
5. Depends on LAG and LEAD setting in the SPI_CONFIG register.

Reset Sequence

CX3's hard reset sequence requirements are specified in this section.

Table 14. Reset and Standby Timing Parameters

Parameter	Definition	Conditions	Min (ms)	Max (ms)
t_{RPW}	Minimum RESET# pulse width	Clock Input	1	–
t_{RH}	Minimum HIGH on RESET#	–	5	–
t_{RR}	Reset recovery time (after which the boot loader begins firmware download)	Clock Input	1	–
t_{SBY}	Time to enter standby/suspend mode (from the time MAIN_CLOCK_EN/ MAIN_POWER_EN bit is set)	–	–	1
t_{WU}	Time to wakeup from standby	Clock Input	1	–
t_{WH}	Minimum time before standby/suspend source may be reasserted	–	5	–

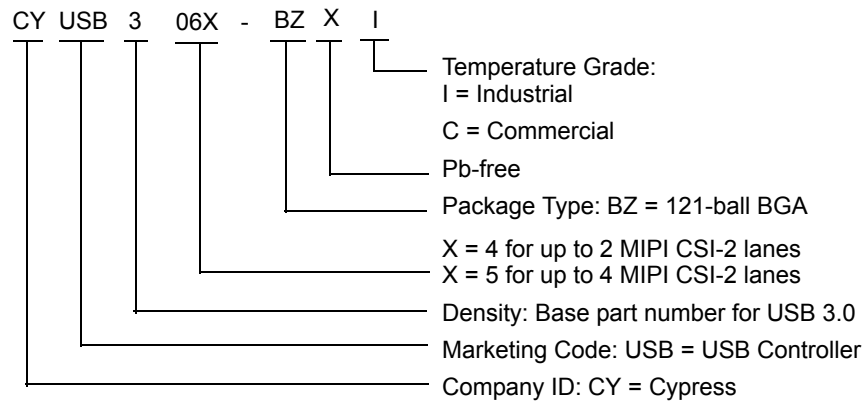


Ordering Information

Table 15. Ordering Information

Ordering Code	MIPI CSI-2 Lanes	Package Type	Temperature Grade
CYUSB3065-BZXI	4	121-ball BGA	Industrial
CYUSB3065-BZXC	4	121-ball BGA	Commercial
CYUSB3064-BZXI	2	121-ball BGA	Industrial
CYUSB3064-BZXC	2	121-ball BGA	Commercial

Ordering Code Definitions



Document History Page

Document Title: CYUSB306X, EZ-USB® CX3: MIPI CSI-2 to SuperSpeed USB Bridge Controller Document Number: 001-87516				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	3994736	KUMR	05/09/2013	New datasheet
*A	4065766	KUMR	07/17/2013	Updated Logic Block Diagram . Updated Pin Description . Updated DC Specifications . Replaced "VBUS" and "VBATT" by "VUSB" in all instances across the document. Updated in new template.
*B	4080302	KUMR	07/29/2013	Updated status as "Preliminary".
*C	4088328	KUMR	08/06/2013	Updated Pin Configuration (Updated Figure).
*D	4113754	KUMR	09/04/2013	Updated Clocking : Added a Note at the bottom of section. Updated Pin Description . Updated Table 6 . Updated DC Specifications : Updated description of V_{DDIO2} parameter. Updated description of V_{DDIO3} parameter. Changed maximum value of I_{CC} Core parameter from 200 mA to 380 mA.
*E	4188453	KUMR	11/14/2013	Changed status from Preliminary to Final. Updated Features : Updated description. Updated Applications : Updated description. Updated Logic Block Diagram . Updated Functional Overview . Updated MIPI CSI-2 RX Interface . Updated Additional Outputs : Updated description. Updated Reset . Updated Soft Reset : Updated description. Updated Power . Updated Power Modes . Updated Table 5 . Updated "Methods of Entry" corresponding to "Suspend Mode with USB 3.0 PHY Enabled". Updated "Characteristics" corresponding to "Standby Mode". Updated EMI : Updated description. Updated System-level ESD : Updated description. Updated Pin Configuration : Updated details of G4, H4, L4, F1, F5, E1, E5, E4, D1, D2, D3, D4, C1, C2, D5, C11 pins in Figure . Updated Pin Description . Updated details in "Pin name" column for G4, H4, L4, F1, F5, E1, E5, E4, D1, D2, D3, D4, C1, C2, D5, C11 pins. Updated Absolute Maximum Ratings : Removed "Ambient temperature with power applied". Removed "Static discharge voltage ESD protection levels". Renamed "Latch-up current" as "Maximum latch-up current" and updated the values. Updated DC Specifications : Updated details in "Notes" column corresponding to V_{IH1} and V_{IH2} parameters. Updated description of I_{OZ} parameter. Updated minimum value of I_{SB1} and I_{SB3} parameters. Updated details in "Notes" column corresponding to I_{SB1} and I_{SB3} parameters. Added MIPI D-PHY Electrical Characteristics . Updated AC Timing Parameters . Updated MIPI Data to Clock Timing Reference .