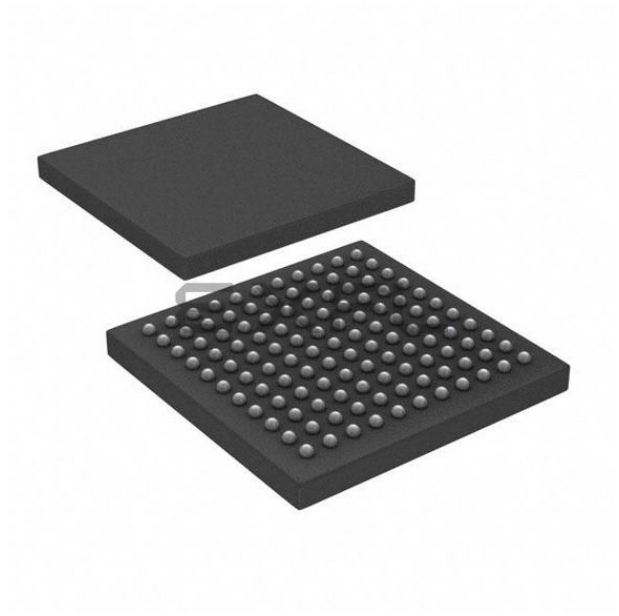

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## Embedded - Microcontrollers - Application Specific: Tailored Solutions for Precision and Performance

Embedded - Microcontrollers - Application Specific represents a category of microcontrollers designed with unique features and capabilities tailored to specific application needs. Unlike general-purpose microcontrollers, application-specific microcontrollers are optimized for particular tasks, offering enhanced performance, efficiency, and functionality to meet the demands of specialized applications.

## What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

| Details | |
|---|---|
| Product Status | Active |
| Applications | USB Host/Peripheral Controller |
| Core Processor | ARM9® |
| Program Memory Type | External Program Memory |
| Controller Series | CYUSB |
| RAM Size | 512K x 8 |
| Interface | GPIF, I²C, I²S, SPI, UART, USB |
| Number of I/O | 12 |
| Voltage - Supply | 1.15V ~ 1.25V |
| Operating Temperature | -40°C ~ 85°C |
| Mounting Type | Surface Mount |
| Package / Case | 121-LFBGA |
| Supplier Device Package | 121-BGA (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/cyusb3065-bzxi |

## Functional Overview

Cypress's EZ-USB CX3 is the next-generation bridge controller that can connect devices with the Mobile Industry Processor Interface – Camera Serial Interface 2 (MIPI CSI-2) interface to any USB 3.0 Host.

CX3 has a 4-lane CSI-2 receiver with up to 1 Gbps on each lane. It supports video data formats such as RAW8/10/12/14, YUV422 (CCIR/ITU 8/10-bit), RGB888/666/565, and user-defined 8-bit.

CX3 has integrated the USB 3.0 and USB 2.0 physical layers (PHYs) along with a 32-bit ARM926EJ-S microprocessor for powerful data processing and for building custom applications.

CX3 contains 512 KB of on-chip SRAM (see Ordering Information on page 27) for code and data. EZ-USB CX3 also provides interfaces to connect to serial peripherals such as UART, SPI, $I^2C$, and $I^2S$.

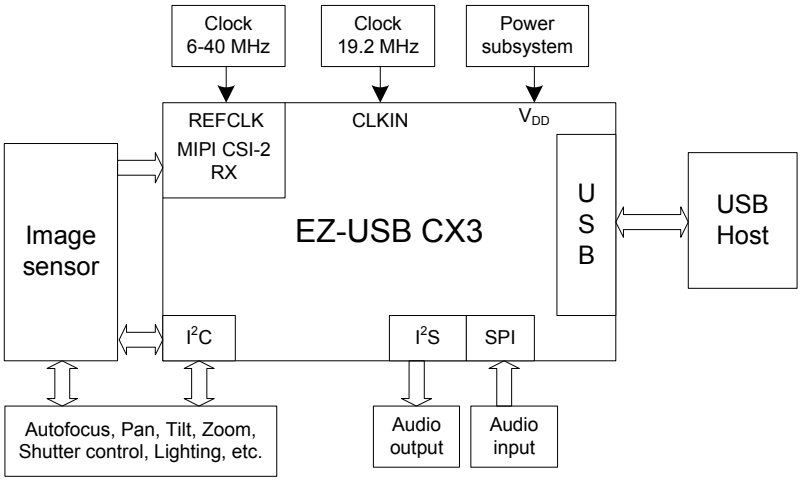
CX3 comes with application development tools. The software development kit comes with application examples for accelerating time-to-market.

CX3 complies with the USB 3.0 v1.0 specification and is also backward compatible with USB 2.0. It also complies with the MIPI CSI-2 v1.01, revision 0.04 specification dated 2nd April 2009.

### Application Examples

In a typical application (see Figure 1), CX3 acts as the main processor and connects to an image sensor, an audio device, or camera control devices amongst others.

**Figure 1. EZ-USB CX3 Example Application**

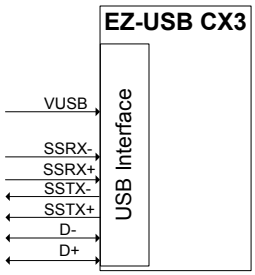


## USB Interface

CX3 complies with the following specifications and supports the following features:

- Supports USB peripheral functionality compliant with USB 3.0 Specification, Revision 1.0, and is also backward compatible with the USB 2.0 Specification.
- As a peripheral, CX3 is capable of SuperSpeed, High-Speed, and Full-Speed.
- Supports up to 16 IN and 16 OUT endpoints
- Supports the USB 3.0 Streams feature
- As a USB peripheral, CX3 supports USB-attached storage (UAS), USB Video Class (UVC), and Media Transfer Protocol (MTP) USB peripheral classes. As a USB peripheral, all other device classes are supported only in pass-through mode when handled entirely by a host processor external to the device.

**Figure 2. USB Interface Signals**




### ReNumeration

Because of CX3's soft configuration, one chip can take on the identities of multiple distinct USB devices.

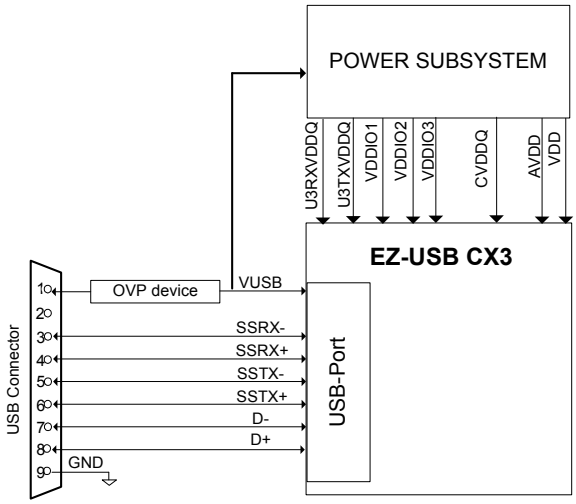
When first plugged into USB, CX3 enumerates automatically with the Cypress Vendor ID (0x04B4) and downloads the firmware and USB descriptors over the USB interface. The downloaded firmware executes an electrical disconnect and connect. CX3 enumerates again, this time as a device defined by the downloaded information. This patented two-step process, called ReNumeration, happens instantly when the device is plugged in.

### VBUS Overvoltage Protection

The maximum input voltage on CX3's VUSB pin is 6 V. A charger can supply up to 9 V on VUSB. In this case, an external overvoltage protection (OVP) device is required to protect CX3 from damage on VUSB. Figure 3 shows the system application diagram with an OVP device connected on VUSB. Refer to DC Specifications on page 17 for the operating range of VUSB.

**Note:** The VBUS pin of the USB connector should be connected to the VUSB pin of CX3.

**Figure 3. System Diagram with OVP Device For VUSB**



The $I^2C$ controller supports bus frequencies of 400 kHz, and 1 MHz. When $V_{DDIO1}$ is 1.8 V, 2.5 V, or 3.3 V, the operating frequencies supported are 400 kHz and 1 MHz. The $I^2C$ controller supports the clock-stretching feature to enable slower devices to exercise flow control.

The $I^2C$ interface's SCL and SDA signals require external pull-up resistors. The pull-up resistors must be connected to $V_{DDIO1}$.

**Note:** $I^2C$ addresses with the pattern 0x0000111x are used internally and no slave devices with those addresses should be connected to the bus.

### $I^2S$ Interface

CX3 has an $I^2S$ port to support external audio codec devices. CX3 functions as $I^2S$ Master as transmitter only. The $I^2S$ interface consists of four signals: clock line (I2S_CLK), serial data line (I2S_SD), word select line (I2S_WS), and master system clock (I2S_MCLK). CX3 can generate the system clock as an output on I2S_MCLK or accept an external system clock input on I2S_MCLK.

The sampling frequencies supported by the $I^2S$ interface are 32 kHz, 44.1 kHz, and 48 kHz.

### SPI Interface

CX3 supports an SPI Master interface on the Serial Peripherals port. The maximum operation frequency is 33 MHz.

The SPI controller supports four modes of SPI communication (see SPI Timing Specification on page 24 for details on the modes) with the Start-Stop clock. This controller is a single-master controller with a single automated SSN control. It supports transaction sizes ranging from 4 bits to 32 bits.

## Boot Options

CX3 can load boot images from various sources, selected by the configuration of the PMODE pins. Following are the CX3 boot options:

- Boot from USB
- Boot from $I^2C$
- Boot from SPI (SPI devices supported are M25P16 (16 Mbit), M25P80 (8 Mbit), and M25P40 (4 Mbit)) or their equivalents

**Table 2. CX3 Booting Options**

| PMODE[2:0][1] | Boot From |
|---|---|
| F11 | USB boot |
| F1F | $I^2C$, On failure, USB boot is enabled |
| 1FF | $I^2C$ only |
| 0F1 | SPI, On failure, USB boot is enabled |

## Reset

### Hard Reset

A hard reset is initiated by asserting the RESET# pin on CX3. The specific reset sequence and timing requirements are detailed in Figure 11 on page 26 and Table 14 on page 26. All I/Os are tristated during a hard reset.

An additional reset pin called MIPI_RESET is provided that resets the MIPI CSI-2 core. It should be pulled down with a resistor for normal operation.

### Soft Reset

There are two types of Soft Reset:

- CPU Reset – The CPU Program Counter is reset. Firmware does not need to be reloaded following a CPU Reset.
- Whole Device Reset – This reset is identical to Hard Reset. The firmware must be reloaded following a Whole Device Reset.

**Note**
1. F indicates Floating.

## Clocking

CX3 requires two clocks for normal operation:

1. A 19.2-MHz clock to be connected at the CLKIN pin
2. A 6-MHz to 40-MHz clock to be connected at the REFCLK pin

Clock inputs to CX3 must meet the phase noise and jitter requirements specified in Table 3 on page 9.

The input clock frequency is independent of the clock and data rate of the CX3 core or any of the device interfaces (including the CSI-2 Rx Port). The internal PLL applies the appropriate clock-multiply option depending on the input frequency.

**Note:** REFCLK and CLKIN must have either separate clock inputs or if the same source is used, the clock must be passed through a buffer with two outputs and then connected to the clock pins.

**Table 3. CX3 Input Clock Specifications**

| Parameter | Description | Specification | | Units |
|---|---|---|---|---|
| | | Min | Max | |
| Phase noise | 100-Hz offset | – | –75 | dB |
| | 1-kHz offset | – | –104 | dB |
| | 10-kHz offset | – | –120 | dB |
| | 100-kHz offset | – | –128 | dB |
| | 1-MHz offset | – | –130 | dB |
| Maximum frequency deviation | – | – | 150 | ppm |
| Duty cycle | – | 30 | 70 | % |
| Overshoot | – | – | 3 | % |
| Undershoot | – | – | –3 | % |
| Rise time/fall time | – | – | 3 | ns |

### 32-kHz Watchdog Timer Clock Input

CX3 includes a watchdog timer. The watchdog timer can be used to interrupt the ARM926EJ-S core, automatically wake up the CX3 in Standby mode, and reset the ARM926EJ-S core. The watchdog timer runs a 32-kHz clock, which may be optionally supplied from an external source on a dedicated CX3 pin.

The firmware can disable the watchdog timer.

Table 4 provides the requirements for the optional 32-kHz clock input

**Table 4. 32-kHz Clock Input Requirements**

| Parameter | Min | Max | Units |
|---|---|---|---|
| Duty cycle | 40 | 60 | % |
| Frequency deviation | – | ±200 | ppm |
| Rise time/fall time | – | 200 | ns |

## Power

CX3 has the following power supply domains:

- **IO_VDDQ**: This is a group of independent supply domains for digital I/Os.
  - **$V_{DDIO1}$**: GPIO, $I^2C$, JTAG, XRST, XSHUTDOWN and REFCLK
  - **$V_{DDIO2}$**: UART and $I^2S$ (except MCLK)
  - **$V_{DDIO3}$**: $I^2S$_MCLK and SPI
  - **$C_{VDDQ}$**: CLKIN
  - **$V_{DD\_MIPI}$**: MIPI CSI-2 clock and data lanes
- **$V_{DD}$**: This is the supply voltage for the logic core. The nominal supply-voltage level is 1.2 V. This supplies the core logic circuits. The same supply must also be used for the following:
  - **$A_{VDD}$**: This is the 1.2-V supply for the PLL, crystal oscillator, and other core analog circuits.
  - **U3TXVDDQ/U3RXVDDQ**: These are the 1.2-V supply voltages for the USB 3.0 interface.
- **VUSB**: This is the 3.2-V to 6-V battery power supply for the USB I/O and analog circuits. This supply powers the USB transceiver through CX3's internal voltage regulator. VUSB is internally regulated to 3.3 V.

**Note**: The different power supplies have to be powered on or off in a specific sequence as illustrated in Figure 4.

### Power Modes

CX3 supports the following power modes:

- Normal mode: This is the full-functional operating mode. The internal CPU clock and the internal PLLs are enabled in this mode.
  - Normal operating power consumption does not exceed the sum of $I_{CC}$ Core max and $I_{CC}$ USB max (see DC Specifications on page 17 for current consumption specifications).
  - The I/O power supplies $V_{DDIO2}$ and $V_{DDIO3}$ can be turned off when the corresponding interface is not in use. $V_{DDIO1}$ should never be turned off for normal operation.
- Low-power modes (see Table 5 on page 11):
  - Suspend mode with USB 3.0 PHY enabled
  - Standby mode
  - Core power-down mode

**Figure 4. Power-up Sequence**

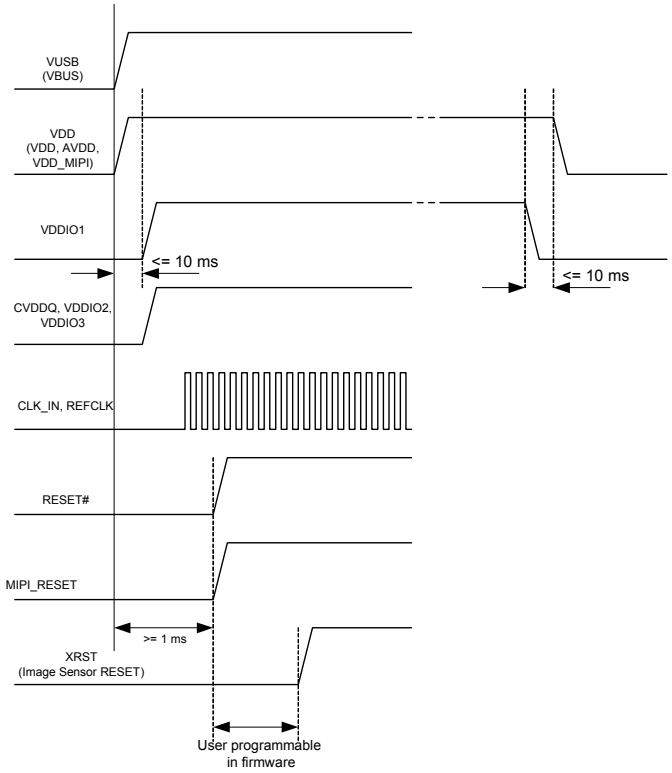


**Table 5. Entry and Exit Methods for Low-Power Modes**

| Low-Power Mode | Characteristics | Methods of Entry | Methods of Exit |
|---|---|---|---|
| Suspend Mode with USB 3.0 PHY Enabled | ■ Power consumption in this mode does not exceed $I_{SB1}$<br>■ USB 3.0 PHY is enabled and is in U3 mode (one of the suspend modes defined by the USB 3.0 specification). This one block alone is operational with its internal clock, while all other clocks are shut down<br>■ All I/Os maintain their previous state<br>■ Power supply for the wakeup source and core power must be retained. All other power domains can be turned on or off individually<br>■ The states of the configuration registers, buffer memory, and all internal RAM are maintained<br>■ All transactions must be completed before CX3 enters suspend mode (state of outstanding transactions are not preserved)<br>■ The firmware resumes operation from where it was suspended (except when woken up by RESET# assertion) because the program counter does not reset | ■ Firmware executing on ARM926EJ-S core can put CX3 into the suspend mode. For example, on USB suspend condition, the firmware may decide to put CX3 into suspend mode | ■ D+ transitioning to low or high<br>■ D- transitioning to low or high<br>■ Resume condition on SSRX±<br>■ Detection of VBUS<br>■ Level detect on UART_CTS (programmable polarity)<br>■ Assertion of RESET# |
| Standby Mode | ■ The power consumption in this mode does not exceed ISB3<br>■ All configuration register settings and program/data RAM contents are preserved. However, data in the buffers or other parts of the data path, if any, is not guaranteed. Therefore, the external processor should take care that the data needed is read before putting CX3 into the standby mode<br>■ The program counter is reset after waking up from the standby mode<br>■ GPIO pins maintain their configuration<br>■ Internal PLL is turned off<br>■ USB transceiver is turned off<br>■ ARM926EJ-S core is powered down. Upon wakeup, the core re-starts and runs the program stored in the program/data RAM<br>■ Power supply for the wakeup source and core power must be retained. All other power domains can be turned on or off individually | ■ The firmware executing on ARM926EJ-S core or external processor configures the appropriate register | ■ Detection of VBUS<br>■ Level detect on UART_CTS (programmable polarity)<br>■ Assertion of RESET# |

**Table 5. Entry and Exit Methods for Low-Power Modes** (continued)

| Low-Power Mode | Characteristics | Methods of Entry | Methods of Exit |
|---|---|---|---|
| Core Power-down Mode | ■ The power consumption in this mode does not exceed $ISB_4$<br>■ Core power is turned off<br>■ All buffer memory, configuration registers, and the program RAM do not maintain state. After exiting this mode, reload the firmware<br>■ In this mode, all other power domains can be turned on or off individually | ■ Turn off $V_{DD}$ | ■ Reapply $V_{DD}$<br>■ Assertion of RESET# |

## Configuration Options

Configuration options are available for specific usage models. Contact Cypress Marketing (usb3@cypress.com) for details.

## Digital I/Os

CX3 has internal firmware-controlled pull-up or pull-down resistors on all digital I/O pins. An internal 50-kΩ resistor pulls the pins high, while an internal 10-kΩ resistor pulls the pins low to prevent them from floating. The I/O pins may have the following states:

- Tristated (High-Z)
- Weak pull-up (via internal 50 kΩ)
- Pull-down (via internal 10 kΩ)
- Hold (I/O hold its value) when in low-power modes
- The JTAG TDI, TMC, and TRST# signals have fixed 50-kΩ internal pull-ups, and the TCK signal has a fixed 10-kΩ pull-down resistor.

All unused I/Os should be pulled high by using the internal pull-up resistors. All unused outputs should be left floating. All I/Os can be driven at full-strength, three-quarter strength, half-strength, or quarter-strength. These drive strengths are configured separately for each interface.

## GPIOs

CX3 provides 12 pins for general purpose I/O (for example, can be used for lighting, sync-in, sync-out and so on). See Pin Configuration on page 14 for pinout details.

All GPIO pins support an external load of up to 16 pF for every pin.

## EMI

CX3 can meet EMI requirements outlined by FCC 15B (USA) and EN55022 (Europe) for consumer electronics at system level. CX3 can tolerate reasonable EMI, conducted by the aggressor, outlined by these specifications and continue to function as expected.

## System-level ESD

CX3 has built-in ESD protection on the D+, D–, and GND pins on the USB interface. The ESD protection levels provided on these ports are:

- ±2.2-kV human body model (HBM) based on JESD22-A114 specification
- ±6-kV contact discharge and ±8-kV air gap discharge based on IEC61000-4-2 level 3A using external system-level protection devices
- ± 8-kV contact discharge and ±15-kV air gap discharge based on IEC61000-4-2 level 4C using external system-level protection devices

This protection ensures that the device continues to function after ESD events up to the levels stated in this section.

The SSRX+, SSRX–, SSTX+, and SSTX– pins only have up to ±2.2-kV HBM internal ESD protection.

## Pin Configuration

**Figure 5. CX3 Ball Map (Top View)**

| A1 | A2 | A3 | A4 | A5 | A6 | A7 | A8 | A9 | A10 | A11 |
|---|---|---|---|---|---|---|---|---|---|---|
| U3VSSQ | U3RXVDDQ | SSRXM | SSRXP | SSTXP | SSTXM | AVDD | VSS | DP | DM | GPIO[24] |
| **B1** | **B2** | **B3** | **B4** | **B5** | **B6** | **B7** | **B8** | **B9** | **B10** | **B11** |
| VDDIO3 | VSS | GPIO[23] | GPIO[21] | U3TXVDDQ | CVDDQ | AVSS | VSS | VSS | VDD | TRST# |
| **C1** | **C2** | **C3** | **C4** | **C5** | **C6** | **C7** | **C8** | **C9** | **C10** | **C11** |
| SPI_SSN / GPIO[54] | SPI_MISO / GPIO[55] | VDD | GPIO[26] | RESET# | GPIO[18] | GPIO[19] | GPIO[22] | GPIO[45] | TDO | I2S_MCLK / GPIO[57] |
| **D1** | **D2** | **D3** | **D4** | **D5** | **D6** | **D7** | **D8** | **D9** | **D10** | **D11** |
| I2S_CLK / GPIO[50] | I2S_SD / GPIO[51] | I2S_WS / GPIO[52] | SPI_SCK / GPIO[53] | SPI_MOSI / GPIO[56] | CLKIN_32 | CLKIN | VSS | I2C_SCL | I2C_SDA | GPIO[17] |
| **E1** | **E2** | **E3** | **E4** | **E5** | **E6** | **E7** | **E8** | **E9** | **E10** | **E11** |
| UART_CTS / GPIO[47] | VSS | VDDIO2 | UART_RX / GPIO[49] | UART_TX / GPIO[48] | GPIO[20] | TDI | TMS | VDD | VUSB | VSS |
| **F1** | **F2** | **F3** | **F4** | **F5** | **F6** | **F7** | **F8** | **F9** | **F10** | **F11** |
| DNU | REFCLK | GPIO[44] | XRST | UART_RTS / GPIO[46] | TCK | DNU | DNU | DNU | DNU | VDD |
| **G1** | **G2** | **G3** | **G4** | **G5** | **G6** | **G7** | **G8** | **G9** | **G10** | **G11** |
| VSS | XSHUTDOWN | MCLK | PMODE[0] / GPIO[30] | GPIO[25] | HSYNC_test | DNU | DNU | DNU | DNU | VSS |
| **H1** | **H2** | **H3** | **H4** | **H5** | **H6** | **H7** | **H8** | **H9** | **H10** | **H11** |
| VDD | DNU | DNU | PMODE[1] / GPIO[31] | VSYNC_test | MIPI RESET | DNU | PCLK_test | DNU | DNU | VDDIO1 |
| **J1** | **J2** | **J3** | **J4** | **J5** | **J6** | **J7** | **J8** | **J9** | **J10** | **J11** |
| DNU | DNU | DNU | DNU | MIPI_D0P | MIPI_D1P[1] | MIPI_CP | MIPI_D2P[1, 2] | MIPI_D2N[1, 2] | DNU | VDD |
| **K1** | **K2** | **K3** | **K4** | **K5** | **K6** | **K7** | **K8** | **K9** | **K10** | **K11** |
| DNU | DNU | VSS | VSS | MIPI_D0N | MIPI_D1N[1] | MIPI_CN | MIPI_D3N[1, 2] | DNU | DNU | DNU |
| **L1** | **L2** | **L3** | **L4** | **L5** | **L6** | **L7** | **L8** | **L9** | **L10** | **L11** |
| VSS | VSS | VSS | PMODE[2] / GPIO[32] | VDD_MIPI | VSS | VDD | MIPI_D3P[1, 2] | VDDIO1 | DNU | VSS |

1. Unused MIPI input data lanes to be connected to GND.
2. The signals MIPI_D2N, MIPI_D2P, MIPI_D3N, and MIPI_D3P are not available in the CYUSB3064 part. These pins should be left "open" in the customer board.

Legend

- Ground
- USB PHY power supply; Clock power supply
- Power supply

## Pin Description

**Table 6. CYUSB306X Pin List**

| CX3 | | |
|---|---|---|
| **Pin#** | **Pin name** | **I/O** |
| F10 | DNU | I/O |
| F9 | DNU | I/O |
| F7 | DNU | I/O |
| G10 | DNU | I/O |
| G9 | DNU | I/O |
| F8 | DNU | I/O |
| H10 | DNU | I/O |
| H9 | DNU | I/O |
| J10 | DNU | I/O |
| H7 | DNU | I/O |
| K11 | DNU | I/O |
| L10 | DNU | I/O |
| K10 | DNU | I/O |
| K9 | DNU | I/O |
| G7 | DNU | I/O |
| G8 | DNU | I/O |
| K2 | DNU | I/O |
| J4 | DNU | I/O |
| K1 | DNU | I/O |
| J2 | DNU | I/O |
| J3 | DNU | I/O |
| J1 | DNU | I/O |
| H2 | DNU | I/O |
| H3 | DNU | I/O |
| G6 | HSYNC_test | I/O |
| H5 | VSYNC_test | I/O |
| H8 | PCLK_test | I/O |
| **VDDIO1 Power Domain** | | |
| D11 | GPIO[17] | I/O |
| C6 | GPIO[18] | I/O |
| C7 | GPIO[19] | I/O |
| E6 | GPIO[20] | I/O |
| B4 | GPIO[21] | I/O |
| C8 | GPIO[22] | I/O |
| B3 | GPIO[23] | I/O |
| A11 | GPIO[24] | I/O |
| G5 | GPIO[25] | I/O |

**Table 6. CYUSB306X Pin List** (continued)

| CX3 | | |
|---|---|---|
| **Pin#** | **Pin name** | **I/O** |
| C4 | GPIO[26] | I/O |
| F3 | GPIO[44] | I/O |
| C9 | GPIO[45] | I/O |
| G4 | PMODE[0] / GPIO[30] | I/O |
| H4 | PMODE[1] / GPIO[31] | I/O |
| L4 | PMODE[2] / GPIO[32] | I/O |
| F1 | DNU | I/O |
| H6 | MIPI RESET | I/O |
| C5 | RESET# | I |
| F4 | XRST | O |
| G2 | XSHUTDOWN | O |
| G3 | MCLK | O |
| **VDDIO2 Power Domain** | | |
| F5 | UART_RTS / GPIO[46] | I/O |
| E1 | UART_CTS / GPIO[47] | I/O |
| E5 | UART_TX / GPIO[48] | I/O |
| E4 | UART_RX / GPIO[49] | I/O |
| D1 | I2S_CLK / GPIO[50] | I/O |
| D2 | I2S_SD / GPIO[51] | I/O |
| D3 | I2S_WS / GPIO[52] | I/O |
| **VDDIO3 Power Domain** | | |
| D4 | SPI_SCK / GPIO[53] | I/O |
| C1 | SPI_SSN / GPIO[54] | I/O |
| C2 | SPI_MISO / GPIO[55] | I/O |
| D5 | SPI_MOSI / GPIO[56] | I/O |
| C11 | I2S_MCLK / GPIO[57] | I/O |
| **USB Port (U3TXVDDQ/U3RXVDDQ Power Domain)** | | |
| A3 | SSRXM | I |
| A4 | SSRXP | I |
| A6 | SSTXM | O |
| A5 | SSTXP | O |
| **USB Port (VUSB Power Domain)** | | |
| A9 | DP | I/O |
| A10 | DM | I/O |
| **VDDIO1 Power Domain** | | |
| F2 | REFCLK | I |
| **VDD_MIPI Power Domain** | | |
| J7 | MIPI_CP | I |

## DC Specifications (continued)

| Parameter | Description | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| $I_{IX}$ | Input leakage current for all pins except SSTXP/SSXM/SSRXP/SSRXM | –1 | 1 | µA | All I/O signals held at $V_{DDQ}$ (For I/Os with a pull-up or pull-down resistor connected, the leakage current increases by $V_{DDQ}/R_{PU}$ or $V_{DDQ}/R_{PD}$) |
| $I_{OZ}$ | Output High-Z leakage current for all pins except SSTXP/ SSXM/ SSRXP/SSRXM and MIPI CSI-2 signals | –1 | 1 | µA | All I/O signals held at $V_{DDQ}$ |
| $I_{CC}$ Core | Core and analog voltage operating current | – | 192 | mA | Total current through $A_{VDD}$, $V_{DD}$ |
| $I_{CC}$ USB | USB voltage supply operating current | – | 60 | mA | – |
| $I_{SB1}$ | Total suspend current during suspend mode with USB 3.0 PHY enabled | Core: 558.35 µA | – | µA | Core Current is measured through $V_{DD}$, $A_{VDD}$ and $V_{DD\_MIPI}$.<br>I/O Current is measured through $V_{DDIO1}$ to $V_{DDIO3}$.<br>USB Current is measured through $V_{USB}$, $U3TX_{VDDQ}$ and $U3RX_{VDDQ}$. |
| | | I/O: 4.58 µA | – | µA | |
| | | USB: 4672 µA | – | µA | |
| $I_{SB3}$ | Total standby current during core power-down mode | Core: 148.31 µA | – | µA | |
| | | I/O: 3.16 µA | – | µA | |
| | | USB: 15.8 µA | – | µA | |
| $V_{RAMP}$ | Voltage ramp rate on core and I/O supplies | 0.2 | 12 | V/ms | Voltage ramp must be monotonic |
| $V_N$ | Noise level permitted on $V_{DD}$ and I/O supplies | – | 100 | mV | Max p-p noise level permitted on all supplies except $A_{VDD}$ |
| $V_{N\_AVDD}$ | Noise level permitted on $A_{VDD}$ supply | – | 20 | mV | Max p-p noise level permitted on $A_{VDD}$ |

## MIPI D-PHY Electrical Characteristics

| Parameter | Description | Spec | | | Unit |
|---|---|---|---|---|---|
| | | Min | Nom | Max | |
| **MIPI D-PHY RX DC Characteristics** | | | | | |
| $V_{PIN}$ | Pin signal voltage range | –50 | – | 1350 | mV |
| $V_{IH}$ | Logic 1 input voltage | 880 | – | – | mV |
| $V_{IL}$ | Logic 0 input voltage | – | – | 550 | mV |
| $V_{CMRX\ (DC)}$ | Common-mode voltage HS receiver mode | 70 | – | 330 | mV |
| $V_{IDTH}$ | Differential input high threshold | | – | 70 | mV |
| $V_{IDTL}$ | Differential input low threshold | –70 | – | – | mV |
| $V_{IHHS}$ | Single-ended input high voltage | | – | 460 | mV |
| $V_{ILHS}$ | Single-ended input low voltage | –40 | – | – | mV |

## AC Timing Parameters

### MIPI Data to Clock Timing Reference

**Figure 6. MIPI CSI Signal Data to Clock Timing Reference**

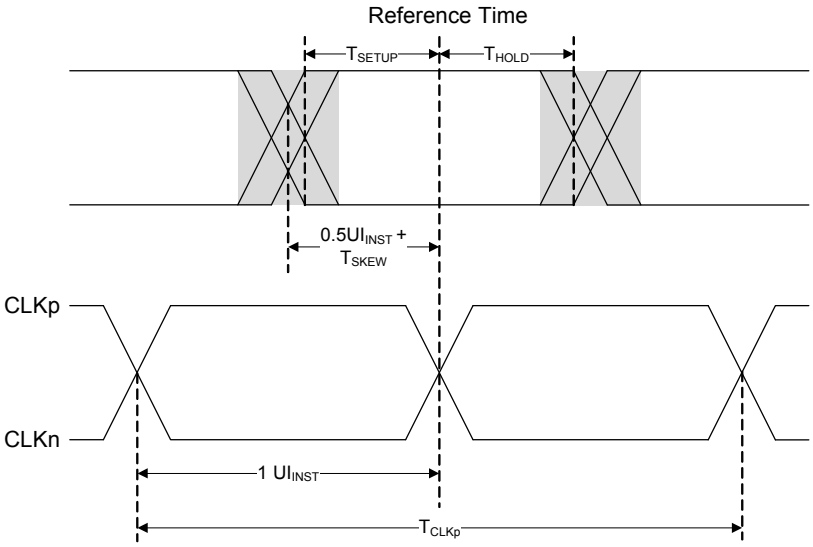



**Table 7. MIPI Data to Clock Timing Reference**

| Parameter | Description | Min | Max | Units |
|---|---|---|---|---|
| $T_{SKEW}$ | Data to clock skew measured at the transmitter | –0.15 | 0.15 | $UI_{INST}$ |
| $T_{SETUP}$ | Data to clock setup time at receiver | 0.15 | – | $UI_{INST}$ |
| $T_{HOLD}$ | Clock to data hold time at receiver | 0.15 | – | $UI_{INST}$ |
| $UI_{INST}$ | One data bit time (instantaneous) | 1 | 12.5 | ns |
| $T_{CLKp}$ | Period of dual data rate clock | 2 | 25 | ns |

### Reference Clock Specifications

**Table 8. Reference Clock Specifications**

| Parameter | Description | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| RefClk | Reference clock frequency | 6 | 40 | MHz | – |
| RefclkDutyCyl | Duty cycle | 40% | 60% | – | – |
| RefClkPJ | Reference clock input period jitter | -100 | 100 | ps | – |

## MIPI CSI Signal Low Power AC Characteristics

**Figure 7. MIPI CSI bus Input Glitch Rejection**

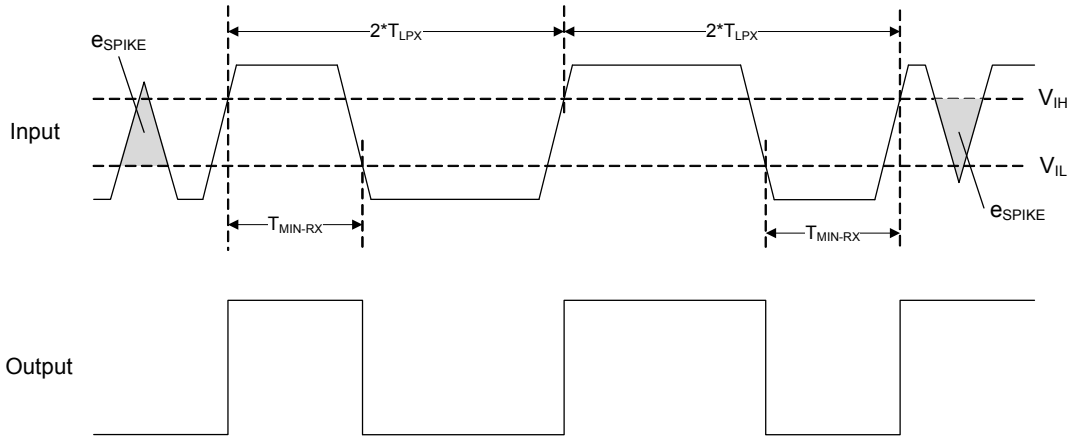



**Table 9. MIPI CSI Signal Low Power AC Characteristics**

| Parameter | Description | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| $e_{SPIKE}$ | Input noise rejection | – | 300 | V.ps | Time-voltage integration of a spike above $V_{IL}$ when being in LP-0 or below $V_{IH}$ when being in LP-1 state. An impulse less than this will not change the receiver state. |
| $T_{MIN-RX}$ | Minimum pulse width response | 20 | – | ns | An input pulse greater than this shall toggle the output. |
| $V_{INT}$ | peak interference amplitude | – | 200 | mV | – |
| $F_{INT}$ | Interference frequency | 450 | – | MHz | – |
| $T_{LPX}$ | Length of any low power state period | 50 | – | ns | – |

## AC Specifications

**Table 10. AC Specifications**

| Parameter | Description | Min | Max | Units | Details / Conditions |
|---|---|---|---|---|---|
| $\Delta V_{CMRX(HF)}$ | Common-mode interference beyond 450 MHz | – | 100 | mV | $\Delta V_{CMRX(HF)}$ is the peak amp. Of a sine wave superimposed on the receiver inputs. |
| $\Delta V_{CMRX(LF)}$ | Common-mode interference beyond 50 - 450 MHz | -50 | 50 | mV | Excluding static ground shift of 50 mV. Voltage difference compared to the DC average common-mode potential |

## Serial Peripherals Timing

*I²C Timing*

**Figure 8. I²C Timing Definition**

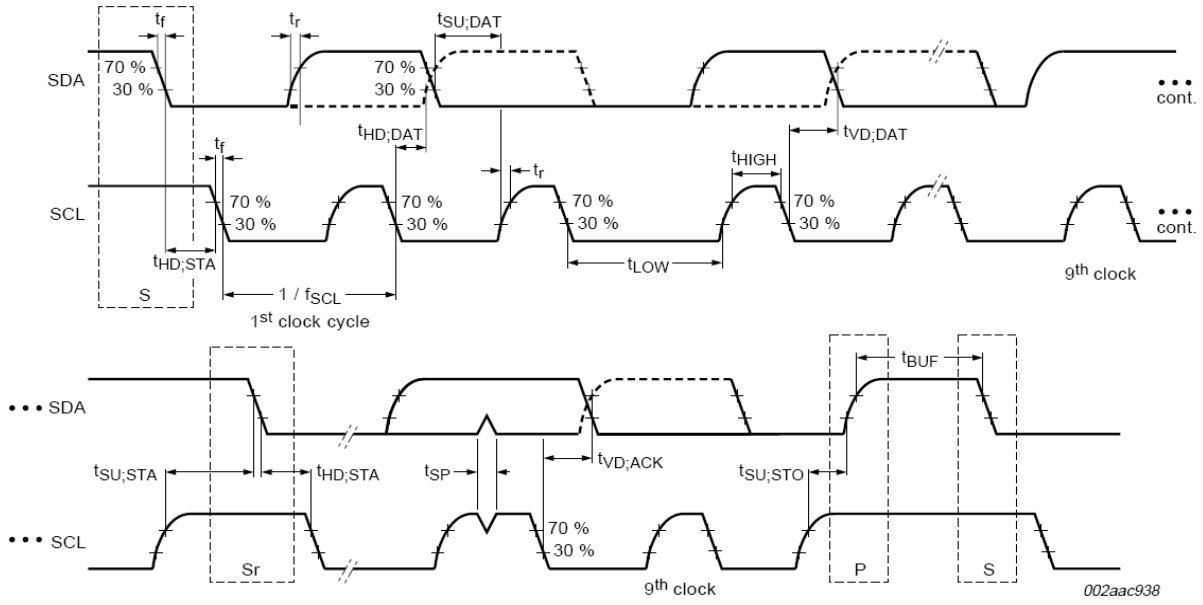



**Table 11. I²C Timing Parameters**[2]

| Parameter | Description | Min | Max | Units |
|---|---|---|---|---|
| **I²C Standard Mode Parameters** | | | | |
| $f_{SCL}$ | SCL clock frequency | 0 | 100 | kHz |
| $t_{HD:STA}$ | Hold time START condition | 4 | – | µs |
| $t_{LOW}$ | LOW period of the SCL | 4.7 | – | µs |
| $t_{HIGH}$ | HIGH period of the SCL | 4 | – | µs |
| $t_{SU:STA}$ | Setup time for a repeated START condition | 4.7 | – | µs |
| $t_{HD:DAT}$ | Data hold time | 0 | – | µs |
| $t_{SU:DAT}$ | Data setup time | 250 | – | ns |
| $t_r$ | Rise time of both SDA and SCL signals | – | 1000 | ns |
| $t_f$ | Fall time of both SDA and SCL signals | – | 300 | ns |
| $t_{SU:STO}$ | Setup time for STOP condition | 4 | – | µs |
| $t_{BUF}$ | Bus free time between a STOP and START condition | 4.7 | – | µs |
| $t_{VD:DAT}$ | Data valid time | – | 3.45 | µs |
| $t_{VD:ACK}$ | Data valid ACK | – | 3.45 | µs |
| $t_{SP}$ | Pulse width of spikes that must be suppressed by input filter | n/a | n/a | |

**Note**
2. All parameters guaranteed by design and validated through characterization.

**Table 11. I²C Timing Parameters**[2] (continued)

| Parameter | Description | Min | Max | Units |
|---|---|---|---|---|
| **I²C Fast Mode Parameters** | | | | |
| $f_{SCL}$ | SCL clock frequency | 0 | 400 | kHz |
| $t_{HD:STA}$ | Hold time START condition | 0.6 | – | µs |
| $t_{LOW}$ | LOW period of the SCL | 1.3 | – | µs |
| $t_{HIGH}$ | HIGH period of the SCL | 0.6 | – | µs |
| $t_{SU:STA}$ | Setup time for a repeated START condition | 0.6 | – | µs |
| $t_{HD:DAT}$ | Data hold time | 0 | – | µs |
| $t_{SU:DAT}$ | Data setup time | 100 | – | ns |
| $t_r$ | Rise time of both SDA and SCL signals | – | 300 | ns |
| $t_f$ | Fall time of both SDA and SCL signals | – | 300 | ns |
| $t_{SU:STO}$ | Setup time for STOP condition | 0.6 | – | µs |
| $t_{BUF}$ | Bus free time between a STOP and START condition | 1.3 | – | µs |
| $t_{VD:DAT}$ | Data valid time | – | 0.9 | µs |
| $t_{VD:ACK}$ | Data valid ACK | – | 0.9 | µs |
| $t_{SP}$ | Pulse width of spikes that must be suppressed by input filter | 0 | 50 | ns |
| **I²C Fast Mode Plus Parameters** | | | | |
| $f_{SCL}$ | SCL clock frequency | 0 | 1000 | kHz |
| $t_{HD:STA}$ | Hold time START condition | 0.26 | – | µs |
| $t_{LOW}$ | LOW period of the SCL | 0.5 | – | µs |
| $t_{HIGH}$ | HIGH period of the SCL | 0.26 | – | µs |
| $t_{SU:STA}$ | Setup time for a repeated START condition | 0.26 | – | µs |
| $t_{HD:DAT}$ | Data hold time | 0 | – | µs |
| $t_{SU:DAT}$ | Data setup time | 50 | – | ns |
| $t_r$ | Rise time of both SDA and SCL signals | – | 120 | ns |
| $t_f$ | Fall time of both SDA and SCL signals | – | 120 | ns |
| $t_{SU:STO}$ | Setup time for STOP condition | 0.26 | – | µs |
| $t_{BUF}$ | Bus-free time between a STOP and START condition | 0.5 | – | µs |
| $t_{VD:DAT}$ | Data valid time | – | 0.45 | µs |
| $t_{VD:ACK}$ | Data valid ACK | – | 0.55 | µs |
| $t_{SP}$ | Pulse width of spikes that must be suppressed by input filter | 0 | 50 | ns |

*I²S Timing Diagram*

**Figure 9. I²S Transmit Cycle**

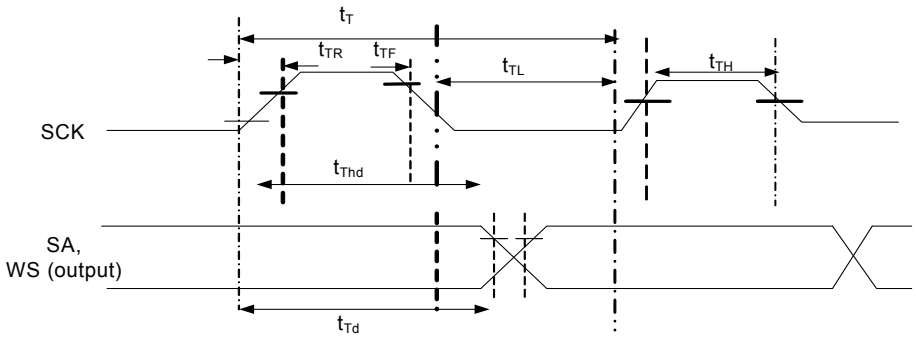



**Table 12. I²S Timing Parameters**[3]

| Parameter | Description | Min | Max | Units |
|---|---|---|---|---|
| $t_T$ | I²S transmitter clock cycle | $t_{TR}$ | – | ns |
| $t_{TL}$ | I²S transmitter cycle LOW period | 0.35 $t_{TR}$ | – | ns |
| $t_{TH}$ | I²S transmitter cycle HIGH period | 0.35 $t_{TR}$ | – | ns |
| $t_{TR}$ | I²S transmitter rise time | – | 0.15 $t_{TR}$ | ns |
| $t_{TF}$ | I²S transmitter fall time | – | 0.15 $t_{TR}$ | ns |
| $t_{Thd}$ | I²S transmitter data hold time | 0 | – | ns |
| $t_{Td}$ | I²S transmitter delay time | – | 0.8 $t_T$ | ns |
| **Note** $t_T$ is selectable through clock gears. Max $t_{TR}$ is designed for 96-kHz codec at 32 bits to be 326 ns (3.072 MHz). | | | | |

**Note**
3. All parameters guaranteed by design and validated through characterization.

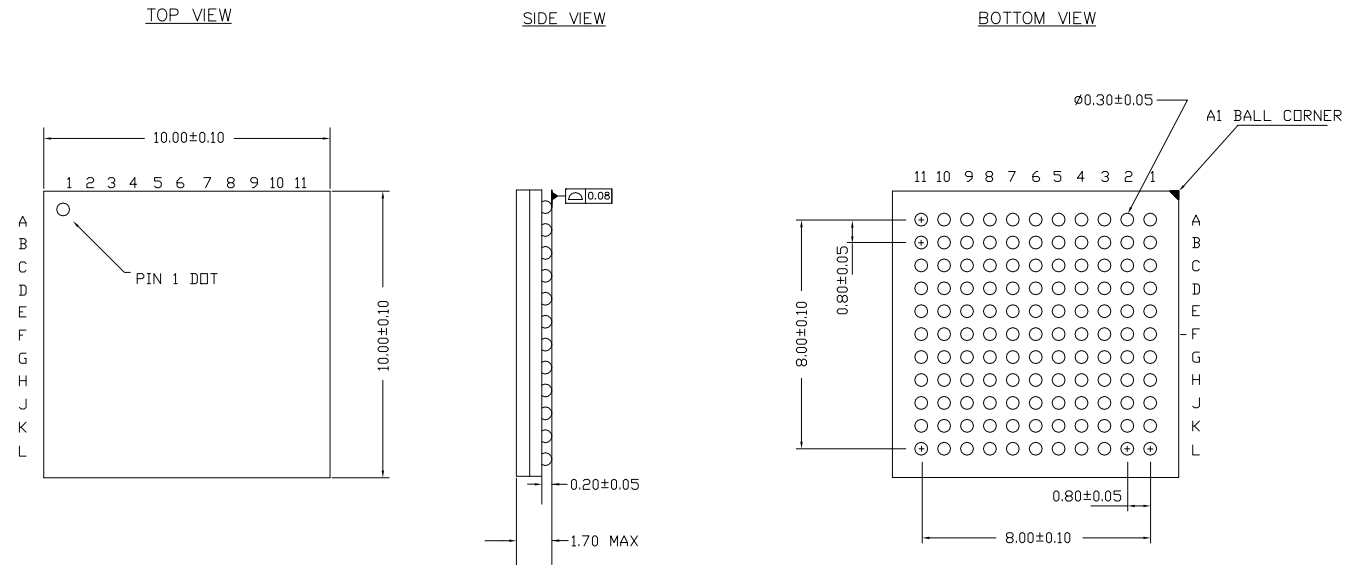
**Table 13. SPI Timing Parameters**[4]

| Parameter | Description | Min | Max | Units |
|---|---|---|---|---|
| $f_{op}$ | Operating frequency | 0 | 33 | MHz |
| $t_{sck}$ | Cycle time | 30 | – | ns |
| $t_{wsck}$ | Clock HIGH/LOW time | 13.5 | – | ns |
| $t_{lead}$ | SSN-SCK lead time | 1/2 $t_{sck}$[5] – 5 | 1.5 $t_{sck}$[5] + 5 | ns |
| $t_{lag}$ | Enable lag time | 0.5 | 1.5 $t_{sck}$[5] + 5 | ns |
| $t_{rf}$ | Rise/fall time | – | 8 | ns |
| $t_{sdd}$ | Output SSN to valid data delay time | – | 5 | ns |
| $t_{dv}$ | Output data valid time | – | 5 | ns |
| $t_{di}$ | Output data invalid | 0 | – | ns |
| $t_{ssnh}$ | Minimum SSN HIGH time | 10 | – | ns |
| $t_{sdi}$ | Data setup time input | 8 | – | ns |
| $t_{hoi}$ | Data hold time input | 0 | – | ns |
| $t_{dis}$ | Disable data output on SSN HIGH | 0 | – | ns |

**Notes**
4. All parameters guaranteed by design and validated through characterization.
5. Depends on LAG and LEAD setting in the SPI_CONFIG register.

## Package Diagram

**Figure 12. 121-ball BGA (10 × 10 × 1.7 mm) Package Outline, 001-87293**




NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS
2. REFERENCE JEDEC : PUB 95, DESIGN GUIDE 4.5

001-87293 **

## Acronyms

**Table 16. Acronyms Used in this Document**

| Acronym | Description |
|---|---|
| CSI - 2 | Camera Serial Interface - 2 |
| DMA | Direct Memory Access |
| DNU | Do Not Use |
| HNP | Host Negotiation Protocol |
| MIPI | Mobile Industry Processor Interface |
| MMC | Multimedia Card |
| MTP | Media Transfer Protocol |
| PLL | Phase Locked Loop |
| PMIC | Power Management IC |
| SD | Secure Digital |
| SDIO | Secure Digital Input / Output |
| SLC | Single-Level Cell |
| SPI | Serial Peripheral Interface |
| SRP | Session Request Protocol |
| USB | Universal Serial Bus |
| WLCSP | Wafer Level Chip Scale Package |

## Document Conventions

### Units of Measure

**Table 17. Units of Measure**

| Symbol | Unit of Measure |
|---|---|
| °C | degree Celsius |
| Mbps | Megabits per second |
| MBps | Megabytes per second |
| MHz | megahertz |
| µA | microampere |
| µs | microsecond |
| mA | milliampere |
| ms | millisecond |
| ns | nanosecond |
| Ω | ohm |
| pF | picofarad |
| V | volt |

## Document History Page (continued)

| Document Title: CYUSB306X, EZ-USB® CX3: MIPI CSI-2 to SuperSpeed USB Bridge Controller<br>Document Number: 001-87516 | | | | |
|---|---|---|---|---|
| **Revision** | **ECN** | **Orig. of Change** | **Submission Date** | **Description of Change** |
| *E (cont.) | 4188453 | KUMR | 11/14/2013 | Updated Figure 6.<br>Updated Table 7.<br>Updated minimum value of $UI_{INST}$ parameter.<br>Updated maximum value of $T_{CLKp}$ parameter.<br>Updated MIPI CSI Signal Low Power AC Characteristics:<br>Updated Figure 7.<br>Updated Serial Peripherals Timing.<br>Updated I2C Timing.<br>Updated Table 11:<br>Removed "(Not supported at I2C_VDDQ = 1.2 V)" in "$I^2C$ Fast Mode Plus Parameters" sub-heading.<br>Updated Reset Sequence.<br>Updated Table 14.<br>Removed "Crystal Input" condition for $t_{RPW}$, $t_{RR}$, $t_{WU}$ parameters.<br>Updated Figure 11.<br>Updated Ordering Information: Updated part numbers. |
| *F | 4214952 | RAJA | 03/12/2014 | Updated Features.<br>Updated Functional Overview.<br>Updated Application Examples.<br>Updated Figure 1.<br>Updated Configuration Options: Added email.<br>Updated Pin Description.<br>Updated caption of Table 6.<br>Updated DC Specifications:<br>Updated maximum value of $V_{IL}$ parameter.<br>Updated maximum value of $V_{RAMP}$ parameter.<br>Updated AC Timing Parameters.<br>Updated MIPI CSI Signal Low Power AC Characteristics.<br>Updated Table 9.<br>Updated details in "Notes" column.<br>Updated to new template. |
| *G | 4417040 | KUMR | 06/23/2014 | Updated Power: Updated details of IO_VDDQ power supply domain.<br>Updated DC Specifications: Updated maximum value of $I_{CC}$ Core parameter. |
| *H | 4467092 | RAJA | 08/06/2014 | Added new part numbers: 2 and 4 MIPI CSI-2 lane parts with Industrial and Commercial temperature grades.<br><br>HSYNC, VSYNC, PCLK test points mentioned in the pin configuration table MCLK - Signal description updated.<br><br>Updated information for CYUSB3064 part number: MIPI_D2P, MIPI_D2N, MIPI_D3P, MIPI_D3N signals not available. |
| *I | 4862446 | RAGO | 08/13/2015 | Added footnote 1, and updated Pin Configuration (Figure 5) and Pin Description (Table 6) to indicate grounding of unused MIPI lanes. |
| *J | 4974015 | RAGO | 10/19/2015 | Added More Information. |
| *K | 5283275 | RAGO | 05/24/2016 | Updated to new template.<br>Completing Sunset Review. |