Renesas Electronics America Inc - UPD78F0451GA-HAB-AX Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0
Core Size	8-Bit
Speed	10MHz
Connectivity	3-Wire SIO, LINbus, UART/USART
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	46
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0451ga-hab-ax

(2) Non-port functions (2/4): 78K0/LF3

Function Name	I/O	Function	After Reset	Alternate Function
SEG0 to SEG3	Output	LCD controller/driver segment signal outputs	Output	COM4 to COM7
SEG4 to SEG7			Input port	P80 to P83
SEG8 to SEG11				P90 to P93
SEG12 to SEG15				P100 to P103
SEG16, SEG17				P110, P111
SEG18				P112/TxD6
SEG19				P113/RxD6
SEG20 to SEG23				P130 to P133
SEG24 (KS0) to SEG27 (KS3)		LCD controller/driver segment signal outputs. Segment key source signal can be simultaneously output.		P140 to P143
SEG28 (KS4) to SEG31 (KS7)				P150 to P153
SEG32[Note 1]		LCD controller/driver segment signal outputs	Digital input port	P27/ANI7[Note 2]
SEG33[Note 1]				P26/ANI6[Note 2]
SEG34[Note 1]				P25/ANI5[Note 2]
SEG35[Note 1]				P24/ANI4[Note 2]
SEG36[Note 1]				P23/ANI3[Note 2]
SEG37[Note 1]				P22/ANI2[Note 2]
SEG38[Note 1]				P21/ANI1[Note 2]
SEG39[Note 1]				P20/ANI0[Note 2]
COM0 to COM3	Output	LCD controller/driver common signal outputs	Output	–
COM4 to COM7				SEG0 to SEG3
V_{LC0} to V_{LC2}	–	LCD drive voltage	–	–
V_{LC3}			Input port	P40/KR0

Notes 1. μPD78F047x and 78F048x only.

2. μPD78F048x and 78F049x only.

Table 3-5. Vector Table

Vector Table Address	Interrupt Source	LC3	LD3	LE3	LF3
0000H	$\overline{\text{RESET}}$ input, POC, LVI, WDT	√	√	√	√
0004H	INTLVI	√	√	√	√
0006H	INTP0	√	√	√	√
0008H	INTP1	√	√	√	√
000AH	INTP2	√	√	√	√
000CH	INTP3	√	√	√	√
000EH	INTP4	–	–	√	√
0010H	INTP5	–	–	–	√
0012H	INTSRE6	√	√	√	√
0014H	INTSR6	√	√	√	√
0016H	INTST6	√	√	√	√
0018H	INTCSI10/INTST0	√Note 1	√	√	√
001AH	INTTMH1	√	√	√	√
001CH	INTTMH0	√	√	√	√
001EH	INTTM50	√	√	√	√
0020H	INTTM000	√	√	√	√
0022H	INTTM010	√	√	√	√
0024H	INTAD	√Note 2	√Note 3	√Note 4	√Note 6
0026H	INTSR0	√	√	√	√
0028H	INTRTC	√	√	√	√
002AH	INTTM51	√	√	√	√
002CH	INTKR	√	√	√	√
002EH	INTRTCI	√	√	√	√
0030H	INTDSAD	–	–	√Note 5	√Note 7
0032H	INTTM52	√	√	√	√
0034H	INTTMH2	√	√	√	√
0036H	INTMCG	√	√	√	√
0038H	INTRIN	–	√	√	√
003AH	INTRERR/INTGP/INTREND/ INTDFULL	–	√	√	√
003CH	INTACSI	–	–	–	√
003EH	BRK	√	√	√	√

Notes 1. INTST0 only.

2. μPD78F041x only.

3. μPD78F043x only.

4. μPD78F045x and 78F046x only.

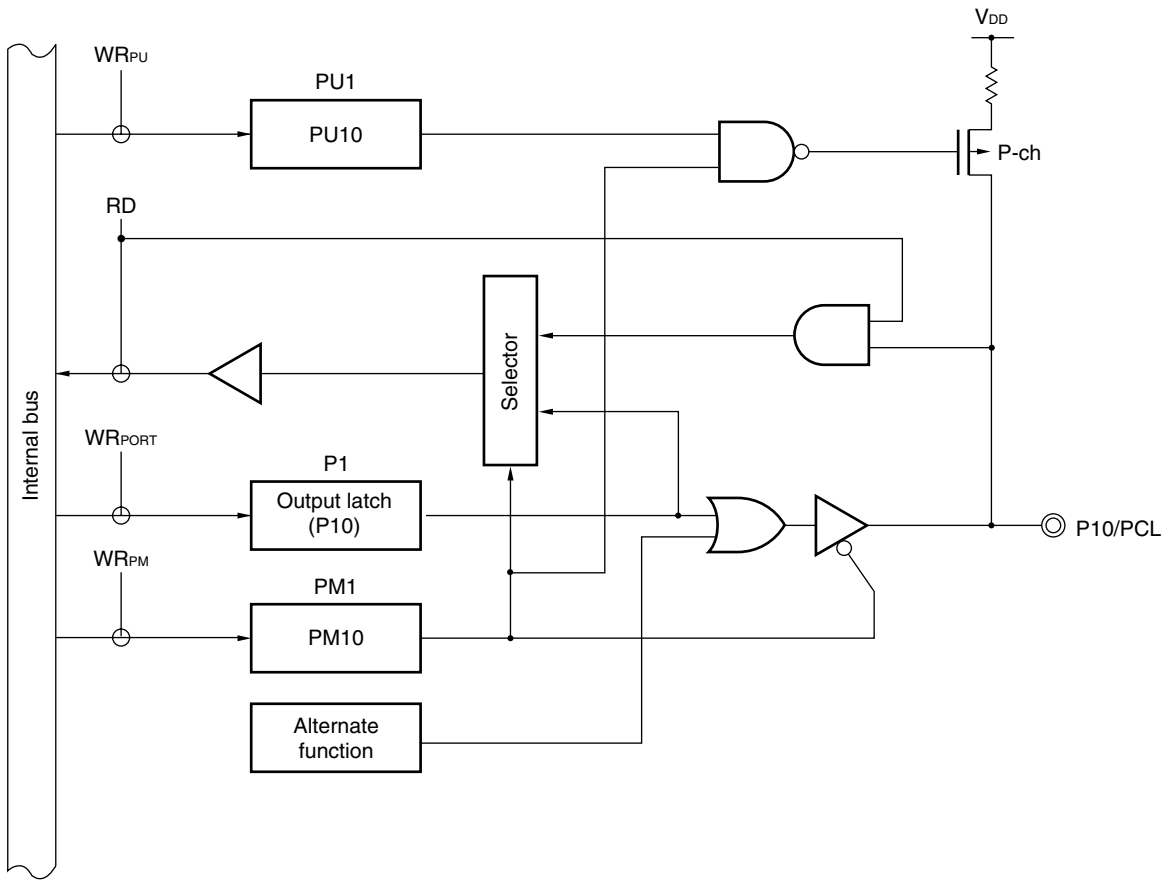
5. μPD78F046x only.

6. μPD78F048x and 78F049x only.

7. μPD78F049x only.

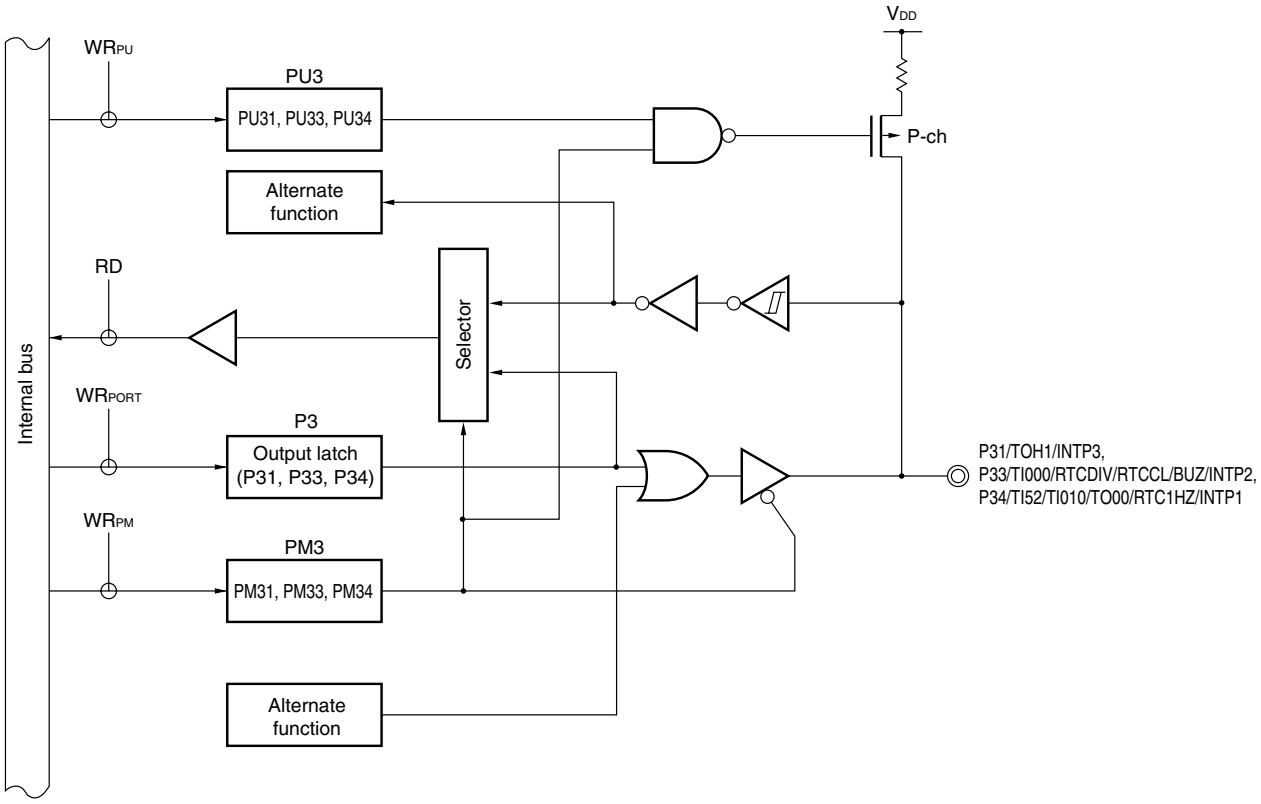
Remark √: Mounted, –: Not mounted

Figure 4-1. Block Diagram of P10



P1: Port register 1
PU1: Pull-up resistor option register 1
PM1: Port mode register 1
RD: Read signal
WR××: Write signal

Figure 4-9. Block Diagram of P31, P33, P34



P3: Port register 3
PU3: Pull-up resistor option register 3
PM3: Port mode register 3
RD: Read signal
WR××: Write signal

4.2.10 Port 13

78K0/LC3	78K0/LD3	78K0/LE3	78K0/LF3
–	–	–	P130/SEG20
–	–	–	P131/SEG21
–	–	–	P132/SEG22
–	–	–	P133/SEG23

Port 13 is an I/O port with an output latch. Port 13 can be set to the input mode or output mode in 1-bit units using port mode register 13 (PM13). When the P130 to P133 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 13 (PU13).

This port can also be used for segment signal output of the LCD controller/driver.

Either I/O port function or segment signal output function can be selected using port function register ALL (PFALL).

Reset signal generation sets port 13 to input mode.

Figure 4-23 shows a block diagram of port 13.

Notes 1. μPD78F045x and 78F046x only.

2. The functions of the P20/ANI0/DS0−, P21/ANI1/DS0+, P22/ANI2/DS1−, P23/ANI3/DS1+, P24/ANI4/DS2−, P25/ANI5/DS2+, P26/ANI6/REF−, and P27/ANI7/REF+ pins are determined according to the settings of port function register 2 (PF2), A/D port configuration register 0 (ADPC0), port mode register 2 (PM2), analog input channel specification register (ADS), and ΔΣ A/D converter mode register 0 (ADDCTL0). For details, see Table 4-8.

3. When using the P121 to P124 pins to connect a resonator for the main system clock (X1, X2) or subsystem clock (XT1, XT2), or to input an external clock for the main system clock (EXCLK), the X1 oscillation mode, XT1 oscillation mode, or external clock input mode must be set by using the clock operation mode select register (OSCCTL) (for details, see **5.3 (1) Clock operation mode select register (OSCCTL)** and **(3) Setting of operation mode for subsystem clock pin**). The reset value of OSCCTL is 00H (all of the P121 to P124 are Input port pins).

4. Targeted at registers corresponding to each port.

5. RxD6 can be set as the input source for TI000 by setting ISC1 = 1.

6. Input enable of TM52 via TMH2 can be controlled by setting ISC2 = 1.

7. RxD6 can be set as the input source for INTP0 by setting ISC0 = 1.

8. μPD78F046x only.

9. When the P40/KR0/V_{LC3} pin is set to the 1/4 bias method, it is used as V_{LC3}. When the pin is set to another bias method, it is used for the port function (P40) or the key interrupt function (KR0).

10. Set PF13 = 0 when using as port function.

11. μPD78F044x and 78F045x only.

Remarks 1. ×: Don't care
−: Does not apply.
PM××: Port mode register
P××: Port output latch

2. The functions within arrowheads (< >) can be assigned by setting the input switch control register (ISC).

3. X1, X2 pins can be used as on-chip debug mode setting pins (OCD1A, OCD1B) when the on-chip debug function is used. For detail, see **CHAPTER 29 ON-CHIP DEBUG FUNCTION.**

(1) Example of setting procedure when restarting oscillation of the internal high-speed oscillation clock[Note 1]

<1> Setting restart of oscillation of the internal high-speed oscillation clock (RCM register)
When RSTOP is cleared to 0, the internal high-speed oscillation clock starts operating.

<2> Waiting for the oscillation accuracy stabilization time of internal high-speed oscillation clock (RCM register)
Wait until RSTS is set to 1[Note 2].

Notes 1. After a reset release, the internal high-speed oscillator automatically starts oscillating and the internal high-speed oscillation clock is selected as the CPU clock.

2. This wait time is not necessary if high accuracy is not necessary for the CPU clock and peripheral hardware clock.

(2) Example of setting procedure when using internal high-speed oscillation clock as CPU clock, and internal high-speed oscillation clock or high-speed system clock as peripheral hardware clock

<1>
- Restarting oscillation of the internal high-speed oscillation clock[Note]
(See **5.6.2 (1) Example of setting procedure when restarting internal high-speed oscillation clock**).
- Oscillating the high-speed system clock[Note]
(This setting is required when using the high-speed system clock as the peripheral hardware clock. See **5.6.1 (1) Example of setting procedure when oscillating the X1 clock** and **(2) Example of setting procedure when using the external main system clock.**)

Note The setting of <1> is not necessary when the internal high-speed oscillation clock or high-speed system clock is already operating.

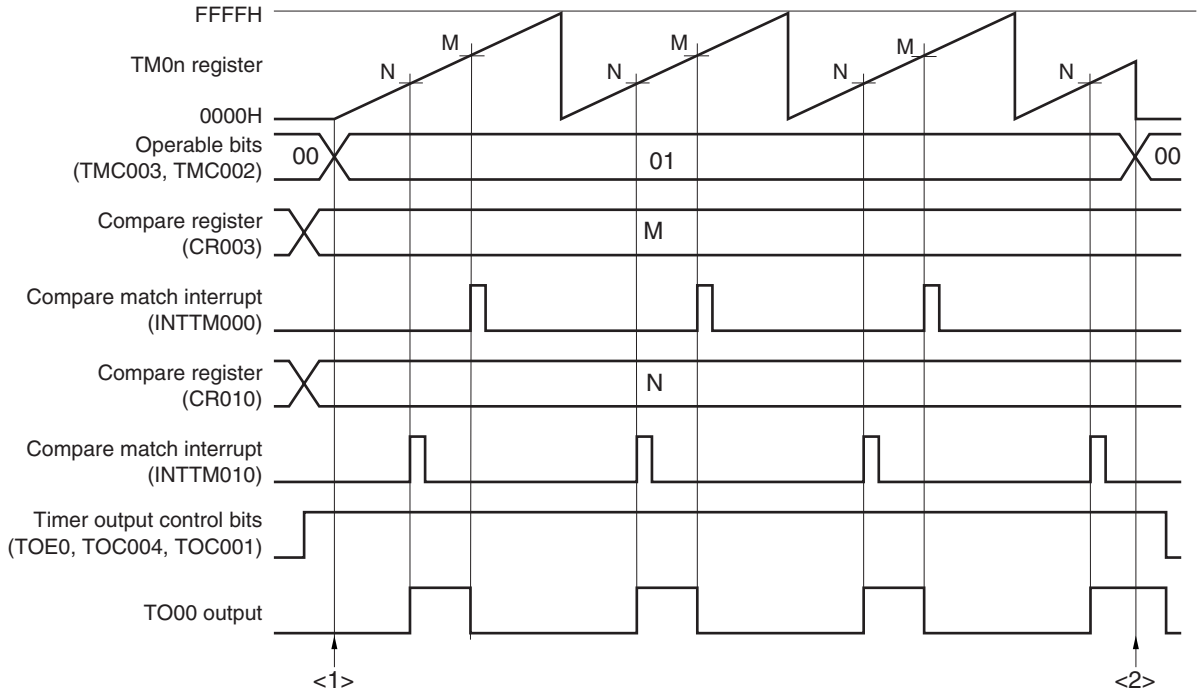
<2> Selecting the clock supplied as the main system clock and peripheral hardware clock (MCM register)
Set the main system clock and peripheral hardware clock using XSEL and MCM0.

XSEL	MCM0	Selection of Main System Clock and Clock Supplied to Peripheral Hardware	
		Main System Clock (f_{XP})	Peripheral Hardware Clock (f_{PRS})
0	0	Internal high-speed oscillation clock (f_{RH})	Internal high-speed oscillation clock (f_{RH})
0	1		
1	0		High-speed system clock (f_{XH})

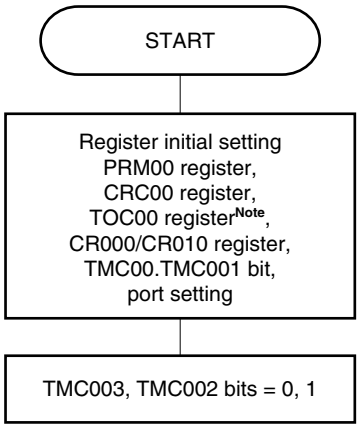
<3> Selecting the CPU clock division ratio (PCC register)
When CSS is cleared to 0, the main system clock is supplied to the CPU. To select the CPU clock division ratio, use PCC0, PCC1, and PCC2.

CSS	PCC2	PCC1	PCC0	CPU Clock (f_{CPU}) Selection
0	0	0	0	f_{XP}
	0	0	1	f_{XP}/2 (default)
	0	1	0	$f_{XP}/2^2$
	0	1	1	$f_{XP}/2^3$
	1	0	0	$f_{XP}/2^4$
	Other than above			Setting prohibited

Figure 6-40. Example of Software Processing in Free-Running Timer Mode



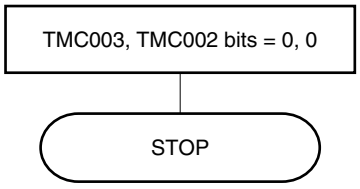
<1> Count operation start flow



Initial setting of these registers is performed before setting the TMC003 and TMC002 bits to 01.

Starts count operation

<2> Count operation stop flow

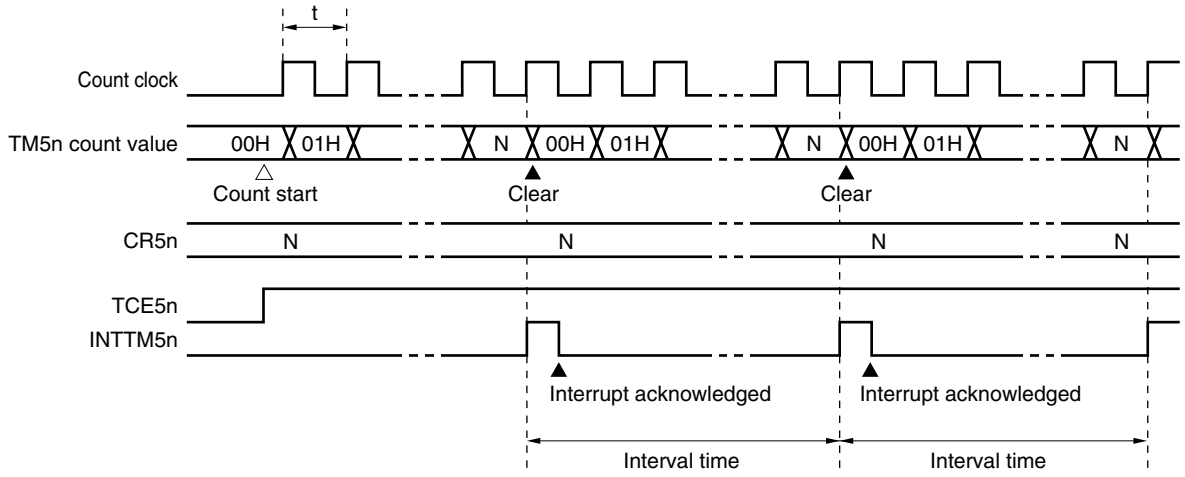


The counter is initialized and counting is stopped by clearing the TMC003 and TMC002 bits to 00.

Note Care must be exercised when setting TOC00. For details, see **6.3 (3) 16-bit timer output control register 00 (TOC00)**.

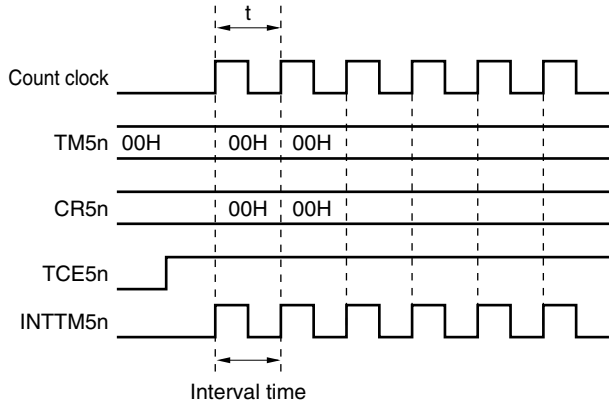
Figure 7-15. Interval Timer Operation Timing (1/2)

(a) Basic operation



Remark Interval time = (N + 1) × t
N = 01H to FFH

(b) When CR5n = 00H



Remark n = 0 to 2

Figure 8-1. Block Diagram of 8-Bit Timer H0

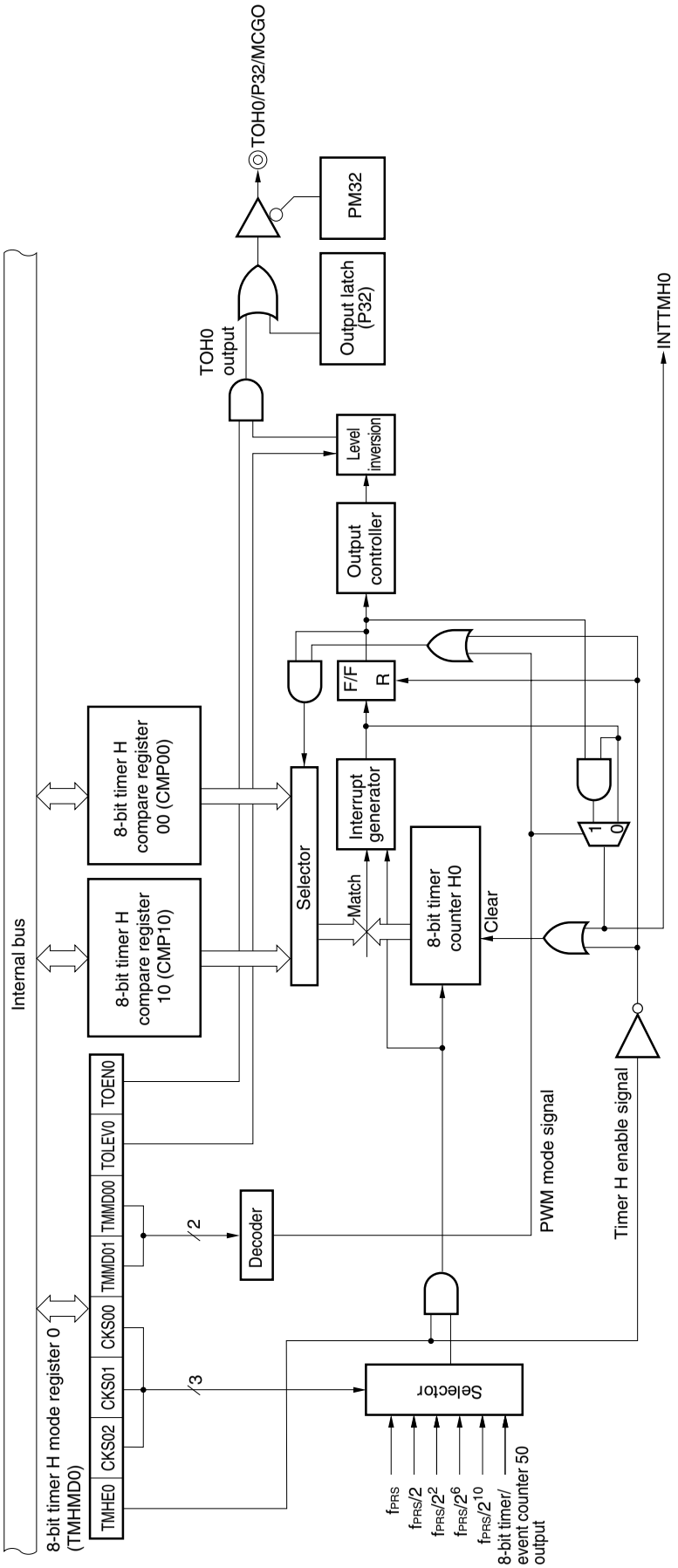
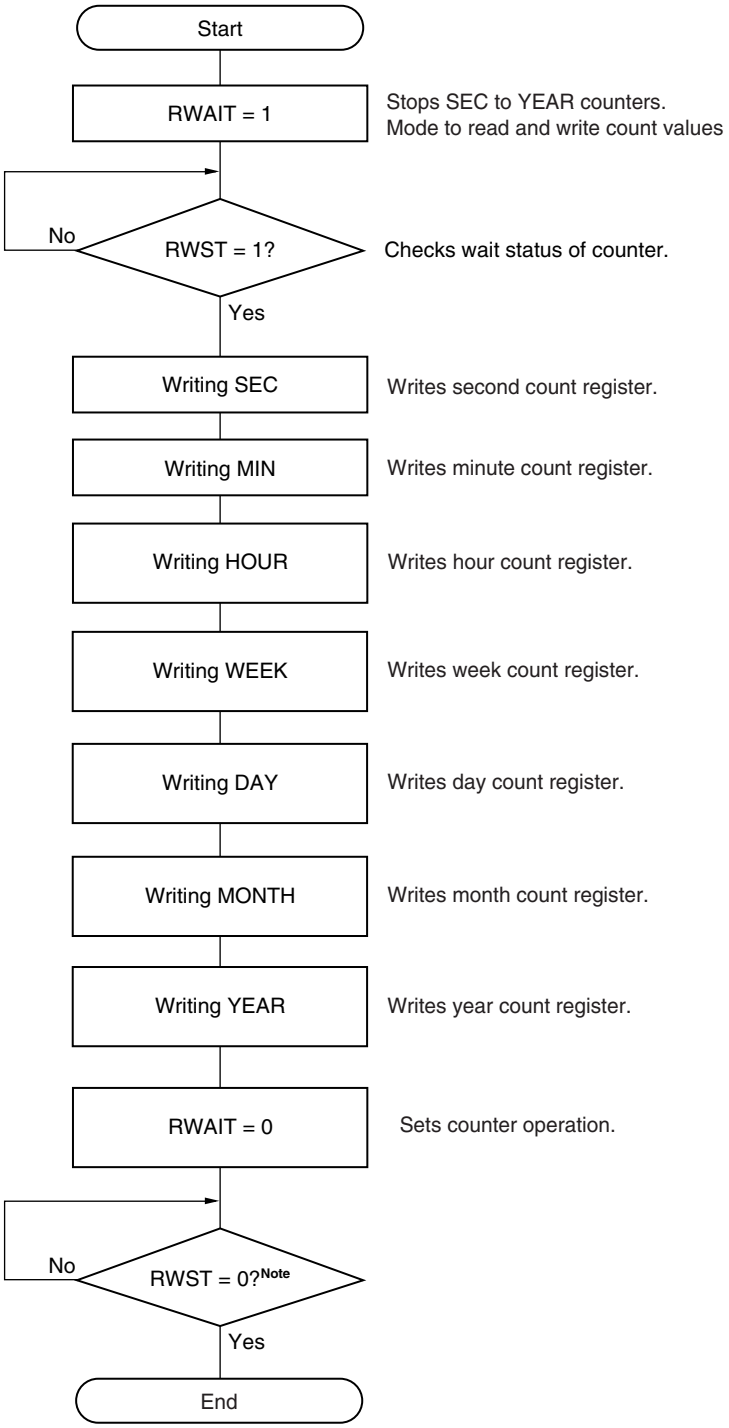


Figure 9-22. Procedure for Writing Real-Time Counter



Note Be sure to confirm that RWST = 0 before setting STOP mode.

Caution Complete the series of operations of setting RWAIT to 1 to clearing RWAIT to 0 within 1 second.

Remark SEC, MIN, HOUR, WEEK, DAY, MONTH, and YEAR may be written in any sequence.
All the registers do not have to be set and only some registers may be written.

Figure 15-10. Format of Asynchronous Serial Interface Control Register 6 (ASICL6) (2/2)

SBL62	SBL61	SBL60	SBF transmission output width control
1	0	1	SBF is output with 13-bit length.
1	1	0	SBF is output with 14-bit length.
1	1	1	SBF is output with 15-bit length.
0	0	0	SBF is output with 16-bit length.
0	0	1	SBF is output with 17-bit length.
0	1	0	SBF is output with 18-bit length.
0	1	1	SBF is output with 19-bit length.
1	0	0	SBF is output with 20-bit length.

DIR6	First-bit specification
0	MSB
1	LSB

TXDLV6	Enables/disables inverting TxD6 output
0	Normal output of TxD6
1	Inverted output of TxD6

Cautions
1. **In the case of an SBF reception error, the mode returns to the SBF reception mode. The status of the SBRF6 flag is held (1).**
2. **Before setting the SBRT6 bit, make sure that bit 7 (POWER6) and bit 5 (RXE6) of ASIM6 = 1. After setting the SBRT6 bit to 1, do not clear it to 0 before SBF reception is completed (before an interrupt request signal is generated).**
3. **The read value of the SBRT6 bit is always 0. SBRT6 is automatically cleared to 0 after SBF reception has been correctly completed.**
4. **Before setting the SBTT6 bit to 1, make sure that bit 7 (POWER6) and bit 6 (TXE6) of ASIM6 = 1. After setting the SBTT6 bit to 1, do not clear it to 0 before SBF transmission is completed (before an interrupt request signal is generated).**
5. **The read value of the SBTT6 bit is always 0. SBTT6 is automatically cleared to 0 at the end of SBF transmission.**
6. **Do not set the SBRT6 bit to 1 during reception, and do not set the SBTT6 bit to 1 during transmission.**
7. **Before rewriting the DIR6 and TXDLV6 bits, clear the TXE6 and RXE6 bits to 0.**
8. **When the TXDLV6 bit is set to 1 (inverted TxD6 output), the TxD6/Pxx pin cannot be used as a general-purpose port, regardless of the settings of POWER6 and TXE6. When using the TxD6/Pxx pin as a general-purpose port, clear the TXDLV6 bit to 0 (normal TxD6 output).**

The relationship between the register settings and pins is shown below.

Table 15-2. Relationship Between Register Settings and Pins (1/4)

(a) 78K0/LC3

(i) When the P12 and P13 are selected as the UART6 pins using the bits 4, 5 (ISC4, ISC5) of the ISC register

POWER6	TXE6	RXE6	PM13	P13	PM12	P12	UART6 Operation	Pin Function	
								TxD6/KR4/TxD0/P13	RxD6/KR3/RxD0/P12
0	0	0	×Note	×Note	×Note	×Note	Stop	KR4/TxD0/P13	KR3/RxD0/P12
1	0	1	×Note	×Note	1	×	Reception	KR4/P13	RxD6
	1	0	0	×	×Note	×Note	Transmission	TxD6	KR3/P12
	1	1	0	×	1	×	Transmission/ reception	TxD6	RxD6

Note Can be set as port function, key interrupt, or serial interface UART0 (only when UART6 is stopped).

Caution TxD6/SEG6/P112 and RxD6/SEG7/P113 pins function as the SEG6/P112 and SEG7/P113.

Remark ×: don't care
POWER6: Bit 7 of asynchronous serial interface operation mode register 6 (ASIM6)
TXE6: Bit 6 of ASIM6
RXE6: Bit 5 of ASIM6
PM1×: Port mode register
P1×: Port output latch

(ii) When the P112 and P113 are selected as the UART6 pins using the bits 4, 5 (ISC4, ISC5) of the ISC register

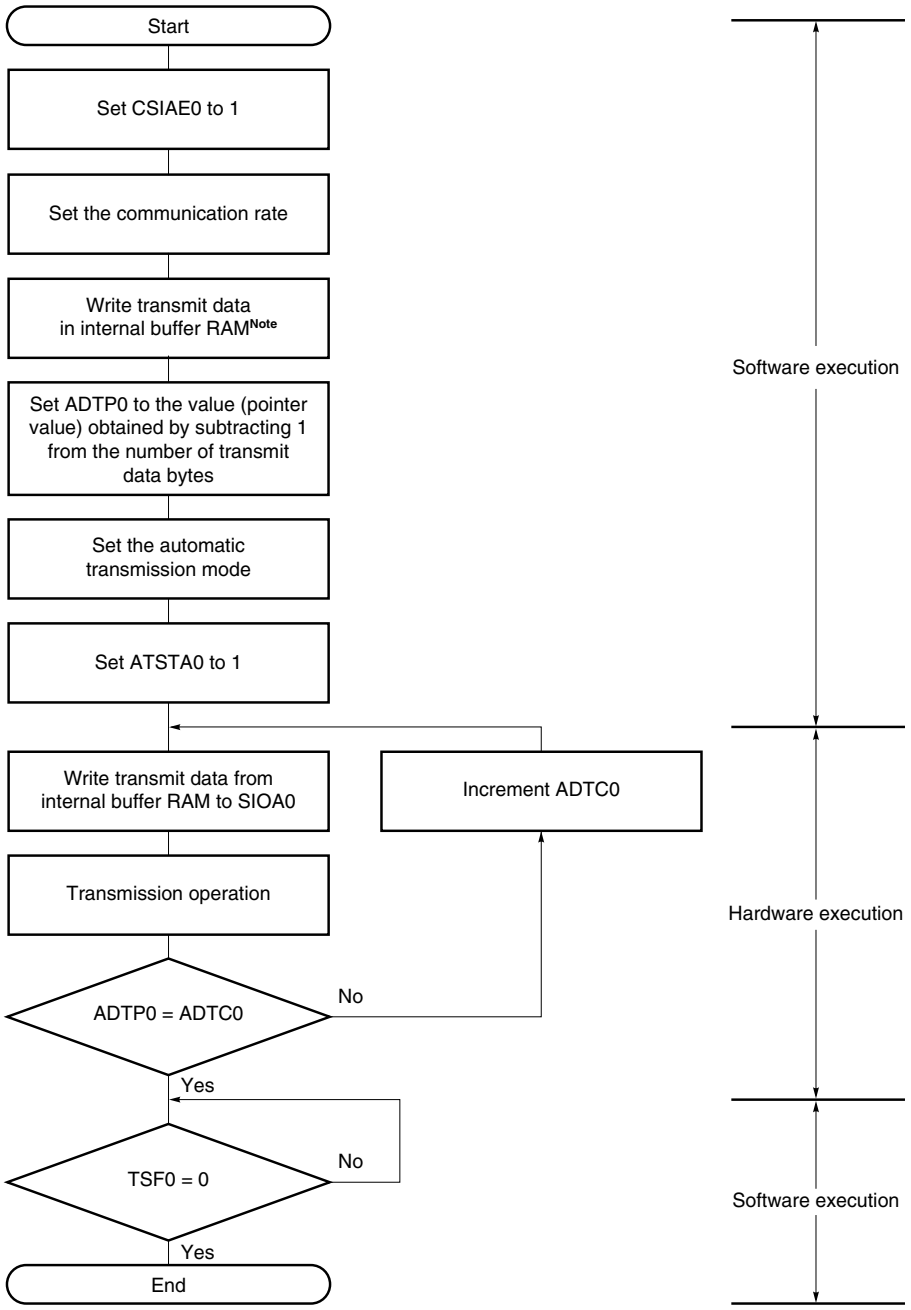
POWER6	TXE6	RXE6	PM112	P112	PM113	P113	UART6 Operation	Pin Function	
								TxD6/SEG6/P112	RxD6/SEG7/P113
0	0	0	×Note	×Note	×Note	×Note	Stop	SEG6/P112	SEG7/P113
1	0	1	×Note	×Note	1	×	Reception	SEG6/P112	RxD6
	1	0	0	1	×Note	×Note	Transmission	TxD6	SEG7/P113
	1	1	0	1	1	×	Transmission/ reception	TxD6	RxD6

Note Can be set as port function or segment output.

Caution TxD6/KR4/TxD0/P13 and RxD6/KR3/RxD0/P12 pins function as the KR4/TxD0/P13 and KR3/RxD0/P12.

Remark ×: don't care
POWER6: Bit 7 of asynchronous serial interface operation mode register 6 (ASIM6)
TXE6: Bit 6 of ASIM6
RXE6: Bit 5 of ASIM6
PM11×: Port mode register
P11×: Port output latch

Figure 17-19. Automatic Transmission Mode Flowchart



CSIAE0: Bit 7 of serial operation mode specification register 0 (CSIMA0)
ADTP0: Automatic data transfer address point specification register 0
ADTI0: Automatic data transfer interval specification register 0
ATSTA0: Bit 0 of serial trigger register 0 (CSIT0)
SIOA0: Serial I/O shift register 0
ADTC0: Automatic data transfer address count register 0
TSF0: Bit 0 of serial status register 0 (CSIS0)

Note A wait state may be generated when data is written to the buffer RAM. For details, see **CHAPTER 34 CAUTIONS FOR WAIT**.

18.4.2 Setting method when using segment key scan function (KSON = 1)

When using the segment key scan function (KSON = 1), set the LCD controller/driver as follows. Set the LCD controller/driver using the following procedure.

<1> Set (VAON = 1) internal gate voltage boosting (bit 4 of the LCD display mode register (LCDM)).[Note 1]

<2> Set the resistance division method via MDSET0 and MDSET1 (bits 4 and 5 of the LCD mode register (LCDMD)) (MDSET0 = 0: external resistance division method, MDSET0 = 1: internal resistance division method).
Set (KSON = 1) KSON (bit 0 of the LCD mode register (LCDMD)).

<3> Set the pins to be used as segment outputs to the port function registers (PF2m, PFnALL).
Set the port function register 1 (PF1) to 00H (PF13 = 0) when using P13/KR4 pin as a segment key scan input pin.[Note 2]

<4> Use port mode register 1 (PM1) and port mode register 4 (PM4) to set the pin to be used as a key scan input pin[Note 3] to PM1p = 1, PM4m = 1 (input mode).

<5> Use pull-up resistor option register 1 (PU1) and pull-up resistor option register 4 (PU4) to set the pin to be used as a key scan input pin[Note 3] to PU1p = 0, PU4m = 0 (connects an on-chip pull-up resistor only during the segment key scan output period).

<6> Use the key return mode register (KRM) to set the pin to be used as a segment key scan input pin to KRMm = 1[Note 4]

<7> Set an initial value to the RAM for LCD display.

<8> Set an initial value of segment key scan output to P14, P15.

<9> Set the number of time slices via LCDM0 to LCDM2 (bits 0 to 2 of the LCD display mode register (LCDM)).

<10> Set the LCD source clock and LCD clock via LCD clock control register 0 (LCDC0).

<11> Set (SCOC = 1) SCOC (bit 6 of the LCD display mode register (LCDM)).
Deselect signals are output from all the segment and common pins, and the non-display status is entered.

<12> Start output corresponding to each data memory by setting (LCDON = 1) LCDON (bit 7 of LCDM).

Hereinafter, set data to the data memory according to the contents displayed, and perform segment key scan output settings for the port registers (P14, P15) according to the contents of the segment key scan output.

Notes 1. Set VAON based on the following conditions.

<When set to the 1/3 bias method>

- When 2.5 V ≤ V_{LCD} = V_{DD} ≤ 5.5 V: VAON = 0
- When 1.8 V ≤ V_{LCD} = V_{DD} ≤ 3.6 V: VAON = 1

<When set to the 1/2 bias method or 1/4 bias method >

- When 2.7 V ≤ V_{LCD} = V_{DD} ≤ 5.5 V: VAON = 0
- When 1.8 V ≤ V_{LCD} = V_{DD} ≤ 3.6 V: VAON = 1

2. 78K0/LC3, 78K0/LD3 only.

3. When using the segment key scan function, be sure to set port 1 and port 4 as a segment key scan input pin and the pull-up resistor option register of the port to be used to PU1p = 0, PU4m = 0 (connects an on-chip pull-up resistor only during the segment key scan output period).
An external pull-up resistor cannot be used, because it affects the LCD display output.

4. An interrupt request flag may be set when KRM has been changed. Consequently, change the KRM register after having disabled interrupts, and enable interrupts after having cleared the interrupt request flag.

18.7.5 Eight-time-slice display example

Figure 18-34 shows how the 15×8 dots LCD panel having the display pattern shown in Figure 18-33 is connected to the segment signals (SEG4 to SEG18) and the common signals (COM0 to COM7) of the 78K0/LF3 chip. This example displays data "123" in the LCD panel. The contents of the display data memory (addresses FA44H to FA52H) correspond to this display.

The following description focuses on numeral "3" (∃) displayed in the first digit. To display "3." in the LCD panel, it is necessary to apply the select or deselect voltage to the SEG4 and SEG8 pins according to Table 18-10 at the timing of the common signals COM0 to COM7; see Figure 18-33 for the relationship between the segment signals and LCD segments.

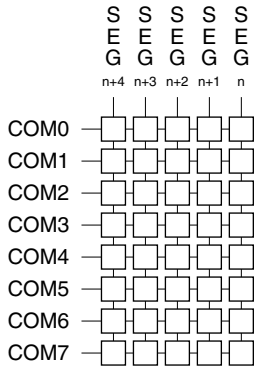
Table 18-10. Select and Deselect Voltages (COM0 to COM7)

Segment / Common	SEG4	SEG5	SEG6	SEG7	SEG8
COM0	Select	Select	Select	Select	Select
COM1	Deselect	Select	Deselect	Deselect	Deselect
COM2	Deselect	Deselect	Select	Deselect	Deselect
COM3	Deselect	Select	Deselect	Deselect	Deselect
COM4	Select	Deselect	Deselect	Deselect	Deselect
COM5	Select	Deselect	Deselect	Deselect	Select
COM6	Deselect	Select	Select	Select	Deselect
COM7	Deselect	Deselect	Deselect	Deselect	Deselect

According to Table 18-10, it is determined that the display data memory location (FA44H) that corresponds to SEG4 must contain 00110001.

Figure 18-35 shows examples of LCD drive waveforms between the SEG4 signal and each common signal. When the select voltage is applied to SEG4 at the timing of COM0, a waveform is generated to turn on the corresponding LCD segment.

Figure 18-33. Eight-Time-Slice LCD Display Pattern and Electrode Connections



(4) External interrupt rising edge enable register (EGP), external interrupt falling edge enable register (EGN)

These registers specify the valid edge for INTP0 to INTP5.

EGP and EGN are set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears these registers to 00H.

Figure 21-5. Format of External Interrupt Rising Edge Enable Register (EGP) and External Interrupt Falling Edge Enable Register (EGN)

(a) 78K0/LC3, 78K0/LD3

Address: FF48H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
EGP	0	0	0	0	EGP3	EGP2	EGP1	EGP0

Address: FF49H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
EGP	0	0	0	0	EGN3	EGN2	EGN1	EGN0

(b) 78K0/LE3

Address: FF48H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
EGP	0	0	0	EGP4	EGP3	EGP2	EGP1	EGP0

Address: FF49H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
EGP	0	0	0	EGN4	EGN3	EGN2	EGN1	EGN0

(c) 78K0/LF3

Address: FF48H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
EGP	0	0	EGP5	EGP4	EGP3	EGP2	EGP1	EGP0

Address: FF49H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
EGN	0	0	EGN5	EGN4	EGN3	EGN2	EGN1	EGN0

EGPn	EGNn	INTPn pin valid edge selection (n = 0 to 5)
0	0	Edge detection disabled
0	1	Falling edge
1	0	Rising edge
1	1	Both rising and falling edges

(2) Oscillation stabilization time select register (OSTS)

This register is used to select the X1 clock oscillation stabilization wait time when the STOP mode is released.

When the X1 clock is selected as the CPU clock, the operation waits for the time set using OSTS after the STOP mode is released.

When the internal high-speed oscillation clock is selected as the CPU clock, confirm with OSTC that the desired oscillation stabilization time has elapsed after the STOP mode is released. The oscillation stabilization time can be checked up to the time set using OSTC.

OSTS can be set by an 8-bit memory manipulation instruction.

Reset signal generation sets OSTS to 05H.

Figure 23-2. Format of Oscillation Stabilization Time Select Register (OSTS)

Address: FFA4H After reset: 05H R/W

Symbol	7	6	5	4	3	2	1	0
OSTS	0	0	0	0	0	OSTS2	OSTS1	OSTS0

OSTS2	OSTS1	OSTS0	Oscillation stabilization time selection	
				fx = 10 MHz
0	0	1	2^{11}/fx	204.8 μs
0	1	0	2^{13}/fx	819.2 μs
0	1	1	2^{14}/fx	1.64 ms
1	0	0	2^{15}/fx	3.27 ms
1	0	1	2^{16}/fx	6.55 ms
Other than above			Setting prohibited	

Cautions 1. To set the STOP mode when the X1 clock is used as the CPU clock, set OSTS before executing the STOP instruction.

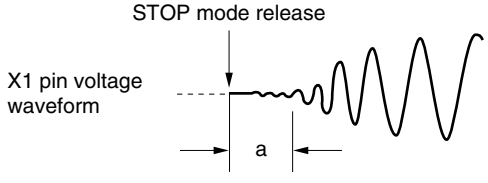
2. Do not change the value of the OSTS register during the X1 clock oscillation stabilization time.

3. The oscillation stabilization time counter counts up to the oscillation stabilization time set by OSTS. If the STOP mode is entered and then released while the internal high-speed oscillation clock is being used as the CPU clock, set the oscillation stabilization time as follows.

- **Desired OSTC oscillation stabilization time ≤ Oscillation stabilization time set by OSTS**

Note, therefore, that only the status up to the oscillation stabilization time set by OSTS is set to OSTC after STOP mode is released.

4. The X1 clock oscillation stabilization wait time does not include the time until clock oscillation starts (“a” below).



Remark fx: X1 clock oscillation frequency

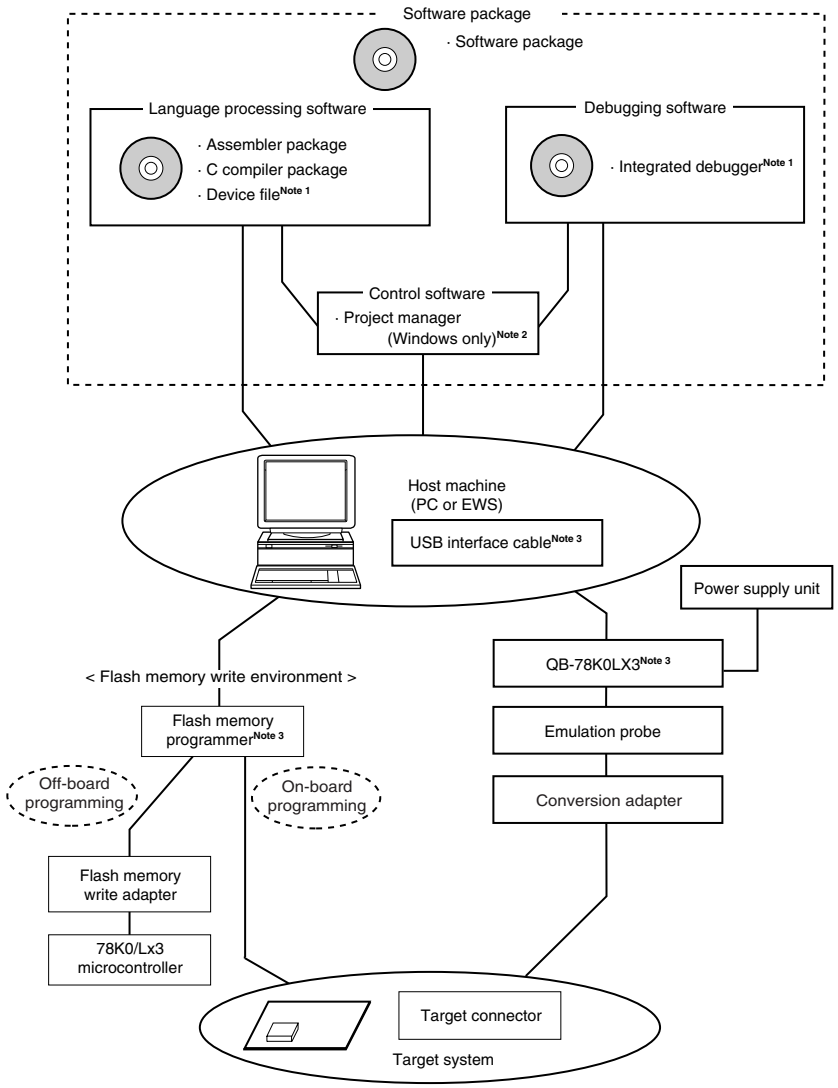
APPENDIX A DEVELOPMENT TOOLS

The following development tools are available for the development of systems that employ the 78K0/Lx3 microcontrollers.

Figure A-1 shows the development tool configuration.

Figure A-1. Development Tool Configuration (1/2)

(1) When using the in-circuit emulator QB-78K0LX3



Notes 1. Download the device file for 78K0/Lx3 microcontrollers (DF780495) and the integrated debugger ID78K0-QB from the download site for development tools (http://www.renesas.com/micro/en/ods/).

2. The project manager PM+ is included in the assembler package.
PM+ cannot be used other than with Windows™.

3. QB-78K0LX3 is supplied with the integrated debugger ID78K0-QB, a USB interface cable, the on-chip debug emulator with programming function QB-MINI2, connection cables (10-pin and 16-pin cables), and the 78K0-OCD board. Any other products are sold separately.

SALES OFFICES Renesas Electronics Corporation http://www.renesas.com

Refer to "http://www.renesas.com/" for the latest and detailed information.

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