Renesas Electronics America Inc - UPD78F0453GA-HAB-AX Datasheet

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0
Core Size	8-Bit
Speed	10MHz
Connectivity	3-Wire SIO, LINbus, UART/USART
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	46
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0453ga-hab-ax

2.2.3 P30 to P34 (port 3)

P30 to P34 function as an I/O port. These pins also function as pins for external interrupt request input, timer I/O, buzzer output, real-time counter output, and manchester code output.

78K0/LC3	78K0/LD3	78K0/LE3	78K0/LF3
–	–	–	P30/INTP5
P31/TOH1/INTP3	P31/TOH1/INTP3	P31/TOH1/INTP3	P31/TOH1/INTP3
P32/TOH0/MCGO	P32/TOH0/MCGO	P32/TOH0/MCGO	P32/TOH0/MCGO
P33/TI000/RTCDIV/ RTCCL/BUZ/INTP2	P33/TI000/RTCDIV/ RTCCL/BUZ/INTP2	P33/TI000/RTCDIV/ RTCCL/BUZ/INTP2	P33/TI000/RTCDIV/ RTCCL/BUZ/INTP2
P34/TI52/TI010/TO00/ RTC1HZ/INTP1	P34/TI52/TI010/TO00/ RTC1HZ/INTP1	P34/TI52/TI010/TO00/ RTC1HZ/INTP1	P34/TI52/TI010/TO00/ RTC1HZ/INTP1

The following operation modes can be specified in 1-bit units.

(1) Port mode

P30 to P34 function as an I/O port. P30 to P34 can be set to input or output port in 1-bit units using port mode register 3 (PM3). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 3 (PU3).

(2) Control mode

P30 to P34 function as external interrupt request input, timer I/O, buzzer output, real-time counter output, and manchester code output.

(a) INTP1 to INTP3 and INTP5

These are the external interrupt request input pins for which the valid edge (rising edge, falling edge, or both rising and falling edges) can be specified.

(b) TO00

This is a 16-bit timer/event counters 00 timer output pin.

(c) TOH0, TOH1

These are 8-bit timer H0, H1 timer output pin.

(d) TI000

This is a pin for inputting an external count clock to 16-bit timer/event counters 00 and is also for inputting a capture trigger signal to the capture registers (CR000 or CR010) of 16-bit timer/event counters 00.

(e) TI010

This is a pin for inputting a capture trigger signal to the capture register (CR000) of 16-bit timer/event counters 00.

(f) TI52

This is the pin for inputting an external count clock to 8-bit timer/event counter 52.

(g) BUZ

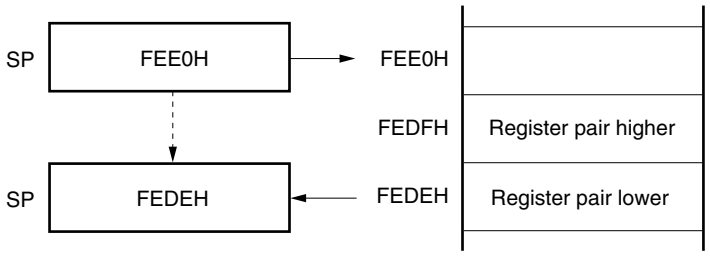
This is a buzzer output pin.

(h) RTCDIV

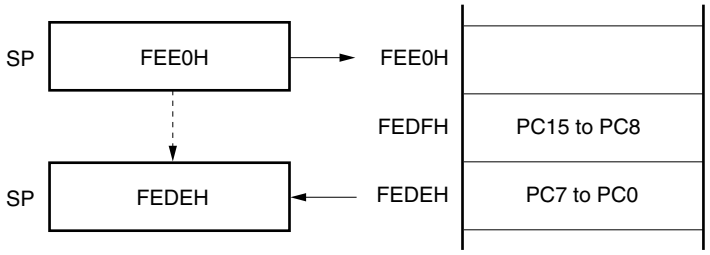
This is a real-time counter clock (32.768 kHz, divided) output pin.

Figure 3-16. Data to Be Saved to Stack Memory

(a) PUSH rp instruction (when SP = FEE0H)



(b) CALL, CALLF, CALLT instructions (when SP = FEE0H)



(c) Interrupt, BRK instructions (when SP = FEE0H)

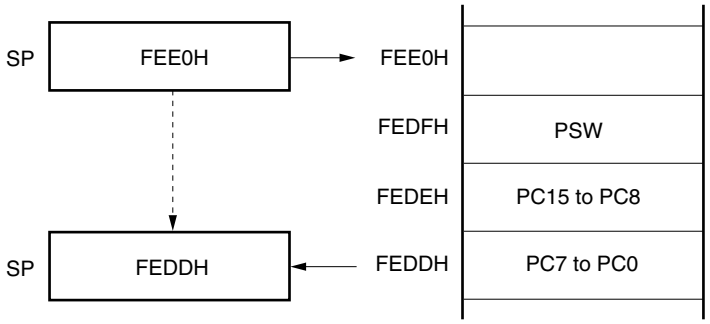
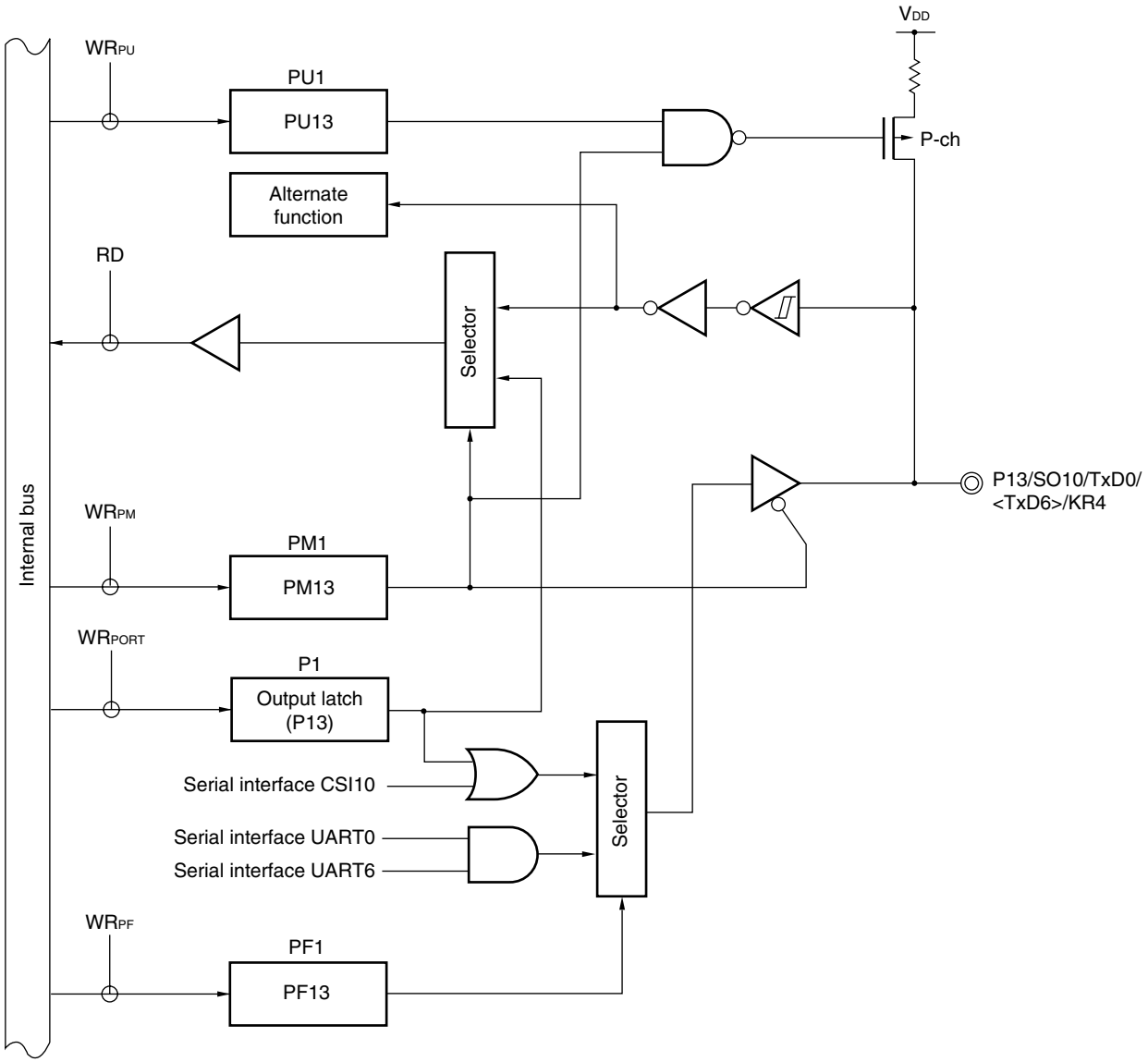


Figure 4-4. Block Diagram of P13 (2/4)

(2) 78K0/LD3



P1: Port register 1
PU1: Pull-up resistor option register 1
PM1: Port mode register 1
PF1: Port function register 1
RD: Read signal
WR××: Write signal

(1) Port mode registers (PMxx)

These registers specify input or output mode for the port in 1-bit units.

These registers can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets these registers to FFH.

When port pins are used as alternate-function pins, set the port mode register by referencing **4.5 Settings of PFALL, PF2, PF1, ISC, Port Mode Register, and Output Latch When Using Alternate Function**.

Figure 4-26. Format of Port Mode Register (78K0/LC3)

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PM1	1	1	1	1	PM13	PM12	1	1	FF21H	FFH	R/W
PM2	1	1	PM25	PM24	PM23	PM22	PM21	PM20	FF22H	FFH	R/W
PM3	1	1	1	PM34	PM33	PM32	PM31	1	FF23H	FFH	R/W
PM4	1	1	1	1	1	1	1	PM40	FF24H	FFH	R/W
PM10	1	1	1	1	1	1	PM101	PM100	FF2AH	FFH	R/W
PM11	1	1	1	1	PM113	PM112	1	1	FF2BH	FFH	R/W
PM12	1	1	1	1	1	1	1	PM120	FF2CH	FFH	R/W
PM14	1	1	1	1	PM143	PM142	PM141	PM140	FF2EH	FFH	R/W
PM15	1	1	1	1	PM153	PM152	PM151	PM150	FF2FH	FFH	R/W

PMmn	Pmn pin I/O mode selection (m = 1 to 4, 10 to 12, 14, 15; n = 0 to 5)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Caution Be sure to set bits 0, 1, and 4 to 7 of PM1, bits 6 and 7 of PM2, bits 0, and 5 to 7 of PM3, bits 1 to 7 of PM4, bits 2 to 7 of PM10, bits 0, 1, and 4 to 7 of PM11, bits 1 to 7 of PM12, bits 4 to 7 of PM14, and bits 4 to 7 of PM15 to "1".

(2) Port registers (Pxx)

These registers write the data that is output from the chip when data is output from a port.

If the data is read in the input mode, the pin level is read. If it is read in the output mode, the output latch value is read.

These registers can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears these registers to 00H.

Figure 4-30. Format of Port Register (78K0/LC3)

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
P1	0	0	0	0	P13	P12	0	0	FF01H	00H (output latch)	R/W
P2	0	0	P25	P24	P23	P22	P21	P20	FF02H	00H (output latch)	R/W
P3	0	0	0	P34	P33	P32	P31	0	FF03H	00H (output latch)	R/W
P4	0	0	0	0	0	0	0	P40	FF04H	00H (output latch)	R/W
P10	0	0	0	0	0	0	P101	P100	FF0AH	00H (output latch)	R/W
P11	0	0	0	0	P113	P112	0	0	FF0BH	00H (output latch)	R/W
P12	0	0	0	P124 Note 2	P123 Note 2	P122 Note 2	P121 Note 2	P120	FF0CH	00H Note 1 (output latch)	R/W Note 1
P14	PK143 Note 3	PK142 Note 3	PK141 Note 3	PK140 Note 3	P143	P142	P141	P140	FF0EH	00H (output latch)	R/W
P15	PK153 Note 3	PK152 Note 3	PK151 Note 3	PK150 Note 3	P153	P152	P151	P150	FF0FH	00H (output latch)	R/W

Pmn	m = 1 to 4, 10 to 12, 14, 15; n = 0 to 5	
	Output data control (in output mode)	Input data read (in input mode)
0	Output 0	Input low level
1	Output 1	Input high level

Notes 1. P121 to P124 are read-only. These become undefined at reset.

2. When the operation mode of the pin is the clock input mode, 0 is always read.

3. This bit is used for the segment key scan function. For details, see **18.3 Registers Controlling LCD Controller/Driver**.

(6) Port function register ALL (PFALL)

This register sets whether to use pins P8 to P11 and P13 to P15 as port pins (other than segment output pins) or segment output pins.

PFALL is set using a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears PFALL to 00H.

Figure 4-40. Format of Port Function Register ALL (PFALL)

(a) 78K0/LC3

Address: FFB6H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PFALL	0	PF15ALL	PF14ALL	0	PF11ALL	PF10ALL	0	0

(b) 78K0/LD3, 78K0/LE3

Address: FFB6H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PFALL	0	PF15ALL	PF14ALL	0	PF11ALL	PF10ALL	0	PF08ALL

(c) 78K0/LF3

Address: FFB6H After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
PFALL	0	PF15ALL	PF14ALL	PF13ALL	PF11ALL	PF10ALL	PF09ALL	PF08ALL

PFnALL	Port/segment output specification
0	Used as port (other than segment output)
1	Used as segment output

Remark n = 08 to 11, 13 to 15

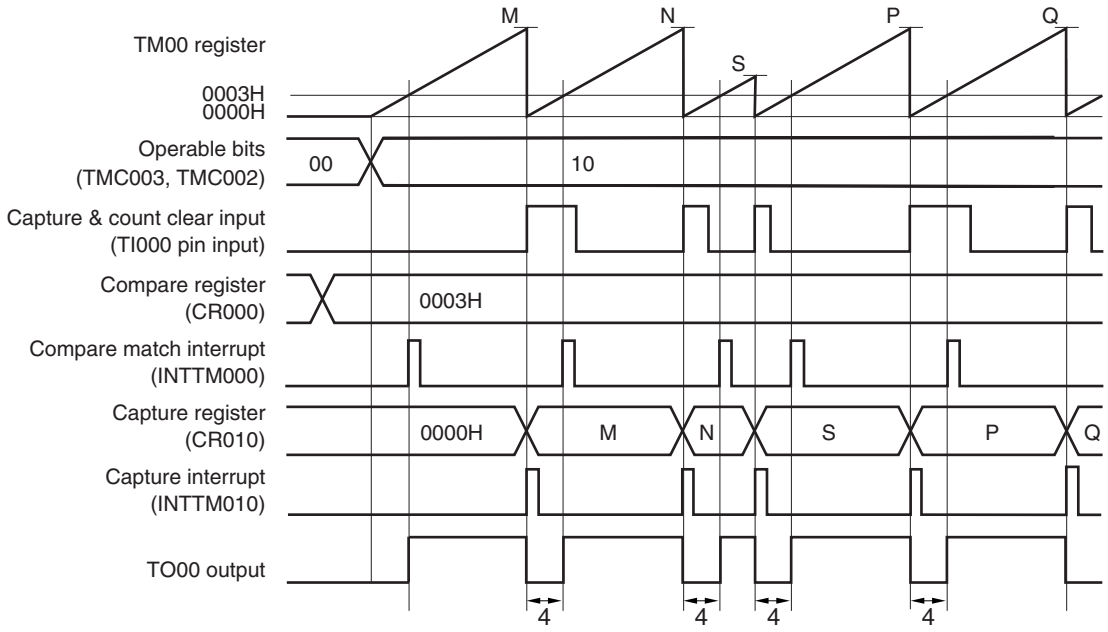
Table 4-12. Settings of PFALL, PF2, PF1, ISC, Port Mode Register, and Output Latch When Using Alternate Function (78K0/LF3) (1/2)

Pin Name	Alternate Function		PFALL, PF2[Note 4]	PF1	ISC	PM××	P××
	Function Name	I/O					
P10	PCL	Output	–			0	0
P11	$\overline{SCK10}$	Input	–			1	×
		Output	–			0	1
P12	SI10	Input	–			1	×
	RxD0	Input	–			1	×
P13[Note 10]	SO10	Output	–	PF13 = 0		0	0
	TxD0	Output	–	PF13 = 1		0	×
P14	$\overline{SCKA0}$	Input	–			1	×
		Output	–			0	1
	INTP4	Input	–			1	×
P15	SIA0	Input	–			1	×
	<RxD6>	Input	–		ISC4 = 1[Note 5, 7], ISC5 = 0	1	×
P16[Note 11]	SOA0	Output	–	PF16 = 0		0	0
	<TxD6>	Output	–	PF16 = 1	ISC4 = 1, ISC5 = 0	0	×
P20 to P27[Note 2]	SEG39 to SEG32[Note 12]	Output	1			×	×
	ANI0 to ANI7[Note 1]	Input	0			1	×
	DS0± to DS2±[Note 8]	Input	0			1	×
	REF±[Note 8]	Input	0			1	×
P30	INTP5	Input	–			1	×
P31	TOH1	Output	–			0	0
	INTP3	Input	–			1	×
P32	TOH0	Output	–			0	0
	MCGO	Output	–			0	0
P33	TI000	Input	–		ISC1 = 0	1	×
	RTCDIV	Output	–			0	0
	RTCCL	Output	–			0	0
	BUZ	Output	–			0	0
	INTP2	Input	–			1	×
P34	TI52	Input	–		**Note 6**	1	×
	TI010	Input	–			1	×
	TO00	Output	–			0	0
	RTC1HZ	Output	–			0	0
	INTP1	Input	–			1	×

(Notes and Remarks are listed on the page after next.)

Figure 6-26. Timing Example of Clear & Start Mode Entered by TI000 Pin Valid Edge Input (CR000: Compare Register, CR010: Capture Register) (2/2)

(b) TOC00 = 13H, PRM00 = 10H, CRC00, = 04H, TMC00 = 0AH, CR000 = 0003H



This is an application example where the width set to CR000 (4 clocks in this example) is to be output from the TO00 pin when the count value has been captured & cleared.

The count value is captured to CR010, a capture interrupt signal (INTTM010) is generated, TM00 is cleared (to 0000H), and the TO00 output is inverted when the valid edge of the TI000 pin is detected. When the count value of TM00 is 0003H (four clocks have been counted), a compare match interrupt signal (INTTM000) is generated and the TO00 output level is inverted.

6.4.6 PPG output operation

A square wave having a pulse width set in advance by CR010 is output from the TO00 pin as a PPG (Programmable Pulse Generator) signal during a cycle set by CR000 when bits 3 and 2 (TMC003 and TMC002) of 16-bit timer mode control register 00 (TMC00) are set to 11 (clear & start upon a match between TM00 and CR000).

The pulse cycle and duty factor of the pulse generated as the PPG output are as follows.

- Pulse cycle = (Set value of CR000 + 1) × Count clock cycle
- Duty = (Set value of CR010 + 1) / (Set value of CR000 + 1)

Caution To change the duty factor (value of CR010) during operation, see 6.5.1 Rewriting CR010 during TM00 operation.

Remarks 1. For the setting of I/O pins, see **6.3 (6) Port mode register 0 (PM0)**.

2. For how to enable the INTTM000 signal interrupt, see **CHAPTER 21 INTERRUPT FUNCTIONS**.

Figure 6-41. Block Diagram of PPG Output Operation

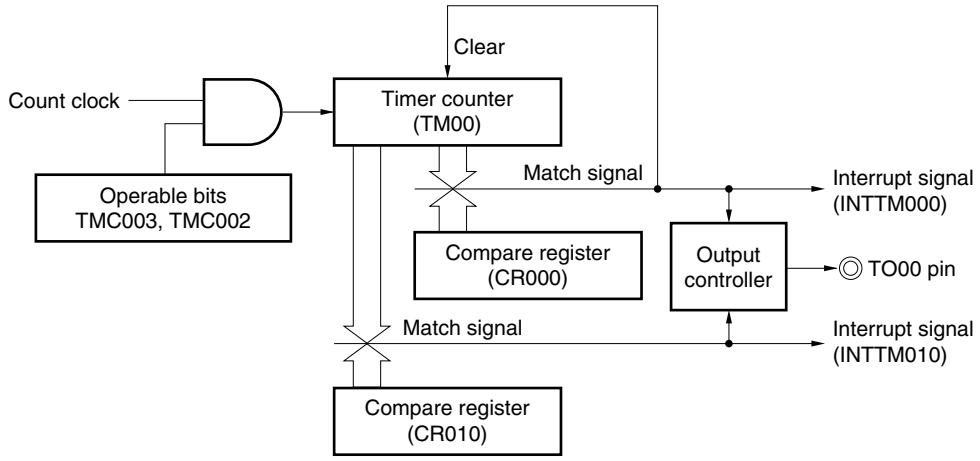


Figure 7-9. Format of 8-Bit Timer Mode Control Register 50 (TMC50) (2/2)

(b) 78K0/LE3, 78K0/LF3

Address: FF6BH After reset: 00H R/W[Note]

Symbol	<7>	6	5	4	<3>	<2>	1	<0>
TMC50	TCE50	TMC506	0	0	LVS50	LVR50	TMC501	TOE50

TCE50	TM50 count operation control
0	After clearing to 0, count operation disabled (counter stopped)
1	Count operation start

TMC506	TM50 operating mode selection
0	Mode in which clear & start occurs on a match between TM50 and CR50
1	PWM (free-running) mode

LVS50	LVR50	Timer output F/F status setting
0	0	No change
0	1	Timer output F/F clear (0) (default value of TO50 output: low level)
1	0	Timer output F/F set (1) (default value of TO50 output: high level)
1	1	Setting prohibited

TMC501	In other modes (TMC506 = 0)	In PWM mode (TMC506 = 1)
	Timer F/F control	Active level selection
0	Inversion operation disabled	Active-high
1	Inversion operation enabled	Active-low

TOE50	Timer output control
0	Output disabled (TO50 output is low level)
1	Output enabled

Note Bits 2 and 3 are write-only.

Cautions 1. The settings of LVS50 and LVR50 are valid in other than PWM mode.

2. Perform <1> to <4> below in the following order, not at the same time.

<1> Set TMC501, TMC506: Operation mode setting

<2> Set TOE50 to enable output: Timer output enable

<3> Set LVS50, LVR50(see Caution 1): Timer F/F setting

<4> Set TCE50

3. When TCE50 = 1, setting the other bits of TMC50 is prohibited.

4. The actual TO50/TI50/P44/KR4 is determined depending on PM44 and P44, besides TO5n output.

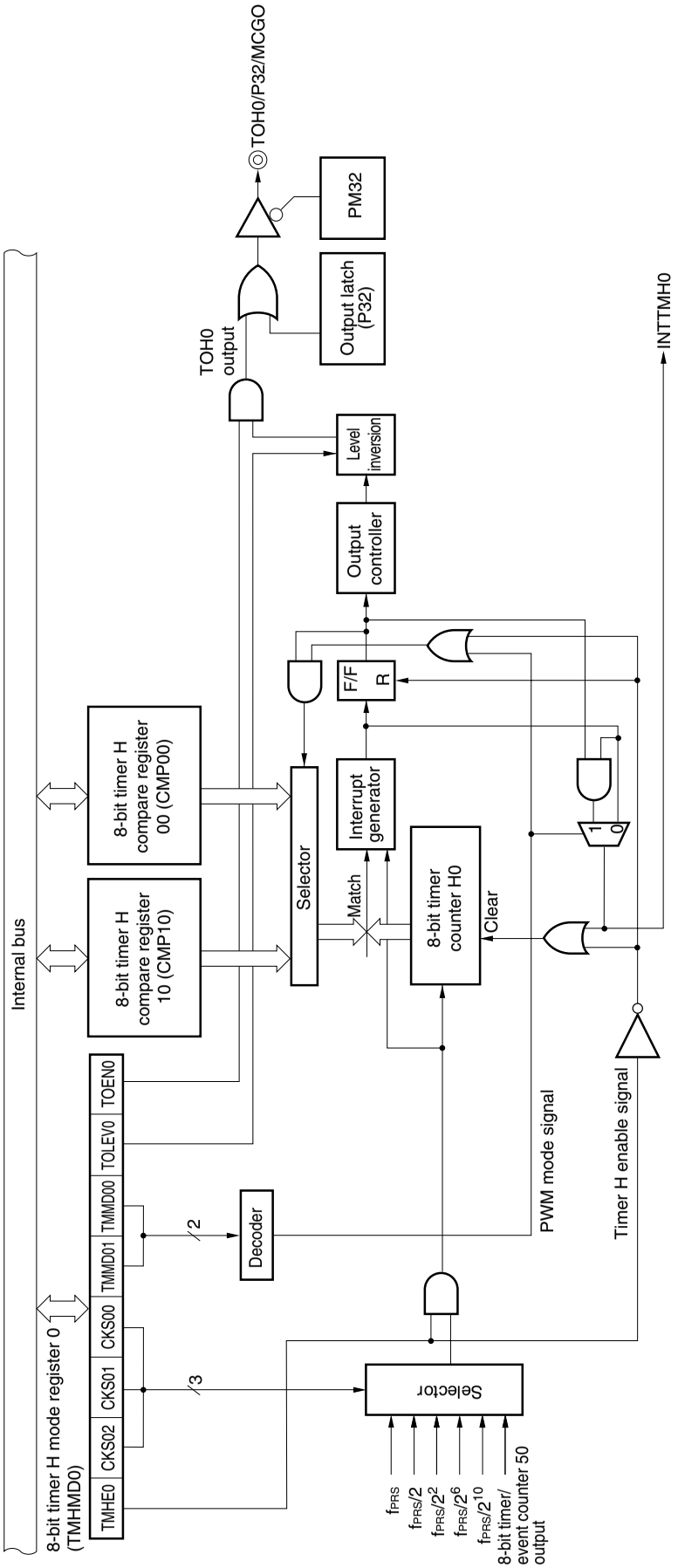
5. Be sure to clear bits 4 and 5 to "0".

Remarks 1. In PWM mode, PWM output is made inactive by clearing TCE50 to 0.

2. If LVS50 and LVR50 are read, the value is 0.

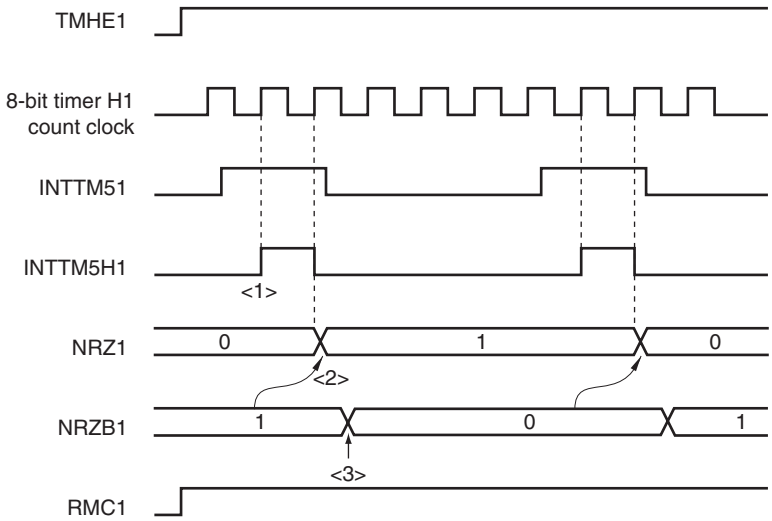
3. The values of the TMC506, LVS50, LVR50, TMC5n1, and TOE50 bits are reflected at the TO50 pin regardless of the value of TCE50.

Figure 8-1. Block Diagram of 8-Bit Timer H0



To control the carrier pulse output during a count operation, the NRZ1 and NRZB1 bits of the TMCYC1 register have a master and slave bit configuration. The NRZ1 bit is read-only but the NRZB1 bit can be read and written. The INTTM51 signal is synchronized with the 8-bit timer H1 count clock and is output as the INTTM5H1 signal. The INTTM5H1 signal becomes the data transfer signal of the NRZ1 bit, and the NRZB1 bit value is transferred to the NRZ1 bit. The timing for transfer from the NRZB1 bit to the NRZ1 bit is as shown below.

Figure 8-15. Transfer Timing



<1> The INTTM51 signal is synchronized with the count clock of the 8-bit timer H1 and is output as the INTTM5H1 signal.

<2> The value of the NRZB1 bit is transferred to the NRZ1 bit at the second clock from the rising edge of the INTTM5H1 signal.

<3> Write the next value to the NRZB1 bit in the interrupt servicing program that has been started by the INTTM5H1 interrupt or after timing has been checked by polling the interrupt request flag. Write data to count the next time to the CR51 register.

Cautions 1. Do not rewrite the NRZB1 bit again until at least the second clock after it has been rewritten, or else the transfer from the NRZB1 bit to the NRZ1 bit is not guaranteed.

2. When the 8-bit timer/event counter 51 is used in the carrier generator mode, an interrupt is generated at the timing of <1>. When the 8-bit timer/event counter 51 is used in a mode other than the carrier generator mode, the timing of the interrupt generation differs.

Remark INTTM5H1 is an internal signal and not an interrupt source.

ANI0/P20 to ANI7/P27 pins are as shown below depending on the settings of PF2, ADPC0, PM2, ADS, and ADDCTL0.

Table 12-3. Setting Functions of P20/ANI0 to P27/ANI7 Pins

(a) μPD78F041x, 78F043x, 78F045x, 78F048x

PF2	ADPC0	PM2	ADS	P20/SEGxx/ANI0 to P27/SEGxx/ANI7 Pins
Digital/Analog selection	Analog input selection	Input mode	Does not select ANI.	Analog input (not to be converted)
			Selects ANI.	Analog input (to be converted by successive approximation type A/D converter)
		Output mode	–	Setting prohibited
	Digital I/O selection	Input mode	–	Digital input
		Output mode	–	Digital output
SEG output selection	–	–	–	Segment output

(b) μPD78F046x, 78F049x

ADPC0	PM2	ADS	ADDCTL0	P20/ANI0/DS0- to P27/ANI7/REF+ Pins
Analog input selection	Input mode	Does not select ANI.	Does not select DSn±.	Analog input (not to be converted)
		Selects ANI.	Does not select DSn±.	Analog input (to be converted by successive approximation type A/D converter)
		Does not select ANI.	Selects DSn±.	Analog input (to be converted by ΔΣ-type A/D converter)
		Selects ANI.	Selects DSn±.	Setting prohibited
	Output mode	–		Setting prohibited
Digital I/O selection	Input mode	–		Digital input
	Output mode	–		Digital output

14.4 Operation of Serial Interface UART0

Serial interface UART0 has the following two modes.

- Operation stop mode
- Asynchronous serial interface (UART) mode

14.4.1 Operation stop mode

In this mode, serial communication cannot be executed, thus reducing the power consumption. In addition, the pins can be used as ordinary port pins in this mode. To set the operation stop mode, clear bits 7, 6, and 5 (POWER0, TXE0, and RXE0) of ASIM0 to 0.

(1) Register used

The operation stop mode is set by asynchronous serial interface operation mode register 0 (ASIM0).

ASIM0 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets this register to 01H.

Address: FF70H After reset: 01H R/W

Symbol	<7>	<6>	<5>	4	3	2	1	0
ASIM0	POWER0	TXE0	RXE0	PS01	PS00	CL0	SL0	1

POWER0	Enables/disables operation of internal operation clock
0[Note 1]	Disables operation of the internal operation clock (fixes the clock to low level) and asynchronously resets the internal circuit[Note 2].

TXE0	Enables/disables transmission
0	Disables transmission (synchronously resets the transmission circuit).

RXE0	Enables/disables reception
0	Disables reception (synchronously resets the reception circuit).

Notes 1. The input from the RxD0 pin is fixed to high level when POWER0 = 0.

2. Asynchronous serial interface reception error status register 0 (ASIS0), transmit shift register 0 (TXS0), and receive buffer register 0 (RXB0) are reset.

Caution Clear POWER0 to 0 after clearing TXE0 and RXE0 to 0 to set the operation stop mode. To start the communication, set POWER0 to 1, and then set TXE0 or RXE0 to 1.

Remark To use the RxD0/P12 and TxD0/P13 pins as general-purpose port pins, see **CHAPTER 4 PORT FUNCTIONS**.

(3) Example of setting baud rate

Table 15-5. Set Data of Baud Rate Generator

Baud Rate [bps]	f_{PRS} = 2.0 MHz				f_{PRS} = 5.0 MHz				f_{PRS} = 10.0 MHz			
	TPS63-TPS60	k	Calculated Value	ERR [%]	TPS63-TPS60	k	Calculated Value	ERR [%]	TPS63-TPS60	k	Calculated Value	ERR [%]
300	8H	13	301	0.16	7H	65	301	0.16	8H	65	301	0.16
600	7H	13	601	0.16	6H	65	601	0.16	7H	65	601	0.16
1200	6H	13	1202	0.16	5H	65	1202	0.16	6H	65	1202	0.16
2400	5H	13	2404	0.16	4H	65	2404	0.16	5H	65	2404	0.16
4800	4H	13	4808	0.16	3H	65	4808	0.16	4H	65	4808	0.16
9600	3H	13	9615	0.16	2H	65	9615	0.16	3H	65	9615	0.16
19200	2H	13	19231	0.16	1H	65	19231	0.16	2H	65	19231	0.16
24000	1H	21	23810	−0.79	3H	13	24038	0.16	4H	13	24038	0.16
31250	1H	16	31250	0	4H	5	31250	0	5H	5	31250	0
38400	1H	13	38462	0.16	0H	65	38462	0.16	1H	65	38462	0.16
48000	0H	21	47619	−0.79	2H	13	48077	0.16	3H	13	48077	0.16
76800	0H	13	76923	0.16	0H	33	75758	−1.36	0H	65	76923	0.16
115200	0H	9	111111	−3.55	1H	11	113636	−1.36	0H	43	116279	0.94
153600	–	–	–	–	1H	8	156250	1.73	0H	33	151515	−1.36
312500	–	–	–	–	0H	8	312500	0	1H	8	312500	0
625000	–	–	–	–	0H	4	625000	0	1H	4	625000	0

Remark TPS63 to TPS60: Bits 3 to 0 of clock selection register 6 (CKSR6) (setting of base clock (f_{XCLK6}))
k: Value set by MDL67 to MDL60 bits of baud rate generator control register 6 (BRGC6) (k = 4, 5, 6, ..., 255)
f_{PRS}: Peripheral hardware clock frequency
ERR: Baud rate error

(3) Priority specification flag registers (PR0L, PR0H, PR1L, PR1H)

The priority specification flag registers are used to set the corresponding maskable interrupt priority order.

PR0L, PR0H, PR1L, and PR1H are set by a 1-bit or 8-bit memory manipulation instruction. If PR0L and PR0H, and PR1L and PR1H are combined to form 16-bit registers PR0 and PR1, they are set by a 16-bit memory manipulation instruction.

Reset signal generation sets these registers to FFH.

Figure 21-4. Format of Priority Specification Flag Registers (PR0L, PR0H, PR1L, PR1H) (1/4)

(a) 78K0/LC3

Address: FFE8H After reset: FFH R/W

Symbol	<7>	6	5	<4>	<3>	<2>	<1>	<0>
PR0L	SREPR6	1	1	PPR3	PPR2	PPR1	PPR0	LVIPR

Address: FFE9H After reset: FFH R/W

Symbol	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
PR0H	TMPR010	TMPR000	TMPR50	TMPRH0	TMPRH1	STPR0	STPR6	SRPR6

Address: FFEAH After reset: FFH R/W

Symbol	<7>	6	<5>	<4>	<3>	<2>	<1>	<0>
PR1L	TMPR52	1	RTCIPR	KRPR	TMPR51	RTCPR	SRPR0	ADPR[Note]

Address: FFEBH After reset: FFH R/W

Symbol	7	6	5	4	3	2	<1>	<0>
PR1H	1	1	1	1	1	1	MCGPR	TMHPR2

XXPRX	Priority level selection
0	High priority level
1	Low priority level

Note μPD78F041x only.

Caution Be sure to set bits 5 and 6 of PR0L, bit 6 of PR1L, and bits 2 to 7 of PR1H to 1.

26.5 Cautions for Low-Voltage Detector

In a system where the supply voltage (V_{DD}) fluctuates for a certain period in the vicinity of the LVI detection voltage (V_{LVI}), the operation is as follows depending on how the low-voltage detector is used.

(1) When used as reset

The system may be repeatedly reset and released from the reset status.

In this case, the time from release of reset to the start of the operation of the microcontroller can be arbitrarily set by taking action (1) below.

(2) When used as interrupt

Interrupt requests may be frequently generated. Take (b) of action (2) below.

<Action>

(1) When used as reset

After releasing the reset signal, wait for the supply voltage fluctuation period of each system by means of a software counter that uses a timer, and then initialize the ports (see **Figure 26-9**).

(2) When used as interrupt

(a) Confirm that "supply voltage (V_{DD}) ≥ detection voltage (V_{LVI})" when detecting the falling edge of V_{DD}, or "supply voltage (V_{DD}) < detection voltage (V_{LVI})" when detecting the rising edge of V_{DD}, in the servicing routine of the LVI interrupt by using bit 0 (LVIF) of the low-voltage detection register (LVIM). Clear bit 0 (LVIIF) of interrupt request flag register 0L (IF0L) to 0.

(b) In a system where the supply voltage fluctuation period is long in the vicinity of the LVI detection voltage, wait for the supply voltage fluctuation period, confirm that "supply voltage (V_{DD}) ≥ detection voltage (V_{LVI})" when detecting the falling edge of V_{DD}, or "supply voltage (V_{DD}) < detection voltage (V_{LVI})" when detecting the rising edge of V_{DD}, using the LVIF flag, and clear the LVIIF flag to 0.

Remark If bit 2 (LVISEL) of the low voltage detection register (LVIM) is set to "1", the meanings of the above words change as follows.

- Supply voltage (V_{DD}) → Input voltage from external input pin (EXLVI)
- Detection voltage (V_{LVI}) → Detection voltage (V_{EXLVI} = 1.21 V)

CHAPTER 27 OPTION BYTE

27.1 Functions of Option Bytes

The flash memory at 0080H to 0084H of the 78K0/Lx3 microcontrollers is an option byte area. When power is turned on or when the device is restarted from the reset status, the device automatically references the option bytes and sets specified functions. When using the product, be sure to set the following functions by using the option bytes.

When the boot swap operation is used during self-programming, 0080H to 0084H are switched to 1080H to 1084H. Therefore, set values that are the same as those of 0080H to 0084H to 1080H to 1084H in advance.

Caution Be sure to set 00H to 0082H and 0083H (0082H/1082H and 0083H/1083H when the boot swap function is used).

(1) 0080H/1080H

- Internal low-speed oscillator operation
  - Can be stopped by software
  - Cannot be stopped
- Watchdog timer overflow time setting
- Watchdog timer counter operation
  - Enabled counter operation
  - Disabled counter operation
- Watchdog timer window open period setting

Caution Set a value that is the same as that of 0080H to 1080H because 0080H and 1080H are switched during the boot swap operation.

(2) 0081H/1081H

- Selecting POC mode
  - During 2.7 V/1.59 V POC mode operation (POCMODE = 1)
    The device is in the reset state upon power application and until the supply voltage reaches 2.7 V (TYP.). It is released from the reset state when the voltage exceeds 2.7 V (TYP.). After that, POC is not detected at 2.7 V but is detected at 1.59 V (TYP.).
    If the supply voltage rises to 1.8 V after power application at a pace slower than 0.5 V/ms (MIN.), use of the 2.7 V/1.59 V POC mode is recommended.
  - During 1.59 V POC mode operation (POCMODE = 0)
    The device is in the reset state upon power application and until the supply voltage reaches 1.59 V (TYP.). It is released from the reset state when the voltage exceeds 1.59 V (TYP.). After that, POC is detected at 1.59 V (TYP.), in the same manner as on power application.

Caution POCMODE can only be written by using a dedicated flash memory programmer. It cannot be set during self-programming or boot swap operation during self-programming. However, because the value of 1081H is copied to 0081H during the boot swap operation, it is recommended to set a value that is the same as that of 0081H to 1081H when the boot swap function is used.

(2) Non-port functions

Port		78K0/LC3	78K0/LD3	78K0/LE3	78K0/LF3
Power supply, ground		V_{DD}, V_{SS}, V_{LC0} to V_{LC3}, AV_{REF}[Note 1], AV_{SS}[Note 1]			
Regulator		REGC			
Reset		$\overline{\text{RESET}}$			
Clock oscillation		X1, X2, XT1, XT2, EXCLK			
Writing to flash memory		FLMD0			
Interrupt		INTP0 to INTP3		INTP0 to INTP4	INTP0 to INTP5
Key interrupt		KR0, KR3, KR4	KR0 to KR4		KR0 to KR7
Timer	TM00	TI000, TI010, TO00			
	TM50	–		TI50, TO50	
	TM51	–		TI51, TO51	
	TM52	TI52			
	TMH0	TOH0			
	TMH1	TOH1			
	RTC	RTC1HZ, RTCCL, RTCDIV			
Serial interface	UART0	RxD0, TxD0			
	UART6	RxD6, TxD6			
	CSI10	–	$\overline{\text{SCK10}}$, SI10, SO10		
	CSIA0	–			$\overline{\text{SCKA0}}$, SIA0, SOA0
LCD	SEG	SEG0 to SEG21	SEG0 to SEG23	SEG0 to SEG23, SEG24 to SEG31[Note 2]	SEG0 to SEG31, SEG32 to SEG39[Note 3]
	COM	COM0-COM7			
Segment key source signal output		SEG8(KS0) to SEG15(KS7)	SEG10(KS0) to SEG17(KS7)	SEG16(KS0) to SEG23(KS7)	SEG24(KS0) to SEG31(KS7)
10-bit successive approximation type A/D		ANI0 to ANI5[Note 4]		ANI0 to ANI7[Note 5]	
16-bit ΔΣ-type A/D		–		DS0+ to DS2+[Note 6], DS0- to DS2-[Note 6], REF+[Note 6], REF-[Note 6]	
Clock output		–			PCL
Buzzer output		BUZ			
Remote controller receiver		–	RIN		
Manchester code generator		MCGO			
LVI circuit		EXLVI			
On-chip debug function		OCD0A, OCD0B			

Notes 1. μPD78F041x, 78F043x, 78F045x, 78F046x, 78F048x and 78F049x only.

2. μPD78F044x and 78F045x only.

3. μPD78F047x and 78F048x only.

4. μPD78F041x and 78F043x only.

5. μPD78F045x, 78F046x, 78F048x and 78F049x only.

6. μPD78F046x and 78F049x only.

SALES OFFICES Renesas Electronics Corporation http://www.renesas.com

Refer to "http://www.renesas.com/" for the latest and detailed information.

Renesas Electronics America Inc.
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
7F, No. 363 Fu Shing North Road Taipei, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
1 harbourFront Avenue, #06-10, keppel Bay Tower, Singapore 098632
Tel: +65-6213-0200, Fax: +65-6278-8001

Renesas Electronics Malaysia Sdn.Bhd.
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.
11F., Samik Lavied' or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

Colophon 1.0