Renesas Electronics America Inc - UPD78F0454GA-HAB-AX Datasheet

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	78K/0
Core Size	8-Bit
Speed	10MHz
Connectivity	3-Wire SIO, LINbus, UART/USART
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	46
Program Memory Size	48KB (48K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0454ga-hab-ax

1.3 Ordering Information

[Part Number]

μPD78F04xy XX - XXX - XX

	Semiconductor	
AX	Lead-free	Product contains no lead in any area (Terminal finish is Ni/Pd/Au plating)

		Package Type
40y, 41y (LC3)	GA-GAM	48-pin plastic LQFP (fine pitch) (7x7)
42y, 43y (LD3)	GB-GAG	52-pin plastic LQFP (10x10)
44y, 45y, 46y (LE3)	GB-GAH	64-pin plastic LQFP (fine pitch) (10x10)
	GK-GAJ	64-pin plastic LQFP (12x12)
45y (LE3)	GA-HAB	64-pin plastic TQFP (fine pitch) (7x7)
47y, 48y, 49y (LF3)	GC-GAD	80-pin plastic LQFP (14x14)
	GK-GAK	80-pin plastic LQFP (fine pitch) (12x12)

	High-speed RAM Capacity	Expansion RAM Capacity	Flash Memory Capacity
4x0	512 bytes	-	8 KB
4x1	768 bytes	-	16 KB
4x2	1 KB	-	24 KB
4x3	1 KB	-	32 KB
4x4	1 KB	1 KB	48 KB
4x5	1 KB	1 KB	60 KB

	Product Type
F	Flash memory version

1.5 Pin Identification

ANI0 to ANI7:	Analog input	REF+:	ΔΣ Analog reference voltage (+)
AV_{REF}:	Analog reference voltage	REF−:	ΔΣ Analog reference voltage (−)
AV_{SS}:	Analog ground	RIN:	Remote control input
BUZ:	Buzzer output	RTC1HZ:	Real-time counter correction clock (1 Hz) output
COM0 to COM7:	Common output		
DS0+ to DS2+:	ΔΣ Analog input (+)	RTCCL:	Real-time counter clock (32.768 kHz original oscillation) output
DS0− to DS2−:	ΔΣ Analog input (−)		
EXCLK:	External clock input (main system clock)	RTCDIV:	Real-time counter clock (32.768 kHz divided frequency) output
EXLVI:	External potential input for low-voltage detector	SEG0 to SEG39:	Segment output
		SEGxx (KS0)	
FLMD0:	Flash programming mode	to SEGxx (KS7):	Segment key scan
INTP0 to INTP5:	External interrupt input	$\overline{SCK10}$:	Serial clock input/output
KR0 to KR7:	Key return	$\overline{SCKA0}$:	Serial clock input/output
MCGO:	Manchester code generator output	SI10:	Serial data input
OCD0A, OCD0B:	On chip debug input/output	SIA0:	Serial data input
P10 to P17:	Port 1	SO10:	Serial data output
P20 to P27:	Port 2	SOA0:	Serial data output
P30 to P34:	Port 3	TI000, TI010:	Timer input
P40 to P47:	Port 4	TI50, TI51, TI52:	Timer input
P80 to P83:	Port 8	TO00:	Timer output
P90 to P93:	Port 9	TO50, TO51:	Timer output
P100 to P103:	Port 10	TOH0, TOH1:	Timer output
P110 to P113:	Port 11	TxD0, TxD6:	Transmit data
P120 to P124:	Port 12	V_{DD}:	Power supply
P130 to P133:	Port 13	V_{SS}:	Ground
P140 to P143:	Port 14	V_{LC0} to V_{LC3}:	LCD power supply
P150 to P153:	Port 15	X1, X2:	Crystal oscillator (main system clock)
PCL:	Programmable clock output		
REGC:	Regulator capacitance	XT1, XT2:	Crystal oscillator (subsystem clock)
$\overline{RESET}$:	Reset		
RxD0, RxD6:	Receive data		

2.2.7 P100 to P103 (port 10)

P100 to P103 function as an I/O port. These pins also function as segment signal output pins for the LCD controller/driver. Either I/O port function or segment signal output function can be selected using port function register ALL (PFALL).

78K0/LC3	78K0/LD3	78K0/LE3	78K0/LF3
P100/SEG4	P100/SEG5	P100/SEG8	P100/SEG12
P101/SEG5	P101/SEG6	P101/SEG9	P101/SEG13
–	–	P102/SEG10	P102/SEG14
–	–	P103/SEG11	P103/SEG15

The following operation modes can be specified in 1-bit units.

(1) Port mode

P100 to P103 function as an I/O port. P100 to P103 can be set to input or output port in 1-bit units using port mode register 10 (PM10). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 10 (PU10).

(2) Control mode

P100 to P103 function as segment signal output for the LCD controller/driver.

(a) SEGxx

These pins are the segment signal output pins for the LCD controller/driver.

2.2.8 P110 to P113 (port 11)

P110 to P113 function as an I/O port. These pins also function as pins for segment signal output for the LCD controller/driver and serial interface data I/O. Either I/O port function (other than segment signal output) or segment signal output function can be selected using port function register ALL (PFALL).

78K0/LC3	78K0/LD3	78K0/LE3	78K0/LF3
–	–	P110/SEG12	P110/SEG16
–	P111/SEG7	P111/SEG13	P111/SEG17
P112/SEG6/TxD6	P112/SEG8/TxD6	P112/SEG14/TxD6	P112/SEG18/TxD6
P113/SEG7/RxD6	P113/SEG9/RxD6	P113/SEG15/RxD6	P113/SEG19/RxD6

The following operation modes can be specified in 1-bit units.

(1) Port mode

P110 to P113 function as an I/O port. P110 to P113 can be set to input or output port in 1-bit units using port mode register 11 (PM11). Use of an on-chip pull-up resistor can be specified by pull-up resistor option register 11 (PU11).

(2) Control mode

P110 to P113 function as segment signal output for the LCD controller/driver and serial interface data I/O.

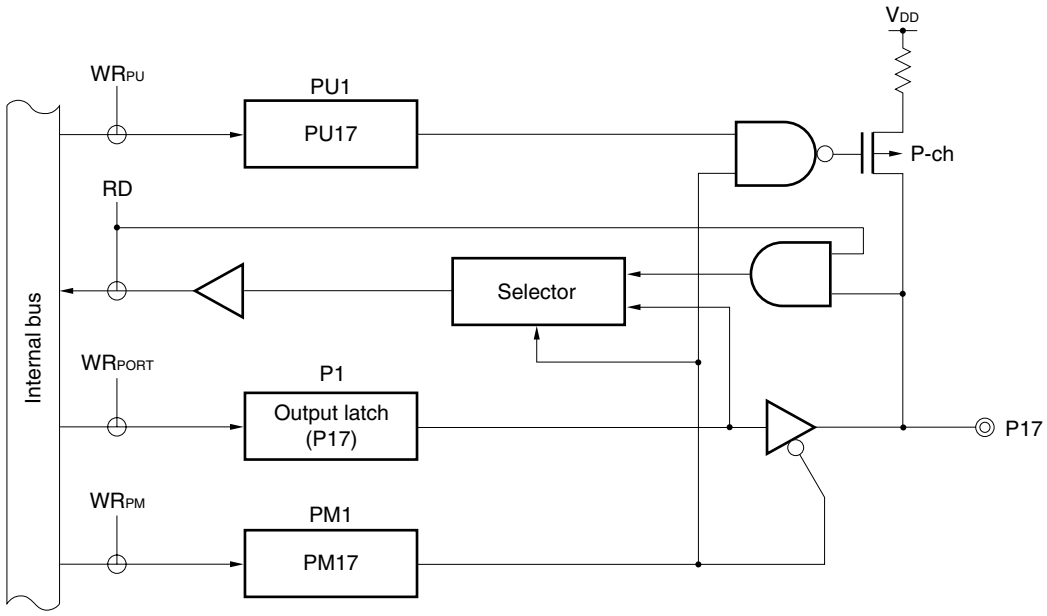
(a) SEGxx

These pins are the segment signal output pins for the LCD controller/driver.

(b) RxD6

This is a serial data input pin of serial interface UART6.

Figure 4-6. Block Diagram of P17



P1: Port register 1
PU1: Pull-up resistor option register 1
PM1: Port mode register 1
RD: Read signal
WR××: Write signal

Table 4-9. Settings of PFALL, PF2, PF1, ISC, Port Mode Register, and Output Latch When Using Alternate Function (78K0/LCF3) (2/2)

Pin Name	Alternate Function		PFALL, PF2[Note 4]	ISC	PM××	P××
	Function Name	I/O				
P113	SEG7	Output	1	ISC3 = 0	×	×
	RxD6	Input	0	ISC3 = 1, ISC4 = ISC5 = 0[Notes 5, 7]	1	×
P120	EXLVI	Input	–		1	×
	INTP0	Input	–	ISC0 = 0	1	×
P121	X1[Note 3]	–	–		×	×
	OCD0A	–	–		×	×
P122	X2[Note 3]	–	–		×	×
	EXCLK[Note 3]	Input	–		×	×
	OCD0B	–	–		×	×
P123	XT1[Note 3]	–	–		×	×
P124	XT2[Note 3]	–	–		×	×
P140 to P143	SEG8(KS0) to SEG11(KS3)	Output	1		×	×
P150 to P153	SEG12(KS4) to SEG15(KS7)	Output	1		×	×

Notes 1. μPD78F041x only.

2. The functions of the P20/ANI0 to P25/ANI5 pins are determined according to the settings of port function register 2 (PF2), A/D port configuration register 0 (ADPC0), port mode register 2 (PM2), analog input channel specification register (ADS). For details, see Table 4-7.

3. When using the P121 to P124 pins to connect a resonator for the main system clock (X1, X2) or subsystem clock (XT1, XT2), or to input an external clock for the main system clock (EXCLK), the X1 oscillation mode, XT1 oscillation mode, or external clock input mode must be set by using the clock operation mode select register (OSCCTL) (for details, see **5.3 (1) Clock operation mode select register (OSCCTL)** and **(3) Setting of operation mode for subsystem clock pin**). The reset value of OSCCTL is 00H (all of the P121 to P124 are Input port pins).

4. Targeted at registers corresponding to each port.

5. RxD6 can be set as the input source for TI000 by setting ISC1 = 1.

6. Input enable of TM52 via TMH2 can be controlled by setting ISC2 = 1.

7. RxD6 can be set as the input source for INTP0 by setting ISC0 = 1.

8. When the P40/KR0/V_{LC3} pin is set to the 1/4 bias method, it is used as V_{LC3}. When the pin is set to another bias method, it is used for the port function (P40) or the key interrupt function (KR0).

9. Set PF13 = 0 when using as port function.

Remarks 1. ×: Don't care
–: Does not apply.
PM××: Port mode register
P××: Port output latch

2. The functions within arrowheads (< >) can be assigned by setting the input switch control register (ISC).

3. X1, X2 pins can be used as on-chip debug mode setting pins (OCD0A, OCD0B) when the on-chip debug function is used. For detail, see **CHAPTER 29 ON-CHIP DEBUG FUNCTION.**

Figure 6-5. Format of 16-Bit Timer Mode Control Register 00 (TMC00)

Address: FFBAH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	<0>
TMC00	0	0	0	0	TMC003	TMC002	TMC001	OVF00

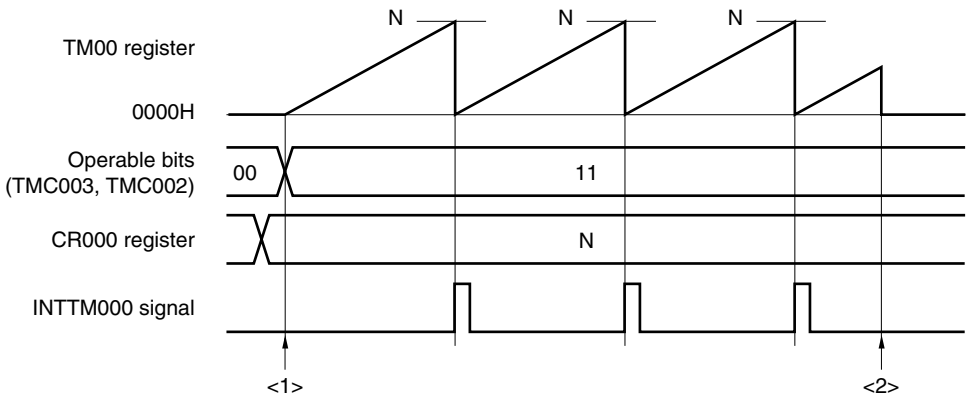
TMC003	TMC002	Operation enable of 16-bit timer/event counter 00
0	0	Disables 16-bit timer/event counter 00 operation. Stops supplying operating clock. Clears 16-bit timer counter 00 (TM00).
0	1	Free-running timer mode
1	0	Clear & start mode entered by TI000 pin valid edge input[Note]
1	1	Clear & start mode entered upon a match between TM00 and CR000

TMC001	Condition to reverse timer output (TO00)
0	• Match between TM00 and CR000 or match between TM00 and CR010
1	• Match between TM00 and CR000 or match between TM00 and CR010 • Trigger input of TI000 pin valid edge

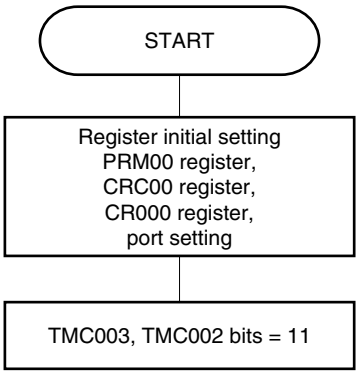
OVF00	TM00 overflow flag
Clear (0)	Clears OVF00 to 0 or TMC003 and TMC002 = 00
Set (1)	Overflow occurs.
OVF00 is set to 1 when the value of TM00 changes from FFFFH to 0000H in all the operation modes (free-running timer mode, clear & start mode entered by TI000 pin valid edge input, and clear & start mode entered upon a match between TM00 and CR000). It can also be set to 1 by writing 1 to OVF00.	

Note The TI000 pin valid edge is set by bits 5 and 4 (ES001, ES000) of prescaler mode register 00 (PRM00).

Figure 6-15. Example of Software Processing for Interval Timer Function



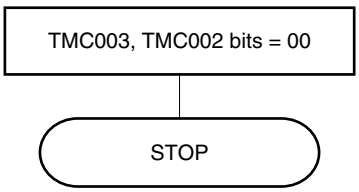
<1> Count operation start flow



Initial setting of these registers is performed before setting the TMC003 and TMC002 bits to 11.

Starts count operation

<2> Count operation stop flow



The counter is initialized and counting is stopped by clearing the TMC003 and TMC002 bits to 00.

(2) Operation in clear & start mode entered by TI000 pin valid edge input
(CR000: compare register, CR010: capture register)

Figure 6-25. Block Diagram of Clear & Start Mode Entered by TI000 Pin Valid Edge Input (CR000: Compare Register, CR010: Capture Register)

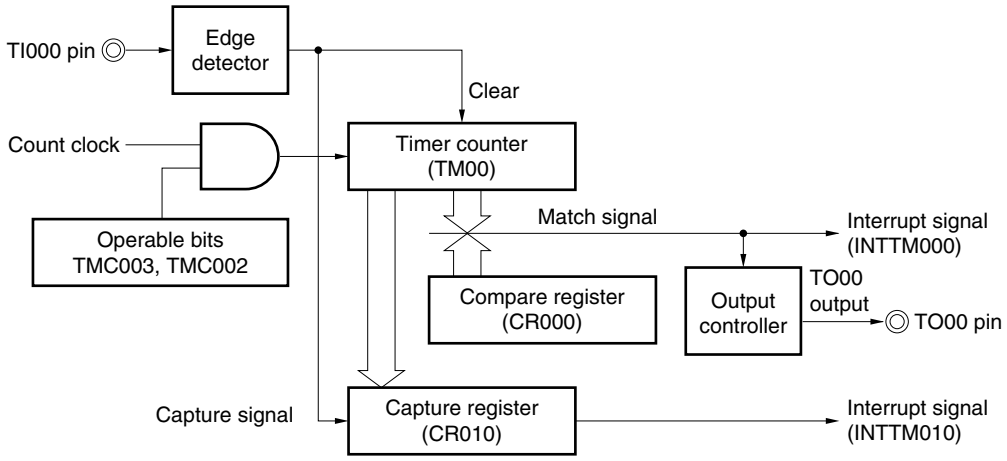
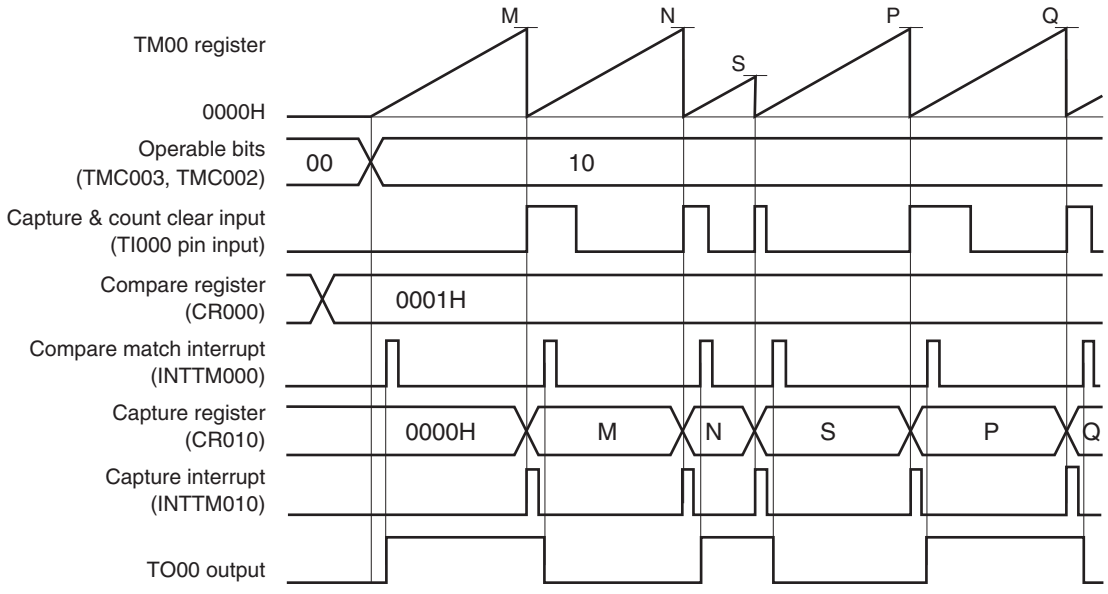


Figure 6-26. Timing Example of Clear & Start Mode Entered by TI000 Pin Valid Edge Input (CR000: Compare Register, CR010: Capture Register) (1/2)

(a) TOC00 = 13H, PRM00 = 10H, CRC00, = 04H, TMC00 = 08H, CR000 = 0001H

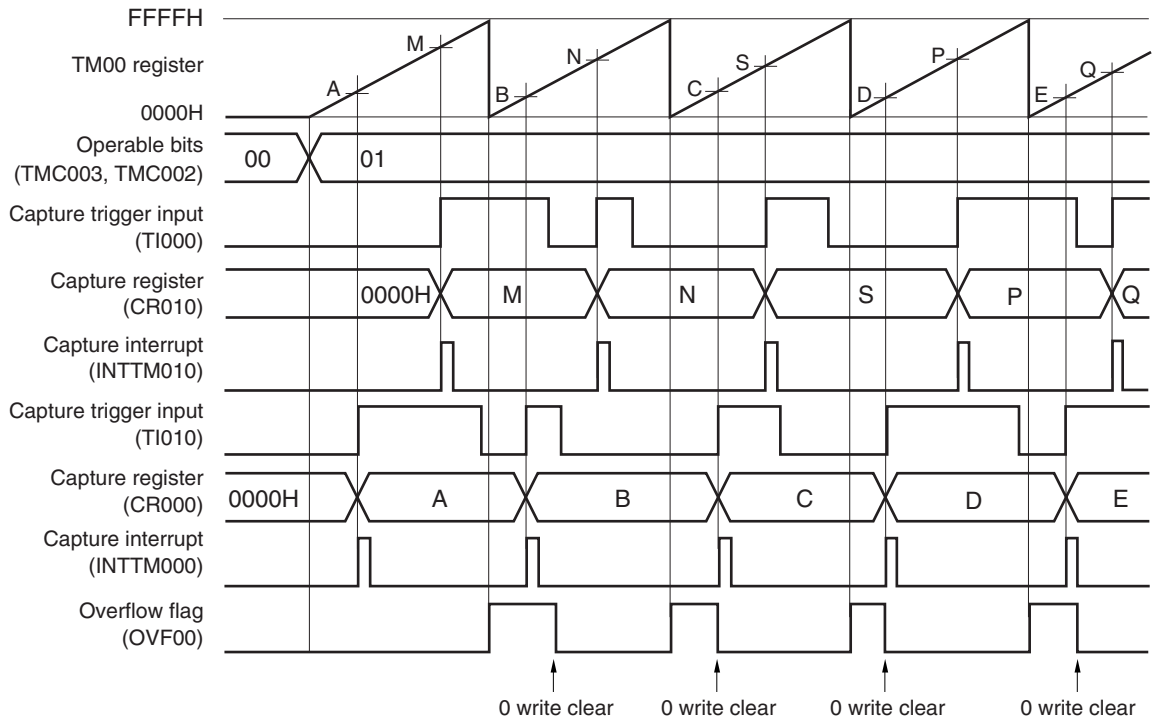


This is an application example where the TO00 output level is inverted when the count value has been captured & cleared.

The count value is captured to CR010 and TM00 is cleared (to 0000H) when the valid edge of the TI000 pin is detected. When the count value of TM00 is 0001H, a compare match interrupt signal (INTTM000) is generated, and the TO00 output level is inverted.

Figure 6-38. Timing Example of Free-Running Timer Mode (CR000: Capture Register, CR010: Capture Register) (1/2)

(a) TOC00 = 13H, PRM00 = 50H, CRC00 = 05H, TMC00 = 04H



This is an application example where the count values that have been captured at the valid edges of separate capture trigger signals are stored in separate capture registers in the free-running timer mode.

The count value is captured to CR010 when the valid edge of the TI000 pin input is detected and to CR000 when the valid edge of the TI010 pin input is detected.

Figure 7-3. Block Diagram of 8-Bit Timer/Event Counter 52

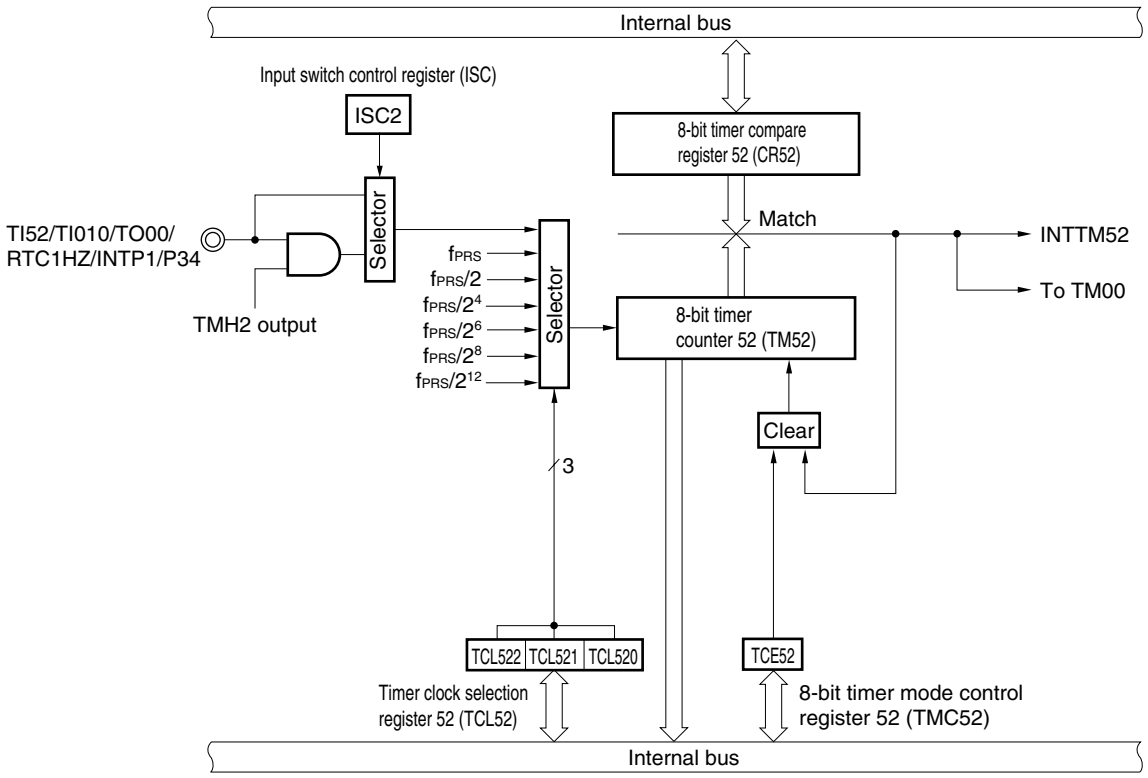


Figure 7-9. Format of 8-Bit Timer Mode Control Register 50 (TMC50) (2/2)

(b) 78K0/LE3, 78K0/LF3

Address: FF6BH After reset: 00H R/W[Note]

Symbol	<7>	6	5	4	<3>	<2>	1	<0>
TMC50	TCE50	TMC506	0	0	LVS50	LVR50	TMC501	TOE50

TCE50	TM50 count operation control
0	After clearing to 0, count operation disabled (counter stopped)
1	Count operation start

TMC506	TM50 operating mode selection
0	Mode in which clear & start occurs on a match between TM50 and CR50
1	PWM (free-running) mode

LVS50	LVR50	Timer output F/F status setting
0	0	No change
0	1	Timer output F/F clear (0) (default value of TO50 output: low level)
1	0	Timer output F/F set (1) (default value of TO50 output: high level)
1	1	Setting prohibited

TMC501	In other modes (TMC506 = 0)	In PWM mode (TMC506 = 1)
	Timer F/F control	Active level selection
0	Inversion operation disabled	Active-high
1	Inversion operation enabled	Active-low

TOE50	Timer output control
0	Output disabled (TO50 output is low level)
1	Output enabled

Note Bits 2 and 3 are write-only.

Cautions 1. The settings of LVS50 and LVR50 are valid in other than PWM mode.

2. Perform <1> to <4> below in the following order, not at the same time.

<1> Set TMC501, TMC506: Operation mode setting

<2> Set TOE50 to enable output: Timer output enable

<3> Set LVS50, LVR50(see Caution 1): Timer F/F setting

<4> Set TCE50

3. When TCE50 = 1, setting the other bits of TMC50 is prohibited.

4. The actual TO50/TI50/P44/KR4 is determined depending on PM44 and P44, besides TO5n output.

5. Be sure to clear bits 4 and 5 to "0".

Remarks 1. In PWM mode, PWM output is made inactive by clearing TCE50 to 0.

2. If LVS50 and LVR50 are read, the value is 0.

3. The values of the TMC506, LVS50, LVR50, TMC5n1, and TOE50 bits are reflected at the TO50 pin regardless of the value of TCE50.

9.4.8 Example of watch error correction of real-time counter

The watch can be corrected with high accuracy when it is slow or fast, by setting a value to the watch error correction register.

Example of calculating the correction value

The correction value used when correcting the count value of the sub-count register (RSUBC) is calculated by using the following expression.

Set DEV to 0 when the correction range is –63.1 ppm or less, or 63.1 ppm or more.

(When DEV = 0)

Correction value[Note] = Number of correction counts in 1 minute ÷ 3 = (Oscillation frequency ÷ Target frequency – 1) × 32768 × 60 ÷ 3

(When DEV = 1)

Correction value[Note] = Number of correction counts in 1 minute = (Oscillation frequency ÷ Target frequency – 1) × 32768 × 60

Note The correction value is the watch error correction value calculated by using bits 6 to 0 of the watch error correction register (SUBCUD).

(When F6 = 0) Correction value = {(F5, F4, F3, F2, F1, F0) – 1} × 2

(When F6 = 1) Correction value = – {(/F5, /F4, /F3, /F2, /F1, /F0) + 1} × 2

When (F6, F5, F4, F3, F2, F1, F0) is (*, 0, 0, 0, 0, 0, *), watch error correction is not performed. "*" is 0 or 1. /F5 to /F0 are bit-inverted values (000011 when 111100).

Remarks 1. The correction value is 2, 4, 6, 8, … 120, 122, 124 or –2, –4, –6, –8, … –120, –122, –124.

2. The oscillation frequency is the input clock (f_{RTC}) value of the real-time counter (RTC).
It can be calculated from the 32 kHz output frequency of the RTCCL pin or the output frequency of the RTC1HZ pin × 32768 when the watch error correction register is set to its initial value (00H).

3. The target frequency is the frequency resulting after correction performed by using the watch error correction register.

11.3 Registers Controlling Clock Output/Buzzer Output Controller

The following two registers are used to control the clock output/buzzer output controller.

- Clock output selection register (CKS)
- Port mode register 3 (PM3)
- Port mode register 1 (PM1)

(1) Clock output selection register (CKS)

This register sets output enable/disable for clock output (PCL) and for the buzzer frequency output (BUZ), and sets the output clock.

CKS is set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears CKS to 00H.

Figure 11-2. Format of Clock Output Selection Register (CKS) (1/2)

(a) 78K0/LC3, 78K0/LD3, 78K0/LE3

Address: FF40H After reset: 00H R/W

Symbol	<7>	6	5	4	3	2	1	0
CKS	BZOE	BCS1	BCS0	0	0	0	0	0

BZOE	BUZ output enable/disable specification
0	Clock division circuit operation stopped. BUZ fixed to low level.
1	Clock division circuit operation enabled. BUZ output enabled.

BCS1	BCS0	BUZ output clock selection		
			f_{PRS} = 5 MHz	f_{PRS} = 10 MHz
0	0	$f_{PRS}/2^{10}$	4.88 kHz	9.77 kHz
0	1	$f_{PRS}/2^{11}$	2.44 kHz	4.88 kHz
1	0	$f_{PRS}/2^{12}$	1.22 kHz	2.44 kHz
1	1	$f_{PRS}/2^{13}$	0.61 kHz	1.22 kHz

Caution Set BCS1 and BCS0 when the buzzer output operation is stopped (BZOE = 0).

Remark f_{PRS}: Peripheral hardware clock frequency

ANI0/P20 to ANI7/P27 pins are as shown below depending on the settings of PF2, ADPC0, PM2, ADS, and ADDCTL0.

Table 12-3. Setting Functions of P20/ANI0 to P27/ANI7 Pins

(a) μPD78F041x, 78F043x, 78F045x, 78F048x

PF2	ADPC0	PM2	ADS	P20/SEGxx/ANI0 to P27/SEGxx/ANI7 Pins
Digital/Analog selection	Analog input selection	Input mode	Does not select ANI.	Analog input (not to be converted)
			Selects ANI.	Analog input (to be converted by successive approximation type A/D converter)
		Output mode	–	Setting prohibited
	Digital I/O selection	Input mode	–	Digital input
		Output mode	–	Digital output
SEG output selection	–	–	–	Segment output

(b) μPD78F046x, 78F049x

ADPC0	PM2	ADS	ADDCTL0	P20/ANI0/DS0- to P27/ANI7/REF+ Pins
Analog input selection	Input mode	Does not select ANI.	Does not select DSn±.	Analog input (not to be converted)
		Selects ANI.	Does not select DSn±.	Analog input (to be converted by successive approximation type A/D converter)
		Does not select ANI.	Selects DSn±.	Analog input (to be converted by ΔΣ-type A/D converter)
		Selects ANI.	Selects DSn±.	Setting prohibited
	Output mode	–		Setting prohibited
Digital I/O selection	Input mode	–		Digital input
	Output mode	–		Digital output

Notes 1. If the peripheral hardware clock (f_{PRS}) operates on the high-speed system clock (f_{XH}) (XSEL = 1), the f_{PRS} operating frequency varies depending on the supply voltage.

- V_{DD} = 2.7 to 5.5 V: $f_{PRS} \leq$ 10 MHz
- V_{DD} = 1.8 to 2.7 V: $f_{PRS} \leq$ 5 MHz

2. Note the following points when selecting the TM50 output as the base clock.

(a) 78K0/LC3, 78K0/LD3

Start the operation of 8-bit timer/event counter 50 first and then enable the timer F/F inversion operation (TMC501 = 1).

(b) 78K0/LE3, 78K0/LF3

- Mode in which the count clock is cleared and started upon a match of TM50 and CR50 (TMC506 = 0)
  Start the operation of 8-bit timer/event counter 50 first and then enable the timer F/F inversion operation (TMC501 = 1).
- PWM mode (TMC506 = 1)
  Start the operation of 8-bit timer/event counter 50 first and then set the count clock to make the duty = 50%.

It is not necessary to enable (TOE50 = 1) TO50 output in any mode.

Cautions 1. Make sure that bit 6 (TXE0) and bit 5 (RXE0) of the ASIM0 register = 0 when rewriting the MDL04 to MDL00 bits.

2. Make sure that bit 7 (POWER0) of the ASIM0 register = 0 when rewriting the TPS01 and TPS00 bits.

3. The baud rate value is the output clock of the 5-bit counter divided by 2.

Remarks 1. f_{XCLK0}: Frequency of base clock selected by the TPS01 and TPS00 bits

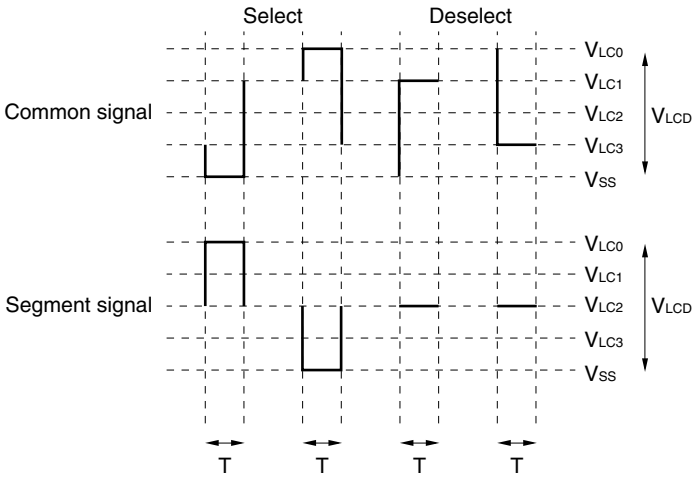
2. f_{PRS}: Peripheral hardware clock frequency

3. k: Value set by the MDL04 to MDL00 bits (k = 8, 9, 10, ..., 31)

4. ×: Don't care

5. TMC506: Bit 6 of 8-bit timer mode control register 50 (TMC50)
TMC501: Bit 1 of TMC50

(d) 1/4 bias method

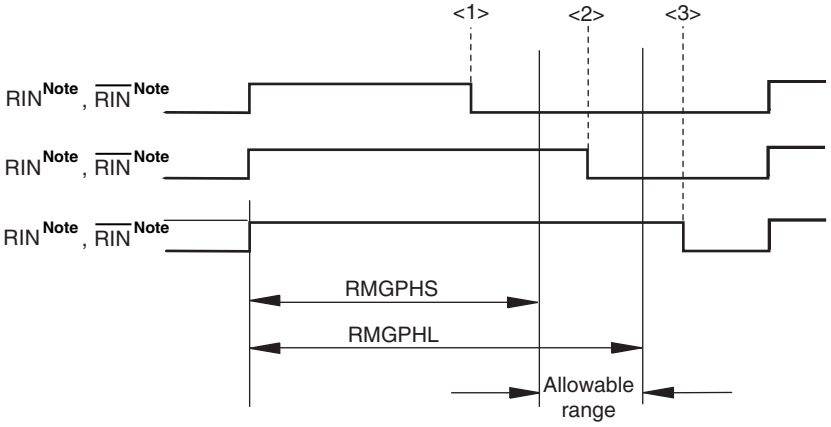


T: One LCD clock period

20.4.7 Timing

Operation varies depending on the positions of the RIN input waveform below.

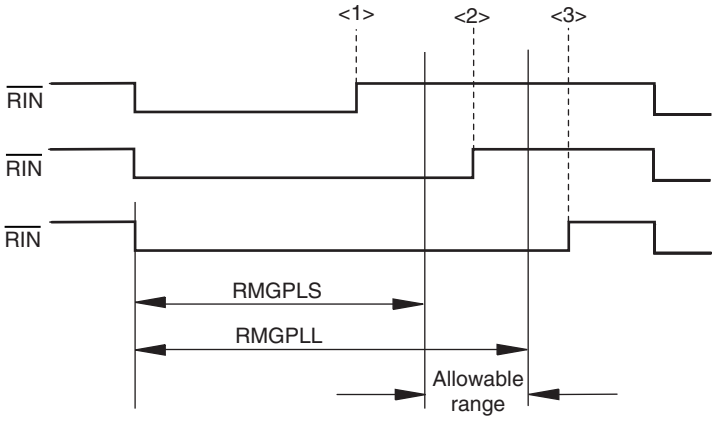
(1) Guide pulse high level width determination (Type A, Type B reception modes only)



Note RIN is generated in type A reception mode, and $\overline{\text{RIN}}$ is generated in type B reception mode.

Relationship Between RMGPHS/RMGPHL/Counter	Position of Waveform	Corresponding Operation
Counter < RMGPHS	<1>: Short	Measuring guide pulse high-level width is started from the next rising edge.
RMGPHS ≤ counter < RMGPHL	<2>: Within the range	INTGP is generated. Data measurement is started.
RMGPHL ≤ counter	<3>: Long	Measuring guide pulse high-level width is started from the next rising edge.

(2) Guide pulse low level width determination (Type B reception mode only)



Relationship Between RMGPLS/RMGPLL/Counter	Position of Waveform	Corresponding Operation
Counter < RMGPLS	<1>: Short	Measuring guide pulse high-level width is started from the next rising edge.
RMGPLS ≤ counter < RMGPLL	<2>: Within the range	INTGP is generated. Data measurement is started.
RMGPLL ≤ counter	<3>: Long	Measuring guide pulse high-level width is started from the next rising edge.

(3) Data low level width determination

Figure 27-1. Format of Option Byte (2/2)

Address: 0081H/1081H[Notes 1, 2]

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	POCMODE

POCMODE	POC mode selection
0	1.59 V POC mode (default)
1	2.7 V/1.59 V POC mode

Notes 1. POCMODE can only be written by using a dedicated flash memory programmer. It cannot be set during self-programming or boot swap operation during self-programming. However, because the value of 1081H is copied to 0081H during the boot swap operation, it is recommended to set a value that is the same as that of 0081H to 1081H when the boot swap function is used.

2. To change the setting for the POC mode, set the value to 0081H again after batch erasure (chip erasure) of the flash memory. The setting cannot be changed after the memory of the specified block is erased.

Caution Be sure to clear bits 7 to 1 to "0".

Address: 0082H/1082H, 0083H/1083H[Note]

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0

Note Be sure to set 00H to 0082H and 0083H, as these addresses are reserved areas. Also set 00H to 1082H and 1083H because 0082H and 0083H are switched with 1082H and 1083H when the boot swap operation is used.

Address: 0084H/1084H[Note]

7	6	5	4	3	2	1	0
0	0	0	0	0	0	OCDEN1	OCDEN0

OCDEN1	OCDEN0	On-chip debug operation control
0	0	Operation disabled
0	1	Setting prohibited
1	0	Operation enabled. Does not erase data of the flash memory in case authentication of the on-chip debug security ID fails.
1	1	Operation enabled. Erases data of the flash memory in case authentication of the on-chip debug security ID fails.

Note To use the on-chip debug function, set 02H or 03H to 0084H. Set a value that is the same as that of 0084H to 1084H because 0084H and 1084H are switched during the boot swap operation.

Remark For the on-chip debug security ID, see **CHAPTER 29 ON-CHIP DEBUG FUNCTION**.

Recommended Oscillator Constants

(1) X1 Oscillator: Ceramic resonator (T_A = –40 to +85°C)

Manufacturer	Part Number	SMD/ Lead	Frequency (MHz)	Recommended circuit invariable		Oscillation Voltage Range	
				C1 (pF)	C2 (pF)	MIN.(V)	MAX.(V)
Murata Mfg.	CSTCC2M00G56-R0	SMD	2.00	Internal (47)	Internal (47)	1.8	5.5
	CSTLS4M00G56-B0	Lead	4.00	Internal (47)	Internal (47)		
	CSTCR4M00G55-R0	SMD		Internal (39)	Internal (39)		
	CSTLS4M19G56-B0	Lead	4.194	Internal (47)	Internal (47)		
	CSTCR4M19G55-R0	SMD		Internal (39)	Internal (39)		
	CSTLS4M91G56-B0	Lead	4.915	Internal (47)	Internal (47)	2.0	
	CSTCR4M91G55-R0	SMD		Internal (39)	Internal (39)	1.8	
	CSTLS5M00G56-B0	Lead	5.00	Internal (47)	Internal (47)	2.0	
	CSTCR5M00G55-R0	SMD		Internal (39)	Internal (39)	1.8	
	CSTLS6M00G56-B0	Lead	6.00	Internal (47)	Internal (47)	2.2	
	CSTCR6M00G55-R0	SMD		Internal (39)	Internal (39)	1.9	
	CSTLS8M00G56-B0	Lead	8.00	Internal (47)	Internal (47)	2.2	
	CSTCE8M00G55-R0	SMD		Internal (33)	Internal (33)	1.8	
	CSTLS8M38G56-B0	Lead	8.388	Internal (47)	Internal (47)	2.2	
	CSTCE8M38G55-R0	SMD		Internal (33)	Internal (33)	1.8	
	CSTLS10M0G53-B0	SMD	10.0	Internal (15)	Internal (15)	1.8	
	CSTCE10M0G55-R0	SMD		Internal (33)	Internal (33)	2.1	
Murata Mfg. (low-capacitance products)	CSTLS4M91G53-B0	Lead	4.915	Internal (15)	Internal (15)	1.8	5.5
	CSTLS5M00G53-B0	Lead	5.00	Internal (15)	Internal (15)	1.8	
	CSTCR6M00G53-R0	SMD	6.00	Internal (15)	Internal (15)	1.8	
	CSTLS6M00G53-B0	Lead		Internal (15)	Internal (15)	1.8	
	CSTLS8M00G53-B0	Lead	8.00	Internal (15)	Internal (15)	1.8	
	CSTLS8M38G53-B0	Lead	8.388	Internal (15)	Internal (15)	1.8	
	CSTCE10M0G52-R0	SMD	10.0	Internal (10)	Internal (10)	1.8	

Caution The oscillator constants shown above are reference values based on evaluation in a specific environment by the resonator manufacturer. If it is necessary to optimize the oscillator characteristics in the actual application, apply to the resonator manufacturer for evaluation on the implementation circuit. The oscillation voltage and oscillation frequency only indicate the oscillator characteristic. Use the 78K0/Lx3 microcontrollers so that the internal operation conditions are within the specifications of the DC and AC characteristics.

(4/4)

<table>
<tr><th>Page</th><th>Description</th><th>Classification</th></tr>
<tr><td colspan="3">CHAPTER 31 ELECTRICAL SPECIFICATIONS (Continuation)</td></tr>
<tr><td>p.866</td><td>Deletion of DC characteristics of conventional-specification products.
<table>
<tr><th>Parameter</th><th>Symbol</th><th colspan="2">Conditions</th><th>MIN.</th><th>TYP.</th><th>MAX.</th><th>Unit</th></tr>
<tr><td rowspan="7">Output voltage, low
(product rank: “K” and “E”)</td><td rowspan="7">V_{OL1}</td><td rowspan="5">P10 to P17, P30 to P34, P40 to P47, P120</td><td>4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 8.5 mA</td><td></td><td></td><td>0.7</td><td>V</td></tr>
<tr><td>2.7 V ≤ V_{DD} < 4.0 V, I_{OL1} = 5.0 mA</td><td></td><td></td><td>0.7</td><td>V</td></tr>
<tr><td>1.8 V ≤ V_{DD} < 2.7 V, I_{OL1} = 2.0 mA</td><td></td><td></td><td>0.5</td><td>V</td></tr>
<tr><td>1.8 V ≤ V_{DD} < 2.7 V, I_{OL1} = 1.0 mA</td><td></td><td></td><td>0.5</td><td>V</td></tr>
<tr><td>1.8 V ≤ V_{DD} < 2.7 V, I_{OL1} = 0.5 mA</td><td></td><td></td><td>0.4</td><td>V</td></tr>
<tr><td>P80 to P83, P90 to P93, P100 to P103, P110 to P113, P130 to P133, P140 to P143, P150 to P153</td><td>I_{OL1} = 0.4 mA</td><td></td><td></td><td>0.4</td><td>V</td></tr>
<tr><td>V_{OL2}</td><td>P20 to P27</td><td>AV_{REF} = V_{DD}, I_{OL2} = 0.4 mA</td><td></td><td></td><td>0.4</td><td>V</td></tr>
</table></td><td>(b)</td></tr>
</table>

Remark “Classification” in the above table classifies revisions as follows.
(a): Error correction, (b): Addition/change of specifications, (c): Addition/change of description or note, (d): Addition/change of package, part number, or management division, (e): Addition/change of related documents