Renesas Electronics America Inc - UPD78F0455GA-HAB-AX Datasheet

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	78K/0
Core Size	8-Bit
Speed	10MHz
Connectivity	3-Wire SIO, LINbus, UART/USART
Peripherals	LCD, LVD, POR, PWM, WDT
Number of I/O	46
Program Memory Size	60KB (60K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/upd78f0455ga-hab-ax

CHAPTER 2 PIN FUNCTIONS

2.1 Pin Function List

There are three types of pin I/O buffer power supplies: AV_{REF}[Note], V_{LC0}, and V_{DD}. The relationship between these power supplies and the pins is shown below.

Table 2-1. Pin I/O Buffer Power Supplies

Power Supply	Corresponding Pins
AV_{REF}[Note]	P20 to P27
V_{LC0}	COM0 to COM7, SEG0 to SEG39, V_{LC0} to V_{LC3}
V_{DD}	Pins other than above

Note μPD78F041x, 78F043x, 78F045x, 78F046x, 78F048x, and 78F049x only.
The power supply is V_{DD} with μPD78F040x, 78F042x, 78F044x, and 78F047x.

2.1.1 78K0/LC3

(1) Port functions (1/2): 78K0/LC3

Function Name	I/O	Function	After Reset	Alternate Function
P12	I/O	Port 1. 2-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	RxD0/KR3/<RxD6>
P13				TxD0/KR4/<TxD6>
P20	I/O	Port 2. 6-bit I/O port. Input/output can be specified in 1-bit units.	Digital input port	SEG21/ANI0[Note]
P21				SEG20/ANI1[Note]
P22				SEG19/ANI2[Note]
P23				SEG18/ANI3[Note]
P24				SEG17/ANI4[Note]
P25				SEG16/ANI5[Note]
P31	I/O	Port 3. 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	TOH1/INTP3
P32				TOH0/MCGO
P33				TI000/RTCDIV/ RTCCL/BUZ/INTP2
P34				TI52/TI010/TO00/ RTC1HZ/INTP1
P40	I/O	Port 4. 1-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	V_{LC3}/KR0

Note μPD78F041x only.

Remark The functions within arrowheads (< >) can be assigned by setting the input switch control register (ISC).

(2) Non-port functions (1/4): 78K0/LF3

Function Name	I/O	Function	After Reset	Alternate Function
ANI0[Note 2]	Input	10-bit successive approximation type A/D converter analog input.	Digital input port	P20/SEG39[Note 1]/ DS0−[Note 3]
ANI1[Note 2]				P21/SEG38[Note 1]/ DS0+[Note 3]
ANI2[Note 2]				P22/SEG37[Note 1]/ DS1−[Note 3]
ANI3[Note 2]				P23/SEG36[Note 1]/ DS1+[Note 3]
ANI4[Note 2]				P24/SEG35[Note 1]/ DS2−[Note 3]
ANI5[Note 2]				P25/SEG34[Note 1]/ DS2+[Note 3]
ANI6[Note 2]				P26/SEG33[Note 1]/ REF−[Note 3]
ANI7[Note 2]				P27/SEG32[Note 1]/ REF+[Note 3]
DS0−[Note 3]	Input	16-bit ΔΣ-type A/D converter analog input.	Digital input port	P20 /ANI0[Note 2]
DS0+[Note 3]				P21/ANI1[Note 2]
DS1−[Note 3]				P22/ANI2[Note 2]
DS1+[Note 3]				P23/ANI3[Note 2]
DS2−[Note 3]				P24/ANI4[Note 2]
DS2+[Note 3]				P25/ANI5[Note 2]
REF−[Note 3]		16-bit ΔΣ-type A/D converter reference voltage input. Make the same potential as V_{SS} and AV_{SS}.		P26/ANI6[Note 2]
REF+[Note 3]		16-bit ΔΣ-type A/D converter reference voltage input. Make the same potential as AV_{REF}.		P27/ANI7[Note 2]
AV_{REF}[Note 2]	Input	10-bit successive approximation type A/D converter reference voltage input, positive power supply for port 2, and 16-bit ΔΣ-type A/D converter [Note3]	–	–
AV_{SS}[Note 2]	–	A/D converter ground potential. Make the same potential as V_{SS}.	–	–

Notes 1. μPD78F047x and 78F048x only.

2. μPD78F048x and 78F049x only.

3. μPD78F049x only.

(2) CALLT instruction table area

The 64-byte area 0040H to 007FH can store the subroutine entry address of a 1-byte call instruction (CALLT).

(3) Option byte area

A 5-byte area of 0080H to 0084H and 1080H to 1084H can be used as an option byte area. Set the option byte at 0080H to 0084H when the boot swap is not used, and at 0080H to 0084H and 1080H to 1084H when the boot swap is used. For details, see **CHAPTER 27 OPTION BYTE**.

(4) CALLF instruction entry area

The area 0800H to 0FFFH can perform a direct subroutine call with a 2-byte call instruction (CALLF).

(5) On-chip debug security ID setting area

A 10-byte area of 0085H to 008EH and 1085H to 108EH can be used as an on-chip debug security ID setting area. Set the on-chip debug security ID of 10 bytes at 0085H to 008EH when the boot swap is not used and at 0085H to 008EH and 1085H to 108EH when the boot swap is used. For details, see **CHAPTER 29 ON-CHIP DEBUG FUNCTION**.

3.4.2 Register addressing

[Function]

The general-purpose register to be specified is accessed as an operand with the register bank select flags (RBS0 to RBS1) and the register specify codes of an operation code.

Register addressing is carried out when an instruction with the following operand format is executed. When an 8-bit register is specified, one of the eight registers is specified with 3 bits in the operation code.

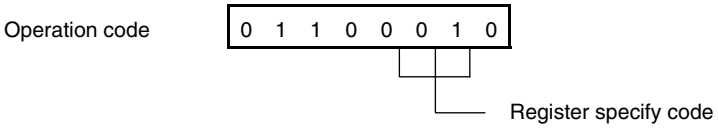
[Operand format]

Identifier	Description
r	X, A, C, B, E, D, L, H
rp	AX, BC, DE, HL

'r' and 'rp' can be described by absolute names (R0 to R7 and RP0 to RP3) as well as function names (X, A, C, B, E, D, L, H, AX, BC, DE, and HL).

[Description example]

MOV A, C; when selecting C register as r



INCW DE; when selecting DE register pair as rp

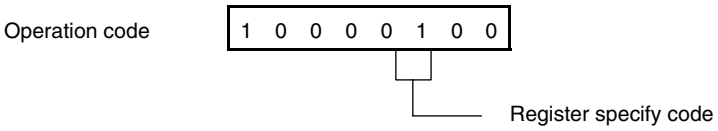


Table 4-3. Port Functions (78K0/LD3) (2/2)

Function Name	I/O	Function	After Reset	Alternate Function
P80	I/O	Port 8. 1-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	SEG4
P100, P101	I/O	Port 10. 2-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	SEG5, SEG6
P111	I/O	Port 11. 3-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	SEG7
P112				SEG8/TxD6
P113				SEG9/RxD6
P120	I/O	Port 12. 1-bit I/O port and 4-bit input port. Only for P120, use of an on-chip pull-up resistor can be specified by a software setting.	Input port	INTP0/EXLVI
P121	Input			X1/OCD0A
P122				X2/EXCLK/OCD0B
P123				XT1
P124				XT2
P140 to P143	I/O	Port 14. 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	SEG10(KS0) to SEG13(KS3)
P150 to P153	I/O	Port 15. 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input port	SEG14(KS4) to SEG17(KS7)

5.4.3 When subsystem clock is not used

If it is not necessary to use the subsystem clock for low power consumption or timer operations, or if not using the subsystem clock as an I/O port, set the XT1 and XT2 pins to Input port mode (OSCSELS = 0) and independently connect to V_{DD} or V_{SS} via a resistor.

Remark OSCSELS: Bit 4 of clock operation mode select register (OSCCTL)

5.4.4 Internal high-speed oscillator

The internal high-speed oscillator is incorporated in the 78K0/Lx3 microcontrollers. Oscillation can be controlled by the internal oscillation mode register (RCM).

After a reset release, the internal high-speed oscillator automatically starts oscillation (8 MHz (TYP.)).

5.4.5 Internal low-speed oscillator

The internal low-speed oscillator is incorporated in the 78K0/Lx3 microcontrollers.

The internal low-speed oscillation clock is only used as the clock of the watchdog timer, 8-bit timer H1, and LCD controller/driver. The internal low-speed oscillation clock cannot be used as the CPU clock.

“Can be stopped by software” or “Cannot be stopped” can be selected by the option byte. When “Can be stopped by software” is set, oscillation can be controlled by the internal oscillation mode register (RCM).

After a reset release, the internal low-speed oscillator automatically starts oscillation, and the watchdog timer is driven (240 kHz (TYP.)) if the watchdog timer operation is enabled using the option byte.

5.4.6 Prescaler

The prescaler generates various clocks by dividing the main system clock when the main system clock is selected as the clock to be supplied to the CPU.

5.5 Clock Generator Operation

The clock generator generates the following clocks and controls the operation modes of the CPU, such as standby mode (see **Figure 5-1**).

- Main system clock f_{XP}
  - High-speed system clock f_{XH}
    X1 clock f_X
    External main system clock f_{EXCLK}
  - Internal high-speed oscillation clock f_{RH}
- Subsystem clock f_{SUB}
  - XT1 clock f_{XT}
- Internal low-speed oscillation clock f_{RL}
- CPU clock f_{CPU}
- Peripheral hardware clock f_{PRS}

The CPU starts operation when the internal high-speed oscillator starts outputting after a reset release in the 78K0/Lx3 microcontrollers, thus enabling the following.

(1) 8-bit timer counter 5n (TM5n)

TM5n is an 8-bit register that counts the count pulses and is read-only.

The counter is incremented in synchronization with the rising edge of the count clock.

Figure 7-4. Format of 8-Bit Timer Counter 5n (TM5n)

Address: FF16H (TM50), FF6FH (TM51), FF51H (TM52) After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
TM5n (n = 0-2)								

In the following situations, the count value is cleared to 00H.

<1> Reset signal generation

<2> When TCE5n is cleared

<3> When TM5n and CR5n match in the mode in which clear & start occurs upon a match of the TM5n and CR5n.

(2) 8-bit timer compare register 5n (CR5n)

CR5n can be read and written by an 8-bit memory manipulation instruction.

Except in PWM mode, the value set in CR5n is constantly compared with the 8-bit timer counter 5n (TM5n) count value, and an interrupt request (INTTM5n) is generated if they match.

In the PWM mode, the TO5n output becomes inactive when the values of TM5n and CR5n match, but no interrupt is generated.

The value of CR5n can be set within 00H to FFH.

Reset signal generation clears CR5n to 00H.

Figure 7-5. Format of 8-Bit Timer Compare Register 5n (CR5n)

Address: FF17H (CR50), FF41H (CR51), FF59H (CR52) After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
CR5n (n = 0-2)								

Cautions 1. In the mode in which clear & start occurs on a match of TM5n and CR5n (TMC5n6 = 0), do not write other values to CR5n during operation.

2. In PWM mode, make the CR5n rewrite period 3 count clocks of the count clock (clock selected by TCL5n) or more.

Remark n = 0 to 2

Figure 8-3. Block Diagram of 8-Bit Timer H2

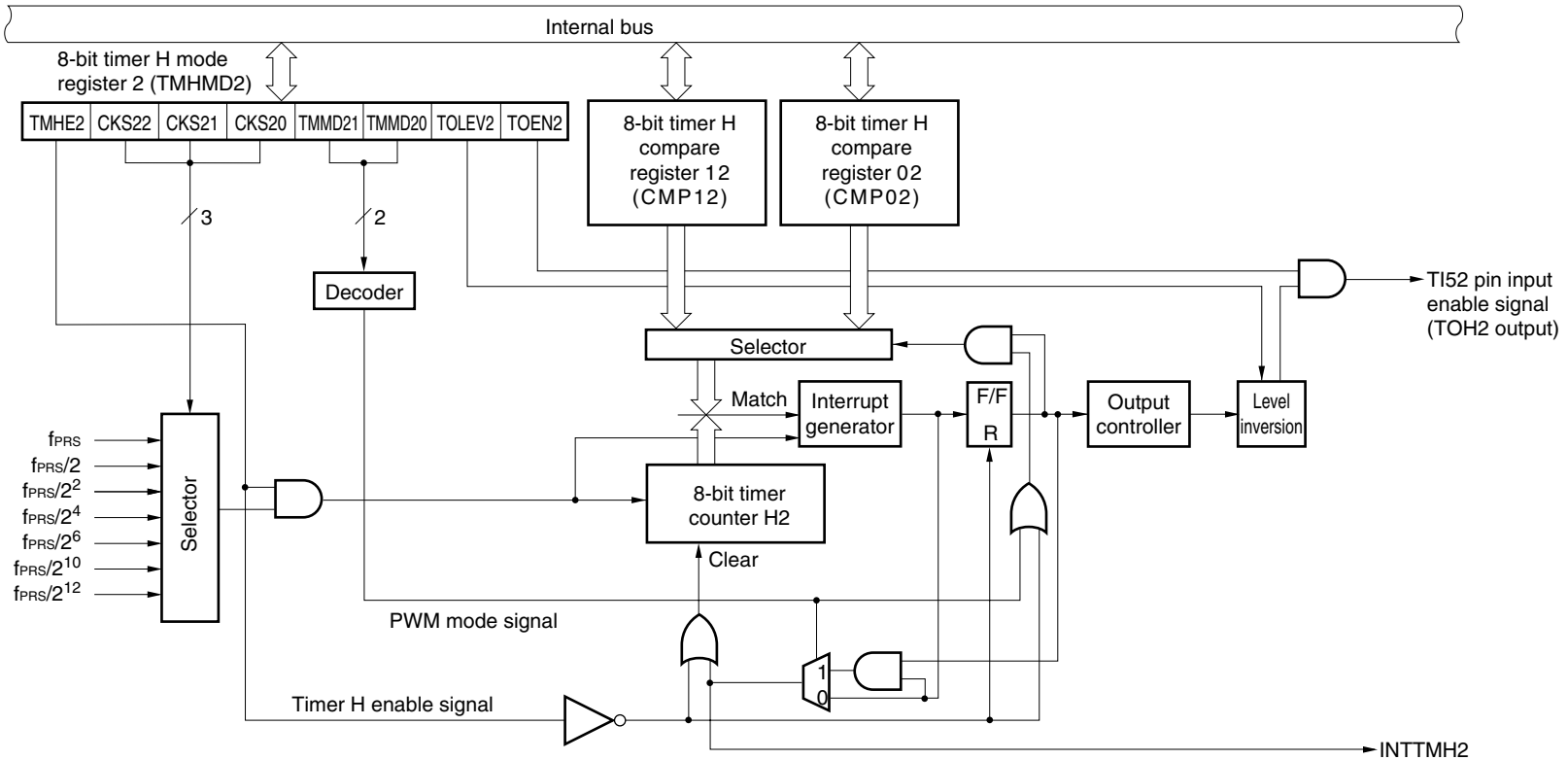


Figure 13-2. Format of 16-Bit ΔΣ-Type A/D Converter Control Register 0 (ADDCTL0)

Address: FF7CH After reset: 00H R/W

Symbol	<7>	<6>	<5>	<4>	3	2	1	0
ADDCTL0	ADPON	ADDCE	HAC	AINMCD	0	0	ADDS1	ADDS0

ADDPON	16-bit ΔΣ-type A/D circuit power supply control
0	Power supply OFF
1	Power supply ON

ADDCE	16-bit ΔΣ-type A/D conversion operation control
0	Stops conversion operation
1	Starts conversion operation

HAC	Setting 16-bit ΔΣ-type A/D conversion high-accuracy mode
0	High-accuracy mode OFF
1	High-accuracy mode ON

AINMOD	16-bit ΔΣ-type A/D conversion input mode control
0	Single input
1	Differential input

ADDS1	ADDS0	16-bit ΔΣ-type analog input specification
0	0	DS0+/DS0-
0	1	DS1+/DS1-
1	0	DS2+/DS2-
1	1	Setting prohibited

Cautions 1. Do not set the ADDPON and ADDCE bits to 1 at the same time. ADDCE must be set to 1, at least 1.2 μs after ADDPON has been set to 1.

2. Setting the ΔΣ analog input channel to be set by ADDS1 and ADDS0 to a pin which has been selected to be used in the analog input mode by the ADPC0 register is prohibited.

3. Operating 16-bit ΔΣ-type A/D conversion and 10-bit successive approximation type A/D conversions at the same time (ADDCE = 1 and ADCS = 1) is prohibited.

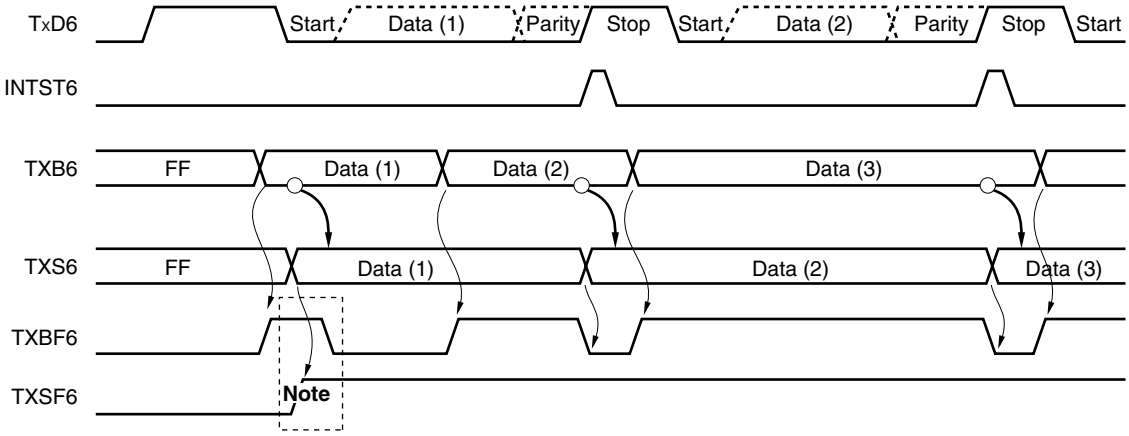
4. If ADDCTL0 is rewritten (including identical data), A/D conversion operation is resumed after it has been initialized.

5. Set the input voltage in accordance with Table 13-4 Input Voltage Range.

6. When executing a STOP instruction, power to the 16-bit ΔΣ-type A/D converter must be turned off (ADDPON = 0).

Figure 15-19 shows the timing of starting continuous transmission, and Figure 15-20 shows the timing of ending continuous transmission.

Figure 15-19. Timing of Starting Continuous Transmission



Note When ASIF6 is read, there is a period in which TXBF6 and TXSF6 = 1, 1. Therefore, judge whether writing is enabled using only the TXBF6 bit.

Remark TxD6: TxD6 pin (output)
INTST6: Interrupt request signal
TXB6: Transmit buffer register 6
TXS6: Transmit shift register 6
ASIF6: Asynchronous serial interface transmission status register 6
TXBF6: Bit 1 of ASIF6
TXSF6: Bit 0 of ASIF6

(2) Error of baud rate

The baud rate error can be calculated by the following expression.

- $\text{Error (\%)} = \left(\frac{\text{Actual baud rate (baud rate with error)}}{\text{Desired baud rate (correct baud rate)}} - 1 \right) \times 100 \text{ [\%]}$

Cautions 1. Keep the baud rate error during transmission to within the permissible error range at the reception destination.

2. Make sure that the baud rate error during reception satisfies the range shown in (4) Permissible baud rate range during reception.

Example: Frequency of base clock = 10 MHz = 10,000,000 Hz
Set value of MDL67 to MDL60 bits of BRGC6 register = 00100001B (k = 33)
Target baud rate = 153600 bps

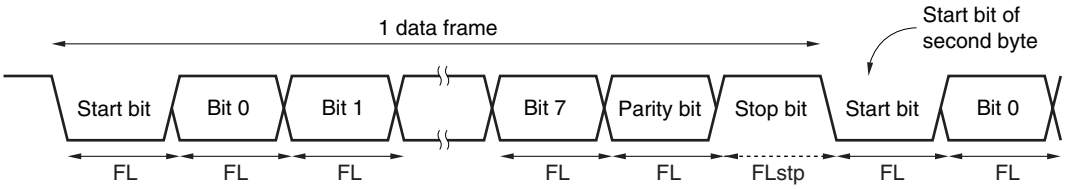
Baud rate = 10 M / (2 × 33)
= 10000000 / (2 × 33) = 151,515 [bps]

Error = (151515/153600 − 1) × 100
= −1.357 [%]

(5) Data frame length during continuous transmission

When data is continuously transmitted, the data frame length from a stop bit to the next start bit is extended by two clocks of base clock from the normal value. However, the result of communication is not affected because the timing is initialized on the reception side when the start bit is detected.

Figure 15-28. Data Frame Length During Continuous Transmission



Where the 1-bit data length is FL, the stop bit length is FLstp, and base clock frequency is f_{XCLK6}, the following expression is satisfied.

$$FLstp = FL + 2/f_{XCLK6}$$

Therefore, the data frame length during continuous transmission is:

$$\text{Data frame length} = 11 \times FL + 2/f_{XCLK6}$$

(7) Automatic data transfer address count register 0 (ADTC0)

This is a register used to indicate buffer RAM addresses during automatic transfer. When automatic transfer is stopped, the data position when transfer stopped can be ascertained by reading ADTC0 register value.

This register can be read by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H. However, reading from ADTC0 is prohibited when bit 0 (TSF0) of serial status register 0 (CSIS0) = 1.

Figure 17-8. Format of Automatic Data Transfer Address Count Register 0 (ADTC0)

Address: FF97H After reset: 00H R

Symbol	7	6	5	4	3	2	1	0
ADTC0	0	0	0	ADTC04	ADTC03	ADTC02	ADTC01	ADTP00

(8) Port function register 1 (PF1)

This register sets the pin functions of P16/SOA0/TxD6 pin.

PF1 is set using a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation clears PF1 to 00H.

Figure 17-9. Format of Port Function Register 1 (PF1)

Address: FF20H After reset: 00H R/W

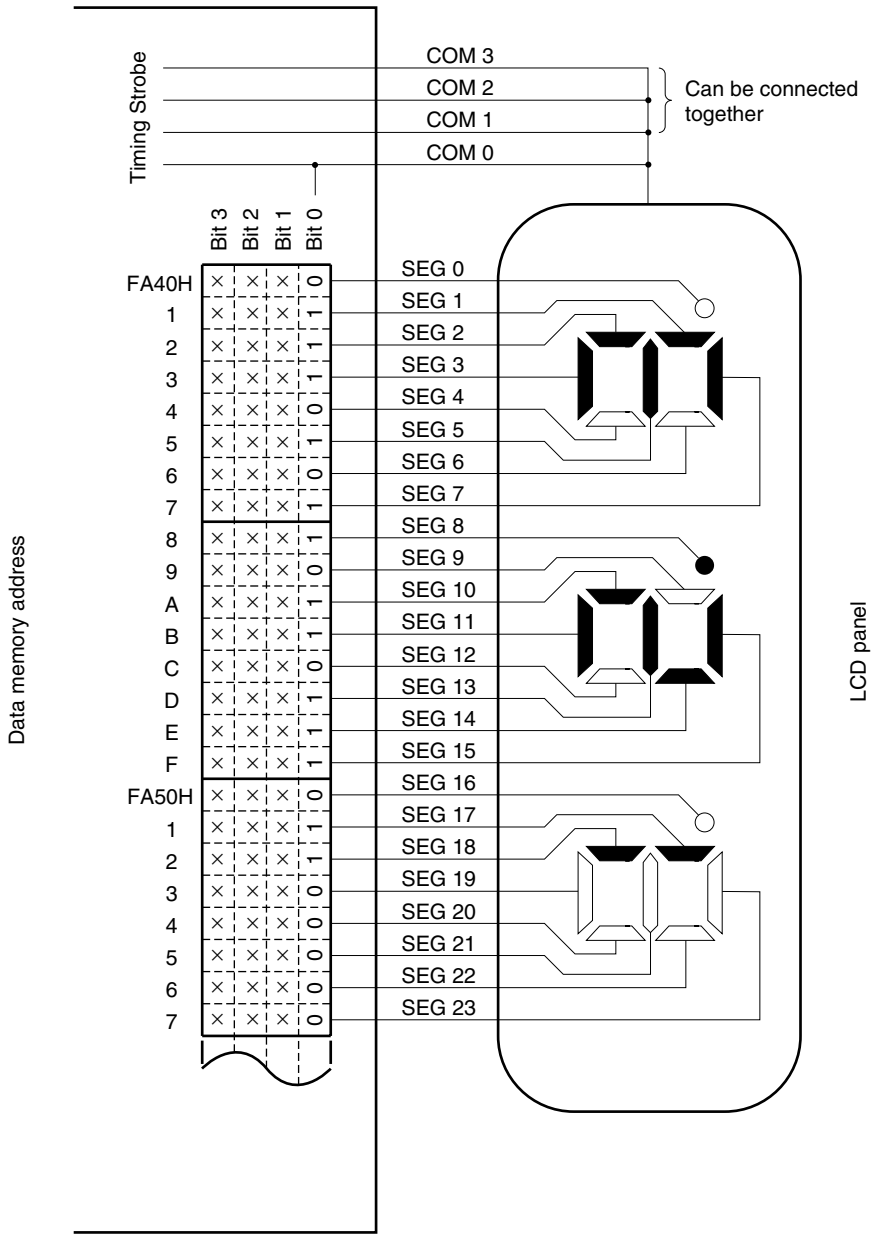
Symbol	7	6	5	4	3	2	1	0
PF1	0	PF16	0	0	PF13	0	0	0

PF16	Port (P16), CSIA0, and UART6 output specification
0	Used as P16 or SOA0
1	Used as TxD6

PF13	Port (P13), CSI10, and UART0 output specification
0	Used as P13 or SO10
1	Used as TxD0

Remark The figure shown above presents the format of port function register 1 of 78K0/LF3 products.

Figure 18-21. Example of Connecting Static LCD Panel



(b) MCG control register 1 (MC0CTL1)

This register is used to set the base clock of the Manchester code generator.

This register can be set by an 8-bit memory manipulation instruction.

Reset signal generation clears this register to 00H.

Address: FF4DH After reset: 00H R/W

Symbol	7	6	5	4	3	2	1	0
MC0CTL1	0	0	0	0	0	MC0CKS2	MC0CKS1	MC0CKS0

MC0CKS2	MC0CKS1	MC0CKS0	Base clock (f_{XCLK}) selection[Note 1]
0	0	0	f_{PRS}[Note 2] (10 MHz)
0	0	1	$f_{PRS}/2$ (5 MHz)
0	1	0	$f_{PRS}/2^2$ (2.5 MHz)
0	1	1	$f_{PRS}/2^3$ (1.25 MHz)
1	0	0	$f_{PRS}/2^4$ (625 kHz)
1	0	1	$f_{PRS}/2^5$ (312.5 kHz)
1	1	0	Setting prohibited
1	1	1	

Notes 1. If the peripheral hardware clock (f_{PRS}) operates on the high-speed system clock (f_{XH}) (XSEL = 1), the f_{PRS} operating frequency varies depending on the supply voltage.

- V_{DD} = 2.7 to 5.5 V: $f_{PRS} \leq$ 10 MHz
- V_{DD} = 1.8 to 2.7 V: $f_{PRS} \leq$ 5 MHz

2. If the peripheral hardware clock (f_{PRS}) operates on the internal high-speed oscillation clock (f_{RH}) (XSEL = 0), when 1.8 V $\leq V_{DD} <$ 2.7 V, the setting of MC0CKS2 = MC0CKS1 = MC0CKS0 = 0 (base clock: f_{PRS}) is prohibited.

Caution Clear bit 7 (MC0PWR) of the MC0CTL0 register to 0 before rewriting the MC0CKS2 to MC0CKS0 bits.

Remarks 1. f_{PRS}: Peripheral hardware clock frequency

2. Figures in parentheses are for operation with f_{PRS} = 10 MHz.

(d) Port mode register 3 (PM3)

This register sets port 3 input/output in 1-bit units.

When using the P32/TOH0/MCGO pin for Manchester code output, clear PM32 to 0 and clear the output latch of P32 to 0.

PM3 can be set by a 1-bit or 8-bit memory manipulation instruction.

Reset signal generation sets these registers to FFH.

Address: FF23H After reset: FFH R/W

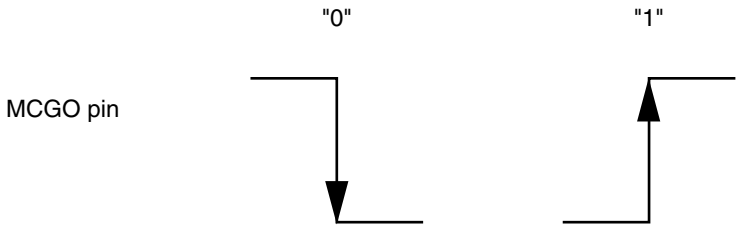
Symbol	7	6	5	4	3	2	1	0
PM3	1	1	1	PM34	PM33	PM32	PM31	PM30

PM3n	P3n pin I/O mode selection (n = 0 to 4)
0	Output mode (output buffer on)
1	Input mode (output buffer off)

Remark The figure shown above presents the format of port mode register 3 of 78K0/LF3 products. For the format of port mode register 3 of other products, see **(1) Port mode registers (PMxx)** in **4.3 Registers Controlling Port Function**.

(2) Format of "0" and "1" of Manchester code output

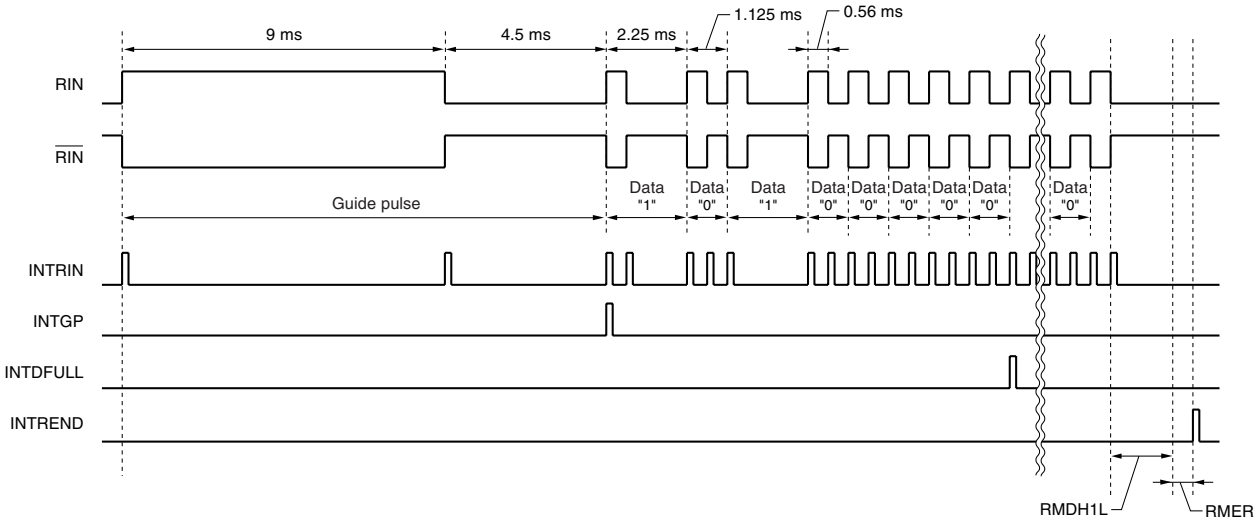
The format of "0" and "1" of Manchester code output in 78K0/Lx3 microcontrollers are as follows.



20.4.3 Format of type B reception mode

Figure 20-8 shows the data format for type B.

Figure 20-8. Example of Type B Data Format



Remark $\overline{\text{RIN}}$ is the internally inverted signal of RIN.

20.4.4 Operation flow of type B reception mode

Figure 20-9 shows the operation flow.

Cautions 1. When INTRERR is generated, RMSR and RMSCR are automatically cleared immediately.

2. When data has been set to all the bits of RMSR, the following processing is automatically performed.

- **The value of RMSR is transferred to RMDR.**
- **INTDFULL is generated.**
- **RMSR is cleared.**

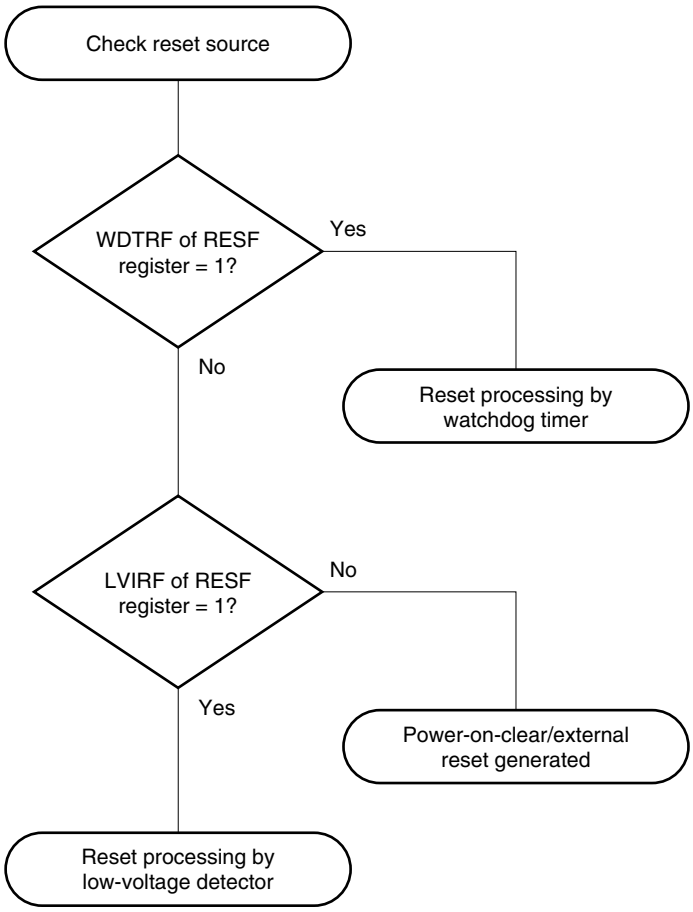
RMDR must then be read before the next data is set to all the bits of RMSR.

3. When INTREND has been generated, read RMSCR first followed by RMSR.
When RMSR has been read, RMSCR and RMSR are automatically cleared.
If INTREND is generated, the next data cannot be received until RMSR is read.

4. RMSR, RMSCR, and RMDR are cleared simultaneously to operation termination (RMEN = 0).

Figure 26-9. Example of Software Processing After Reset Release (2/2)

• Checking reset source



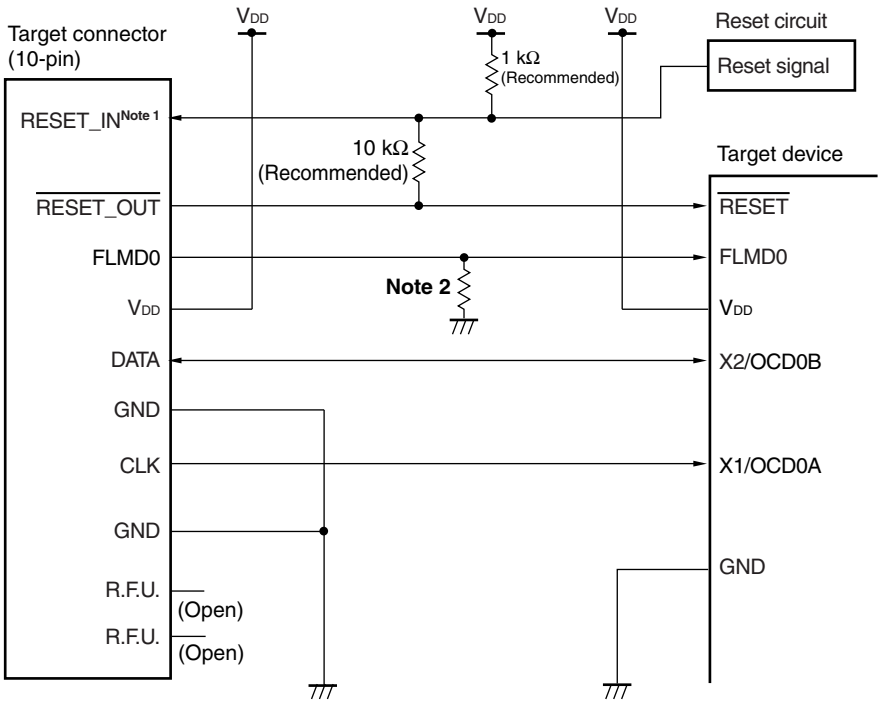
CHAPTER 29 ON-CHIP DEBUG FUNCTION

29.1 Connecting QB-MINI2 to 78K0/Lx3 microcontrollers

The 78K0/Lx3 microcontrollers uses the V_{DD}, FLMD0, $\overline{RESET}$, OCD0A/X1, OCD0B/X2, and V_{SS} pins to communicate with the host machine via an on-chip debug emulator (QB-MINI2).

Caution The 78K0/Lx3 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

Figure 29-1. Connection Example of QB-MINI2 and 78K0/Lx3 microcontrollers



Notes 1. This connection is designed assuming that the reset signal is output from the N-ch open-drain buffer (output resistance: 100 Ω or less). For details, refer to **QB-MINI2 User's Manual (U18371E)**.

2. Make pull-down resistor 470 Ω or more (10 kΩ: recommended).

Caution Input the clock from the OCD0A/X1 pin during on-chip debugging.

CHAPTER 30 INSTRUCTION SET

This chapter lists each instruction set of the 78K0/Lx3 microcontrollers in table form. For details of each operation and operation code, refer to the separate document **78K/0 Series Instructions User's Manual (U12326E)**.

30.1 Conventions Used in Operation List

30.1.1 Operand identifiers and specification methods

Operands are written in the "Operand" column of each instruction in accordance with the specification method of the instruction operand identifier (refer to the assembler specifications for details). When there are two or more methods, select one of them. Uppercase letters and the symbols #, !, $ and [ ] are keywords and must be written as they are. Each symbol has the following meaning.

- #: Immediate data specification
- !: Absolute address specification
- $: Relative address specification
- [ ]: Indirect address specification

In the case of immediate data, describe an appropriate numeric value or a label. When using a label, be sure to write the #, !, $, and [ ] symbols.

For operand register identifiers r and rp, either function names (X, A, C, etc.) or absolute names (names in parentheses in the table below, R0, R1, R2, etc.) can be used for specification.

Table 30-1. Operand Identifiers and Specification Methods

Identifier	Specification Method
r	X (R0), A (R1), C (R2), B (R3), E (R4), D (R5), L (R6), H (R7)
rp	AX (RP0), BC (RP1), DE (RP2), HL (RP3)
sfr	Special function register symbol[Note]
sfrp	Special function register symbol (16-bit manipulatable register even addresses only)[Note]
saddr	FE20H to FF1FH Immediate data or labels
saddrp	FE20H to FF1FH Immediate data or labels (even address only)
addr16	0000H to FFFFH Immediate data or labels (Only even addresses for 16-bit data transfer instructions)
addr11	0800H to 0FFFH Immediate data or labels
addr5	0040H to 007FH Immediate data or labels (even address only)
word	16-bit immediate data or label
byte	8-bit immediate data or label
bit	3-bit immediate data or label
RBn	RB0 to RB3

Note Addresses from FFD0H to FFDFH cannot be accessed with these operands.

Remark For special function register symbols, see **Table 3-9 Special Function Register List**.