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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM® Cortex®-A9
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	800MHz
Co-Processors/DSP	Multimedia; NEON™ SIMD
RAM Controllers	DDR3, LPDDR2, LVDDR3
Graphics Acceleration	Yes
Display & Interface Controllers	Keypad, LCD
Ethernet	10/100/1000Mbps (1)
SATA	-
USB	USB 2.0 + PHY (4)
Voltage - I/O	1.8V, 2.5V, 2.8V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	ARM TZ, Boot Security, Cryptography, RTIC, Secure Fusebox, Secure JTAG, Secure Memory, Secure RTC, Tamper Detection
Package / Case	624-LFBGA
Supplier Device Package	624-MAPBGA (21x21)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx6u7cvm08ad

The i.MX 6Solo/6DualLite processors are specifically useful for applications such as:

- Graphics rendering for Human Machine Interfaces (HMI)
- High-performance speech processing with large databases
- Video processing and display
- Portable medical
- Home energy management systems
- Industrial control and automation

The i.MX 6Solo/6DualLite applications processors feature:

- Multilevel memory system—The multilevel memory system of each processor is based on the L1 instruction and data caches, L2 cache, and internal and external memory. The processors support many types of external memory devices, including DDR3, DDR3L, LPDDR2, NOR Flash, PSRAM, cellular RAM, NAND Flash (MLC and SLC), OneNAND™, and managed NAND, including eMMC up to rev 4.4/4.41.
- Smart speed technology—The processors have power management throughout the IC that enables the rich suite of multimedia features and peripherals to consume minimum power in both active and various low power modes. Smart speed technology enables the designer to deliver a feature-rich product, requiring levels of power far lower than industry expectations.
- Dynamic voltage and frequency scaling—The processors improve the power efficiency of devices by scaling the voltage and frequency to optimize performance.
- Multimedia powerhouse—The multimedia performance of each processor is enhanced by a multilevel cache system, NEON™ MPE (Media Processor Engine) co-processor, a multi-standard hardware video codec, an image processing unit (IPU), a programmable smart DMA (SDMA) controller, and an asynchronous sample rate converter.
- Powerful graphics acceleration—Each processor provides two independent, integrated graphics processing units: an OpenGL® ES 2.0 3D graphics accelerator with a shader and a 2D graphics accelerator.
- Interface flexibility—Each processor supports connections to a variety of interfaces: LCD controller for up to two displays (including parallel display, HDMI1.4, MIPI display, and LVDS display), dual CMOS sensor interface (parallel or through MIPI), high-speed USB on-the-go with PHY, high-speed USB host with PHY, multiple expansion card ports (high-speed MMC/SDIO host and other), 10/100/1000 Mbps Gigabit Ethernet controller two CAN ports, ESAI audio interface, and a variety of other popular interfaces (such as UART, I^2C, and I^2S serial audio, and PCIe-II).
- Advanced security—The processors deliver hardware-enabled security features that enable secure e-commerce, digital rights management (DRM), information encryption, secure boot, and secure software downloads. The security features are discussed in detail in the *i.MX 6Solo/6DualLite Security Reference Manual* (IMX6DQ6SDLSRM).
- Integrated power management—The processors integrate linear regulators and internally generate voltage levels for different domains. This significantly simplifies system power management structure.

4.1.3 Operating Ranges

Table 8 provides the operating ranges of the i.MX 6Solo/6DualLite processors. For details on the chip's power structure, see the "Power Management Unit (PMU)" chapter of the *i.MX 6Solo/6DualLite Reference Manual (*IMX6SDLRM*)*.

Table 8. Operating Ranges

Parameter Description	Symbol	Min	Typ	Max[1]	Unit	Comment[2]
Run mode: LDO enabled	VDD_ARM_IN	1.275[3]	—	1.5	V	LDO Output Set Point (VDD_ARM_CAP) = 1.150 V minimum for operation up to 792MHz.
		1.275[3]	—	1.5	V	LDO Output Set Point (VDD_ARM_CAP) = 1.125 V minimum for operation up to 396MHz.
	VDD_SOC_IN	1.275[3,4]	—	1.5	V	VPU ≤ 328 MHz, VDD_SOC and VDD_PU LDO outputs (VDD_SOC_CAP and VDD_PU_CAP) = 1.225 V[5] maximum and 1.15 V minimum.
Run mode: LDO bypassed	VDD_ARM_IN	1.150	—	1.3	V	LDO bypassed for operation up to 792 MHz
		1.125	—	1.3	V	LDO bypassed for operation up to 396 MHz
	VDD_SOC_IN	1.150[6]	—	1.21[5]	V	LDO bypassed for operation VPU ≤ 328 MHz
Standby/DSM mode	VDD_ARM_IN	0.9	—	1.3	V	Refer to Table 11, "Stop Mode Current and Power Consumption," on page 29.
	VDD_SOC_IN	0.9	—	1.225[5]	V	—
VDD_HIGH internal regulator	VDD_HIGH_IN	2.8	—	3.3	V	Must match the range of voltages that the rechargeable backup battery supports.
Backup battery supply range	VDD_SNVS_IN[7]	2.9	—	3.3	V	Must be supplied from the same supply as VDD_HIGH_IN if the system does not require keeping real time and other data on OFF state.
USB supply voltages	USB_OTG_VBUS	4.4	—	5.25	V	—
	USB_H1_VBUS	4.4	—	5.25	V	—
DDR I/O supply voltage	NVCC_DRAM	1.14	1.2	1.3	V	LPDDR2
		1.425	1.5	1.575	V	DDR3
		1.283	1.35	1.45	V	DDR3L
Supply for RGMII I/O power group[8]	NVCC_RGMII	1.15	—	2.625	V	1.15 V–1.30 V in HSIC 1.2 V mode 1.43 V–1.58 V in RGMII 1.5 V mode 1.70 V–1.90 V in RGMII 1.8 V mode 2.25 V–2.625 V in RGMII 2.5 V mode

Table 10. Maximum Supply Currents (continued)

Power Line	Conditions	Max Current	Unit
NVCC_LVDS2P5[6]	—	NVCC_LVDS2P5 is connected to VDD_HIGH_CAP at the board level. VDD_HIGH_CAP is capable of handing the current required by NVCC_LVDS2P5.	—
MISC			
DDR_VREF	—	1	mA

1 The actual maximum current drawn from VDD_HIGH_IN will be as shown plus any additional current drawn from the VDD_HIGH_CAP outputs, depending upon actual application configuration (for example, NVCC_LVDS_2P5, NVCC_MIPI, or HDMI and PCIe VPH supplies).

2 Under normal operating conditions, the maximum current on VDD_SNVS_IN is shown in Table 10. The maximum VDD_SNVS_IN current may be higher depending on specific operating configurations, such as BOOT_MODE[1:0] not equal to 00, or use of the Tamper feature. During initial power on, VDD_SNVS_IN can draw up to 1 mA if the supply is capable of sourcing that current. If less than 1 mA is available, the VDD_SNVS_CAP charge time will increase.

3 This is the maximum current per active USB physical interface.

4 The DRAM power consumption is dependent on several factors, such as external signal termination. DRAM power calculators are typically available from the memory vendors. They take in account factors, such as signal termination. See the i.MX 6Solo/DualLite Power Consumption Measurement Application Note (AN4576) for examples of DRAM power consumption during specific use case scenarios.

5 General equation for estimated, maximum power consumption of an IO power supply:

Imax = N x C x V x (0.5 x F)

Where:

N—Number of IO pins supplied by the power line

C—Equivalent external capacitive load

V—IO voltage

(0.5 xF)—Data change rate. Up to 0.5 of the clock rate (F)

In this equation, Imax is in Amps, C in Farads, V in Volts, and F in Hertz.

6 NVCC_LVDS2P5 is supplied by VDD_HIGH_CAP (by external connection) so the maximum supply current is included in the current shown for VDD_HIGH_IN. The maximum supply current for NVCC_LVDS2P5 has not been characterized separately.

4.1.6 Low Power Mode Supply Currents

Table 11 shows the current core consumption (not including I/O) of i.MX 6Solo/6DualLite processors in selected low power modes.

Table 11. Stop Mode Current and Power Consumption

Mode	Test Conditions	Supply	Typical[1]	Units
WAIT	• ARM, SoC, and PU LDOs are set to 1.225 • HIGH LDO set to 2.5 V • Clocks are gated. • DDR is in self refresh. • PLLs are active in bypass (24MHz) • Supply Voltages remain ON	VDD_ARM_IN (1.4V)	4.5	mA
		VDD_SOC_IN (1.4V)	23	
		VDD_HIGH_IN (3.0V)	13.5	
		Total	79	mW

4.1.7 USB PHY Current Consumption

4.1.7.1 Power Down Mode

In power down mode, everything is powered down, including the USB_VBUS valid detectors in typical condition. Table 12 shows the USB interface current consumption in power down mode.

Table 12. USB PHY Current Consumption in Power Down Mode

	VDD_USB_CAP (3.0 V)	VDD_HIGH_CAP (2.5 V)	NVCC_PLL_OUT (1.1 V)
Current	5.1 µA	1.7 µA	<0.5 µA

NOTE

The currents on the VDD_HIGH_CAP and VDD_USB_CAP were identified to be the voltage divider circuits in the USB-specific level shifters.

4.1.8 PCIe 2.0 Power Consumption

Table 13 provides PCIe PHY currents under certain Tx operating modes.

Table 13. PCIe PHY Current Drain

Mode	Test Conditions	Supply	Max Current	Unit
P0: Normal Operation	5G Operations	PCIE_VP (1.1 V)	40	mA
		PCIE_VPTX (1.1 V)	20	
		PCIE_VPH (2.5 V)	21	
	2.5G Operations	PCIE_VP (1.1 V)	27	
		PCIE_VPTX (1.1 V)	20	
		PCIE_VPH (2.5 V)	20	
P0s: Low Recovery Time Latency, Power Saving State	5G Operations	PCIE_VP (1.1 V)	30	mA
		PCIE_VPTX (1.1 V)	2.4	
		PCIE_VPH (2.5 V)	18	
	2.5G Operations	PCIE_VP (1.1 V)	20	
		PCIE_VPTX (1.1 V)	2.4	
		PCIE_VPH (2.5 V)	18	
P1: Longer Recovery Time Latency, Lower Power State	—	PCIE_VP (1.1 V)	12	mA
		PCIE_VPTX (1.1 V)	2.4	
		PCIE_VPH (2.5 V)	12	

4.4.5 ARM PLL

Table 19. ARM PLL's Electrical Parameters

Parameter	Value
Clock output range	650 MHz ~ 1.3 GHz
Reference clock	24 MHz
Lock time	<2250 reference cycles

4.5 On-Chip Oscillators

4.5.1 OSC24M

This block implements an amplifier that when combined with a suitable quartz crystal and external load capacitors implements an oscillator. The oscillator is powered from NVCC_PLL_OUT.

The system crystal oscillator consists of a Pierce-type structure running off the digital supply. A straight forward biased-inverter implementation is used.

4.5.2 OSC32K

This block implements an amplifier that when combined with a suitable quartz crystal and external load capacitors implements a low power oscillator. It also implements a power mux such that it can be powered from either a ~3 V backup battery (VDD_SNVS_IN) or VDD_HIGH_IN such as the oscillator consumes power from VDD_HIGH_IN when that supply is available and transitions to the back up battery when VDD_HIGH_IN is lost.

In addition, if the clock monitor determines that the OSC32K is not present, then the source of the 32 kHz clock will automatically switch to the internal ring oscillator.

CAUTION

The internal RTC oscillator does not provide an accurate frequency and is affected by process, voltage, and temperature variations. NXP strongly recommends using an external crystal as the RTC_XTALI reference. If the internal oscillator is used instead, careful consideration must be given to the timing implications on all of the SoC modules dependent on this clock.

The OSC32k runs from VDD_SNVS_CAP supply, which comes from VDD_HIGH_IN/VDD_SNVS_IN.

4.6.5 LVDS I/O DC Parameters

The LVDS interface complies with TIA/EIA 644-A standard. See TIA/EIA STANDARD 644-A, "*Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits*" for details.

Table 26 shows the Low Voltage Differential Signaling (LVDS) I/O DC parameters.

Table 26. LVDS I/O DC Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Differential Voltage	VOD	Rload-100 Ω Diff	250	350	450	mV
Output High Voltage	VOH	IOH = 0 mA	1.25	1.375	1.6	V
Output Low Voltage	VOL	IOL = 0 mA	0.9	1.025	1.25	V
Offset Voltage	VOS	—	1.125	1.2	1.375	V

4.7 I/O AC Parameters

This section includes the AC parameters of the following I/O types:

- General Purpose I/O (GPIO)
- Double Data Rate I/O (DDR) for LPDDR2 and DDR3/DDR3L modes
- LVDS I/O

The GPIO and DDR I/O load circuit and output transition time waveforms are shown in Figure 5 and Figure 6.

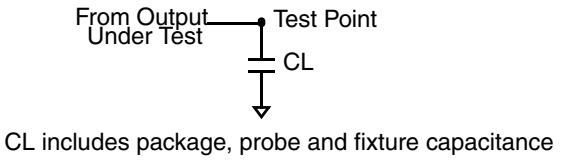

Figure 5. Load Circuit for Output

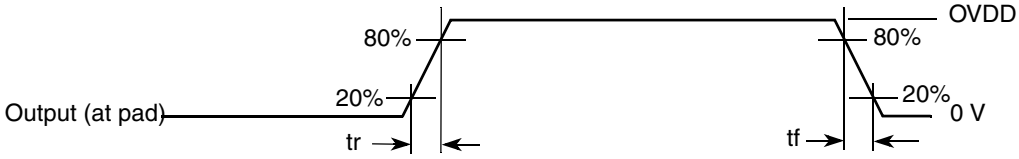

Figure 6. Output Transition Time Waveform

4.7.1 General Purpose I/O AC Parameters

The I/O AC parameters for GPIO in slow and fast modes are presented in the Table 27 and Table 28, respectively. Note that the fast or slow I/O behavior is determined by the appropriate control bits in the IOMUXC control registers.

4.7.3 LVDS I/O AC Parameters

The differential output transition time waveform is shown in Figure 7.

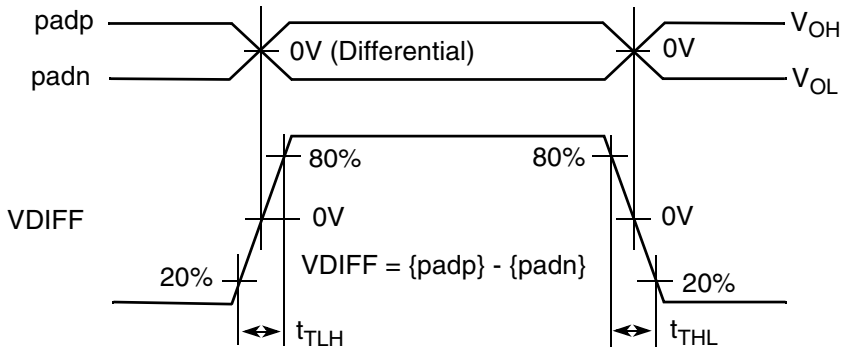

Figure 7. Differential LVDS Driver Transition Time Waveform

Table 31 shows the AC parameters for LVDS I/O.

Table 31. I/O AC Parameters of LVDS Pad

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Differential pulse skew[1]	t_{SKD}	Rload = 100 Ω, Cload = 2 pF	—	—	0.25	ns
Transition Low to High Time[2]	t_{TLH}		—	—	0.5	
Transition High to Low Time[2]	t_{THL}		—	—	0.5	
Operating Frequency	f	—	—	600	800	MHz
Offset voltage imbalance	Vos	—	—	—	150	mV

1 t_{SKD} = | t_{PHLD} - t_{PLHD} |, is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.

2 Measurement levels are 20-80% from output voltage.

4.8 Output Buffer Impedance Parameters

This section defines the I/O impedance parameters of the i.MX 6Solo/6DualLite processors for the following I/O types:

- General Purpose I/O (GPIO)
- Double Data Rate I/O (DDR) for LPDDR2, and DDR3/DDR3L modes
- LVDS I/O

NOTE

GPIO and DDR I/O output driver impedance is measured with “long” transmission line of impedance Ztl attached to I/O pad and incident wave launched into transmission line. Rpu/Rpd and Ztl form a voltage divider that defines specific voltage of incident wave relative to OVDD. Output driver impedance is calculated from this voltage divider (see Figure 8).

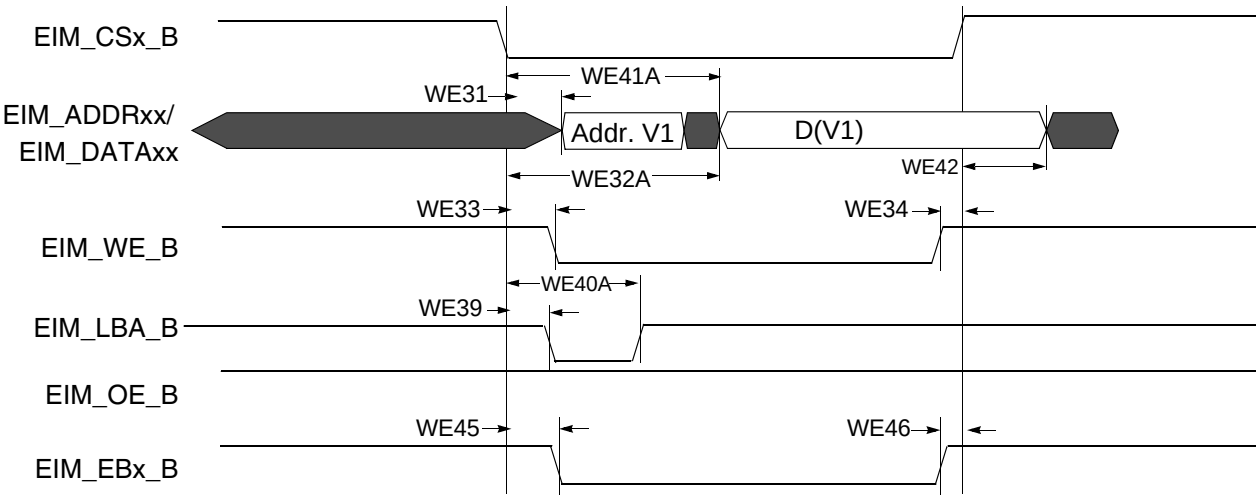

Figure 20. Asynchronous A/D Muxed Write Access

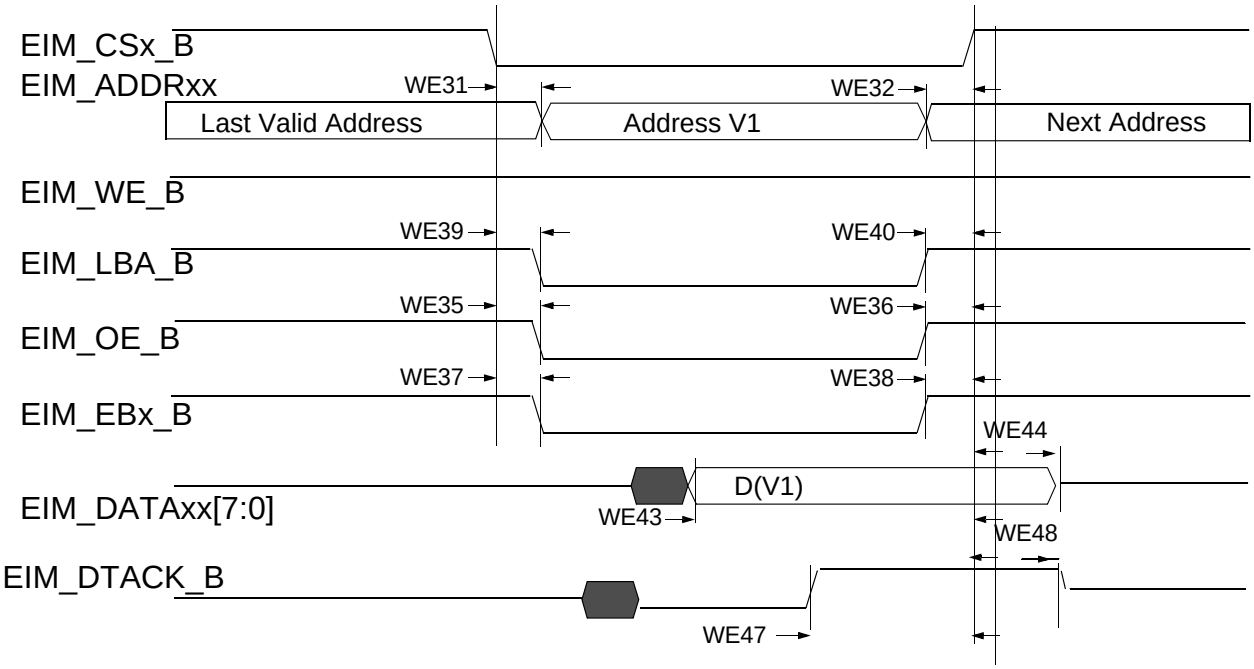

Figure 21. DTACK Mode Read Access (DAP=0)

Table 39. EIM Asynchronous Timing Parameters Table Relative Chip to Select (continued)

Ref No.	Parameter	Determination by Synchronous measured parameters[1]	Min	Max	Unit
WE47	EIM_DTACK_B Active to EIM_CSx_B Invalid	MAXCO - MAXCSO + MAXDTI	MAXCO - MAXCSO + MAXDTI	—	ns
WE48	EIM_CSx_B Invalid to EIM_DTACK_B Invalid	0	0	—	ns

1 For more information on configuration parameters mentioned in this table, see the i.MX 6Solo/6DualLite reference manual.
2 In this table, CSA means WCSA when write operation or RCSA when read operation.
3 In this table, CSN means WCSN when write operation or RCSN when read operation.
4 t is ACLK_EIM_SLOW_CLK_ROOT cycle time.
5 In this table, ADVN means WADVN when write operation or RADVN when read operation.
6 In this table, ADVA means WADVA when write operation or RADVA when read operation.

4.9.4 Multi-Mode DDR Controller (MMDC)

The Multi-Mode DDR Controller is a dedicated interface to DDR3/DDR3L/LPDDR2 SDRAM.

4.9.4.1 MMDC Compatibility with JEDEC-compliant SDRAMs

The i.MX 6Solo/6DualLite MMDC supports the following memory types:

- LPDDR2 SDRAM compliant to JESD209-2B LPDDR2 JEDEC standard release June, 2009
- DDR3/DDR3L SDRAM compliant to JESD79-3D DDR3 JEDEC standard release April, 2008

MMDC operation with the standards stated above is contingent upon the board DDR design adherence to the DDR design and layout requirements stated in the *Hardware Development Guide for i.MX 6Quad, 6Dual, 6DualLite, 6Solo Families of Applications Processors* (IMX6DQ6SDLHDG).

4.9.4.2 MMDC Supported DDR3/DDR3L/LPDDR2 Configurations

Table 40 and Table 41 show the supported DDR3/DDR3L/LPDDR2 configurations.

Table 40. i.MX 6Solo Supported DDR3/DDR3L/LPDDR2 Configurations

Parameter	LPDDR2	DDR3	DDR3L
Clock frequency	400 MHz	400 MHz	400 MHz
Bus width	16/32-bit	16/32-bit	16/32-bit
Channel	Single	Single	Single
Chip selects	2	2	2

4.10.2 Source Synchronous Mode AC Timing (ONFI 2.x Compatible)

Figure 28 to Figure 30 show the write and read timing of Source Synchronous Mode.

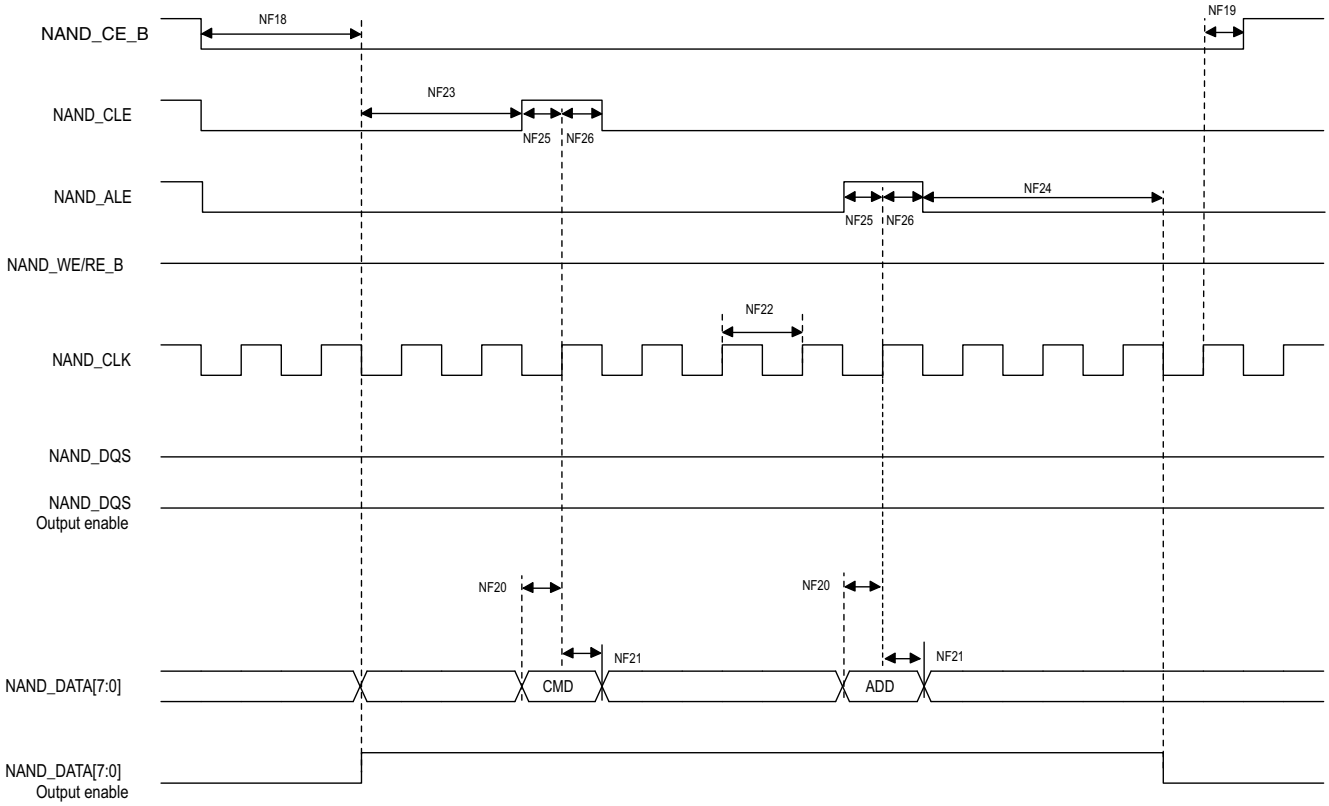

Figure 28. Source Synchronous Mode Command and Address Timing Diagram

[1] 1 Clock duty cycle will be in the range of 47% to 53%.

4.11.4.3 SDR50/SDR104 AC Timing

Figure 40 depicts the timing of SDR50/SDR104, and Table 50 lists the SDR50/SDR104 timing characteristics.

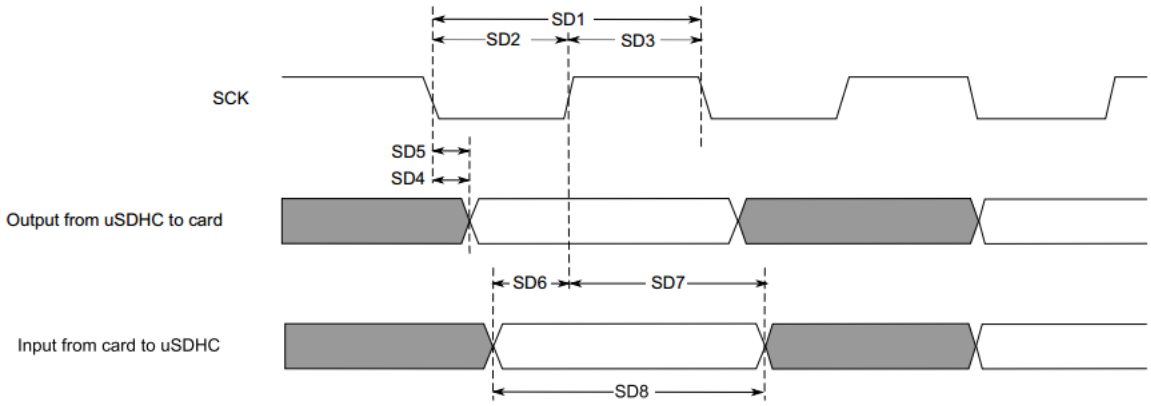

Figure 40. SDR50/SDR104 Timing

Table 50. SDR50/SDR104 Interface Timing Specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency Period	t_{CLK}	4.8	—	ns
SD2	Clock Low Time	t_{CL}	$0.46 \times t_{CLK}$	$0.54 \times t_{CLK}$	ns
SD3	Clock High Time	t_{CH}	$0.46 \times t_{CLK}$	$0.54 \times t_{CLK}$	ns
uSDHC Output/Card Inputs SDx_CMD, SDx_DATAx in SDR50 (Reference to CLK)					
SD4	uSDHC Output Delay	t_{OD}	–3	1	ns
uSDHC Output/Card Inputs SDx_CMD, SDx_DATAx in SDR104 (Reference to CLK)					
SD5	uSDHC Output Delay	t_{OD}	–1.6	0.74	ns
uSDHC Input/Card Outputs SDx_CMD, SDx_DATAx in SDR50 (Reference to CLK)					
SD6	uSDHC Input Setup Time	t_{ISU}	2.5	—	ns
SD7	uSDHC Input Hold Time	t_{IH}	1.5	—	ns
uSDHC Input/Card Outputs SDx_CMD, SDx_DATAx in SDR104 (Reference to CLK)[1]					
SD8	Card Output Data Window	t_{ODW}	$0.5 \times t_{CLK}$	—	ns

[1]Data window in SDR100 mode is variable.

Table 56. RGMII Signal Switching Specifications[1]

Symbol	Description	Min	Max	Unit
T_{cyc}[2]	Clock cycle duration	7.2	8.8	ns
T_{skewT}[3]	Data to clock output skew at transmitter	-500	500	ps
T_{skewR}[3]	Data to clock input skew at receiver	1	2.6	ns
Duty_G[4]	Duty cycle for Gigabit	45	55	%
Duty_T[4]	Duty cycle for 10/100T	40	60	%
Tr/Tf	Rise/fall time (20–80%)	—	0.75	ns

1 The timings assume the following configuration:
DDR_SEL = (11)b
DSE (drive-strength) = (111)b

2 For 10 Mbps and 100 Mbps, T_{cyc} will scale to 400 ns ±40 ns and 40 ns ±4 ns respectively.

3 For all versions of RGMII prior to 2.0; This implies that PC board design will require clocks to be routed such that an additional trace delay of greater than 1.5 ns and less than 2.0 ns will be added to the associated clock signal. For 10/100, the Max value is unspecified.

4 Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domain as long as minimum duty cycle is not violated and stretching occurs for no more than three Tcyc of the lowest speed transitioned between.

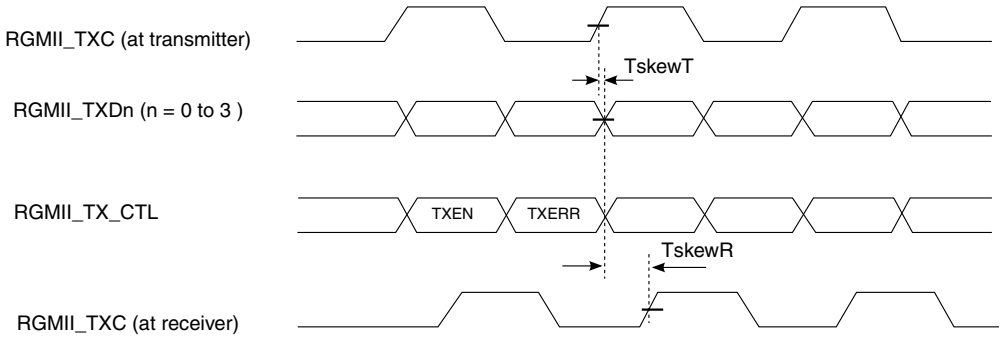

Figure 46. RGMII Transmit Signal Timing Diagram Original

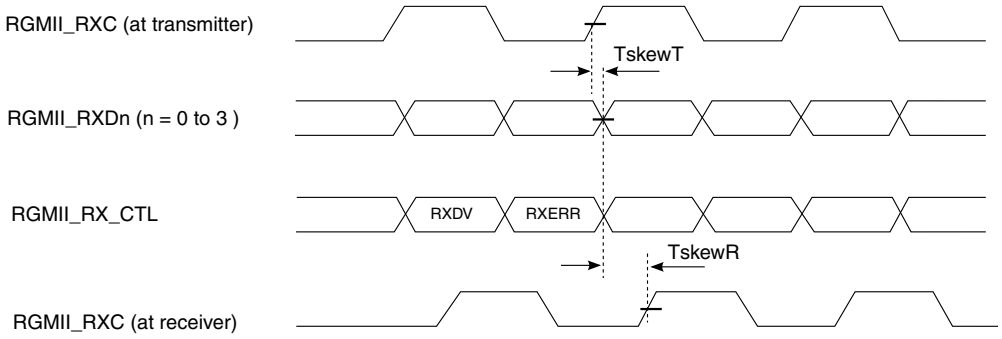

Figure 47. RGMII Receive Signal Timing Diagram Original

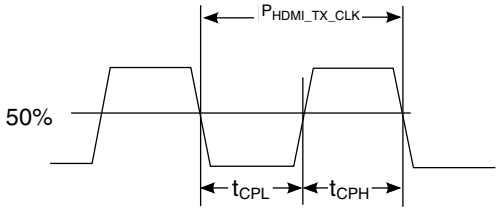

Figure 52. TMDS Clock Signal Definitions

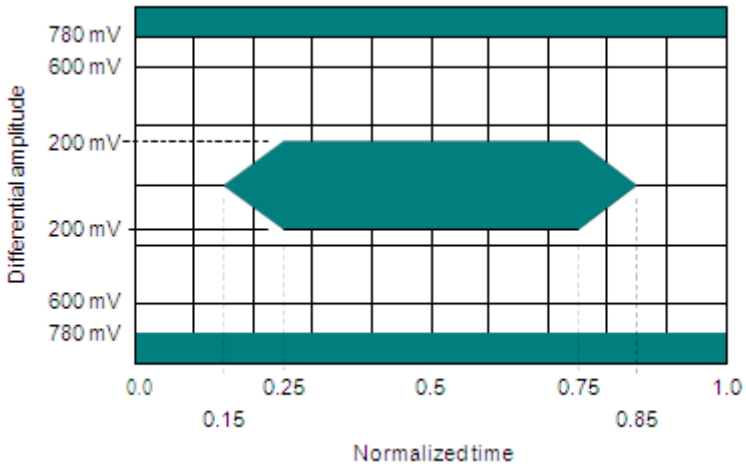

Figure 53. Eye Diagram Mask Definition for HDMI Driver Signal Specification at TP1

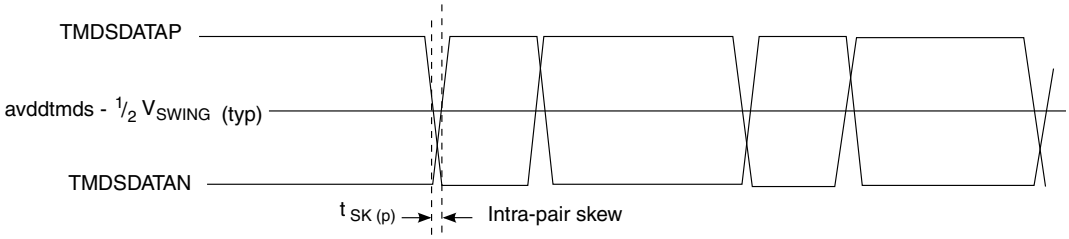

Figure 54. Intra-Pair Skew Definition

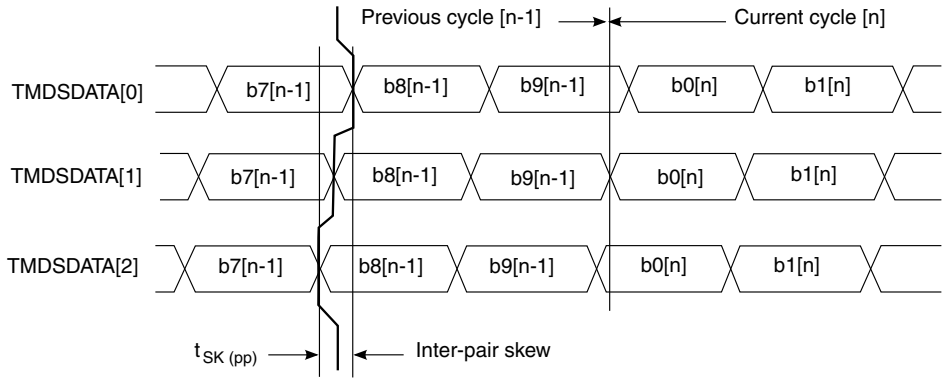

Figure 55. Inter-Pair Skew Definition

corresponding internal events—local start points. The timing diagrams correspond to inverse polarity of the IPP_DISP_CLK signal and active-low polarity of the HSYNC, VSYNC, and DRDY signals.

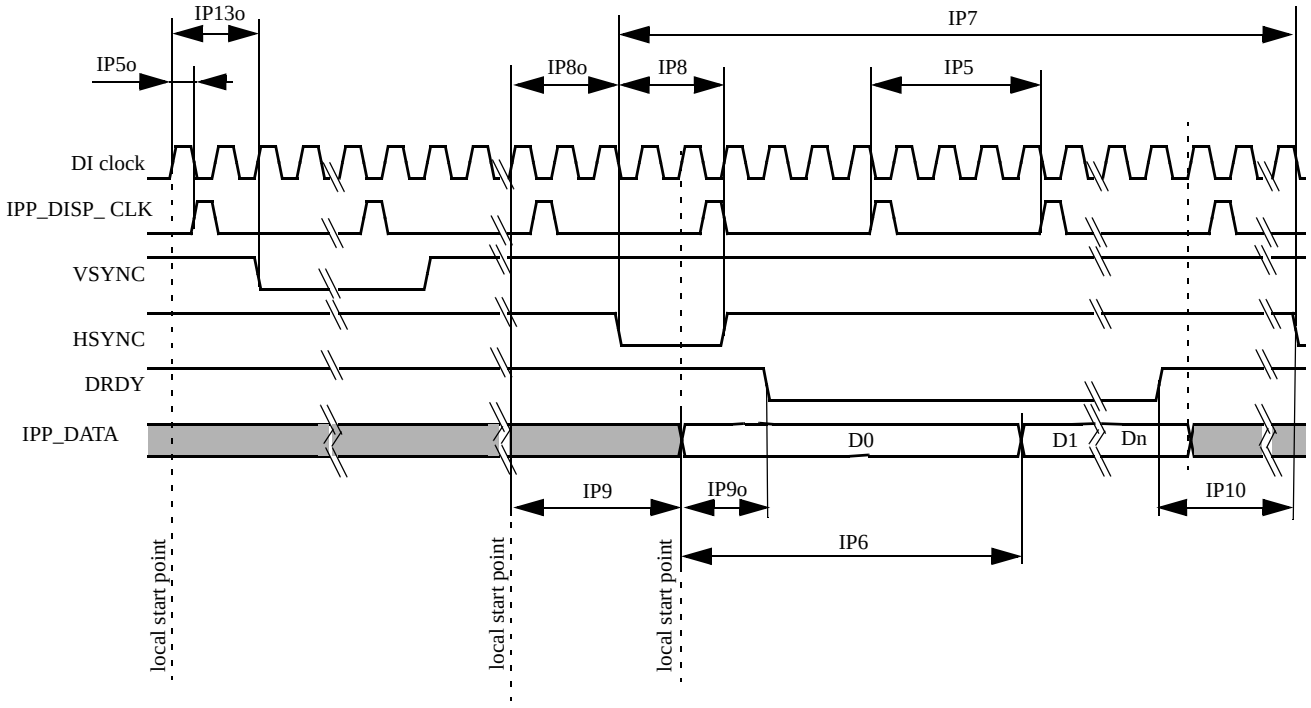

Figure 62. TFT Panels Timing Diagram—Horizontal Sync Pulse

Figure 63 depicts the vertical timing (timing of one frame). All parameters shown in the figure are programmable.

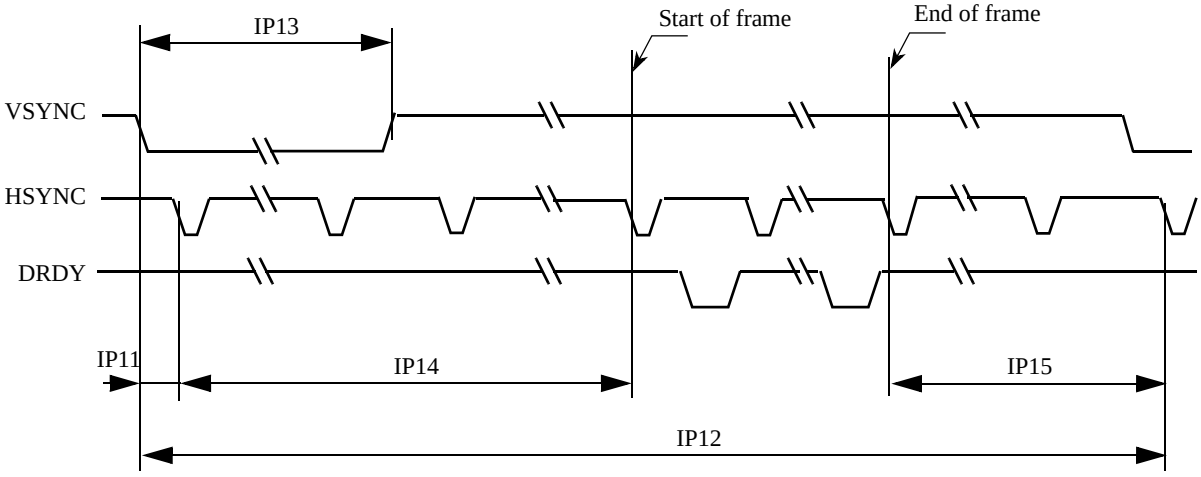

Figure 63. TFT Panels Timing Diagram—Vertical Sync Pulse

Table 76. SSI Receiver Timing with External Clock

ID	Parameter	Min	Max	Unit
External Clock Operation				
SS22	AUDx_TXC/AUDx_RXC clock period	81.4	—	ns
SS23	AUDx_TXC/AUDx_RXC clock high period	36	—	ns
SS24	AUDx_TXC/AUDx_RXC clock rise time	—	6.0	ns
SS25	AUDx_TXC/AUDx_RXC clock low period	36	—	ns
SS26	AUDx_TXC/AUDx_RXC clock fall time	—	6.0	ns
SS28	AUDx_RXC high to AUDx_TXFS (bl) high	-10	15.0	ns
SS30	AUDx_RXC high to AUDx_TXFS (bl) low	10	—	ns
SS32	AUDx_RXC high to AUDx_TXFS (wl) high	-10	15.0	ns
SS34	AUDx_RXC high to AUDx_TXFS (wl) low	10	—	ns
SS35	AUDx_TXC/AUDx_RXC External AUDx_TXFS rise time	—	6.0	ns
SS36	AUDx_TXC/AUDx_RXC External AUDx_TXFS fall time	—	6.0	ns
SS40	AUDx_RXD setup time before AUDx_RXC low	10	—	ns
SS41	AUDx_RXD hold time after AUDx_RXC low	2	—	ns

NOTE

- All the timings for the SSI are given for a non-inverted serial clock polarity (TSCKP/RSCKP = 0) and a non-inverted frame sync (TFSI/RFSI = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the clock signal AUDx_TXC/AUDx_RXC and/or the frame sync AUDx_TXFS/AUDx_RXFS shown in the tables and in the figures.
- All timings are on Audiomux Pads when SSI is being used for data transfer.
- The terms, WL and BL, refer to Word Length (WL) and Bit Length(BL).
- For internal Frame Sync operation using external clock, the frame sync timing is same as that of transmit data (for example, during AC97 mode of operation).

Table 86 shows the 21 × 21 mm BGA package details.

Table 86. 21 x 21, 0.8 mm BGA Package Details

Parameter	Symbol	Common Dimensions		
		Minimum	Normal	Maximum
Total Thickness	A	—	—	1.6
Stand Off	A1	0.36	—	0.46
Substrate Thickness	A2	0.26 REF		
Mold Thickness	A3	0.7 REF		
Body Size	D	21 BSC		
	E	21 BSC		
Ball Diameter	—	0.5		
Ball Opening	—	0.4		
Ball Width	b	0.44	—	0.64
Ball Pitch	e	0.8 BSC		
Ball Count	n	624		
Edge Ball Center to Center	D1	19.2 BSC		
	E1	19.2 BSC		
Body Center to Contact Ball	SD	—		
	SE	—		
Package Edge Tolerance	aaa	0.1		
Mold Flatness	bbb	0.2		
Coplanarity	ddd	0.15		
Ball Offset (Package)	eee	0.15		
Ball Offset (Ball)	fff	0.08		

Table 88. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function	Input/ Output	Value[2]
DISP0_DAT4	P20	NVCC_LCD	GPIO	ALT5	GPIO4_IO25	Input	100 kΩ pull-up
DISP0_DAT5	R25	NVCC_LCD	GPIO	ALT5	GPIO4_IO26	Input	100 kΩ pull-up
DISP0_DAT6	R23	NVCC_LCD	GPIO	ALT5	GPIO4_IO27	Input	100 kΩ pull-up
DISP0_DAT7	R24	NVCC_LCD	GPIO	ALT5	GPIO4_IO28	Input	100 kΩ pull-up
DISP0_DAT8	R22	NVCC_LCD	GPIO	ALT5	GPIO4_IO29	Input	100 kΩ pull-up
DISP0_DAT9	T25	NVCC_LCD	GPIO	ALT5	GPIO4_IO30	Input	100 kΩ pull-up
DRAM_A0	AC14	NVCC_DRAM	DDR	ALT0	DRAM_ADDR00	Output	Low
DRAM_A1	AB14	NVCC_DRAM	DDR	ALT0	DRAM_ADDR01	Output	Low
DRAM_A10	AA15	NVCC_DRAM	DDR	ALT0	DRAM_ADDR10	Output	Low
DRAM_A11	AC12	NVCC_DRAM	DDR	ALT0	DRAM_ADDR11	Output	Low
DRAM_A12	AD12	NVCC_DRAM	DDR	ALT0	DRAM_ADDR12	Output	Low
DRAM_A13	AC17	NVCC_DRAM	DDR	ALT0	DRAM_ADDR13	Output	Low
DRAM_A14	AA12	NVCC_DRAM	DDR	ALT0	DRAM_ADDR14	Output	Low
DRAM_A15	Y12	NVCC_DRAM	DDR	ALT0	DRAM_ADDR15	Output	Low
DRAM_A2	AA14	NVCC_DRAM	DDR	ALT0	DRAM_ADDR02	Output	Low
DRAM_A3	Y14	NVCC_DRAM	DDR	ALT0	DRAM_ADDR03	Output	Low
DRAM_A4	W14	NVCC_DRAM	DDR	ALT0	DRAM_ADDR04	Output	Low
DRAM_A5	AE13	NVCC_DRAM	DDR	ALT0	DRAM_ADDR05	Output	Low
DRAM_A6	AC13	NVCC_DRAM	DDR	ALT0	DRAM_ADDR06	Output	Low
DRAM_A7	Y13	NVCC_DRAM	DDR	ALT0	DRAM_ADDR07	Output	Low
DRAM_A8	AB13	NVCC_DRAM	DDR	ALT0	DRAM_ADDR08	Output	Low
DRAM_A9	AE12	NVCC_DRAM	DDR	ALT0	DRAM_ADDR09	Output	Low
DRAM_CAS	AE16	NVCC_DRAM	DDR	ALT0	DRAM_CAS	Output	Low
DRAM_CS0	Y16	NVCC_DRAM	DDR	ALT0	DRAM_CS0	Output	Low
DRAM_CS1	AD17	NVCC_DRAM	DDR	ALT0	DRAM_CS1	Output	Low
DRAM_D0	AD2	NVCC_DRAM	DDR	ALT0	DRAM_DATA00	Input	100 kΩ pull-up
DRAM_D1	AE2	NVCC_DRAM	DDR	ALT0	DRAM_DATA01	Input	100 kΩ pull-up
DRAM_D10	AA6	NVCC_DRAM	DDR	ALT0	DRAM_DATA10	Input	100 kΩ pull-up
DRAM_D11	AE7	NVCC_DRAM	DDR	ALT0	DRAM_DATA11	Input	100 kΩ pull-up
DRAM_D12	AB5	NVCC_DRAM	DDR	ALT0	DRAM_DATA12	Input	100 kΩ pull-up
DRAM_D13	AC5	NVCC_DRAM	DDR	ALT0	DRAM_DATA13	Input	100 kΩ pull-up
DRAM_D14	AB6	NVCC_DRAM	DDR	ALT0	DRAM_DATA14	Input	100 kΩ pull-up
DRAM_D15	AC7	NVCC_DRAM	DDR	ALT0	DRAM_DATA15	Input	100 kΩ pull-up
DRAM_D16	AB7	NVCC_DRAM	DDR	ALT0	DRAM_DATA16	Input	100 kΩ pull-up
DRAM_D17	AA8	NVCC_DRAM	DDR	ALT0	DRAM_DATA17	Input	100 kΩ pull-up
DRAM_D18	AB9	NVCC_DRAM	DDR	ALT0	DRAM_DATA18	Input	100 kΩ pull-up

Table 88. 21 x 21 mm Functional Contact Assignments (continued)

Ball Name	Ball	Power Group	Ball Type	Out of Reset Condition[1]			
				Default Mode (Reset Mode)	Default Function	Input/ Output	Value[2]
RGMII_TD1	F20	NVCC_RGMII	DDR	ALT5	GPIO6_IO21	Input	100 kΩ pull-up
RGMII_TD2	E21	NVCC_RGMII	DDR	ALT5	GPIO6_IO22	Input	100 kΩ pull-up
RGMII_TD3	A24	NVCC_RGMII	DDR	ALT5	GPIO6_IO23	Input	100 kΩ pull-up
RGMII_TX_CTL	C23	NVCC_RGMII	DDR	ALT5	GPIO6_IO26	Input	100 kΩ pull-down
RGMII_TXC	D21	NVCC_RGMII	DDR	ALT5	GPIO6_IO19	Input	100 kΩ pull-down
RTC_XTALI	D9	VDD_SNVS_CAP	—	—	RTC_XTALI	—	—
RTC_XTALO	C9	VDD_SNVS_CAP	—	—	RTC_XTALO	—	—
SD1_CLK	D20	NVCC_SD1	GPIO	ALT5	GPIO1_IO20	Input	100 kΩ pull-up
SD1_CMD	B21	NVCC_SD1	GPIO	ALT5	GPIO1_IO18	Input	100 kΩ pull-up
SD1_DAT0	A21	NVCC_SD1	GPIO	ALT5	GPIO1_IO16	Input	100 kΩ pull-up
SD1_DAT1	C20	NVCC_SD1	GPIO	ALT5	GPIO1_IO17	Input	100 kΩ pull-up
SD1_DAT2	E19	NVCC_SD1	GPIO	ALT5	GPIO1_IO19	Input	100 kΩ pull-up
SD1_DAT3	F18	NVCC_SD1	GPIO	ALT5	GPIO1_IO21	Input	100 kΩ pull-up
SD2_CLK	C21	NVCC_SD2	GPIO	ALT5	GPIO1_IO10	Input	100 kΩ pull-up
SD2_CMD	F19	NVCC_SD2	GPIO	ALT5	GPIO1_IO11	Input	100 kΩ pull-up
SD2_DAT0	A22	NVCC_SD2	GPIO	ALT5	GPIO1_IO15	Input	100 kΩ pull-up
SD2_DAT1	E20	NVCC_SD2	GPIO	ALT5	GPIO1_IO14	Input	100 kΩ pull-up
SD2_DAT2	A23	NVCC_SD2	GPIO	ALT5	GPIO1_IO13	Input	100 kΩ pull-up
SD2_DAT3	B22	NVCC_SD2	GPIO	ALT5	GPIO1_IO12	Input	100 kΩ pull-up
SD3_CLK	D14	NVCC_SD3	GPIO	ALT5	GPIO7_IO03	Input	100 kΩ pull-up
SD3_CMD	B13	NVCC_SD3	GPIO	ALT5	GPIO7_IO02	Input	100 kΩ pull-up
SD3_DAT0	E14	NVCC_SD3	GPIO	ALT5	GPIO7_IO04	Input	100 kΩ pull-up
SD3_DAT1	F14	NVCC_SD3	GPIO	ALT5	GPIO7_IO05	Input	100 kΩ pull-up
SD3_DAT2	A15	NVCC_SD3	GPIO	ALT5	GPIO7_IO06	Input	100 kΩ pull-up
SD3_DAT3	B15	NVCC_SD3	GPIO	ALT5	GPIO7_IO07	Input	100 kΩ pull-up
SD3_DAT4	D13	NVCC_SD3	GPIO	ALT5	GPIO7_IO01	Input	100 kΩ pull-up
SD3_DAT5	C13	NVCC_SD3	GPIO	ALT5	GPIO7_IO00	Input	100 kΩ pull-up
SD3_DAT6	E13	NVCC_SD3	GPIO	ALT5	GPIO6_IO18	Input	100 kΩ pull-up
SD3_DAT7	F13	NVCC_SD3	GPIO	ALT5	GPIO6_IO17	Input	100 kΩ pull-up
SD3_RST	D15	NVCC_SD3	GPIO	ALT5	GPIO7_IO08	Input	100 kΩ pull-up
SD4_CLK	E16	NVCC_NANDF	GPIO	ALT5	GPIO7_IO10	Input	100 kΩ pull-up
SD4_CMD	B17	NVCC_NANDF	GPIO	ALT5	GPIO7_IO09	Input	100 kΩ pull-up
SD4_DAT0	D18	NVCC_NANDF	GPIO	ALT5	GPIO2_IO08	Input	100 kΩ pull-up
SD4_DAT1	B19	NVCC_NANDF	GPIO	ALT5	GPIO2_IO09	Input	100 kΩ pull-up
SD4_DAT2	F17	NVCC_NANDF	GPIO	ALT5	GPIO2_IO10	Input	100 kΩ pull-up
SD4_DAT3	A20	NVCC_NANDF	GPIO	ALT5	GPIO2_IO11	Input	100 kΩ pull-up

Table 90. 21 x 21 mm, 0.8 mm Pitch Ball Map i.MX 6Solo (continued)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	
AE	GND	DRAM_D1	DRAM_SDQS0	DRAM_D7	DRAM_D9	DRAM_SDQS1_B	DRAM_	DRAM_SDQS2_B	DRAM_D24	DRAM_DQM3	DRAM_D26	DRAM_A9	DRAM_A5	DRAM_SDCLK_1_B	DRAM_SDCLK_0_B	DRAM_CAS	ZQPAD	NC	NC	NC	NC	NC	NC	NC	NC	GND	**AE**
AD	DRAM_D5	DRAM_D0	DRAM_SDQS0_B	GND	DRAM_D8	DRAM_SDQS1	GND	DRAM_SDQS2	DRAM_D29	GND	DRAM_D30	DRAM_A12	GND	DRAM_SDCLK_1	DRAM_SDCLK_0	GND	DRAM_CS1	NC	GND	NC	NC	GND	NC	NC	NC	NC	**AD**
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**	**25**	

Table 91 shows the 21 x 21 mm, 0.8 mm pitch ball map for the i.MX 6DualLite.

Table 91. 21 x 21 mm, 0.8 mm Pitch Ball Map i.MX 6DualLite

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	
A		PCIE_REXT	PCIE_TXM	GND	FA_ANA	USB_OTG_DP	XTALI	GND	NC	NC	NC	NC	GND	NC	SD3_DAT2	NANDF_ALE	NANDF_CS2	NANDF_D0	NANDF_D4	SD4_DAT3	SD1_DAT0	SD2_DAT0	SD2_DAT2	RGMII_TD3	GND	**A**
B	PCIE_RXM	PCIE_RXP	PCIE_TXP	GND	VDD_FA	USB_OTG_DN	XTALO	USB_OTG_CHD_B	NC	NC	NC	NC	SD3_CMD	NC	SD3_DAT3	NANDF_RB0	SD4_CMD	NANDF_D5	SD4_DAT1	SD4_DAT6	SD1_CMD	SD2_DAT3	RGMII_RD1	RGMII_RD2	RGMII_RXC	**B**
C	GND	JTAG_TRSTB	JTAG_TMS	GND	CLK2_N	GND	CLK1_N	GPANAIO	RTC_XTALO	GND	POR_B	BOOT_MODE0	SD3_DAT5	NC	NANDF_CLE	NANDF_CS1	NANDF_D1	NANDF_D7	SD4_DAT5	SD1_DAT1	SD2_CLK	RGMII_TD0	RGMII_TX_CTL	RGMII_RD0	EIM_D16	**C**
D	CSI_D1M	CSI_D1P	GND	CSI_REXT	CLK2_P	GND	CLK1_P	GND	RTC_XTALI	USB_H1_VBUS	PMIC_ON_REQ	ONOFF	SD3_DAT4	SD3_CLK	SD3_RST	NANDF_CS3	NANDF_D3	SD4_DAT0	SD4_DAT7	SD1_CLK	RGMII_TXC	RGMII_RX_CTL	RGMII_RD3	EIM_D18	EIM_D23	**D**
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**	**25**	

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