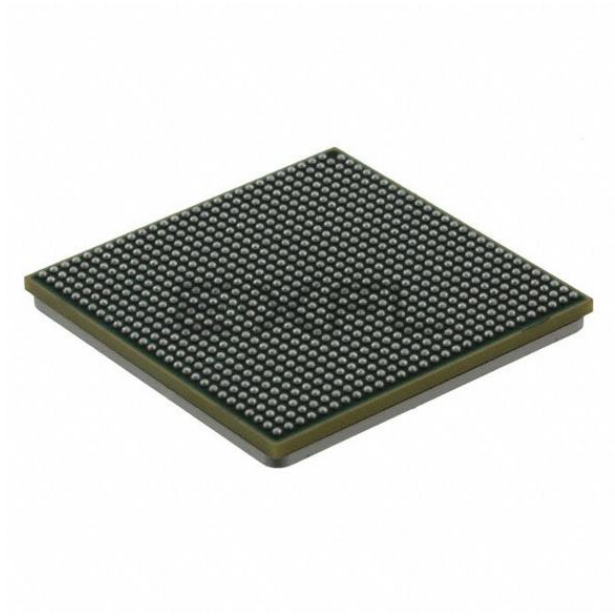

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	SC3850 Six Core
Interface	Ethernet, I²C, PCI, RGMII, Serial RapidIO, SGMII, SPI, UART/USART
Clock Rate	1GHz
Non-Volatile Memory	ROM (96kB)
On-Chip RAM	576kB
Voltage - I/O	2.50V
Voltage - Core	1.00V
Operating Temperature	0°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=msc8156esvt1000b

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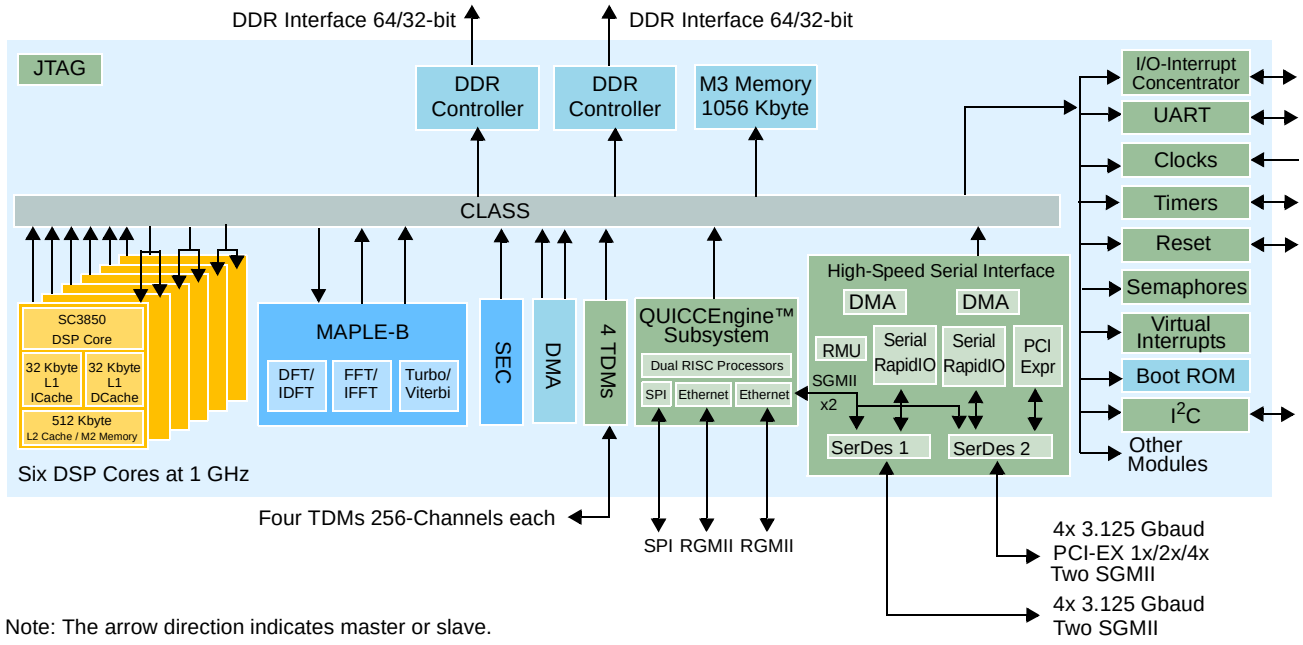


Figure 1. MSC8156E Block Diagram

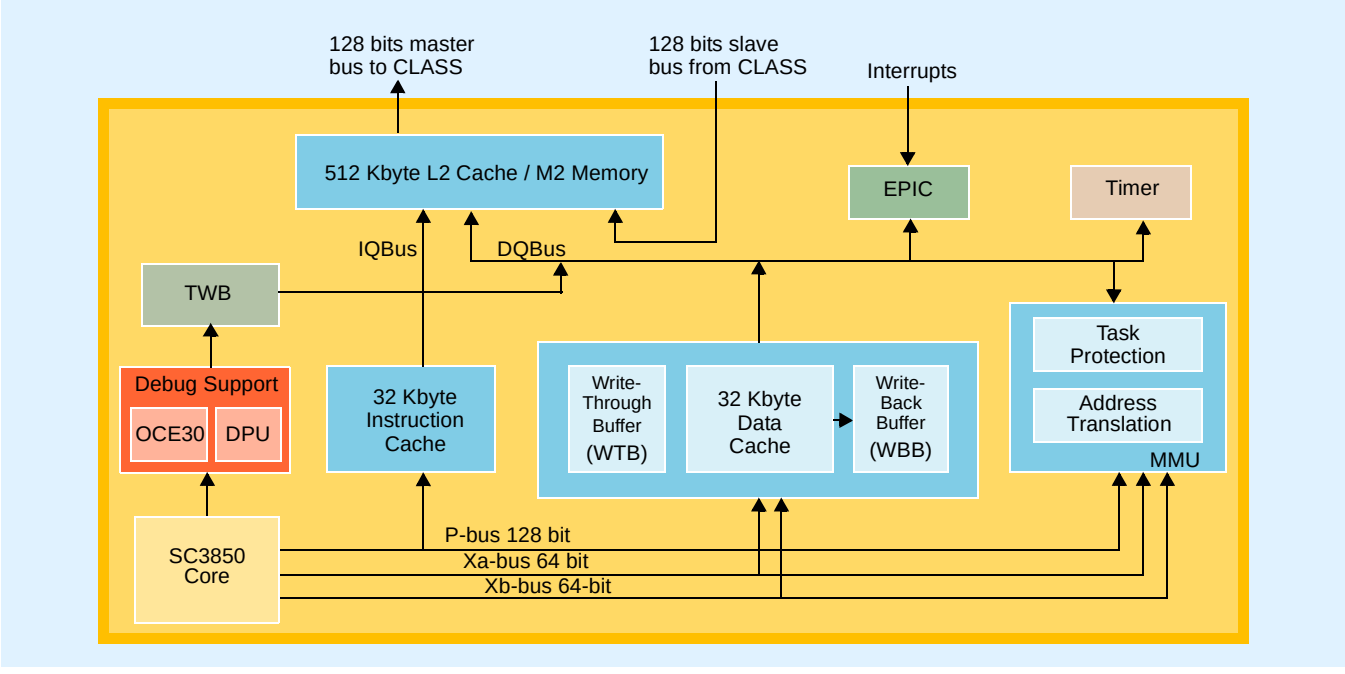


Figure 2. StarCore SC3850 DSP Subsystem Block Diagram

1 Pin Assignment

This section includes diagrams of the MSC8156E package ball grid array layouts and tables showing how the pinouts are allocated for the package.

1.1 FC-PBGA Ball Layout Diagram

The top view of the FC-PBGA package is shown in Figure 3 with the ball location index numbers.

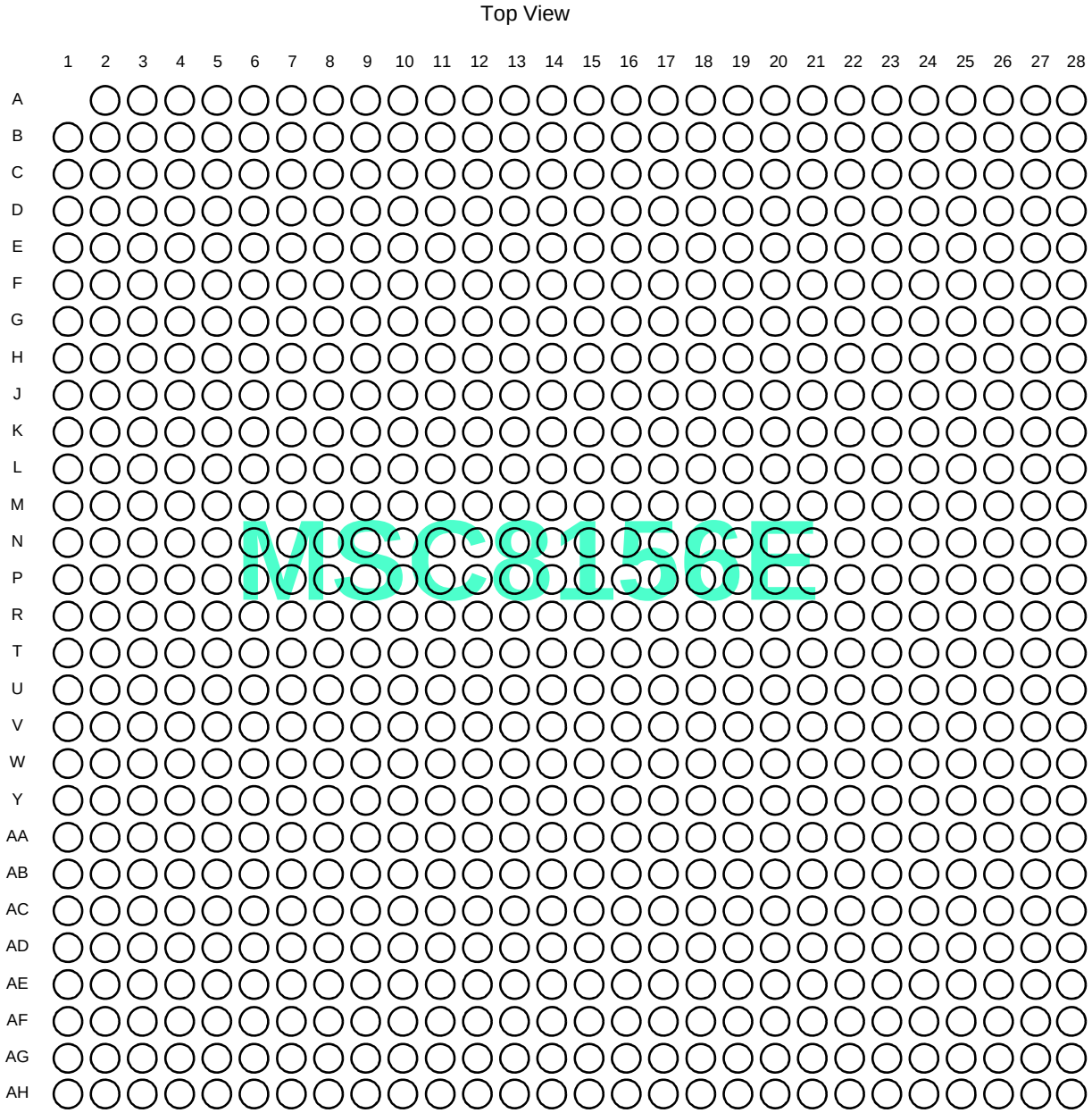


Figure 3. MSC8156E FC-PBGA Package, Top View

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[10]	Power Rail Name
C27	Reserved	NC	—
C28	Reserved	NC	—
D1	GVDD2	Power	N/A
D2	VSS	Ground	N/A
D3	M2DQ29	I/O	GVDD2
D4	GVDD2	Power	N/A
D5	VSS	Ground	N/A
D6	M2ECC5	I/O	GVDD2
D7	GVDD2	Power	N/A
D8	VSS	Ground	N/A
D9	M2A8	O	GVDD2
D10	GVDD2	Power	N/A
D11	VSS	Ground	N/A
D12	M2A0	O	GVDD2
D13	GVDD2	Power	N/A
D14	VSS	Ground	N/A
D15	M2DQ39	I/O	GVDD2
D16	GVDD2	Power	N/A
D17	VSS	Ground	N/A
D18	M2DQ54	I/O	GVDD2
D19	GVDD2	Power	N/A
D20	VSS	Ground	N/A
D21	SXPVSS1	Ground	N/A
D22	SXPVDD1	Power	N/A
D23	SR1_TXD1	O	SXPVDD1
D24	$\overline{\text{SR1\_TXD1}}$	O	SXPVDD1
D25	SXCVSS1	Ground	N/A
D26	SXCVDD1	Power	N/A
D27	$\overline{\text{SR1\_RXD1}}$	I	SXCVDD1
D28	SR1_RXD1	I	SXCVDD1
E1	M2DQ31	I/O	GVDD2
E2	M2DQ30	I/O	GVDD2
E3	M2DQ27	I/O	GVDD2
E4	M2ECC7	I/O	GVDD2
E5	M2ECC6	I/O	GVDD2
E6	M2ECC3	I/O	GVDD2
E7	M2A9	O	GVDD2
E8	M2A6	O	GVDD2
E9	M2A3	O	GVDD2
E10	M2A10	O	GVDD2
E11	$\overline{\text{M2RAS}}$	O	GVDD2
E12	M2A2	O	GVDD2
E13	M2DQ38	I/O	GVDD2
E14	$\overline{\text{M2DQS5}}$	I/O	GVDD2
E15	M2DQS5	I/O	GVDD2
E16	M2DQ33	I/O	GVDD2

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[10]	Power Rail Name
E17	M2DQ56	I/O	GVDD2
E18	M2DQ57	I/O	GVDD2
E19	$\overline{\text{M2DQS7}}$	I/O	GVDD2
E20	Reserved	NC	—
E21	Reserved	NC	—
E22	Reserved	NC	—
E23	SXPVDD1	Power	N/A
E24	SXPVSS1	Ground	N/A
E25	SR1_PLL_AGND[9]	Ground	SXCVSS1
E26	SR1_PLL_AVDD[9]	Power	SXCVDD1
E27	SXCVSS1	Ground	N/A
E28	SXCVDD1	Power	N/A
F1	VSS	Ground	N/A
F2	GVDD2	Power	N/A
F3	M2DQ16	I/O	GVDD2
F4	VSS	Ground	N/A
F5	GVDD2	Power	N/A
F6	M2DQ17	I/O	GVDD2
F7	VSS	Ground	N/A
F8	GVDD2	Power	N/A
F9	M2BA2	O	GVDD2
F10	VSS	Ground	N/A
F11	GVDD2	Power	N/A
F12	M2A4	O	GVDD2
F13	VSS	Ground	N/A
F14	GVDD2	Power	N/A
F15	M2DQ42	I/O	GVDD2
F16	VSS	Ground	N/A
F17	GVDD2	Power	N/A
F18	M2DQ58	I/O	GVDD2
F19	M2DQS7	I/O	GVDD2
F20	GVDD2	Power	N/A
F21	SXPVDD1	Power	N/A
F22	SXPVSS1	Ground	N/A
F23	SR1_TXD2/SG1_TX[4]	O	SXPVDD1
F24	$\overline{\text{SR1\_TXD2}}$/$\overline{\text{SG1\_TX}}$[4]	O	SXPVDD1
F25	SXCVDD1	Power	N/A
F26	SXCVSS1	Ground	N/A
F27	$\overline{\text{SR1\_RXD2}}$/$\overline{\text{SG1\_RX}}$[4]	I	SXCVDD1
F28	SR1_RXD2/SG1_RX[4]	I	SXCVDD1
G1	$\overline{\text{M2DQS2}}$	I/O	GVDD2
G2	M2DQS2	I/O	GVDD2
G3	M2DQ19	I/O	GVDD2
G4	M2DM2	O	GVDD2
G5	M2DQ21	I/O	GVDD2
G6	M2DQ22	I/O	GVDD2

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[10]	Power Rail Name
H25	SXCVSS1	Ground	N/A
H26	SXCVDD1	Power	N/A
H27	$\overline{\text{SR1\_RXD3}}$/$\overline{\text{SG2\_RX}}$[4]	I	SXCVDD1
H28	SR1_RXD3/SG2_RX[4]	I	SXCVDD1
J1	M2DQS1	I/O	GVDD2
J2	$\overline{\text{M2DQS1}}$	I/O	GVDD2
J3	M2DQ10	I/O	GVDD2
J4	M2DQ11	I/O	GVDD2
J5	M2DQ14	I/O	GVDD2
J6	M2DQ23	I/O	GVDD2
J7	M2ODT0	O	GVDD2
J8	M2A12	O	GVDD2
J9	M2A14	O	GVDD2
J10	VSS	Ground	N/A
J11	GVDD2	Power	N/A
J12	VSS	Ground	N/A
J13	GVDD2	Power	N/A
J14	VSS	Ground	N/A
J15	GVDD2	Power	N/A
J16	VSS	Ground	N/A
J17	GVDD2	Power	N/A
J18	VSS	Ground	N/A
J19	GVDD2	Power	N/A
J20	Reserved	NC	—
J21	Reserved	NC	—
J22	Reserved	NC	—
J23	SXPVDD1	Power	N/A
J24	SXPVSS1	Ground	N/A
J25	SXCVDD1	Power	N/A
J26	SXCVSS1	Ground	N/A
J27	SXCVDD1	Power	N/A
J28	SXCVSS1	Ground	N/A
K1	VSS	Ground	N/A
K2	GVDD2	Power	N/A
K3	M2DM1	O	GVDD2
K4	VSS	Ground	N/A
K5	GVDD2	Power	N/A
K6	M2DQ0	I/O	GVDD2
K7	VSS	Ground	N/A
K8	GVDD2	Power	N/A
K9	M2DQ5	I/O	GVDD2
K10	VSS	Ground	N/A
K11	VDD	Power	N/A
K12	VSS	Ground	N/A
K13	VDD	Power	N/A
K14	VSS	Ground	N/A

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[10]	Power Rail Name
AB1	$\overline{\text{M1DQS2}}$	I/O	GVDD1
AB2	M1DQS2	I/O	GVDD1
AB3	M1DQ19	I/O	GVDD1
AB4	M1DM2	O	GVDD1
AB5	M1DQ21	I/O	GVDD1
AB6	M1DQ22	I/O	GVDD1
AB7	M1CKE0	O	GVDD1
AB8	M1A11	O	GVDD1
AB9	M1A7	O	GVDD1
AB10	$\overline{\text{M1CK2}}$	O	GVDD1
AB11	M1APAR_OUT	O	GVDD1
AB12	M1ODT1	O	GVDD1
AB13	$\overline{\text{M1APAR\_IN}}$	I	GVDD1
AB14	M1DQ43	I/O	GVDD1
AB15	M1DM5	O	GVDD1
AB16	M1DQ44	I/O	GVDD1
AB17	M1DQ40	I/O	GVDD1
AB18	M1DQ59	I/O	GVDD1
AB19	M1DM7	O	GVDD1
AB20	M1DQ60	I/O	GVDD1
AB21	VSS	Ground	N/A
AB22	GPIO31/I2C_SDA[5,8]	I/O	NVDD
AB23	GPIO27/TMR4/RCW_SRC0[5,8]	I/O	NVDD
AB24	GPIO25/TMR2/RCW_SRC1[5,8]	I/O	NVDD
AB25	GPIO24/TMR1/RCW_SRC2[5,8]	I/O	NVDD
AB26	GPIO10/$\overline{\text{IRQ10}}$/RC10[5,8]	I/O	NVDD
AB27	GPIO5/$\overline{\text{IRQ5}}$/RC5[5,8]	I/O	NVDD
AB28	GPIO0/$\overline{\text{IRQ0}}$/RC0[5,8]	I/O	NVDD
AC1	VSS	Ground	N/A
AC2	GVDD1	Power	N/A
AC3	M1DQ16	I/O	GVDD1
AC4	VSS	Ground	N/A
AC5	GVDD1	Power	N/A
AC6	M1DQ17	I/O	GVDD1
AC7	VSS	Ground	N/A
AC8	GVDD1	Power	N/A
AC9	M1BA2	O	GVDD1
AC10	VSS	Ground	N/A
AC11	GVDD1	Power	N/A
AC12	M1A4	O	GVDD1
AC13	VSS	Ground	N/A
AC14	GVDD1	Power	N/A
AC15	M1DQ42	I/O	GVDD1
AC16	VSS	Ground	N/A
AC17	GVDD1	Power	N/A
AC18	M1DQ58	I/O	GVDD1

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[10]	Power Rail Name
AC19	VSS	Ground	N/A
AC20	GVDD1	Power	N/A
AC21	VSS	Ground	N/A
AC22	NVDD	Power	N/A
AC23	GPIO30/I2C_SCL[5,8]	I/O	NVDD
AC24	GPIO26/TMR3[5,8]	I/O	NVDD
AC25	VSS	Ground	N/A
AC26	NVDD	Power	N/A
AC27	GPIO23/TMR0[5,8]	I/O	NVDD
AC28	GPIO22[5,8]	I/O	NVDD
AD1	M1DQ31	I/O	GVDD1
AD2	M1DQ30	I/O	GVDD1
AD3	M1DQ27	I/O	GVDD1
AD4	M1ECC7	I/O	GVDD1
AD5	M1ECC6	I/O	GVDD1
AD6	M1ECC3	I/O	GVDD1
AD7	M1A9	O	GVDD1
AD8	M1A6	O	GVDD1
AD9	M1A3	O	GVDD1
AD10	M1A10	O	GVDD1
AD11	$\overline{\text{M1RAS}}$	O	GVDD1
AD12	M1A2	O	GVDD1
AD13	M1DQ38	I/O	GVDD1
AD14	$\overline{\text{M1DQS}}$5	I/O	GVDD1
AD15	M1DQS5	I/O	GVDD1
AD16	M1DQ33	I/O	GVDD1
AD17	M1DQ56	I/O	GVDD1
AD18	M1DQ57	I/O	GVDD1
AD19	$\overline{\text{M1DQS7}}$	I/O	GVDD1
AD20	M1DQS7	I/O	GVDD1
AD21	VSS	Ground	N/A
AD22	GE2_TX_CTL	O	NVDD
AD23	GPIO15/DDN0/$\overline{\text{IRQ15}}$/RC15[5,8]	I/O	NVDD
AD24	GPIO13/$\overline{\text{IRQ13}}$/RC13[5,8]	I/O	NVDD
AD25	GE_MDC	O	NVDD
AD26	GE_MDIO	I/O	NVDD
AD27	TDM2TCK/GE1_TD3[3]	I/O	NVDD
AD28	TDM2RCK/GE1_TD0[3]	I/O	NVDD
AE1	GVDD1	Power	N/A
AE2	VSS	Ground	N/A
AE3	M1DQ29	I/O	GVDD1
AE4	GVDD1	Power	N/A
AE5	VSS	Ground	N/A
AE6	M1ECC5	I/O	GVDD1
AE7	GVDD1	Power	N/A
AE8	VSS	Ground	N/A

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[10]	Power Rail Name
AE9	M1A8	O	GVDD1
AE10	GVDD1	Power	N/A
AE11	VSS	Ground	N/A
AE12	M1A0	O	GVDD1
AE13	GVDD1	Power	N/A
AE14	VSS	Ground	N/A
AE15	M1DQ39	I/O	GVDD1
AE16	GVDD1	Power	N/A
AE17	VSS	Ground	N/A
AE18	M1DQ54	I/O	GVDD1
AE19	GVDD1	Power	N/A
AE20	VSS	Ground	N/A
AE21	GPIO29/UART_TXD[5,8]	I/O	NVDD
AE22	TDM1TCK/GE2_RX_CLK[3]	I	NVDD
AE23	TDM1RSN/GE2_RX_CTL[3]	I/O	NVDD
AE24	VSS	Ground	N/A
AE25	TDM3RCK/GE1_GTX_CLK[3]	I/O	NVDD
AE26	TDM3TSN/GE1_RX_CLK[3]	I/O	NVDD
AE27	TDM2RSN/GE1_TD2[3]	I/O	NVDD
AE28	TDM2RDT/GE1_TD1[3]	I/O	NVDD
AF1	M1DQ28	I/O	GVDD1
AF2	M1DM3	O	GVDD1
AF3	M1DQ26	I/O	GVDD1
AF4	M1ECC4	I/O	GVDD1
AF5	M1DM8	O	GVDD1
AF6	M1ECC2	I/O	GVDD1
AF7	M1CKE1	O	GVDD1
AF8	M1CK0	O	GVDD1
AF9	$\overline{\text{M1CK0}}$	O	GVDD1
AF10	M1BA1	O	GVDD1
AF11	M1A1	O	GVDD1
AF12	$\overline{\text{M1WE}}$	O	GVDD1
AF13	M1DQ37	I/O	GVDD1
AF14	M1DM4	O	GVDD1
AF15	M1DQ36	I/O	GVDD1
AF16	M1DQ32	I/O	GVDD1
AF17	M1DQ55	I/O	GVDD1
AF18	M1DM6	O	GVDD1
AF19	M1DQ53	I/O	GVDD1
AF20	M1DQ52	I/O	GVDD1
AF21	GPIO28/UART_RXD[5,8]	I/O	NVDD
AF22	TDM0RSN/GE2_TD2[3]	I/O	NVDD
AF23	TDM0TDT/GE2_TD3[3]	I/O	NVDD
AF24	NVDD	Power	N/A
AF25	TDM2TSN/GE1_TX_CTL[3]	I/O	NVDD
AF26	GE1_RX_CTL	I	NVDD

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[10]	Power Rail Name
AF27	TDM2TDT/GE1_TX_CLK[3]	I/O	NVDD
AF28	TDM3RSN/GE1_RD1[3]	I/O	NVDD
AG1	M1DQ24	I/O	GVDD1
AG2	GVDD1	Power	N/A
AG3	M1DQ25	I/O	GVDD1
AG4	VSS	Ground	N/A
AG5	GVDD1	Power	N/A
AG6	M1ECC1	I/O	GVDD1
AG7	VSS	Ground	N/A
AG8	GVDD1	Power	N/A
AG9	M1A13	O	GVDD1
AG10	VSS	Ground	N/A
AG11	GVDD1	Power	N/A
AG12	$\overline{\text{M1CS1}}$	O	GVDD1
AG13	VSS	Ground	N/A
AG14	GVDD1	Power	N/A
AG15	M1DQ35	I/O	GVDD1
AG16	VSS	Ground	N/A
AG17	GVDD1	Power	N/A
AG18	M1DQ51	I/O	GVDD1
AG19	VSS	Ground	N/A
AG20	GVDD1	Power	N/A
AG21	NVDD	Power	N/A
AG22	TDM1TSN/GE2_TD1[3]	I/O	NVDD
AG23	TDM1RDT/GE2_TX_CLK[3]	I/O	NVDD
AG24	TDM0TCK/GE2_GTX_CLK[3]	I/O	NVDD
AG25	TDM1TDT/GE2_TD0[3]	I/O	NVDD
AG26	VSS	Ground	N/A
AG27	NVDD	Power	N/A
AG28	TDM3RDT/GE1_RD0[3]	I/O	NVDD
AH1	Reserved.	NC	—
AH2	$\overline{\text{M1DQS3}}$	I/O	GVDD1
AH3	M1DQS3	I/O	GVDD1
AH4	M1ECC0	I/O	GVDD1
AH5	$\overline{\text{M1DQS8}}$	I/O	GVDD1
AH6	M1DQS8	I/O	GVDD1
AH7	M1A5	O	GVDD1
AH8	$\overline{\text{M1CK1}}$	O	GVDD1
AH9	M1CK1	O	GVDD1
AH10	$\overline{\text{M1CS0}}$	O	GVDD1
AH11	M1BA0	O	GVDD1
AH12	$\overline{\text{M1CAS}}$	O	GVDD1
AH13	M1DQ34	I/O	GVDD1
AH14	$\overline{\text{M1DQS4}}$	I/O	GVDD1
AH15	M1DQS4	I/O	GVDD1
AH16	M1DQ50	I/O	GVDD1

2 Electrical Characteristics

This document contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications. For additional information, see the *MSC8156E Reference Manual*.

2.1 Maximum Ratings

In calculating timing requirements, adding a maximum value of one specification to a minimum value of another specification does not yield a reasonable sum. A maximum specification is calculated using a worst case variation of process parameter values in one direction. The minimum specification is calculated using the worst case for the same parameters in the opposite direction. Therefore, a "maximum" value for a specification never occurs in the same device with a "minimum" value for another specification; adding a maximum to a minimum represents a condition that can never exist.

Table 2 describes the maximum electrical ratings for the MSC8156E.

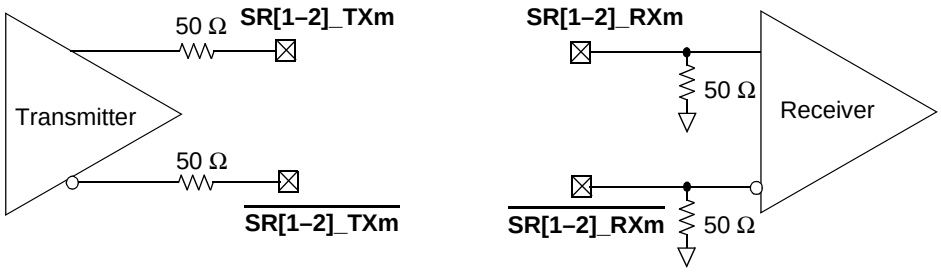
Table 2. Absolute Maximum Ratings

Rating	Power Rail Name	Symbol	Value	Unit
Core supply voltage • Cores 0–5	VDD	V_{DD}	–0.3 to 1.1	V
PLL supply voltage[3]		V_{DDPLL0} V_{DDPLL1} V_{DDPLL2}	–0.3 to 1.1 –0.3 to 1.1 –0.3 to 1.1	V V V
M3 memory supply voltage	M3VDD	V_{DDM3}	–0.3 to 1.1	V
MAPLE-B supply voltage	MVDD	V_{DDM}	–0.3 to 1.1	V
DDR memory supply voltage • DDR2 mode • DDR3 mode	GVDD1, GVDD2	V_{DDDDR}	 –0.3 to 1.98 –0.3 to 1.65	 V V
DDR reference voltage	MVREF	MV_{REF}	–0.3 to 0.51 × V_{DDDDR}	V
Input DDR voltage		V_{INDDR}	–0.3 to V_{DDDDR} + 0.3	V
I/O voltage excluding DDR and RapidIO lines	NVDD, QVDD	V_{DDIO}	–0.3 to 2.625	V
Input I/O voltage		V_{INIO}	–0.3 to V_{DDIO} + 0.3	V
RapidIO pad voltage	SXPVDD1, SXPVDD2	V_{DDSXP}	–0.3 to 1.26	V
Rapid I/O core voltage	SXCVDD1, SXCVDD2	V_{DDSXC}	–0.3 to 1.21	V
Rapid I/O PLL voltage[3]		$V_{DDRIOPLL}$	–0.3 to 1.21	V
Input RapidIO I/O voltage		V_{INRIO}	–0.3 to V_{DDSXC} + 0.3	V
Operating temperature		T_J	–40 to 105	°C
Storage temperature range		T_{STG}	–55 to +150	°C

Notes:
1. Functional operating conditions are given in Table 3.
2. Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond the listed limits may affect device reliability or cause permanent damage.
3. PLL supply voltage is specified at input of the filter and not at pin of the MSC8156E (see Figure 37 and Figure 38)

2.5.2.3 SerDes Transmitter and Receiver Reference Circuits

Figure 6 shows the reference circuits for SerDes data lane transmitter and receiver.



Note: The [1–2] indicates the specific SerDes Interface (1 or 2) and the m indicates the specific channel within that interface (0,1,2,3). Actual signals are assigned by the HRCW assignments at reset (see **Chapter 5**, *Reset* in the reference manual for details)

Figure 6. SerDes Transmitter and Receiver Reference Circuits

2.5.3 DC-Level Requirements for SerDes Interfaces

The following subsections define the DC-level requirements for the SerDes reference clocks, the PCI Express data lines, the Serial RapidIO data lines, and the SGMII data lines.

2.5.3.1 DC-Level Requirements for SerDes Reference Clocks

The DC-level requirement for the SerDes reference clock inputs is different depending on the signaling mode used to connect the clock driver chip and SerDes reference clock inputs, as described below:

- Differential Mode
  - The input amplitude of the differential clock must be between 400 mV and 1600 mV differential peak-peak (or between 200 mV and 800 mV differential peak). In other words, each signal wire of the differential pair must have a single-ended swing of less than 800 mV and greater than 200 mV. This requirement is the same for both external DC-coupled or AC-coupled connection.
  - For an external DC-coupled connection, the maximum average current requirements sets the requirement for average voltage (common mode voltage) as between 100 mV and 400 mV. Figure 7 shows the SerDes reference clock input requirement for DC-coupled connection scheme.

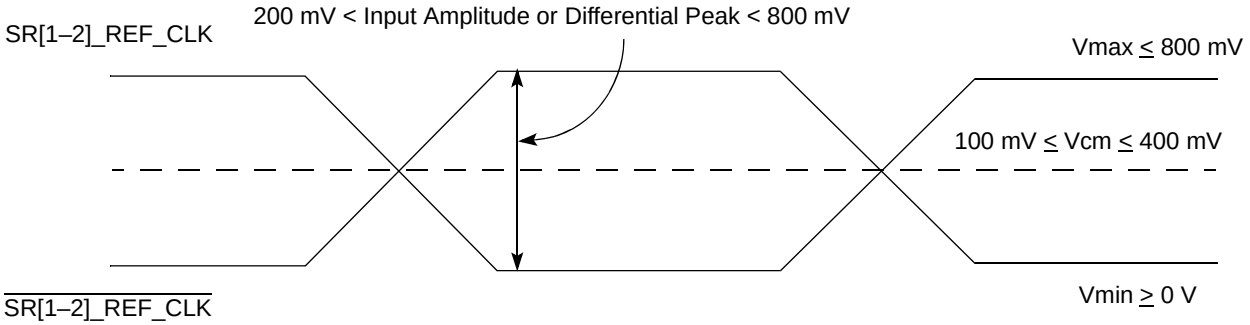


Figure 7. Differential Reference Clock Input DC Requirements (External DC-Coupled)

— For an external AC-coupled connection, there is no common mode voltage requirement for the clock driver. Because the external AC-coupling capacitor blocks the DC-level, the clock driver and the SerDes reference clock receiver operate in different command mode voltages. The SerDes reference clock receiver in this connection scheme has its common mode voltage set to GND_{SXC}. Each signal wire of the differential inputs is allowed to swing below and above the command mode voltage GND_{SXC}. Figure 8 shows the SerDes reference clock input requirement for AC-coupled connection scheme.

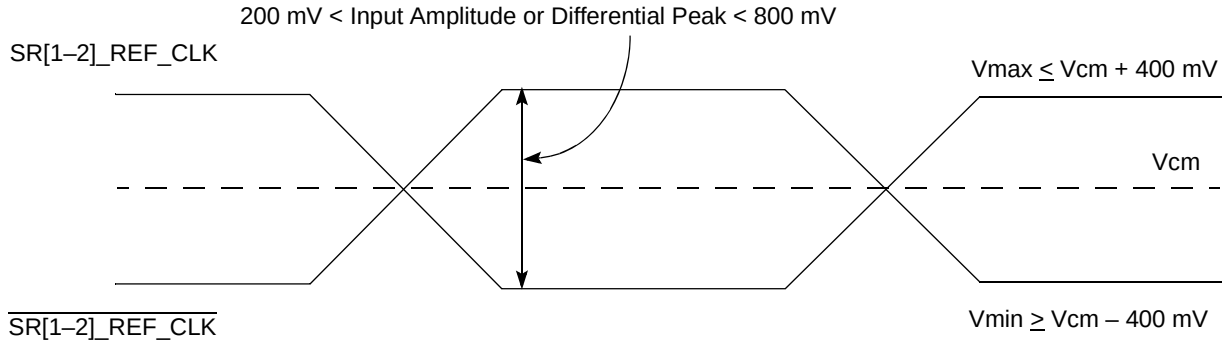


Figure 8. Differential Reference Clock Input DC Requirements (External AC-Coupled)

- Single-Ended Mode
  — The reference clock can also be single-ended. The SR[1–2]_REF_CLK input amplitude (single-ended swing) must be between 400 mV and 800 mV peak-peak (from V_{MIN} to V_{MAX}) with $\overline{\text{SR[1–2]\_REF\_CLK}}$ either left unconnected or tied to ground.
  — The SR[1–2]_REF_CLK input average voltage must be between 200 and 400 mV. Figure 9 shows the SerDes reference clock input requirement for single-ended signalling mode.
  — To meet the input amplitude requirement, the reference clock inputs may need to be DC- or AC-coupled externally. For the best noise performance, the reference of the clock could be DC- or AC-coupled into the unused phase ($\overline{\text{SR[1–2]\_REF\_CLK}}$) through the same source impedance as the clock input (SR[1–2]_REF_CLK) in use.

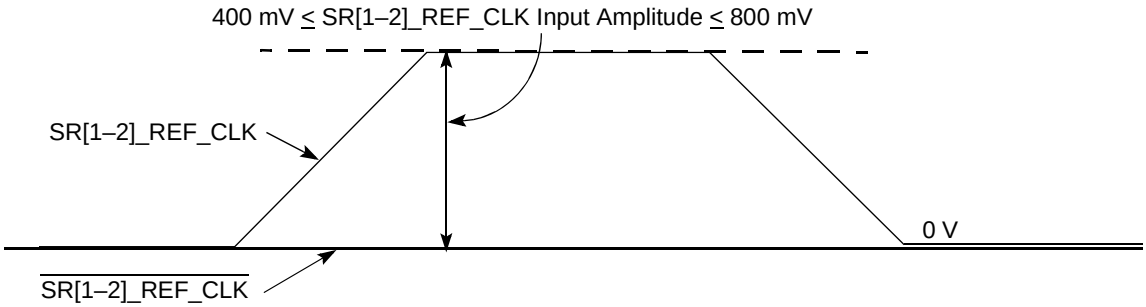


Figure 9. Single-Ended Reference Clock Input DC Requirements

2.5.3.2 DC-Level Requirements for PCI Express Configurations

The DC-level requirements for PCI Express implementations have separate requirements for the Tx and Rx lines. The MSC8156E supports a 2.5 Gbps PCI Express interface defined by the *PCI Express Base Specification, Revision 1.0a*. The transmitter specifications are defined in Table 11 and the receiver specifications are defined in Table 12.

Table 14. Serial RapidIO Receiver DC Specifications

Parameter	Symbol	Min	Typical	Max	Units	Notes
Differential input voltage	V_{IN}	200	—	1600	mVp-p	1

Notes: **1.** Measured at receiver.

2.5.3.4 DC-Level Requirements for SGMII Configurations

Note: Specifications are valid at the recommended operating conditions listed in Table 3

Table 15 describes the SGMII SerDes transmitter AC-coupled DC electrical characteristics. Transmitter DC characteristics are measured at the transmitter outputs (SR[1–2]_TX[n] and $\overline{\text{SR[1–2]\_TX[n]}}$) as shown in Figure 10.

Table 15. SGMII DC Transmitter Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output high voltage	V_{OH}	—	—	$XV_{DD\_SRDS\text{-}Typ}/2 + \lvert V_{OD}\rvert_{\text{-}max}/2$	mV	1
Output low voltage	V_{OL}	$XV_{DD\_SRDS\text{-}Typ}/2 - \lvert V_{OD}\rvert_{\text{-}max}/2$	—	—	mV	1
Output differential voltage ($XV_{DD\text{-}Typ}$ at 1.0 V)	$\lvert V_{OD}\rvert$	323	500	725	mV	2,3,4
		296	459	665		2,3,5
		269	417	604		2,3,6
		243	376	545		2,3,7
		215	333	483		2,3,8
		189	292	424		2,3,9
		162	250	362		2,3,10
Output impedance (single-ended)	R_O	40	50	60	Ω	—

Notes:
1. This does not align to DC-coupled SGMII. $XV_{DD\_SRDS2\text{-}Typ} = 1.1$ V.
2. The $\lvert V_{OD}\rvert$ value shown in the table assumes full multitude by setting srd_smit_lvl as 000 and the following transmit equalization setting in the XMITEQ**AB** (for lanes A and B) or XMITEQ**EF** (for lanes E and F) bit field of Control Register:
• The MSB (bit 0) of the above bit field is set to zero (selecting the full $V_{DD\text{-}DIFF\text{-}p\text{-}p}$ amplitude which is power up default);
• The LSB (bit [1–3]) of the above bit field is set based on the equalization settings listed in notes 4 through 10.
3. The $\lvert V_{OD}\rvert$ value shown in the Typ column is based on the condition of $XV_{DD\_SRDS2\text{-}Typ} = 1.0$ V, no common mode offset variation (V_{OS} =500mV), SerDes transmitter is terminated with 100-Ω differential load between
4. Equalization setting: 1.0x: 0000.
5. Equalization setting: 1.09x: 1000.
6. Equalization setting: 1.2x: 0100.
7. Equalization setting: 1.33x: 1100.
8. Equalization setting: 1.5x: 0010.
9. Equalization setting: 1.71x: 1010.
10. Equalization setting: 2.0x: 0110.
11. $\lvert V_{OD}\rvert = \lvert V_{SR[1–2]\_TXn} - V_{\overline{SR[1–2]\_TXn}}\rvert$. $\lvert V_{OD}\rvert$ is also referred to as output differential peak voltage. $V_{TX\text{-}DIFFp\text{-}p} = 2*\lvert V_{OD}\rvert$.

Table 24. SR[1–2]_REF_CLK and $\overline{\text{SR[1–2]\_REF\_CLK}}$ Input Clock Requirements (continued)

Parameter	Symbol	Min	Typical	Max	Units	Notes

Notes:
1. Caution: Only 100 and 125 have been tested. Other values will not work correctly with the rest of the system.
2. Limits from PCI Express CEM Rev 1.0a
3. Measured from –200 mV to +200 mV on the differential waveform (derived from SR[1–2]_REF_CLK minus $\overline{\text{SR[1–2]\_REF\_CLK}}$). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing. See Figure 16.
4. Measurement taken from differential waveform
5. Measurement taken from single-ended waveform
6. Matching applies to rising edge for SR[1–2]_REF_CLK and falling edge rate for $\overline{\text{SR[1–2]\_REF\_CLK}}$. It is measured using a 200 mV window centered on the median cross point where SR[1–2]_REF_CLK rising meets $\overline{\text{SR[1–2]\_REF\_CLK}}$ falling. The median cross point is used to calculate the voltage thresholds that the oscilloscope uses for the edge rate calculations. The rise edge rate of SR[1–2]_REF_CLK should be compared to the fall edge rate of $\overline{\text{SR[1–2]\_REF\_CLK}}$; the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 17.

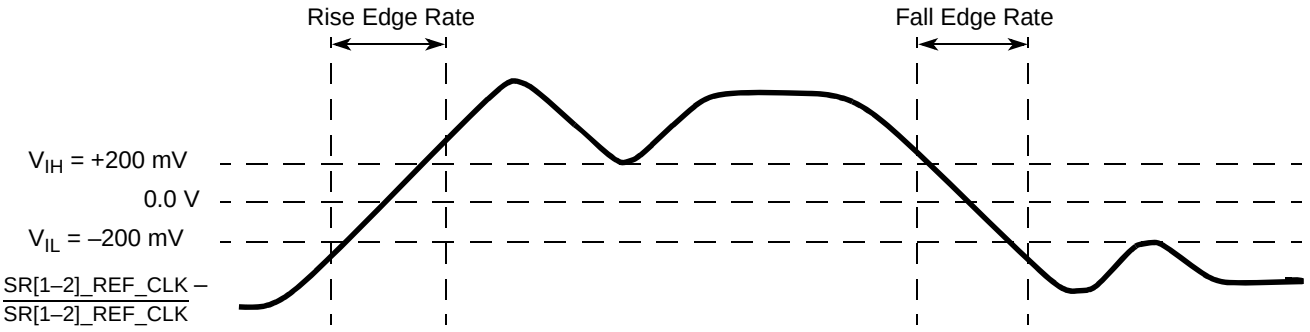


Figure 16. Differential Measurement Points for Rise and Fall Time

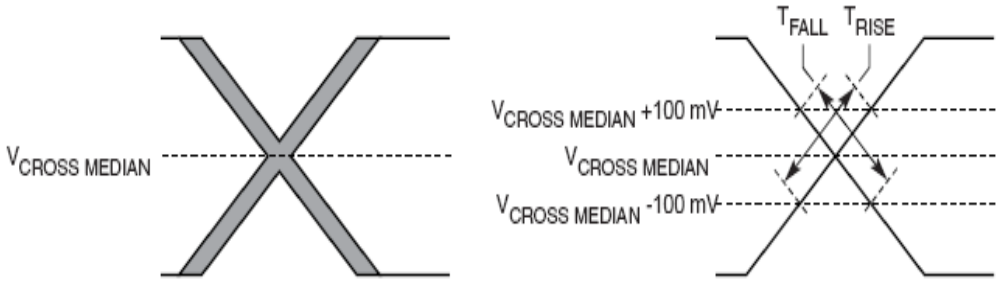


Figure 17. Single-Ended Measurement Points for Rise and Fall Time Matching

2.6.2.4 SGMII AC Timing Specifications

Note: Specifications are valid at the recommended operating conditions listed in Table 3.

Transmitter and receiver AC characteristics are measured at the transmitter outputs (SR[1–2]_TX[n] and $\overline{\text{SR[1–2]\_TX}}$[n]) or at the receiver inputs (SR[1–2]_RX[n] and $\overline{\text{SR[1–2]\_RX}}$[n]) as depicted in Figure 19, respectively.

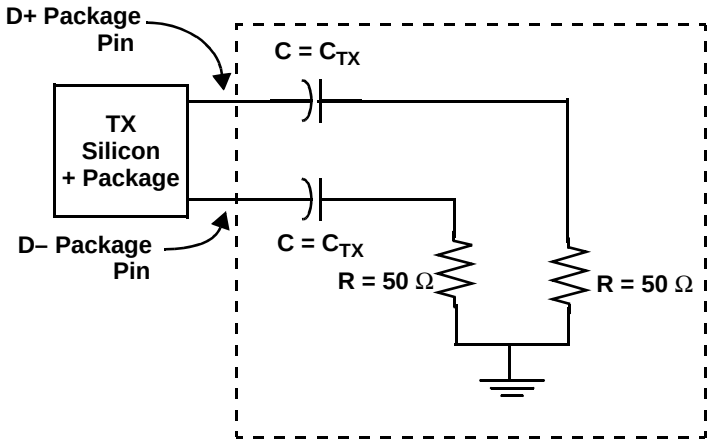


Figure 19. SGMII AC Test/Measurement Load

Table 29 provides the SGMII transmit AC timing specifications. A source synchronous clock is not supported. The AC timing specifications do not include REF_CLK jitter.

Table 29. SGMII Transmit AC Timing Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Deterministic Jitter	JD	—	—	0.17	UI p-p	—
Total Jitter	JT	—	—	0.35	UI p-p	2
Unit Interval	UI	799.92	800	800.08	ps	1

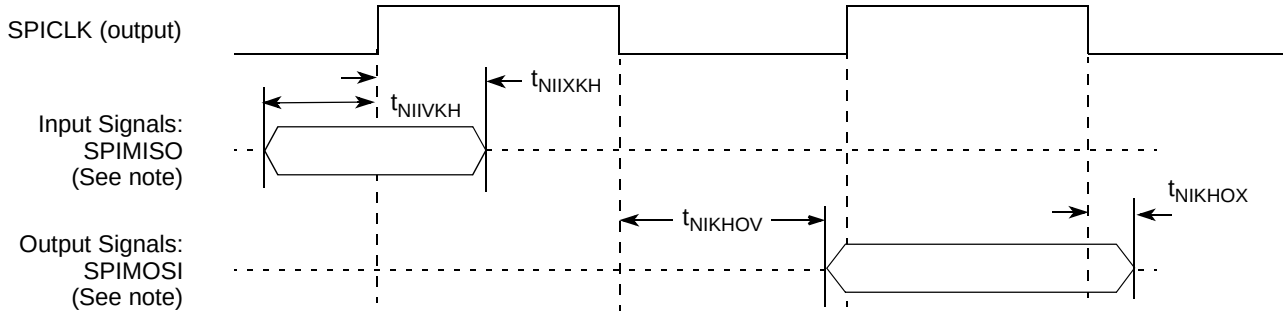
Notes: 1. See Figure 18 for single frequency sinusoidal jitter limits
2. Each UI is 800 ps ± 100 ppm.

Table 30 provides the SGMII receiver AC timing specifications. The AC timing specifications do not include REF_CLK jitter.

Table 30. SGMII Receive AC Timing Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Deterministic Jitter Tolerance	JD	0.37	—	—	UI p-p	1, 2
Combined Deterministic and Random Jitter Tolerance	JDR	0.55	—	—	UI p-p	1, 2
Total Jitter Tolerance	JT	0.65	—	—	UI p-p	1,2
Bit Error Ratio	BER	—	—	10^{-12}	—	—
Unit Interval	UI	799.92	800.00	800.08	ps	3

Notes: 1. Measured at receiver.
2. Refer to RapidIO™ 1x/4x LP Serial Physical Layer Specification for interpretation of jitter specifications. Also see Figure 18.
3. Each UI is 800 ps ± 100 ppm.



Note: measured with SPMODE[CI] = 0, SPMODE[CP] = 0

Figure 28. SPI AC Timing in Master Mode (Internal Clock)

The device power rails should rise in the following sequence:

1. VDD (and all coupled supplies)
2. After the above rails rise to 90% of their nominal voltage, the following I/O power rails may rise in any sequence (see Figure 34): QVDD, NVDD, GVDD1, and GVDD2.

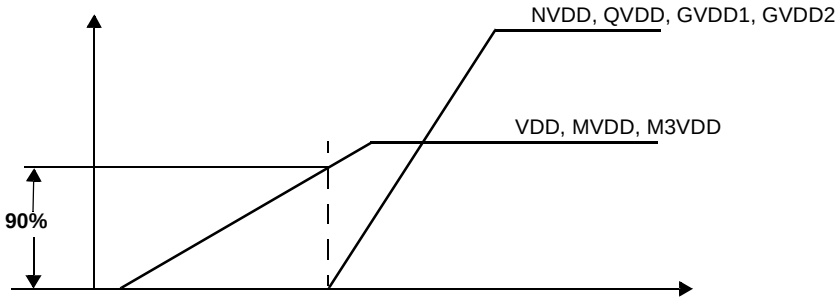


Figure 34. Supply Ramp-Up Sequence

Notes:
1. If the M3 memory is not used, M3VDD can be tied to GND.
2. If the MAPLE-B is not used, MVDD can be tied to GND.
3. If the HSSI port1 is not used, SXCVDD1and SXPVDD1 must be connected to the designated power supplies.
4. If the HSSI port2 is not used, SXCVDD2 and SXPVDD2 must be connected to the designated power supplies.
5. If the DDR port 1 interface is not used, it is recommended that GVDD1 be left unconnected.
6. If the DDR port 2 interface is not used, it is recommended that GVDD2 be left unconnected.

3.1.4 Reset Guidelines

When a debugger is not used, implement the connection scheme shown in Figure 35.

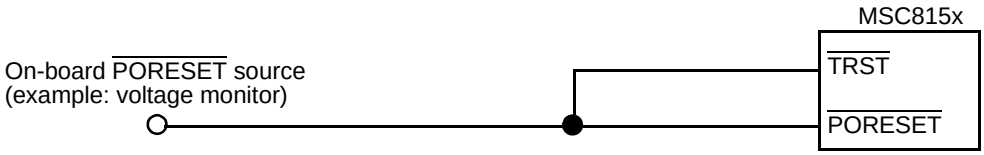


Figure 35. Reset Connection in Functional Application

When a debugger is used, implement the connection scheme shown in Figure 36.

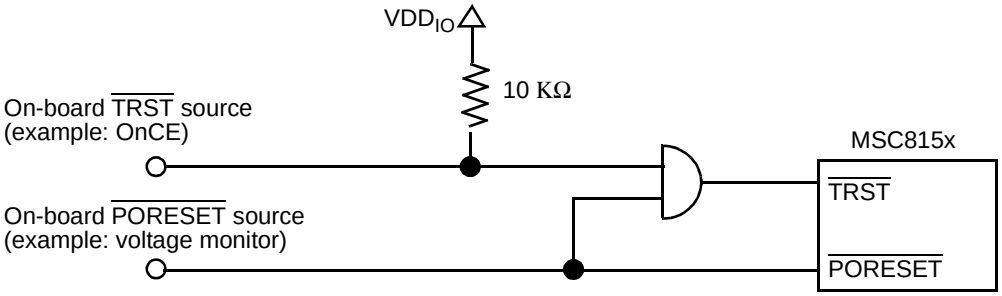


Figure 36. Reset Connection in Debugger Application

3.3 Clock and Timing Signal Board Layout Considerations

When laying out the system board, use the following guidelines:

- Keep clock and timing signal paths as short as possible and route with 50 Ω impedance.
- Use a serial termination resistor placed close to the clock buffer to minimize signal reflection. Use the following equation to compute the resistor value:

  Rterm = Rim – Rbuf

  where Rim = trace characteristic impedance

  Rbuf = clock buffer internal impedance.

3.4 SGMII AC-Coupled Serial Link Connection Example

Figure 39 shows an example of a 4-wire AC-coupled serial link connection. For additional layout suggestions, see *AN3556 MSC815x High Speed Serial Interface Hardware Design Considerations*, available on the Freescale website or from your local sales office or representative.

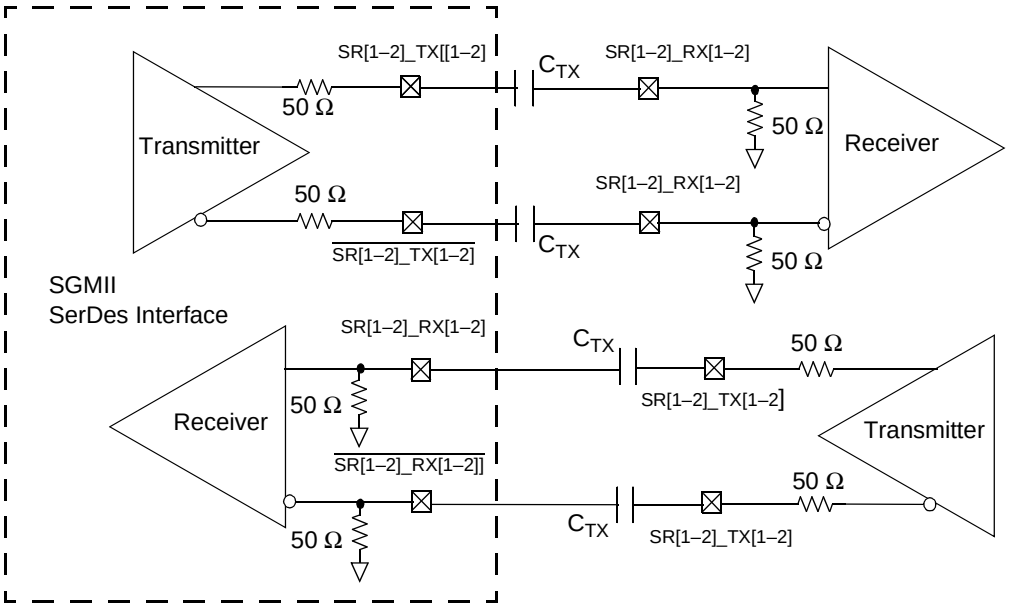
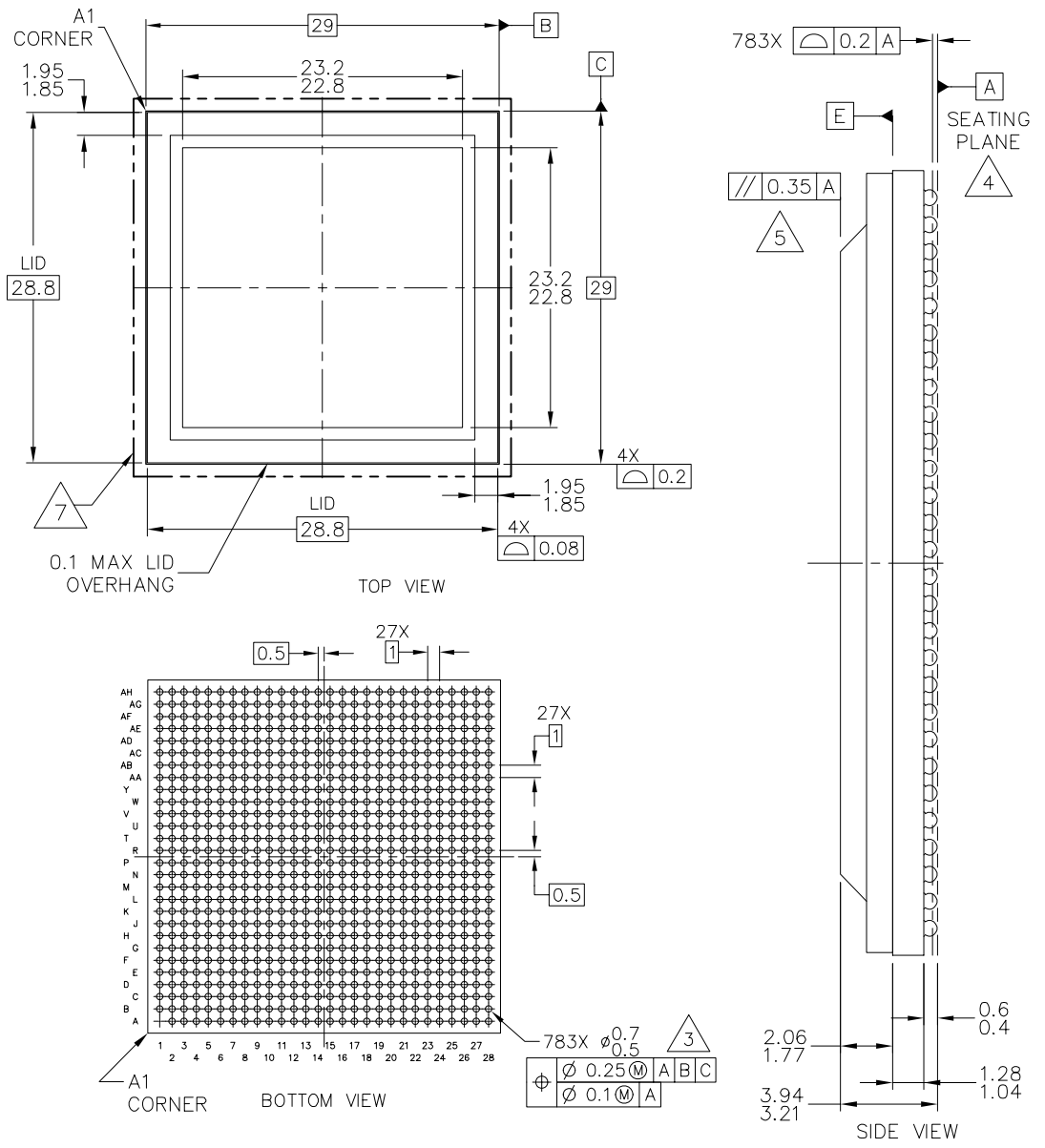


Figure 39. 4-Wire AC-Coupled SGMII Serial Link Connection Example

5 Package Information



NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURE PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.
6. ALL DIMENSIONS ARE SYMMETRIC ACROSS THE PACKAGE CENTER LINES, UNLESS DIMENSIONED OTHERWISE.
7. 29.2MM MAXIMUM PACKAGE ASSEMBLY (LID + LAMINATE) X AND Y.

Figure 40. MSC8156E Mechanical Information, 783-ball FC-PBGA Package