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Understanding <u>Embedded - DSP (Digital</u> <u>Signal Processors)</u>

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of <u>Embedded - DSP (Digital</u> <u>Signal Processors)</u>

Details

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Product Status	Obsolete
Туре	SC3850 Six Core
Interface	Ethernet, I ² C, PCI, RGMII, Serial RapidIO, SGMII, SPI, UART/USART
Clock Rate	1GHz
Non-Volatile Memory	ROM (96kB)
On-Chip RAM	576kB
Voltage - I/O	2.50V
Voltage - Core	1.00V
Operating Temperature	-40°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=msc8156etvt1000b

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

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Figure 1. MSC8156E Block Diagram



Figure 2. StarCore SC3850 DSP Subsystem Block Diagram

Pin Assignment

1 Pin Assignment

This section includes diagrams of the MSC8156E package ball grid array layouts and tables showing how the pinouts are allocated for the package.

1.1 FC-PBGA Ball Layout Diagram

The top view of the FC-PBGA package is shown in Figure 3 with the ball location index numbers.

Top View



Figure 3. MSC8156E FC-PBGA Package, Top View

Ball Number	Signal Name ^{1,2}	Pin Type ¹⁰	Power Rail Name	
G7	M2CKE0	0	GVDD2	
G8	M2A11	0	GVDD2	
G9	M2A7	0	GVDD2	
G10	M2CK2	0	GVDD2	
G11	M2APAR_OUT	0	GVDD2	
G12	M2ODT1	0	GVDD2	
G13	M2APAR_IN	I	GVDD2	
G14	M2DQ43	I/O	GVDD2	
G15	M2DM5	0	GVDD2	
G16	M2DQ44	I/O	GVDD2	
G17	M2DQ40	I/O	GVDD2	
G18	M2DQ59	I/O	GVDD2	
G19	M2DM7	0	GVDD2	
G20	M2DQ60	I/O	GVDD2	
G21	Reserved	NC	_	
G22	Reserved	NC	_	
G23	SXPVSS1	Ground	N/A	
G24	SXPVDD1	Power	N/A	
G25	SR1_IMP_CAL_TX	I	SXCVDD1	
G26	SXCVSS1	Ground	N/A	
G27	Reserved	NC	_	
G28	Reserved	NC	_	
H1	GVDD2	Power	N/A	
H2	VSS	Ground	N/A	
H3	M2DQ18	I/O	GVDD2	
H4	GVDD2	Power	N/A	
H5	VSS	Ground	N/A	
H6	M2DQ20	I/O	GVDD2	
H7	GVDD2	Power	N/A	
H8	VSS	Ground	N/A	
H9	M2A15	0	GVDD2	
H10	M2CK2	0	GVDD2	
H11	M2MDIC0	I/O	GVDD2	
H12	M2VREF	I	GVDD2	
H13	M2MDIC1	I/O	GVDD2	
H14	M2DQ46	I/O	GVDD2	
H15	M2DQ47	I/O	GVDD2	
H16	M2DQ45	I/O	GVDD2	
H17	M2DQ41	I/O	GVDD2	
H18	M2DQ62	I/O	GVDD2	
H19	M2DQ63	I/O	GVDD2	
H20	M2DQ61	I/O	GVDD2	
H21	Reserved	NC		
H22	Reserved	NC		
H23	SR1_TXD3/SG2_TX ⁴	0	SXPVDD1	
H24	SR1_TXD3/SG2_TX ⁴	0	SXPVDD1	

Ball Number	Signal Name ^{1,2}	Pin Type ¹⁰	Power Rail Name	
H25	SXCVSS1	Ground	N/A	
H26	SXCVDD1	Power	N/A	
H27	SR1_RXD3/SG2_RX ⁴	I	SXCVDD1	
H28	SR1_RXD3/SG2_RX ⁴	I	SXCVDD1	
J1	M2DQS1	I/O	GVDD2	
J2	M2DQS1	I/O	GVDD2	
J3	M2DQ10	I/O	GVDD2	
J4	M2DQ11	I/O	GVDD2	
J5	M2DQ14	I/O	GVDD2	
J6	M2DQ23	I/O	GVDD2	
J7	M2ODT0	0	GVDD2	
J8	M2A12	0	GVDD2	
J9	M2A14	0	GVDD2	
J10	VSS	Ground	N/A	
J11	GVDD2	Power	N/A	
J12	VSS	Ground	N/A	
J13	GVDD2	Power	N/A	
J14	VSS	Ground	N/A	
J15	GVDD2	Power	N/A	
J16	VSS	Ground	N/A	
J17	GVDD2	Power	N/A	
J18	VSS	Ground	N/A	
J19	GVDD2	Power	N/A	
J20	Reserved	NC	_	
J21	Reserved	NC	—	
J22	Reserved	NC	—	
J23	SXPVDD1	Power	N/A	
J24	SXPVSS1	Ground	N/A	
J25	SXCVDD1	Power	N/A	
J26	SXCVSS1	Ground	N/A	
J27	SXCVDD1	Power	N/A	
J28	SXCVSS1	Ground	N/A	
K1	VSS	Ground	N/A	
K2	GVDD2	Power	N/A	
K3	M2DM1	0	GVDD2	
K4	VSS	Ground	N/A	
K5	GVDD2	Power	N/A	
K6	M2DQ0	I/O	GVDD2	
K7	VSS	Ground	N/A	
K8	GVDD2	Power	N/A	
K9	M2DQ5	I/O	GVDD2	
K10	VSS	Ground	N/A	
K11	VDD	Power	N/A	
K12	VSS	Ground	N/A	
K13	VDD	Power	N/A	
K14	VSS	Ground	N/A	

Ball Number	umber Signal Name ^{1,2} Pin Type ¹⁰		
M5	M2DQ1	I/O	GVDD2
M6	VSS	Ground	N/.A
M7	GVDD2	Power	N/A
M8	M2DQ7	I/O	GVDD2
M9	M2DQ6	I/O	GVDD2
M10	VSS	Ground	N/A
M11	VDD	Power	N/A
M12	VSS	Ground	N/A
M13	VDD	Power	N/A
M14	VSS	Ground	N/A
M15	VDD	Power	N/A
M16	VSS	Ground	N/A
M17	VDD	Power	N/A
M18	VSS	Ground	N/A
M19	VDD	Power	N/A
M20	Reserved	NC	_
M21	Reserved	NC	_
M22	Reserved	NC	
M23	SXPVSS2	Ground	N/A
M24	SXPVDD2	Power	N/A
M25	SR2_IMP_CAL_TX	1	SXCVDD2
M26	SXCVSS2	Ground	N/A
M27	Reserved	NC	
M28	Reserved	NC	
N1	VSS	Ground	N/A
N2	TRST ⁷	I	QVDD
N3	PORESET ⁷	I	QVDD
N4	VSS	Ground	N/A
N5	TMS ⁷	I	QVDD
N6	CLKOUT	0	QVDD
N7	VSS	Ground	N/A
N8	VSS	Ground	N/A
N9	VSS	Ground	N/A
N10	VDD	Power	N/A
N11	VSS	Ground	N/A
N12	M3VDD	Power	N/A
N13	VSS	Ground	N/A
N14	VDD	Power	N/A
N15	VSS	Ground	N/A
N16	VDD	Power	N/A
N17	VSS	Ground	N/A
N18	VDD	Power	N/A
N19	VSS	Ground	N/A
N20	Reserved	NC	—
N21	SXPVDD2	Power	N/A
N22	SXPVSS2	Ground	N/A

N23 SR2_TXD2/PE_TXD2/SG_TX ⁴ O SXPVDD2 N24 SR2_TXD2/PE_TXD2/SG_TX ⁴ O SXPVDD2 N26 SXCVDD2 Power N/A N26 SXCVD2 Power N/A N27 SR2_RXD2/PE_RXD2/SG_TX ⁴ I SXCVDD2 N28 SR2_RXD2/PE_RXD2/SG_TX ⁴ I SXCVDD2 P1 CLKIN I QVDD P2 EE0 I QVDD P3 GVDD Power N/A P4 VSS Ground N/A P5 STOP_BS I QVDD P6 QVDD Power N/A P7 VSS Ground N/A P7 VSS Ground N/A P10 VDD Power VDD P11 VDD Power N/A P12 VSS Ground N/A P14 VSS Ground N/A P15 MVDD <td< th=""><th>Ball Number</th><th>Signal Name^{1,2}</th><th>Pin Type¹⁰</th><th colspan="2">Power Rail Name</th></td<>	Ball Number	Signal Name ^{1,2}	Pin Type ¹⁰	Power Rail Name	
N24 SR2_TND2#E_TXD2/SG1_TX ⁴ O SXPVDD2 N25 SXCVDD2 Power N/A N26 SXCVDD2 Ground N/A N27 SR2_RXD2/FE_RXD2/SG1_RX ⁴ I SXCVDD2 N28 SR2_RXD2/FE_RXD2/SG1_RX ⁴ I SXCVDD2 P1 CLKIN I QVDD P2 E60 I QVDD P3 QVDD Power N/A P4 VSS Ground N/A P5 STOP_BS I QVDD P6 QVDD Power N/A P7 VSS Ground N/A P7 VSS Ground N/A P70 VSS Ground N/A P11 VDD Power VDD P11 VDD Power N/A P13 VDD Power N/A P16 VSS Ground N/A P16 VSS Ground	N23	SR2_TXD2/PE_TXD2/SG1_TX ⁴	0	SXPVDD2	
N25 SXCVDD2 Power N/A N26 SXCVD2 Ground N/A N27 SR2_RXD2/FE_RXD2/SG1_RX ⁴ I SKCVDD2 N28 SR2_RXD2/FE_RXD2/SG1_RX ⁴ I SKCVDD2 P1 CUKIN I OVDD P2 EE0 I OVDD P3 OVDD Power N/A P4 VSS Ground N/A P5 STOP_BS I QVDD P6 QVDD Power N/A P7 VSS Ground N/A P6 QVDD Power N/A P7 VSS Ground N/A P7 VSS Ground N/A P10 VSS Ground N/A P11 VDD Power N/A P13 VDD Power N/A P14 VSS Ground N/A P14 VSS Ground N/A <td>N24</td> <td>SR2_TXD2/PE_TXD2/SG1_TX⁴</td> <td>0</td> <td>SXPVDD2</td>	N24	SR2_TXD2/PE_TXD2/SG1_TX ⁴	0	SXPVDD2	
N26 SR2_NXD2/FE_RXD2/SG1_RX ⁴ Ground N/A N27 SR2_RXD2/FE_RXD2/SG1_RX ⁴ I SXCVDD2 P1 CLKIN I SXCVDD2 P1 CLKIN I QVDD P2 EE0 I QVDD P3 GVDD Power N/A P4 VSS Ground N/A P6 STOP_BS I QVDD P6 GVDD Power N/A P7 VSS Ground N/A P8 PLL0_AVD0 ⁹ Power VDD P9 PLL2_AVD0 ⁹ Power VDD P10 VSS Ground N/A P11 VDD Power N/A P12 VSS Ground N/A P13 VDD Power N/A P14 VSS Ground N/A P15 MVDD Power N/A P15 MVDD Power N/A </td <td>N25</td> <td>SXCVDD2</td> <td>Power</td> <td>N/A</td>	N25	SXCVDD2	Power	N/A	
N27 SR2_RXD2/PE_RXD2/SG1_RX ⁴ I SXCVDD2 N28 SR2_RXD2/PE_RXD2/SG1_RX ⁴ I SXCVDD2 P1 CLKIN I QVDD P2 EE0 I QVDD P3 QVDD Power N/A P4 VSS Ground N/A P6 STOP_BS I QVDD P6 QVDD Power N/A P7 VSS Ground N/A P6 QVDD Power VDD P9 PLL2_AVD0 ⁸ Power VDD P10 VSS Ground N/A P11 VDD Power N/A P12 VSS Ground N/A P13 VDD Power N/A P14 VSS Ground N/A P15 M/DD Power N/A P16 VSS Ground N/A P17 M/DD Power N/A <	N26	SXCVSS2	Ground	N/A	
N28 SR2_RXD2/PE_RXD2/SG1_RX ⁴ I SXCVDD2 P1 CLKIN I QVDD P3 QVDD Power N/A P4 VSS Ground N/A P6 QVDD Power N/A P6 STOP_BS I QVDD P6 QVDD Power N/A P7 VSS Ground N/A P8 PLLQ_AVDD ⁸ Power VDD P9 PLL2_AVDD ⁹ Power VDD P10 VSS Ground N/A P11 VDD Power N/A P12 VSS Ground N/A P13 VDD Power N/A P14 VSS Ground N/A P15 M/DD Power N/A P16 VSS Ground N/A P18 VSS Ground N/A P19 VDD Power N/A <t< td=""><td>N27</td><td>SR2_RXD2/PE_RXD2/SG1_RX⁴</td><td>I</td><td>SXCVDD2</td></t<>	N27	SR2_RXD2/PE_RXD2/SG1_RX ⁴	I	SXCVDD2	
P1 CLKIN I QVDD P2 EE0 I QVDD P3 QVDD Power N/A P4 VSS Ground N/A P6 STOP_BS I QVDD P6 Ground N/A P7 VSS Ground N/A P7 VSS Ground N/A P8 PLL2_AVDD ⁹ Power VDD P10 VSS Ground N/A P11 VDD Power N/A P12 VSS Ground N/A P13 VDD Power N/A P14 VSS Ground N/A P15 M/DD Power N/A P16 VSS Ground N/A P17 M/DD Power N/A P18 VSS Ground N/A P20 Reserved NC - P21 Reserved	N28	SR2_RXD2/PE_RXD2/SG1_RX ⁴	I	SXCVDD2	
P2 EE0 I QVDD P3 QVDD Power N/A P4 VSS Ground N/A P5 STOP_BS I QVDD P6 QVDD Power N/A P7 VSS Ground N/A P7 VSS Ground N/A P8 PLL0_AVDD ⁹ Power VDD P9 PL12_AVDD ⁹ Power VDD P10 VSS Ground N/A P11 VDD Power N/A P12 VSS Ground N/A P13 VDD Power N/A P14 VSS Ground N/A P15 MVDD Power N/A P16 VSS Ground N/A P18 VSS Ground N/A P19 VDD Power N/A P20 Reserved NC - P21	P1	CLKIN	I	QVDD	
P3 QVDD Power N/A P4 VSS Ground NA P5 STOP_BS I QVDD P6 QVDD Power N/A P7 VSS Ground NA P8 PLL0_AVDD ⁹ Power VDD P9 PLL2_AVDD ⁹ Power VDD P10 VSS Ground N/A P11 VDD Power N/A P12 VSS Ground N/A P13 VDD Power N/A P14 VSS Ground N/A P14 VSS Ground N/A P14 VSS Ground N/A P16 VSS Ground N/A P17 MVDD Power N/A P18 VSS Ground N/A P20 Reserved NC - P21 Reserved NC - P23 <td>P2</td> <td>EE0</td> <td>I</td> <td>QVDD</td>	P2	EE0	I	QVDD	
P4 VSS Ground N/A P5 STOP_BS 1 QVDD P6 QVDD Power N/A P7 VSS Ground N/A P8 PLL0_AVDD ⁹ Power VDD P9 PLL2_AVDD ⁹ Power VDD P10 VSS Ground N/A P11 VDD Power N/A P12 VSS Ground N/A P13 VDD Power N/A P14 VSS Ground N/A P15 MVDD Power N/A P16 VSS Ground N/A P17 MVDD Power N/A P18 VSS Ground N/A P19 VDD Power N/A P20 Reserved NC - P21 Reserved NC - P22 Reserved NC - P23 </td <td>P3</td> <td>QVDD</td> <td>Power</td> <td>N/A</td>	P3	QVDD	Power	N/A	
P5 STOP_BS I QVDD P6 QVDD Power N/A P7 VSS Ground N/A P8 PLL0_AVDD ⁹ Power VDD P9 PLL2_AVDD ⁹ Power VDD P10 VSS Ground N/A P11 VDD Power N/A P12 VSS Ground N/A P13 VDD Power N/A P14 VSS Ground N/A P15 MVDD Power N/A P16 VSS Ground N/A P17 MVDD Power N/A P18 VSS Ground N/A P19 VDD Power N/A P20 Reserved NC - P21 Reserved NC - P22 Reserved NC - P23 SXPVD2 Power N/A P2	P4	VSS	Ground	N/A	
P6 QVDD Power N/A P7 VSS Ground N/A P8 PLL0_AVDD ⁹ Power VDD P9 PLL2_AVDD ³ Power VDD P10 VSS Ground N/A P11 VDD Power N/A P12 VSS Ground N/A P11 VDD Power N/A P12 VSS Ground N/A P13 VDD Power N/A P14 VSS Ground N/A P15 M/DD Power N/A P16 VSS Ground N/A P17 M/DD Power N/A P18 VSS Ground N/A P20 Reserved NC - P21 Reserved NC - P22 Reserved NC - P23 SXPVD2 Power N/A P	P5	STOP_BS	I	QVDD	
P7 VSS Ground N/A P8 PLLQ_AVDD ⁹ Power VDD P9 PLL2_AVDD ⁹ Power VDD P10 VSS Ground N/A P11 VDD Power N/A P12 VSS Ground N/A P13 VDD Power N/A P14 VSS Ground N/A P15 M/DD Power N/A P16 VSS Ground N/A P17 M/DD Power N/A P17 M/DD Power N/A P16 VSS Ground N/A P17 M/DD Power N/A P18 VSS Ground N/A P19 VDD Power N/A P20 Reserved NC - P21 Reserved NC - P23 SXPVDD2 Power N/A <t< td=""><td>P6</td><td>QVDD</td><td>Power</td><td>N/A</td></t<>	P6	QVDD	Power	N/A	
P8 PLLQ_AVDD ⁹ Power VDD P9 PLL2_AVDD ⁹ Power VDD P10 VSS Ground N/A P11 VDD Power N/A P12 VSS Ground N/A P13 VDD Power N/A P14 VSS Ground N/A P15 MVDD Power N/A P16 VSS Ground N/A P17 MVDD Power N/A P18 VSS Ground N/A P19 VDD Power N/A P19 VDD Power N/A P20 Reserved NC - P21 Reserved NC - P23 SXPVDD2 Power N/A P24 SXPVSS2 Ground N/A P25 SR2_PL_AGND ⁹ Ground N/A P26 SR2_PL_AGND ⁹ Power N/A	P7	VSS	Ground	N/A	
P9 PLL2_AVDD ⁹ Power VDD P10 VSS Ground N/A P11 VDD Power N/A P12 VSS Ground N/A P13 VDD Power N/A P14 VSS Ground N/A P15 MVDD Power N/A P16 VSS Ground N/A P17 MVDD Power N/A P18 VSS Ground N/A P18 VSS Ground N/A P18 VSS Ground N/A P20 Reserved NC - P21 Reserved NC - P22 Reserved NC - P23 SXPVDD2 Power N/A P24 SXPVS2 Ground N/A P25 SR2_PLL_AOD ⁹ Power SXCVS2 P26 SR2_PL_AOD ⁹ Power N/A	P8	PLL0_AVDD ⁹	Power	VDD	
P10 VSS Ground N/A P11 VDD Power N/A P12 VSS Ground N/A P13 VDD Power N/A P14 VSS Ground N/A P15 MVDD Power N/A P16 VSS Ground N/A P17 MVDD Power N/A P18 VSS Ground N/A P19 VDD Power N/A P19 VDD Power N/A P20 Reserved NC - P21 Reserved NC - P23 SXPVD2 Power N/A P24 SXPVS2 Ground N/A P25 SR2_PLL_AGND ⁹ Ground N/A P28 SXCVD2 Power N/A P28 SXCVD2 Power N/A R1 VSS Ground N/A	P9	PLL2_AVDD ⁹	Power	VDD	
P11 VDD Power N/A P12 VSS Ground N/A P13 VDD Power N/A P14 VSS Ground N/A P14 VSS Ground N/A P15 M/DD Power N/A P16 VSS Ground N/A P17 M/DD Power N/A P18 VSS Ground N/A P19 VDD Power N/A P19 VDD Power N/A P20 Reserved NC - P21 Reserved NC - P22 Reserved NC - P23 SXPVDD2 Power N/A P24 SXPVSS2 Ground N/A P25 SR2_PLL_ADD ⁹ Power N/A R1 VSS Ground N/A R2 NMI I QVDD R3 <td>P10</td> <td>VSS</td> <td>Ground</td> <td>N/A</td>	P10	VSS	Ground	N/A	
P12 VSS Ground N/A P13 VDD Power N/A P14 VSS Ground N/A P15 MVDD Power N/A P16 VSS Ground N/A P17 MVDD Power N/A P18 VSS Ground N/A P19 VDD Power N/A P20 Reserved NC - P21 Reserved NC - P21 Reserved NC - P21 Reserved NC - P22 Reserved NC - P23 SXPUDD2 Power N/A P24 SXPUSS2 Ground N/A P25 SR2_PLL_AGND ⁹ Ground N/A P28 SXCVDD2 Power N/A R1 VSS Ground N/A R1 VSS Ground N/A	P11	VDD	Power	N/A	
P13 VDD Power N/A P14 VSS Ground N/A P15 MVDD Power N/A P16 VSS Ground N/A P17 MVDD Power N/A P18 VSS Ground N/A P19 VDD Power N/A P20 Reserved NC P21 Reserved NC P22 Reserved NC P23 SXPVDD2 Power N/A P24 SXPVD2 Power N/A P25 SR2_PLL_AGND ⁹ Ground N/A P26 SR2_PLL_AVD9 ⁶ Power N/A P27 SXCVS2 Ground N/A P28 SXCVD02 Power N/A R1 VSS Ground N/A R2 NMI I QVDD R3 NM_OUT ⁶ O QVDD	P12	VSS	Ground	N/A	
P14 VSS Ground N/A P15 MVDD Power N/A P16 VSS Ground N/A P17 MVDD Power N/A P17 MVDD Power N/A P17 MVDD Power N/A P18 VSS Ground N/A P18 VSD Power N/A P20 Reserved NC P21 Reserved NC P22 Reserved NC P23 SXPVDD2 Power N/A P24 SXPVSS2 Ground N/A P25 SR2_PLL_AGND ⁹ Ground N/A P28 SXCVDD2 Power N/A P28 SXCVDD2 Power N/A R1 VSS Ground N/A R2 NMI I QVDD R3 NMI_OUT ⁶ O QVDD	P13	VDD	Power	N/A	
P15 MVDD Power N/A P16 VSS Ground N/A P17 MVDD Power N/A P18 VSS Ground N/A P18 VSS Ground N/A P19 VDD Power N/A P20 Reserved NC P21 Reserved NC P22 Reserved NC P23 SXPVDD2 Power N/A P24 SXPVSS2 Ground N/A P25 SR2_PLL_AOD ⁹ Power N/A P26 SR2_PLL_AVDD ⁹ Power N/A P27 SXCVSS2 Ground N/A P28 SXCVDD2 Power N/A R1 VSS Ground N/A R2 NMI I QVDD R3 NMI_OUT ⁶ O QVDD R4 HRESET ^{6,7} I/O QVDD <	P14	VSS	Ground	N/A	
P16 VSS Ground N/A P17 MVDD Power N/A P18 VSS Ground N/A P19 VDD Power N/A P20 Reserved NC - P21 Reserved NC - P22 Reserved NC - P23 SXPVDD2 Power N/A P24 SXPVSS2 Ground N/A P25 SR2_PLL_AGND ⁹ Ground SXCVSS2 P26 SR2_PLL_AGND ⁹ Power SXCVDD2 P27 SXCVSS2 Ground N/A P28 SXCVDD2 Power N/A P28 SXCVDD2 Power N/A R1 VSS Ground N/A R2 NMI I QVDD R3 NML_OUT ⁶ O QVDD R4 HRESET ^{6,7} I/O QVDD R6 EE1 O QVDD	P15	MVDD	Power	N/A	
P17 MVDD Power N/A P18 VSS Ground N/A P19 VDD Power N/A P20 Reserved NC - P21 Reserved NC - P22 Reserved NC - P23 SXPVDD2 Power N/A P24 SXPVS2 Ground N/A P25 SR2_PLL_AGND ⁹ Ground SXCVS2 P26 SR2_PLL_AVD9 Power N/A P27 SXCVS2 Ground N/A P28 SXCVDD2 Power N/A P28 SXCVD2 Power N/A R1 VSS Ground N/A R2 IMI I QVDD R3 MMLOUT6 O QVDD R4 HRESET ^{6,7} I/O QVDD R6 EE1 O QVDD R6 EE1 O QVDD	P16	VSS	Ground	N/A	
P18 VSS Ground N/A P19 VDD Power N/A P20 Reserved NC P21 Reserved NC P22 Reserved NC P23 SXPVDD2 Power N/A P24 SXPVSS2 Ground N/A P25 SR2_PLL_AGND ⁹ Ground SXCVSS2 P26 SR2_PLL_AOND ⁹ Power SXCVDD2 P27 SXCVD2 Power N/A P28 SXCVD2 Power N/A P28 SXCVD2 Power N/A R1 VSS Ground N/A R2 NMI I QVDD R3 NMI_OUT ⁶ O QVDD R4 HRESET ^{6,7} I/O QVDD R6 EE1 O QVDD R6 EE1 O QVDD R9 VSS Ground N/A <td>P17</td> <td>MVDD</td> <td>Power</td> <td>N/A</td>	P17	MVDD	Power	N/A	
P19 VDD Power N/A P20 Reserved NC P21 Reserved NC P22 Reserved NC P23 SXPVDD2 Power N/A P24 SXPVSS2 Ground N/A P25 SR2_PLL_AGND ⁹ Ground SXCVSS2 P26 SR2_PLL_AVDD ⁹ Power SXCVDD2 P27 SXCVSS2 Ground N/A P28 SXCVDD2 Power N/A R1 VSS Ground N/A R2 NMI I QVDD R3 NM_OUT ⁶ O QVDD R4 HRESET ^{6,7} I/O QVDD R6 EE1 O QVDD R7 VSS Ground N/A R8 PL1_AVD ⁹ Power VD R10 VDD Power N/A R11 VSS Ground N/A	P18	VSS	Ground	N/A	
P20ReservedNC-P21ReservedNC-P22ReservedNC-P23SXPVDD2PowerN/AP24SXPVSS2GroundN/AP25SR2_PLL_AGND ⁹ GroundSXCVSS2P26SR2_PLL_AVDD ⁹ PowerSXCVDD2P27SXCVSS2GroundN/AP28SXCVDD2PowerN/AR1VSSGroundN/AR2NMIIQVDDR3NMI_OUT ⁶ OQVDDR4HRESET ^{6,7} I/OQVDDR6EE1OQVDDR7VSSGroundN/AR8PLL1_AVDD ⁹ PowerV/AR10VDDPowerN/AR11VSSMon-userN/AR11VSSNon-userN/AR12VDDPowerN/A	P19	VDD	Power	N/A	
P21 Reserved NC P22 Reserved NC P23 SXPVDD2 Power N/A P24 SXPVSS2 Ground N/A P25 SR2_PLL_AGND ⁹ Ground SXCVSS2 P26 SR2_PLL_AVDD ⁹ Power SXCVDD2 P27 SXCVSS2 Ground N/A P28 SXCVDD2 Power N/A R1 VSS Ground N/A R2 NMI I QVDD R3 NM_OUT ⁶ O QVDD R4 HRESET ^{6,7} I/O QVDD R5 INT_OUT ⁶ O QVDD R6 EE1 O QVDD R7 VSS Ground N/A R10 VDD Power N/A R11 VSS Ground N/A R14 HRESET ^{6,7} I/O QVDD R6 EE1 O QVDD	P20	Reserved	NC	_	
P22 Reserved NC P23 SXPVDD2 Power N/A P24 SXPVSS2 Ground N/A P25 SR2_PLL_AGND ⁹ Ground SXCVSS2 P26 SR2_PLL_AVDD ⁹ Power SXCVDD2 P27 SXCVSS2 Ground N/A P28 SXCVDD2 Power N/A R1 VSS Ground N/A R2 NMI I QVDD R3 NMI_OUT ⁶ O QVDD R4 HRESET ^{6,7} I/O QVDD R5 INT_OUT ⁶ O QVDD R6 EE1 O QVDD R7 VSS Ground N/A R8 PLL1_AVDD ⁹ Power N/A R10 VDD Power N/A R11 VSS Non-user N/A	P21	Reserved	NC	_	
P23 SXPVDD2 Power N/A P24 SXPVSS2 Ground N/A P25 SR2_PLL_AGND ⁹ Ground SXCVSS2 P26 SR2_PLL_AVDD ⁹ Power SXCVDD2 P27 SXCVSS2 Ground N/A P28 SXCVDD2 Power N/A R1 VSS Ground N/A R2 NMI I QVDD R3 NMI_OUT ⁶ O QVDD R4 HRESET ^{6,7} I/O QVDD R5 INT_OUT ⁶ O QVDD R6 EE1 O QVDD R8 PLL1_AVDD ⁹ Power V/A R10 VDD Power N/A R11 VSS Ground N/A R11 VSS Non-user N/A	P22	Reserved	NC	_	
P24SXPVSS2GroundN/AP25SR2_PLL_AGND9GroundSXCVSS2P26SR2_PLL_AVDD9PowerSXCVD2P27SXCVSS2GroundN/AP28SXCVDD2PowerN/AR1VSSGroundN/AR2NMIIQVDDR3NMI_OUT6OQVDDR4HRESET6.7I/OQVDDR5INT_OUT6OQVDDR6EE1OQVDDR7VSSGroundN/AR8PLL1_AVDD9PowerVDDR9VSSGroundN/AR11VSSNon-userN/AR12VDDPowerN/A	P23	SXPVDD2	Power	N/A	
P25SR2_PLL_AGND9GroundSXCVSS2P26SR2_PLL_AVDD9PowerSXCVDD2P27SXCVSS2GroundN/AP28SXCVDD2PowerN/AR1VSSGroundN/AR2NMIIQVDDR3NMI_OUT6OQVDDR4HRESET ^{6,7} I/OQVDDR5INT_OUT6OQVDDR6EE1OQVDDR7VSSGroundN/AR8PLL1_AVDD9GroundN/AR10VDDPowerN/AR11VSSGroundN/AR11VSSNon-userN/AR11VSSNon-userN/AR11VDDPowerN/AR12VDDPowerN/A	P24	SXPVSS2	Ground	N/A	
P26SR2_PLL_AVDD ⁹ PowerSXCVD2P27SXCVSS2GroundN/AP28SXCVDD2PowerN/AR1VSSGroundN/AR2NMIIQVDDR3NMI_OUT ⁶ OQVDDR4HRESET ^{6,7} I/OQVDDR5INT_OUT ⁶ OQVDDR6EE1OQVDDR7VSSGroundN/AR8PLL1_AVDD ⁹ PowerVDDR9VSSGroundN/AR10VDDPowerN/AR11VSSNon-userN/AR12VDDPowerN/A	P25	SR2_PLL_AGND ⁹	Ground	SXCVSS2	
P27SXCVSS2GroundN/AP28SXCVDD2PowerN/AR1VSSGroundN/AR2NMIIQVDDR3NMI_OUT6OQVDDR4HRESET6.7I/OQVDDR5INT_OUT6OQVDDR6EE1OQVDDR7VSSGroundN/AR8PLL1_AVDD9PowerVDDR9VSSGroundN/AR10VDDPowerN/AR11VSSNon-userN/AR12VDDPowerN/A	P26	SR2_PLL_AVDD ⁹	Power	SXCVDD2	
P28SXCVDD2PowerN/AR1VSSGroundN/AR2NMIIQVDDR3NMI_OUT6OQVDDR4HRESET6.7I/OQVDDR5INT_OUT6OQVDDR6EE1OQVDDR7VSSGroundN/AR8PLL1_AVDD9PowerVDDR9VSSGroundN/AR10VDDPowerN/AR11VSSNon-userN/AR12VDDPowerN/A	P27	SXCVSS2	Ground	N/A	
R1VSSGroundN/AR2NMIIQVDDR3NMI_OUT6OQVDDR4HRESET6.7I/OQVDDR5INT_OUT6OQVDDR6EE1OQVDDR7VSSGroundN/AR8PLL1_AVDD9PowerVDDR9VSSGroundN/AR10VDDPowerN/AR11VSSNon-userN/AR12VDDPowerN/A	P28	SXCVDD2	Power	N/A	
R2NMIIQVDDR3NMI_OUT6OQVDDR4HRESET6.7I/OQVDDR5INT_OUT6OQVDDR6EE1OQVDDR7VSSGroundN/AR8PLL1_AVDD9PowerVDDR9VSSGroundN/AR10VDDPowerN/AR11VSSNon-userN/AR12VDDPowerN/A	R1	VSS	Ground	N/A	
R3NMI_OUT6OQVDDR4HRESET6,7I/OQVDDR5INT_OUT6OQVDDR6EE1OQVDDR7VSSGroundN/AR8PLL1_AVDD9PowerVDDR9VSSGroundN/AR10VDDPowerN/AR11VSSNon-userN/AR12VDDPowerN/A	R2	NMI	I	QVDD	
R4HRESET ^{6,7} I/OQVDDR5INT_OUT ⁶ OQVDDR6EE1OQVDDR7VSSGroundN/AR8PLL1_AVDD ⁹ PowerVDDR9VSSGroundN/AR10VDDPowerN/AR11VSSNon-userN/AR12VDDPowerN/A	R3	NMI OUT ⁶	0	QVDD	
R5INT_OUT6OQVDDR6EE1OQVDDR7VSSGroundN/AR8PLL1_AVDD9PowerVDDR9VSSGroundN/AR10VDDPowerN/AR11VSSNon-userN/AR12VDDPowerN/A	R4	HRESET ^{6,7}	I/O	QVDD	
R6EE1OQVDDR7VSSGroundN/AR8PLL1_AVDD9PowerVDDR9VSSGroundN/AR10VDDPowerN/AR11VSSNon-userN/AR12VDDPowerN/A	R5	INT OUT ⁶	0	QVDD	
R7VSSGroundN/AR8PLL1_AVDD9PowerVDDR9VSSGroundN/AR10VDDPowerN/AR11VSSNon-userN/AR12VDDPowerN/A	R6	EE1	0	QVDD	
R8PLL1_AVDD9PowerVDDR9VSSGroundN/AR10VDDPowerN/AR11VSSNon-userN/AR12VDDPowerN/A	R7	VSS	Ground	N/A	
R9 VSS Ground N/A R10 VDD Power N/A R11 VSS Non-user N/A R12 VDD Power N/A	R8	PLL1_AVDD ⁹	Power	VDD	
R10 VDD Power N/A R11 VSS Non-user N/A R12 VDD Power N/A	R9	VSS	Ground	N/A	
R11 VSS Non-user N/A R12 VDD Power N/A	R10	VDD	Power	N/A	
R12 VDD Power N/A	R11	VSS	Non-user	N/A	
	R12	VDD	Power	N/A	

Ball Number	Signal Name ^{1,2}	Pin Type ¹⁰	Power Rail Name
AB1	M1DQS2	I/O	GVDD1
AB2	M1DQS2	I/O	GVDD1
AB3	M1DQ19	I/O	GVDD1
AB4	M1DM2	0	GVDD1
AB5	M1DQ21	I/O	GVDD1
AB6	M1DQ22	I/O	GVDD1
AB7	M1CKE0	0	GVDD1
AB8	M1A11	0	GVDD1
AB9	M1A7	0	GVDD1
AB10	M1CK2	0	GVDD1
AB11	M1APAR_OUT	0	GVDD1
AB12	M1ODT1	0	GVDD1
AB13	M1APAR_IN	I	GVDD1
AB14	M1DQ43	I/O	GVDD1
AB15	M1DM5	0	GVDD1
AB16	M1DQ44	I/O	GVDD1
AB17	M1DQ40	I/O	GVDD1
AB18	M1DQ59	I/O	GVDD1
AB19	M1DM7	0	GVDD1
AB20	M1DQ60	I/O	GVDD1
AB21	VSS	Ground	N/A
AB22	GPIO31/I2C_SDA ^{5,8}	I/O	NVDD
AB23	GPIO27/TMR4/RCW_SRC0 ^{5,8}	I/O	NVDD
AB24	GPIO25/TMR2/RCW_SRC1 ^{5,8}	I/O	NVDD
AB25	GPIO24/TMR1/RCW_SRC2 ^{5,8}	I/O	NVDD
AB26	GPIO10/IRQ10/RC10 ^{5,8}	I/O	NVDD
AB27	GPI05/IRQ5/RC5 ^{5,8}	I/O	NVDD
AB28	GPIO0/IRQ0/RC0 ^{5,8}	I/O	NVDD
AC1	VSS	Ground	N/A
AC2	GVDD1	Power	N/A
AC3	M1DQ16	I/O	GVDD1
AC4	VSS	Ground	N/A
AC5	GVDD1	Power	N/A
AC6	M1DQ17	I/O	GVDD1
AC7	VSS	Ground	N/A
AC8	GVDD1	Power	N/A
AC9	M1BA2	0	GVDD1
AC10	VSS	Ground	N/A
AC11	GVDD1	Power	N/A
AC12	M1A4	0	GVDD1
AC13	VSS	Ground	N/A
AC14	GVDD1	Power	N/A
AC15	M1DQ42	I/O	GVDD1
AC16	VSS	Ground	N/A
AC17	GVDD1	Power	N/A
AC18	M1DQ58	I/O	GVDD1

Ball Number	umber Signal Name ^{1,2} Pin Type ¹⁰		Power Rail Name
AC19	VSS	Ground	N/A
AC20	GVDD1	Power	N/A
AC21	VSS	Ground	N/A
AC22	NVDD	Power	N/A
AC23	GPIO30/I2C_SCL ^{5,8}	I/O	NVDD
AC24	GPIO26/TMR3 ^{5,8}	I/O	NVDD
AC25	VSS	Ground	N/A
AC26	NVDD	Power	N/A
AC27	GPIO23/TMR0 ^{5,8}	I/O	NVDD
AC28	GPIO22 ^{5,8}	I/O	NVDD
AD1	M1DQ31	I/O	GVDD1
AD2	M1DQ30	I/O	GVDD1
AD3	M1DQ27	I/O	GVDD1
AD4	M1ECC7	I/O	GVDD1
AD5	M1ECC6	I/O	GVDD1
AD6	M1ECC3	I/O	GVDD1
AD7	M1A9	0	GVDD1
AD8	M1A6	0	GVDD1
AD9	M1A3	0	GVDD1
AD10	M1A10	0	GVDD1
AD11	MIRAS	0	GVDD1
AD12	M1A2	0	GVDD1
AD13	M1DQ38	I/O	GVDD1
AD14	M1DQS5	I/O	GVDD1
AD15	M1DQS5	I/O	GVDD1
AD16	M1DQ33	I/O	GVDD1
AD17	M1DQ56	I/O	GVDD1
AD18	M1DQ57	I/O	GVDD1
AD19	M1DQS7	I/O	GVDD1
AD20	M1DQS7	I/O	GVDD1
AD21	VSS	Ground	N/A
AD22	GE2_TX_CTL	0	NVDD
AD23	GPIO15/DDN0/IRQ15/RC15 ^{5,8}	I/O	NVDD
AD24	GPI013/IRQ13/RC13 ^{5,8}	I/O	NVDD
AD25	GE_MDC	0	NVDD
AD26	GE_MDIO	I/O	NVDD
AD27	TDM2TCK/GE1_TD3 ³	I/O	NVDD
AD28	TDM2RCK/GE1_TD0 ³	I/O	NVDD
AE1	GVDD1	Power	N/A
AE2	VSS	Ground	N/A
AE3	M1DQ29	I/O	GVDD1
AE4	GVDD1	Power	N/A
AE5	VSS	Ground	N/A
AE6	M1ECC5	I/O	GVDD1
AE7	GVDD1	Power	N/A
AE8	VSS	Ground	N/A

Electrical Characteristics

To illustrate these definitions using real values, consider the example of a current mode logic (CML) transmitter that has a common mode voltage of 2.25 V and outputs, TD and TD. If these outputs have a swing from 2.0 V to 2.5 V, the peak-to-peak voltage swing of each signal (TD or TD) is 500 mV p-p, which is referred to as the single-ended swing for each signal. Because the differential signaling environment is fully symmetrical in this example, the transmitter output differential swing (V_{OD}) has the same amplitude as each signal single-ended swing. The differential output signal ranges between 500 mV and -500 mV. In other words, V_{OD} is 500 mV in one phase and -500 mV in the other phase. The peak differential voltage (V_{DIFFp}) is 500 mV. The peak-to-peak differential voltage (V_{DIFFp}) is 1000 mV p-p.

2.5.2.2 SerDes Reference Clock Receiver Characteristics

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clock inputs are SR1_REF_CLK/SR1_REF_CLK or SR2_REF_CLK/SR2_REF_CLK. Figure 5 shows a receiver reference diagram of the SerDes reference clocks.



Figure 5. Receiver of SerDes Reference Clocks

The characteristics of the clock signals are as follows:

- The supply voltage requirements for V_{DDSXC} are as specified in Table 3.
- The SerDes reference clock receiver reference circuit structure is as follows:
 - The SR[1–2]_REF_CLK and SR[1–2]_REF_CLK are internally AC-coupled differential inputs as shown in Figure 5. Each differential clock input (SR[1–2]_REF_CLK or SR[1–2]_REF_CLK) has on-chip 50-Ω termination to GND_{SXC} followed by on-chip AC-coupling.
 - The external reference clock driver must be able to drive this termination.
 - The SerDes reference clock input can be either differential or single-ended. Refer to the differential mode and single-ended mode descriptions below for detailed requirements.
- The maximum average current requirement also determines the common mode voltage range.
 - When the SerDes reference clock differential inputs are DC coupled externally with the clock driver chip, the maximum average current allowed for each input pin is 8 mA. In this case, the exact common mode input voltage is not critical as long as it is within the range allowed by the maximum average current of 8 mA because the input is AC-coupled on-chip.
 - This current limitation sets the maximum common mode input voltage to be less than 0.4 V (0.4 V / 50 = 8 mA)while the minimum common mode input level is 0.1 V above GND_{SXC}. For example, a clock with a 50/50 duty cycle can be produced by a clock driver with output driven by its current source from 0 mA to 16 mA (0–0.8 V), such that each phase of the differential input has a single-ended swing from 0 V to 800 mV with the common mode voltage at 400 mV.
 - If the device driving the SR[1–2]_REF_CLK and $\overline{SR[1-2]}_REF_CLK$ inputs cannot drive 50 Ω to GND_{SXC} DC or the drive strength of the clock driver chip exceeds the maximum input current limitations, it must be AC-coupled externally.
- The input amplitude requirement is described in detail in the following sections.

2.5.2.3 SerDes Transmitter and Receiver Reference Circuits

Figure 6 shows the reference circuits for SerDes data lane transmitter and receiver.



Note: The [1–2] indicates the specific SerDes Interface (1 or 2) and the m indicates the specific channel within that interface (0,1,2,3). Actual signals are assigned by the HRCW assignments at reset (see **Chapter 5**, *Reset* in the reference manual for details)

Figure 6. SerDes Transmitter and Receiver Reference Circuits

2.5.3 DC-Level Requirements for SerDes Interfaces

The following subsections define the DC-level requirements for the SerDes reference clocks, the PCI Express data lines, the Serial RapidIO data lines, and the SGMII data lines.

2.5.3.1 DC-Level Requirements for SerDes Reference Clocks

The DC-level requirement for the SerDes reference clock inputs is different depending on the signaling mode used to connect the clock driver chip and SerDes reference clock inputs, as described below:

- Differential Mode
 - The input amplitude of the differential clock must be between 400 mV and 1600 mV differential peak-peak (or between 200 mV and 800 mV differential peak). In other words, each signal wire of the differential pair must have a single-ended swing of less than 800 mV and greater than 200 mV. This requirement is the same for both external DC-coupled or AC-coupled connection.
 - For an external DC-coupled connection, the maximum average current requirements sets the requirement for average voltage (common mode voltage) as between 100 mV and 400 mV. Figure 7 shows the SerDes reference clock input requirement for DC-coupled connection scheme.









Figure 13. DDR SDRAM Output Timing

Figure 14 provides the AC test load for the DDR2 and DDR3 controller bus.



Figure 14. DDR2 and DDR3 Controller Bus AC Test Load

2.6.1.3 DDR2 and DDR3 SDRAM Differential Timing Specifications

This section describes the DC and AC differential timing specifications for the DDR2 and DDR3 SDRAM controller interface. Figure 15 shows the differential timing specification.



Figure 15. DDR2 and DDR3 SDRAM Differential Timing Specifications

Note: VTR specifies the true input signal (such as MCK or MDQS) and VCP is the complementary input signal (such as \overline{MCK} or \overline{MDQS}).

Table 24. SR[1–2]_REF_CLK and SR[1–2]_REF_CLK Input Clock Requirements (continued)

		Parameter	Symbol	Min	Typical	Мах	Units	Notes
Notes:	1.	1. Caution: Only 100 and 125 have been tested. Other values will not work correctly with the rest of the system.						
	2.	Limits from PCI Express CEM Rev	1.0a					
	3.	Measured from -200 mV to +200 i	mV on the differentia	I waveform (de	rived from SR[1	-2]_REF_CLK	minus	
		SR[1-2]_REF_CLK). The signal m	ust be monotonic th	rough the meas	urement region	for rise and fal	l time. The 400	mV
		measurement window is centered	on the differential ze	ero crossing. Se	e Figure 16.			
	4.	Measurement taken from different	al waveform					
	5.	Measurement taken from single-er	nded waveform					
	6.	Matching applies to rising edge for	SR[1-2]_REF_CLK	and falling edg	e rate for SR[1	-2]_REF_CLK.	It is measured	using a
	200 mV window centered on the median cross point where SR[1-2]_REF_CLK rising meets SR[1-2]_REF_CLK falling. The						ing. The	
	median cross point is used to calculate the voltage thresholds that the oscilloscope uses for the edge rate calculations. The							ns. The
		rise edge rate of SR[1-2]_REF_C	K should be compa	red to the fall e	dge rate of SR[1-2]_REF_CLK	; the maximum	allowed
		difference should not exceed 20%	of the slowest edge	rate. See Figur	e 17.			



Figure 16. Differential Measurement Points for Rise and Fall Time



Figure 17. Single-Ended Measurement Points for Rise and Fall Time Matching

2.6.2.2 PCI Express AC Physical Layer Specifications

The AC requirements for PCI Express implementations have separate requirements for the Tx and Rx lines. The MSC8156E supports a 2.5 Gbps PCI Express interface defined by the *PCI Express Base Specification, Revision 1.0a*. The transmitter specifications are defined in Table 25 and the receiver specifications are defined in Table 26. The parameters are specified at the component pins. the AC timing specifications do not include REF_CLK jitter.

Note: Specifications are valid at the recommended operating conditions listed in Table 3.

Table 25. PCI Express (2.5 Gbps) Differential Transmitter (Tx) Output AC Specifications

Parameter	Symbol	Min	Typical	Мах	Units	Notes
Unit interval	UI	399.88	400.00	400.12	ps	1
Minimum Tx eye width	T _{TX-EYE}	0.70	—	—	UI	2, 3
Maximum time between the jitter median and maximum deviation from the median.	T _{TX-EYE-MEDIAN-} to-MAX-JITTER	_	_	0.15	UI	3, 4
AC coupling capacitor	C _{TX}	75	—	200	nF	5

Notes: 1. Each UI is 400 ps ± 300 ppm. UI does not account for spread spectrum clock dictated variations. No test load is necessarily associated with this value.

2. The maximum transmitter jitter can be derived as $T_{TX-MAX-JITTER} = 1 - T_{TX-EYE} = 0.3$ UI.

3. Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 8 and measured over any 250 consecutive Tx UIs. A T_{TX-EYE} = 0.70 UI provides for a total sum of deterministic and random jitter budget of T_{TX-JITTER-MAX} = 0.30 UI for the transmitter collected over any 250 consecutive Tx UIs. The T_{TX-EYE-MEDIAN-to-MAX-JITTER} median is less than half of the total Tx jitter budget collected over any 250 consecutive Tx UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. Jitter is defined as the measurement variation of the crossing points (V_{TX-DIFFp-p} = 0 V) in relation to a recovered Tx UI. A recovered Tx UI is calculated over 3500 consecutive unit intervals of sample data.

4. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the Tx UI.

5. All transmitters shall be AC-coupled. The AC coupling is required either within the media or within the transmitting component itself. The SerDes transmitter does not have built-in Tx capacitance. An external AC coupling capacitor is required.

Table 26. PCI Express (2.5 Gbps) Differential Receiver (Rx) Input AC Specifications

Parameter	Symbol	Min	Typical	Мах	Units	Notes
Unit Interval	UI	399.88	400.00	400.12	ps	1
Minimum receiver eye width	T _{RX-EYE}	0.4	—	—	UI	2, 3, 4
Maximum time between the jitter median and maximum deviation from the median.	T _{RX-EYE-MEDIAN-to-MAX} -JITTER	_	_	0.3	UI	3, 4, 5

Notes: 1. Each UI is 400 ps ± 300 ppm. UI does not account for spread spectrum clock dictated variations. No test load is necessarily associated with this value.

2. The maximum interconnect media and transmitter jitter that can be tolerated by the receiver can be derived as $T_{RX-MAX-JITTER} = 1 - T_{RX-EYE} = 0.6$ UI.

3. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 8 should be used as the Rx device when taking measurements. If the clocks to the Rx and Tx are not derived from the same reference clock, the Tx UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.

4. A T_{RX-EYE} = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the transmitter and interconnect collected any 250 consecutive UIs. The T_{RX-EYE-MEDIAN-to-MAX-JITTER} specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive Tx UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the Rx and Tx are not derived from the same reference clock, the Tx UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.

5. Jitter is defined as the measurement variation of the crossing points (V_{RX-DIFFp-p} = 0 V) in relation to a recovered Tx UI. A recovered Tx UI is calculated over 3500 consecutive unit intervals of sample data. Jitter is measured using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the Tx UI. It is recommended that the recovered Tx UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

2.6.6 SPI Timing

Table 36 lists the SPI input and output AC timing specifications.

Table 36. SPI AC Timing Specifications

Parameter	Symbol ¹	Min	Max	Unit	Note
SPI outputs valid—Master mode (internal clock) delay	t _{NIKHOV}	—	6	ns	2
SPI outputs hold—Master mode (internal clock) delay	t _{NIKHOX}	0.5	—	ns	2
SPI outputs valid—Slave mode (external clock) delay	t _{NEKHOV}	—	12	ns	2
SPI outputs hold—Slave mode (external clock) delay	t _{NEKHOX}	2	—	ns	2
SPI inputs—Master mode (internal clock) input setup time	t _{NIIVKH}	12	—	ns	—
SPI inputs—Master mode (internal clock) input hold time	t _{NIIXKH}	0	—	ns	—
SPI inputs—Slave mode (external clock) input setup time	t _{NEIVKH}	4	—	ns	—
SPI inputs—Slave mode (external clock) input hold time	t _{NEIXKH}	2	—	ns	

Notes: 1. The symbols used for timing specifications follow the pattern of t_{(first two letters of functional block)(signal)(state)} (reference)(state) for inputs and t_(first two letters of functional block)(reference)(state)(signal)(state) for outputs. For example, t_{NIKHOX} symbolizes the internal timing (NI) for the time SPICLK clock reference (K) goes to the high state (H) until outputs (O) are invalid (X).

2. Output specifications are measured from the 50% level of the rising edge of SPICLK to the 50% level of the signal. Timings are measured at the pin.

Figure 26 provides the AC test load for the SPI.



Figure 26. SPI AC Test Load

Figure 27 and Figure 28 represent the AC timings from Table 36. Note that although the specifications generally reference the rising edge of the clock, these AC timing diagrams also apply when the falling edge is the active edge.

Figure 27 shows the SPI timings in slave mode (external clock).



Note: measured with SPMODE[CI] = 0, SPMODE[CP] = 0

Figure 27. SPI AC Timing in Slave Mode (External Clock)

Figure 28 shows the SPI timings in master mode (internal clock).

3.3 Clock and Timing Signal Board Layout Considerations

When laying out the system board, use the following guidelines:

- Keep clock and timing signal paths as short as possible and route with 50 Ω impedance.
- Use a serial termination resistor placed close to the clock buffer to minimize signal reflection. Use the following equation to compute the resistor value:

Rterm = Rim - Rbuf

where Rim = trace characteristic impedance

Rbuf = clock buffer internal impedance.

3.4 SGMII AC-Coupled Serial Link Connection Example

Figure 39 shows an example of a 4-wire AC-coupled serial link connection. For additional layout suggestions, see AN3556 MSC815x High Speed Serial Interface Hardware Design Considerations, available on the Freescale website or from your local sales office or representative.



Figure 39. 4-Wire AC-Coupled SGMII Serial Link Connection Example

3.5.1.2 DDR Interface Is Used With 32-Bit DDR Memory Only

Table 41 lists unused pin connection when using 32-bit DDR memory. The 32 most significant data lines are not used.

Table 41. Connectivity of DDR Related Pins When Using 32-bit DDR Memory Only

Signal Name	Pin Connection			
MDQ[31-0]	in use			
MDQ[63-32]	NC			
MDQS[3-0]	in use			
MDQS[7-4]	NC			
MDQS[3-0]	in use			
MDQS[7-4]	NC			
MA[15–0]	in use			
MCK[2-0]	in use			
MCK[2-0]	in use			
MCS[1-0]	in use			
MDM[3-0]	in use			
MDM[7-4]	NC			
MBA[2-0]	in use			
MCAS	in use			
MCKE[1-0]	in use			
MODT[1-0] in use				
MMDIC[1-0]	in use			
MRAS	in use			
MWE	in use			
MVREF	in use			
GVDD1/GVDD2 in use				
 Notes: 1. For the signals listed in this table, the initial M stands for M1 or M2 depending on which DDR controller is not used. 2. For MSC8156E Revision 1 silicon, these pins were connected to GND (or VDD). For newer revisions of the MSC8156E. 				

connecting these pins to GND increases device power consumption.

3.5.1.3 ECC Unused Pin Connections

When the error code correction mechanism is not used in any 32- or 64-bit DDR configuration, refer to Table 42 to determine the correct pin connections.

|--|

Signal Name		Pin connection		
MECC[7-0]		NC		
MDM8		NC		
MDQS8 NC		NC		
MDQS8 NC		NC		
Notes: 1. 2.	For the signals listed in this table, the initial M stands for M1 or M2 depending on which DDR controller is not used. For MSC8156E Revision 1 silicon, these pins were connected to GND (or VDD). For newer revisions of the MSC8156E, connecting these pins to GND increases device power consumption.			

3.6 Guide to Selecting Connections for Remote Power Supply Sensing

To assure consistency of input power levels, some applications use a practice of connecting the remote sense signal input of an on-board power supply to one of power supply pins of the IC device. The advantage of using this connection is the ability to compensate for the slow components of the IR drop caused by resistive supply current path from on-board power supply to the pins layer on the package. However, because of specific device requirements, not every ball connection can be selected as the remote sense pin. Some of these pins must be connected to the appropriate power supply or ground to ensure correct device functionality. Some connections supply critical power to a specific high usage area of the IC die; using such a connection as a non-supply pin could impact necessary supply current during high current events. The following balls can be used as the board supply remote sense output without degrading the power and ground supply quality:

- *VDD:* W10, T19
- *VSS:* J18, Y10
- M3VDD: None

Do not use any other connections for remote sensing. Use of any other connections for this purpose can result in application and device failure.

4 Ordering Information

Consult a Freescale Semiconductor sales office or authorized distributor to determine product availability and place an order.

Part	Package Type	Spheres	Core Voltage	Operating Temperature	Core Frequency (MHz)	Order Number
MSC8156E	Flip Chip Plastic Ball Grid Array (FC-PBGA)	Lead-free	1.0 V	0° C to 105°C	1000	MSC8156ESVT1000B
				-40° to 105°C	1000	MSC8156ETVT1000B

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http://www.freescale.com/support

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