Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	50MHz
Connectivity	EBI/EMI, I²C, LINbus, SPI, UART/USART
Peripherals	CapSense, DMA, POR, PWM, WDT
Number of I/O	62
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 16x12b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c3244axi-153t

Figure 2-3. 48-pin SSOP Part Pinout

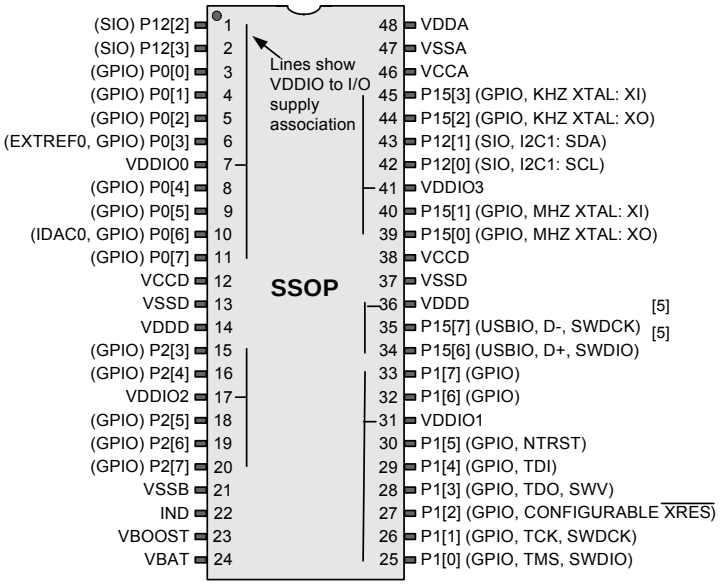
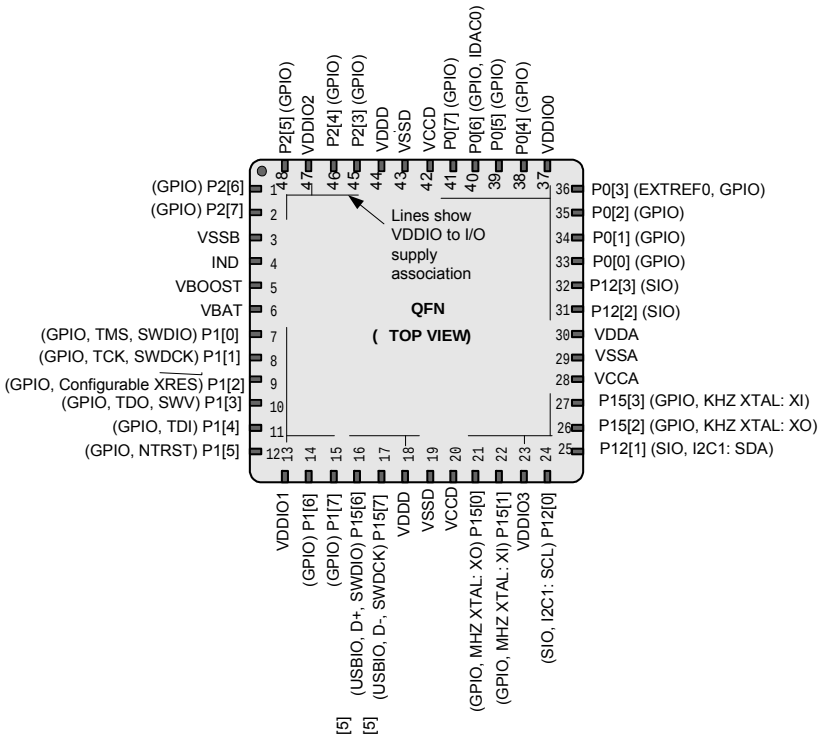


Figure 2-4. 48-pin QFN Part Pinout[6]



Notes
5. Pins are Do Not Use (DNU) on devices without USB. The pin must be left floating.
6. The center pad on the QFN package should be connected to digital ground (VSSD) for best mechanical, thermal, and electrical performance. If not connected to ground, it should be electrically floated and not connected to any other signal. For more information, see AN72845, Design Guidelines for QFN Devices.

Figure 2-6. 100-pin TQFP Part Pinout

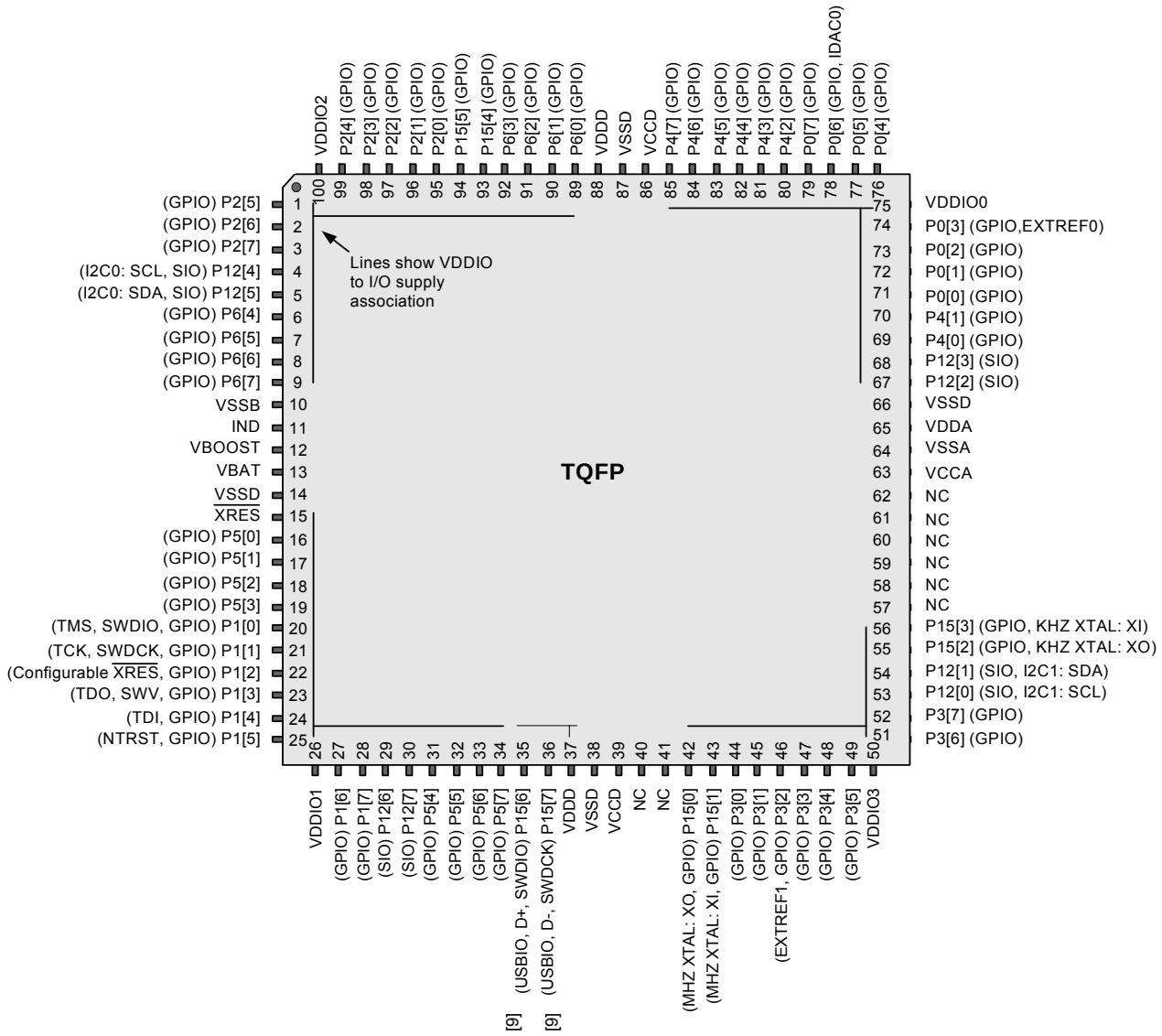
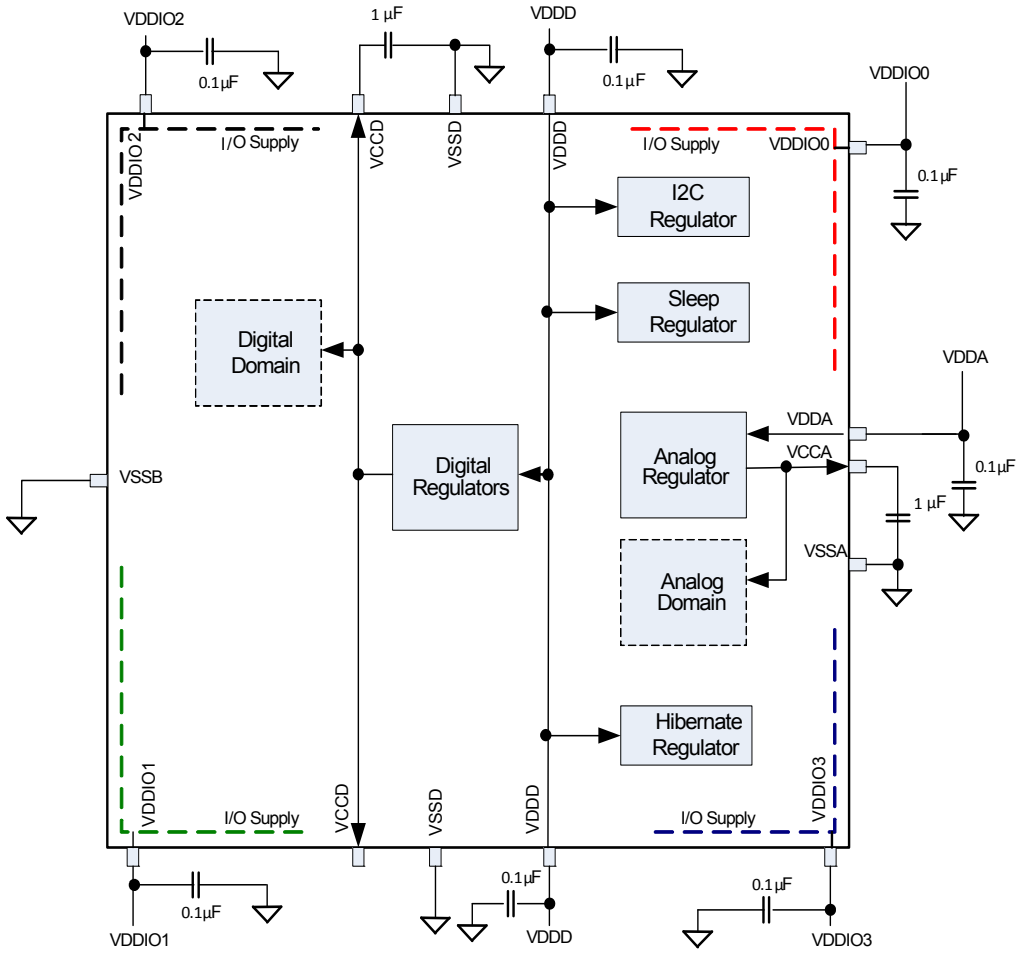


Table 2-1. VDDIO and Port Pin Associations

VDDIO	Port Pins
VDDIO0	P0[7:0], P4[7:0], P12[3:2]
VDDIO1	P1[7:0], P5[7:0], P12[7:6]
VDDIO2	P2[7:0], P6[7:0], P12[5:4], P15[5:4]
VDDIO3	P3[7:0], P12[1:0], P15[3:0]
VDDD	P15[7:6] (USB D+, D-)

Note
9. Pins are Do Not Use (DNU) on devices without USB. The pin must be left floating.

Figure 6-4. PSoC Power System



Notes

- The two VCCD pins must be connected together with as short a trace as possible. A trace under the device is recommended, as shown in Figure 2-8 on page 12.
- It is good practice to check the datasheets for your bypass capacitors, specifically the working voltage and the DC bias specifications. With some capacitors, the actual capacitance can decrease considerably when the DC bias (VDDX or VCCX in Figure 6-4) is a significant percentage of the rated working voltage.
- You can power the device in internally regulated mode, where the voltage applied to the VDDx pins is as high as 5.5 V, and the internal regulators provide the core voltages. **In this mode, do not apply power to the VCCx pins, and do not tie the VDDx pins to the VCCx pins.**
- You can also power the device in externally regulated mode, that is, by directly powering the VCCD and VCCA pins. In this configuration, the VDDD pins should be shorted to the VCCD pins and the VDDA pin should be shorted to the VCCA pin. The allowed supply range in this configuration is 1.71 V to 1.89 V. After power up in this configuration, the internal regulators are on by default, and should be disabled to reduce power consumption.

7. Digital Subsystem

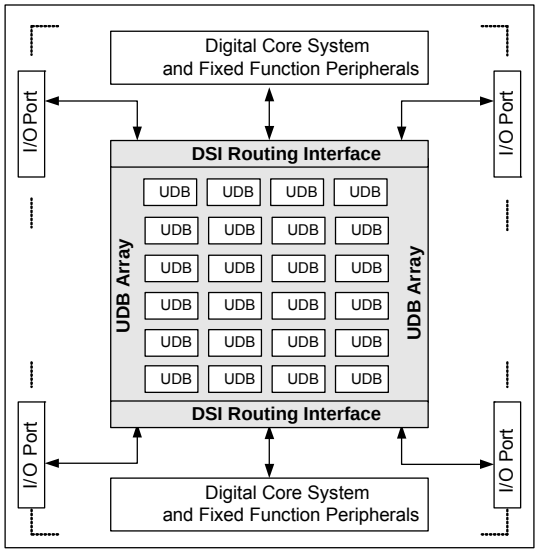
The digital programmable system creates application specific combinations of both standard and advanced digital peripherals and custom logic functions. These peripherals and logic are then interconnected to each other and to any pin on the device, providing a high level of design flexibility and IP security.

The features of the digital programmable system are outlined here to provide an overview of capabilities and architecture. You do not need to interact directly with the programmable digital system at the hardware and register level. PSoC Creator provides a high level schematic capture graphical interface to automatically place and route resources similar to PLDs.

The main components of the digital programmable system are:

- Universal Digital Blocks (UDB) – These form the core functionality of the digital programmable system. UDBs are a collection of uncommitted logic (PLD) and structural logic (Datapath) optimized to create all common embedded peripherals and customized functionality that are application or design specific.
- Universal Digital Block Array – UDB blocks are arrayed within a matrix of programmable interconnect. The UDB array structure is homogeneous and allows for flexible mapping of digital functions onto the array. The array supports extensive and flexible routing interconnects between UDBs and the Digital System Interconnect.
- Digital System Interconnect (DSI) – Digital signals from Universal Digital Blocks (UDBs), fixed function peripherals, I/O pins, interrupts, DMA, and other system core signals are attached to the Digital System Interconnect to implement full featured device connectivity. The DSI allows any digital function to any pin or other feature routability when used with the Universal Digital Block Array.

Figure 7-1. CY8C32 Digital Programmable Architecture



7.1 Example Peripherals

The flexibility of the CY8C32 family's Universal Digital Blocks (UDBs) and Analog Blocks allow the user to create a wide range of components (peripherals). The most common peripherals were built and characterized by Cypress and are shown in the PSoC Creator component catalog, however, users may also create their own custom components using PSoC Creator. Using PSoC Creator, users may also create their own components for reuse within their organization, for example sensor interfaces, proprietary algorithms, and display interfaces.

The number of components available through PSoC Creator is too numerous to list in the datasheet, and the list is always growing. An example of a component available for use in CY8C32 family, but, not explicitly called out in this datasheet is the UART component.

7.1.1 Example Digital Components

The following is a sample of the digital components available in PSoC Creator for the CY8C32 family. The exact amount of hardware resources (UDBs, routing, RAM, flash) used by a component varies with the features selected in PSoC Creator for the component.

- Communications
  - I^2C
  - UART
  - SPI
- Functions
  - EMIF
  - PWMs
  - Timers
  - Counters
- Logic
  - NOT
  - OR
  - XOR
  - AND

7.1.2 Example Analog Components

The following is a sample of the analog components available in PSoC Creator for the CY8C32 family. The exact amount of hardware resources (routing, RAM, flash) used by a component varies with the features selected in PSoC Creator for the component.

- ADC
  - Delta-sigma
- DACs
  - Current
  - Voltage
  - PWM
- Comparators

7.1.3 Example System Function Components

The following is a sample of the system function components available in PSoC Creator for the CY8C32 family. The exact amount of hardware resources (UDBs, routing, RAM, flash) used by a component varies with the features selected in PSoC Creator for the component.

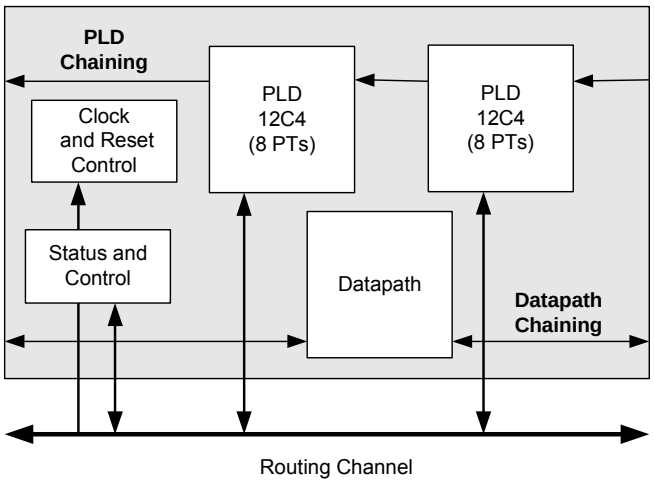
- CapSense
- LCD Drive
- LCD Control

7.2 Universal Digital Block

The Universal Digital Block (UDB) represents an evolutionary step to the next generation of PSoC embedded digital peripheral functionality. The architecture in first generation PSoC digital blocks provides coarse programmability in which a few fixed functions with a small number of options are available. The new UDB architecture is the optimal balance between configuration granularity and efficient implementation. A cornerstone of this approach is to provide the ability to customize the devices digital operation to match application requirements.

To achieve this, UDBs consist of a combination of uncommitted logic (PLD), structured logic (Datapath), and a flexible routing scheme to provide interconnect between these elements, I/O connections, and other peripherals. UDB functionality ranges from simple self contained functions that are implemented in one UDB, or even a portion of a UDB (unused resources are available for other functions), to more complex functions that require multiple UDBs. Examples of basic functions are timers, counters, CRC generators, PWMs, dead band generators, and communications functions, such as UARTs, SPI, and I^2C. Also, the PLD blocks and connectivity provide full featured general purpose programmable logic within the limits of the available resources.

Figure 7-2. UDB Block Diagram



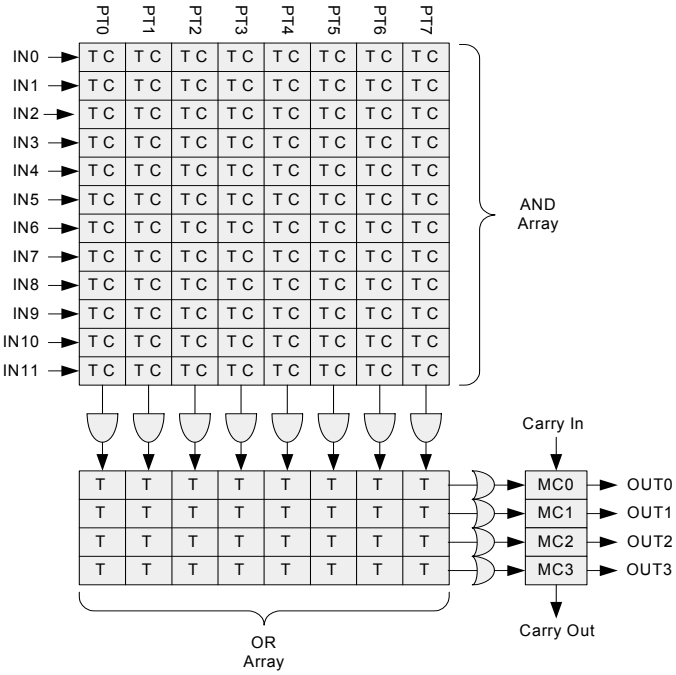
The main component blocks of the UDB are:

- PLD blocks – There are two small PLDs per UDB. These blocks take inputs from the routing array and form registered or combinational sum-of-products logic. PLDs are used to implement state machines, state bits, and combinational logic equations. PLD configuration is automatically generated from graphical primitives.
- Datapath Module – This 8-bit wide datapath contains structured logic to implement a dynamically configurable ALU, a variety of compare configurations and condition generation. This block also contains input/output FIFOs, which are the primary parallel data interface between the CPU/DMA system and the UDB.
- Status and Control Module – The primary role of this block is to provide a way for CPU firmware to interact and synchronize with UDB operation.
- Clock and Reset Module – This block provides the UDB clocks and reset selection and control.

7.2.1 PLD Module

The primary purpose of the PLD blocks is to implement logic expressions, state machines, sequencers, lookup tables, and decoders. In the simplest use model, consider the PLD blocks as a standalone resource onto which general purpose RTL is synthesized and mapped. The more common and efficient use model is to create digital functions from a combination of PLD and datapath blocks, where the PLD implements only the random logic and state portion of the function while the datapath (ALU) implements the more structured elements.

Figure 7-3. PLD 12C4 Structure



One 12C4 PLD block is shown in Figure 7-3. This PLD has 12 inputs, which feed across eight product terms. Each product term (AND function) can be from 1 to 12 inputs wide, and in a given product term, the true (T) or complement (C) of each input can be selected. The product terms are summed (OR function) to create the PLD outputs. A sum can be from 1 to 8 product terms wide. The 'C' in 12C4 indicates that the width of the OR gate (in this case 8) is constant across all outputs (rather than variable as in a 22V10 device). This PLA like structure gives maximum flexibility and insures that all inputs and outputs are permutable for ease of allocation by the software tools. There are two 12C4 PLDs in each UDB.

Analog local buses (abus) are routing resources located within the analog subsystem and are used to route signals between different analog blocks. There are eight abus routes in CY8C32, four in the left half (abusl [0:3]) and four in the right half (abusr [0:3]) as shown in Figure 8-2. Using the abus saves the analog globals and analog mux buses from being used for interconnecting the analog blocks.

Multiplexers and switches exist on the various buses to direct signals into and out of the analog blocks. A multiplexer can have only one connection on at a time, whereas a switch can have multiple connections on simultaneously. In Figure 8-2, multiplexers are indicated by grayed ovals and switches are indicated by transparent ovals.

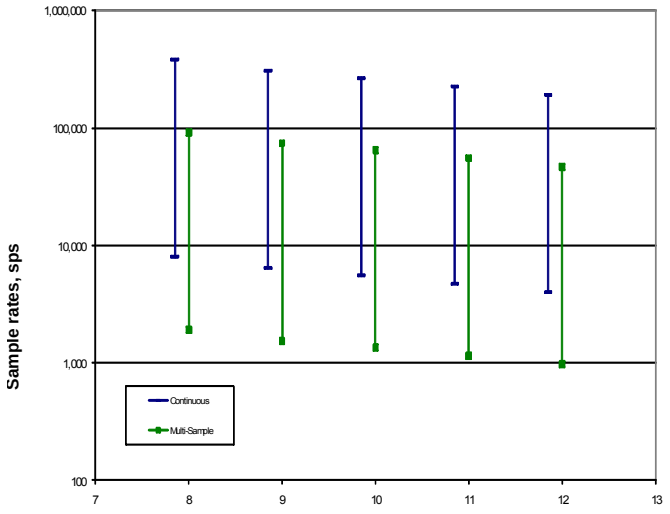
8.2 Delta-sigma ADC

The CY8C32 device contains one delta-sigma ADC. This ADC offers differential input, high resolution and excellent linearity, making it a good ADC choice for measurement applications. The converter can be configured to output 12-bit resolution at data rates of up to 192 ksps. At a fixed clock rate, resolution can be traded for faster data rates as shown in Table 8-1 and Figure 8-3.

Table 8-1. Delta-sigma ADC Performance

Bits	Maximum Sample Rate (sps)	SINAD (dB)
12	192 k	66
8	384 k	43

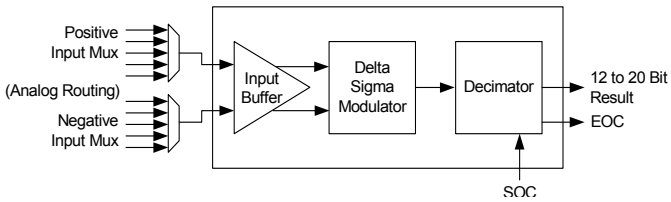
Figure 8-3. Delta-sigma ADC Sample Rates, Range = ±1.024 V



8.2.1 Functional Description

The ADC connects and configures three basic components, input buffer, delta-sigma modulator, and decimator. The basic block diagram is shown in Figure 8-4. The signal from the input muxes is delivered to the delta-sigma modulator either directly or through the input buffer. The delta-sigma modulator performs the actual analog to digital conversion. The modulator over-samples the input and generates a serial data stream output. This high speed data stream is not useful for most applications without some type of post processing, and so is passed to the decimator through the Analog Interface block. The decimator converts the high speed serial data stream into parallel ADC results. The modulator/decimator frequency response is $[(\sin x)/x]^4$.

Figure 8-4. Delta-sigma ADC Block Diagram



Resolution and sample rate are controlled by the Decimator. Data is pipelined in the decimator; the output is a function of the last four samples. When the input multiplexer is switched, the output data is not valid until after the fourth sample after the switch.

8.2.2 Operational Modes

The ADC can be configured by the user to operate in one of four modes: Single Sample, Multi Sample, Continuous, or Multi Sample (Turbo). All four modes are started by either a write to the start bit in a control register or an assertion of the Start of Conversion (SoC) signal. When the conversion is complete, a status bit is set and the output signal End of Conversion (EoC) asserts high and remains high until the value is read by either the DMA controller or the CPU.

8.2.2.1 Single Sample

In Single Sample mode, the ADC performs one sample conversion on a trigger. In this mode, the ADC stays in standby state waiting for the SoC signal to be asserted. When SoC is signaled the ADC performs four successive conversions. The first three conversions prime the decimator. The ADC result is valid and available after the fourth conversion, at which time the EoC signal is generated. To detect the end of conversion, the system may poll a control register for status or configure the external EoC signal to generate an interrupt or invoke a DMA request. When the transfer is done the ADC reenters the standby state where it stays until another SoC event.

8.2.2.2 Continuous

Continuous sample mode is used to take multiple successive samples of a single input signal. Multiplexing multiple inputs should not be done with this mode. There is a latency of three conversion times before the first conversion result is available. This is the time required to prime the decimator. After the first result, successive conversions are available at the selected sample rate.

8.2.2.3 Multi Sample

Multi sample mode is similar to continuous mode except that the ADC is reset between samples. This mode is useful when the input is switched between multiple signals. The decimator is re-primed between each sample so that previous samples do not affect the current conversion. Upon completion of a sample, the next sample is automatically initiated. The results can be transferred using either firmware polling, interrupt, or DMA.

8.4.4 LCD DAC

The LCD DAC generates the contrast control and bias voltage for the LCD system. The LCD DAC produces up to five LCD drive voltages plus ground, based on the selected bias ratio. The bias voltages are driven out to GPIO pins on a dedicated LCD bias bus, as required.

8.5 CapSense

The CapSense system provides a versatile and efficient means for measuring capacitance in applications such as touch sense buttons, sliders, proximity detection, etc. The CapSense system uses a configuration of system resources, including a few hardware functions primarily targeted for CapSense. Specific resource usage is detailed in each CapSense component in PSoC Creator.

A capacitive sensing method using a delta-sigma modulator (CSD) is used. It provides capacitance sensing using a switched capacitor technique with a delta-sigma modulator to convert the sensing current to a digital code.

8.6 Temp Sensor

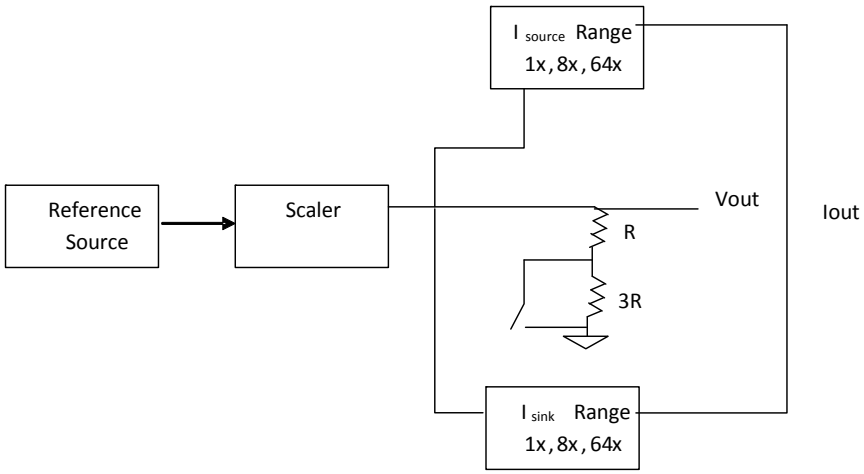
Die temperature is used to establish programming parameters for writing flash. Die temperature is measured using a dedicated sensor based on a forward biased transistor. The temperature sensor has its own auxiliary ADC.

8.7 DAC

The CY8C32 parts contain a Digital to Analog Converter (DAC). The DAC is 8-bit and can be configured for either voltage or current output. The DAC supports CapSense, power supply regulation, and waveform generation. The DAC has the following features:

- Adjustable voltage or current output in 255 steps
- Programmable step size (range selection)
- Eight bits of calibration to correct ± 25 percent of gain error
- Source and sink option for current output
- High and low speed / power modes
- 8 Msps conversion rate for current output
- 1 Msps conversion rate for voltage output
- Monotonic in nature
- Data and strobe inputs can be provided by the CPU or DMA, or routed directly from the DSI
- Dedicated low-resistance output pin for high-current mode

Figure 8-7. DAC Block Diagram



8.7.1 Current DAC

The current DAC (IDAC) can be configured for the ranges 0 to 31.875 µA, 0 to 255 µA, and 0 to 2.04 mA. The IDAC can be configured to source or sink current.

8.7.2 Voltage DAC

For the voltage DAC (VDAC), the current DAC output is routed through resistors. The two ranges available for the VDAC are 0 to 1.02 V and 0 to 4.08 V. In voltage mode any load connected to the output of a DAC should be purely capacitive (the output of the VDAC is not buffered).

9.3 Debug Features

Using the JTAG or SWD interface, the CY8C32 supports the following debug features:

- Halt and single-step the CPU
- View and change CPU and peripheral registers, and RAM addresses
- Eight program address breakpoints
- One memory access breakpoint—break on reading or writing any memory address and data value
- Break on a sequence of breakpoints (non recursive)
- Debugging at the full speed of the CPU
- Compatible with PSoC Creator and MiniProg3 programmer and debugger
- Standard JTAG programming and debugging interfaces make CY8C32 compatible with other popular third-party tools (for example, ARM / Keil)

9.4 Trace Features

The CY8C32 supports the following trace features when using JTAG or SWD:

- Trace the 8051 program counter (PC), accumulator register (ACC), and one SFR / 8051 core RAM register
- Trace depth up to 1000 instructions if all registers are traced, or 2000 instructions if only the PC is traced (on devices that include trace memory)
- Program address trigger to start tracing
- Trace windowing, that is, only trace when the PC is within a given range
- Two modes for handling trace buffer full: continuous (overwriting the oldest trace data) or break when trace buffer is full

9.5 Single Wire Viewer Interface

The SWV interface is closely associated with SWD but can also be used independently. SWV data is output on the JTAG interface's TDO pin. If using SWV, you must configure the device for SWD, not JTAG. SWV is not supported with the JTAG interface.

SWV is ideal for application debug where it is helpful for the firmware to output data similar to 'printf' debugging on PCs. The SWV is ideal for data monitoring, because it requires only a single pin and can output data in standard UART format or Manchester encoded format. For example, it can be used to tune a PID control loop in which the output and graphing of the three error terms greatly simplifies coefficient tuning.

The following features are supported in SWV:

- 32 virtual channels, each 32 bits long
- Simple, efficient packing and serializing protocol
- Supports standard UART format (N81)

9.6 Programming Features

The JTAG and SWD interfaces provide full programming support. The entire device can be erased, programmed, and verified. You can increase flash protection levels to protect firmware IP. Flash protection can only be reset after a full device erase. Individual flash blocks can be erased, programmed, and verified, if block security settings permit.

9.7 Device Security

PSoC 3 offers an advanced security feature called device security, which permanently disables all test, programming, and debug ports, protecting your application from external access. The device security is activated by programming a 32-bit key (0×50536F43) to a Write Once Latch (WOL).

The Write Once Latch is a type of nonvolatile latch (NVL). The cell itself is an NVL with additional logic wrapped around it. Each WOL device contains four bytes (32 bits) of data. The wrapper outputs a '1' if a super-majority (28 of 32) of its bits match a pre-determined pattern (0×50536F43); it outputs a '0' if this majority is not reached. When the output is 1, the Write Once NV latch locks the part out of Debug and Test modes; it also permanently gates off the ability to erase or alter the contents of the latch. Matching all bits is intentionally not required, so that single (or few) bit failures do not deassert the WOL output. The state of the NVL bits after wafer processing is truly random with no tendency toward 1 or 0.

The WOL only locks the part after the correct 32-bit key (0×50536F43) is loaded into the NVL's volatile memory, programmed into the NVL's nonvolatile cells, and the part is reset. The output of the WOL is only sampled on reset and used to disable the access. This precaution prevents anyone from reading, erasing, or altering the contents of the internal memory.

The user can write the key into the WOL to lock out external access only if no flash protection is set (see "Flash Security" on page 24). However, after setting the values in the WOL, a user still has access to the part until it is reset. Therefore, a user can write the key into the WOL, program the flash protection data, and then reset the part to lock it.

If the device is protected with a WOL setting, Cypress cannot perform failure analysis and, therefore, cannot accept RMAs from customers. The WOL can be read out via SWD port to electrically identify protected parts. The user can write the key in WOL to lock out external access only if no flash protection is set. For more information on how to take full advantage of the security features in PSoC see the PSoC 3 TRM.

Disclaimer

Note the following details of the flash code protection features on Cypress devices.

Cypress products meet the specifications contained in their particular Cypress datasheets. Cypress believes that its family of products is one of the most secure families of its kind on the market today, regardless of how they are used. There may be methods, unknown to Cypress, that can breach the code protection features. Any of these methods, to our knowledge, would be dishonest and possibly illegal. Neither Cypress nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Cypress is willing to work with the customer who is concerned about the integrity of their code. Code protection is constantly evolving. We at Cypress are committed to continuously improving the code protection features of our products.

11.2 Device Level Specifications

Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

11.2.1 Device Level Specifications

Table 11-2. DC Specifications

Parameter	Description	Conditions		Min	Typ[22]	Max	Units
V_{DDA}	Analog supply voltage and input to analog core regulator	Analog core regulator enabled		1.8	–	5.5	V
V_{DDA}	Analog supply voltage, analog regulator bypassed	Analog core regulator disabled		1.71	1.8	1.89	V
V_{DDD}	Digital supply voltage relative to V_{SSD}	Digital core regulator enabled		1.8	–	V_{DDA}[18]	V
				–	–	V_{DDA} + 0.1[24]	
V_{DDD}	Digital supply voltage, digital regulator bypassed	Digital core regulator disabled		1.71	1.8	1.89	V
V_{DDIO}[19]	I/O supply voltage relative to V_{SSIO}			1.71	–	V_{DDA}[18]	V
				–	–	V_{DDA} + 0.1[24]	
V_{CCA}	Direct analog core voltage input (Analog regulator bypass)	Analog core regulator disabled		1.71	1.8	1.89	V
V_{CCD}	Direct digital core voltage input (Digital regulator bypass)	Digital core regulator disabled		1.71	1.8	1.89	V
I_{DD} [20, 21]	**Active Mode**						
	Only IMO and CPU clock enabled. CPU executing simple loop from instruction buffer.	V_{DDX} = 2.7 V – 5.5 V; F_{CPU} = 6 MHz[23]	T = –40 °C	–	1.2	2.9	mA
			T = 25 °C	–	1.2	3.1	
			T = 85 °C	–	4.9	7.7	
	IMO enabled, bus clock and CPU clock enabled. CPU executing program from flash.	V_{DDX} = 2.7 V – 5.5 V; F_{CPU} = 3 MHz[23]	T = –40 °C	–	1.3	2.9	
			T = 25 °C	–	1.6	3.2	
			T = 85 °C	–	4.8	7.5	
		V_{DDX} = 2.7 V – 5.5 V; F_{CPU} = 6 MHz	T = –40 °C	–	2.1	3.7	
			T = 25 °C	–	2.3	3.9	
			T = 85 °C	–	5.6	8.5	
		V_{DDX} = 2.7 V – 5.5 V; F_{CPU} = 12 MHz[23]	T = –40 °C	–	3.5	5.2	
			T = 25 °C	–	3.8	5.5	
			T = 85 °C	–	7.1	9.8	
		V_{DDX} = 2.7 V – 5.5 V; F_{CPU} = 24 MHz[23]	T = –40 °C	–	6.3	8.1	
			T = 25 °C	–	6.6	8.3	
			T = 85 °C	–	10	13	
		V_{DDX} = 2.7 V – 5.5 V; F_{CPU} = 48 MHz[23]	T = –40 °C	–	11.5	13.5	
			T = 25 °C	–	12	14	
			T = 85 °C	–	15.5	18.5	

Notes

18. The power supplies can be brought up in any sequence however once stable V_{DDA} must be greater than or equal to all other supplies.
19. The V_{DDIO} supply voltage must be greater than the maximum voltage on the associated GPIO pins. Maximum voltage on GPIO pin ≤ V_{DDIO} ≤ V_{DDA}.
20. Total current for all power domains: digital (I_{DDD}), analog (I_{DDA}), and I/Os ($I_{DDIO0, 1, 2, 3}$). Boost not included. All I/Os floating.
21. The current consumption of additional peripherals that are implemented only in programmed logic blocks can be found in their respective datasheets, available in PSoC Creator, the integrated design environment. To estimate total current, find the CPU current at the frequency of interest and add peripheral currents for your particular system from the device datasheet and component datasheets.
22. V_{DDX} = 3.3 V.
23. Based on device characterizations (Not production tested).
24. Guaranteed by design, not production tested.

Table 11-2. DC Specifications *(continued)*

Parameter	Description	Conditions		Min	Typ[22]	Max	Units
	Sleep Mode[25]						
	CPU = OFF RTC = ON (= ECO32K ON, in low-power mode) Sleep timer = ON (= ILO ON at 1 kHz)[26] WDT = OFF I^2C Wake = OFF Comparator = OFF POR = ON Boost = OFF SIO pins in single ended input, unregulated output mode	$V_{DD} = V_{DDIO}$ = 4.5 V - 5.5 V	T = –40 °C	–	1.1	2.3	µA
			T = 25 °C	–	1.1	2.2	
			T = 85 °C	–	15	30	
		$V_{DD} = V_{DDIO}$ = 2.7 V – 3.6 V	T = –40 °C	–	1	2.2	
			T = 25 °C	–	1	2.1	
			T = 85 °C	–	12	28	
		$V_{DD} = V_{DDIO}$ = 1.71 V – 1.95 V[27]	T = 25 °C	–	2.2	4.2	
	Comparator = ON CPU = OFF RTC = OFF Sleep timer = OFF WDT = OFF I^2C Wake = OFF POR = ON Boost = OFF SIO pins in single ended input, unregulated output mode	$V_{DD} = V_{DDIO}$ = 2.7 V – 3.6 V[28]	T = 25 °C	–	2.2	2.7	
	I^2C Wake = ON CPU = OFF RTC = OFF Sleep timer = OFF WDT = OFF Comparator = OFF POR = ON Boost = OFF SIO pins in single ended input, unregulated output mode	$V_{DD} = V_{DDIO}$ = 2.7 V – 3.6 V[28]	T = 25 °C	–	2.2	2.8	
	Hibernate Mode[25]						
	Hibernate mode current All regulators and oscillators off SRAM retention GPIO interrupts are active Boost = OFF SIO pins in single ended input, unregulated output mode	$V_{DD} = V_{DDIO}$ = 4.5 V - 5.5 V	T = –40 °C	–	0.2	1.5	µA
			T = 25 °C	–	0.5	1.5	
			T = 85 °C	–	4.1	5.3	
		$V_{DD} = V_{DDIO}$ = 2.7 V – 3.6 V	T = –40 °C	–	0.2	1.5	
			T = 25 °C	–	0.2	1.5	
			T = 85 °C	–	3.2	4.2	
		$V_{DD} = V_{DDIO}$ = 1.71 V – 1.95 V[27]	T = –40 °C	–	0.2	1.5	
			T = 25 °C	–	0.3	1.5	
			T = 85 °C	–	3.3	4.3	
I_{DDAR}	Analog current consumption while device is reset[29]	$V_{DDA} \leq 3.6$ V		–	0.3	0.6	mA
		$V_{DDA} > 3.6$ V		–	1.4	3.3	mA
I_{DDDR}	Digital current consumption while device is reset[29]	$V_{DDD} \leq 3.6$ V		–	1.1	3.1	mA
		$V_{DDD} > 3.6$ V		–	0.7	3.1	mA

11.3 Power Regulators

Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

11.3.1 Digital Core Regulator

Table 11-4. Digital Core Regulator DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{DDD}	Input voltage		1.8	–	5.5	V
V_{CCD}	Output voltage		–	1.80	–	V
	Regulator output capacitor	±10%, X5R ceramic or better. The two V_{CCD} pins must be shorted together, with as short a trace as possible, see Power System on page 31	0.9	1	1.1	µF

Figure 11-5. Regulators V_{CC} vs V_{DD}

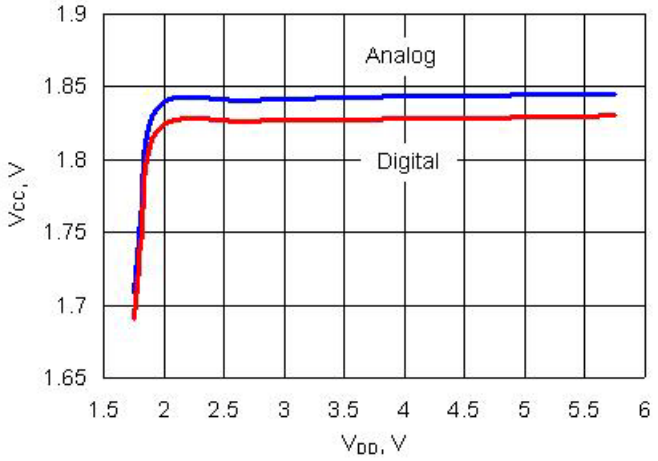
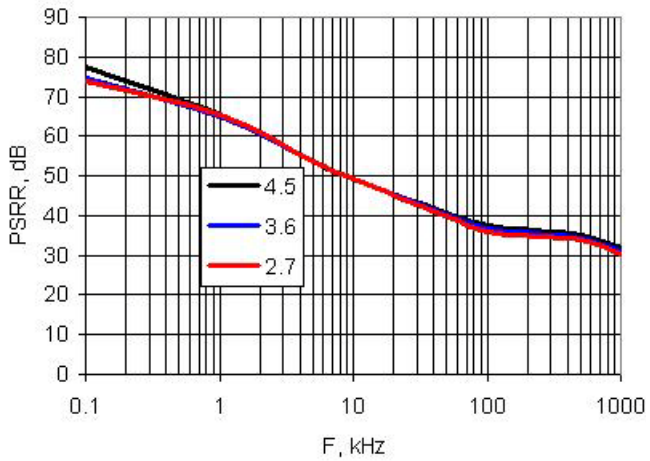


Figure 11-6. Digital Regulator PSRR vs Frequency and V_{DD}



11.3.2 Analog Core Regulator

Table 11-5. Analog Core Regulator DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{DDA}	Input voltage		1.8	–	5.5	V
V_{CCA}	Output voltage		–	1.80	–	V
	Regulator output capacitor	±10%, X5R ceramic or better	0.9	1	1.1	µF

Figure 11-7. Analog Regulator PSRR vs Frequency and V_{DD}

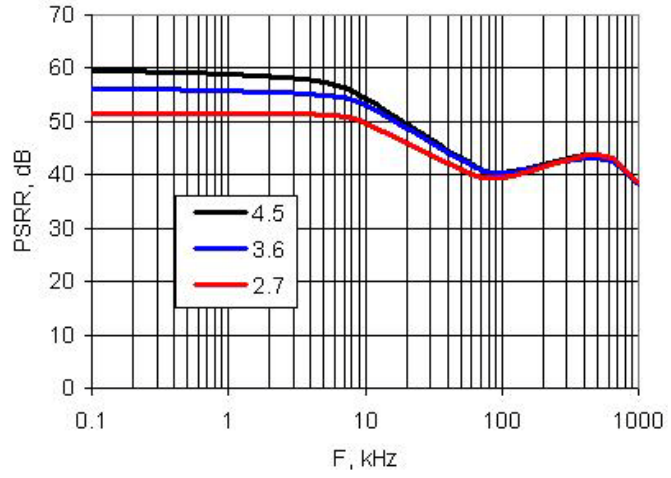


Table 11-7. Recommended External Components for Boost Circuit

Parameter	Description	Conditions	Min	Typ	Max	Units
L_{BOOST}	Boost inductor	4.7 µH nominal	3.7	4.7	5.7	µH
		10 µH nominal	8.0	10.0	12.0	µH
		22 µH nominal	17.0	22.0	27.0	µH
C_{BOOST}	Total capacitance sum of V_{DDD}, V_{DDA}, V_{DDIO}[34]		17.0	26.0	31.0	µF
C_{BAT}	Battery filter capacitor		17.0	22.0	27.0	µF
I_F	Schottky diode average forward current		1.0	–	–	A
V_R	Schottky reverse voltage		20.0	–	–	V

Figure 11-8. T_A range over V_{BAT} and V_{OUT}

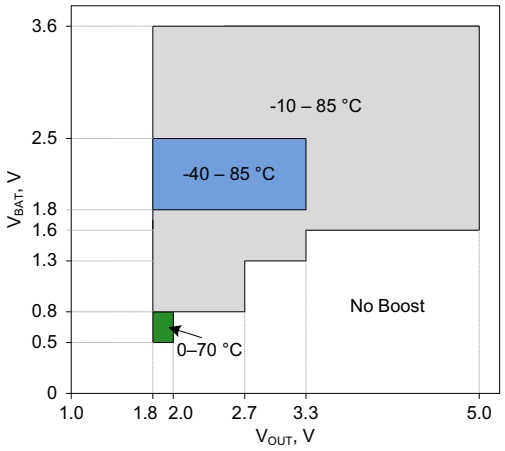


Figure 11-9. I_{OUT} range over V_{BAT} and V_{OUT}

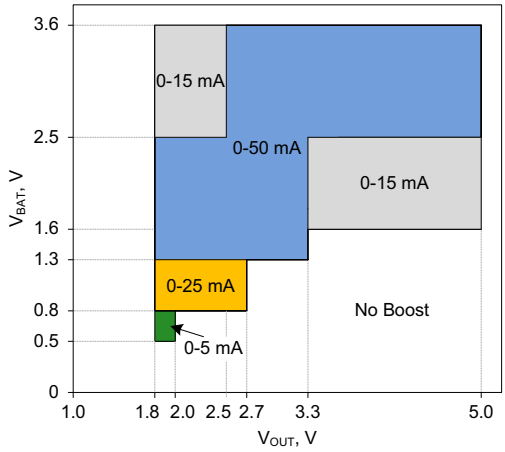
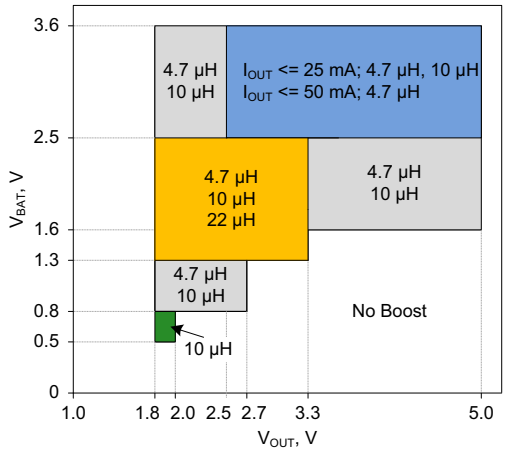


Figure 11-10. L_{BOOST} values over V_{BAT} and V_{OUT}



Note
34. Based on device characterization (Not production tested).

Figure 11-11. Efficiency vs V_{BAT}, L_{BOOST} = 4.7 µH [35]

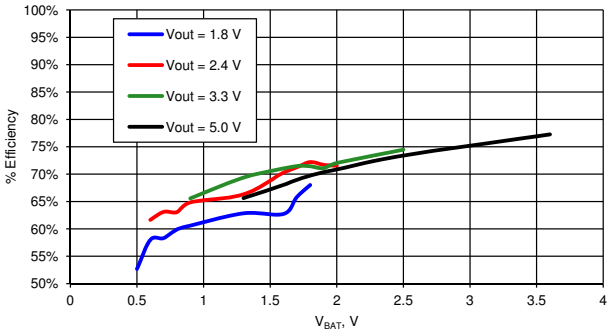


Figure 11-12. Efficiency vs V_{BAT}, L_{BOOST} = 10 µH [35]

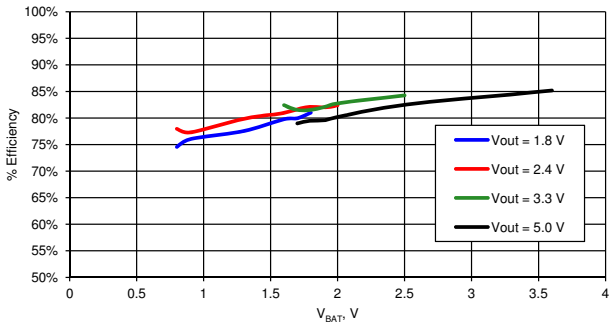


Figure 11-13. Efficiency vs V_{BAT}, L_{BOOST} = 22 µH [35]

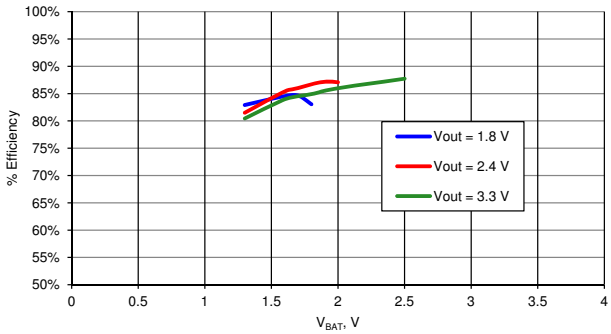
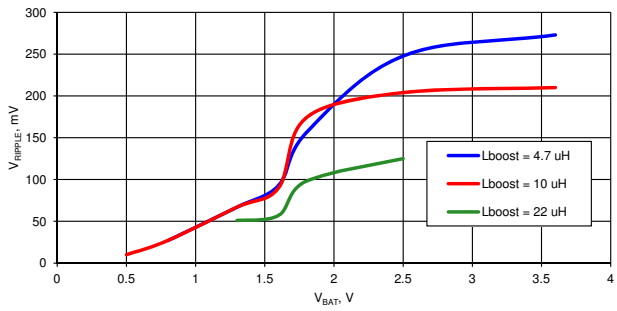


Figure 11-14. V_{RIPPLE} vs V_{BAT} [35]



Note
35. Typical example. Actual values may vary depending on external component selection, PCB layout, and other design parameters.

V_{DDD} = 3.3 V, 25 pF Load

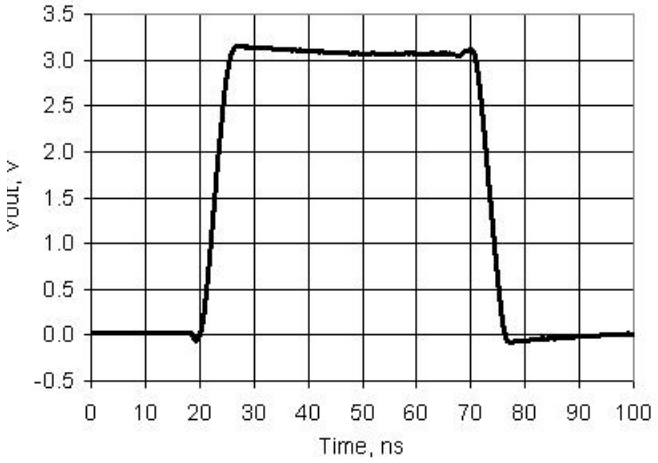


Table 11-16. USB Driver AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Tr	Transition rise time		–	–	20	ns
Tf	Transition fall time		–	–	20	ns
TR	Rise/fall time matching	V_{USB_5}, $V_{USB\_3.3}$, see USB DC Specifications on page 98	90%	–	111%	
Vcrs	Output signal crossover voltage		1.3	–	2	V

11.4.4 XRES

Table 11-17. XRES DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{IH}	Input voltage high threshold		0.7 × V_{DDIO}	–	–	V
V_{IL}	Input voltage low threshold		–	–	0.3 × V_{DDIO}	V
Rpullup	Pull-up resistor		3.5	5.6	8.5	kΩ
C_{IN}	Input capacitance[43]		–	3	–	pF
V_H	Input voltage hysteresis (Schmitt-Trigger)[43]		–	100	–	mV
Idiode	Current through protection diode to V_{DDIO} and V_{SSIO}		–	–	100	µA

Table 11-18. XRES AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
T_{RESET}	Reset pulse width		1	–	–	µs

Note
43. Based on device characterization (Not production tested).

Table 11-26. IDAC DC Specifications *(continued)*

Parameter	Description	Conditions	Min	Typ	Max	Units
I_{DD}	Operating current, code = 0	Low speed mode, source mode, range = 31.875 µA	–	44	100	µA
		Low speed mode, source mode, range = 255 µA,	–	33	100	µA
		Low speed mode, source mode, range = 2.04 mA	–	33	100	µA
		Low speed mode, sink mode, range = 31.875 µA	–	36	100	µA
		Low speed mode, sink mode, range = 255 µA	–	33	100	µA
		Low speed mode, sink mode, range = 2.04 mA	–	33	100	µA
		High speed mode, source mode, range = 31.875 µA	–	310	500	µA
		High speed mode, source mode, range = 255 µA	–	305	500	µA
		High speed mode, source mode, range = 2.04 mA	–	305	500	µA
		High speed mode, sink mode, range = 31.875 µA	–	310	500	µA
		High speed mode, sink mode, range = 255 µA	–	300	500	µA
		High speed mode, sink mode, range = 2.04 mA	–	300	500	µA

Figure 11-26. IDAC INL vs Input Code, Range = 255 µA, Source Mode

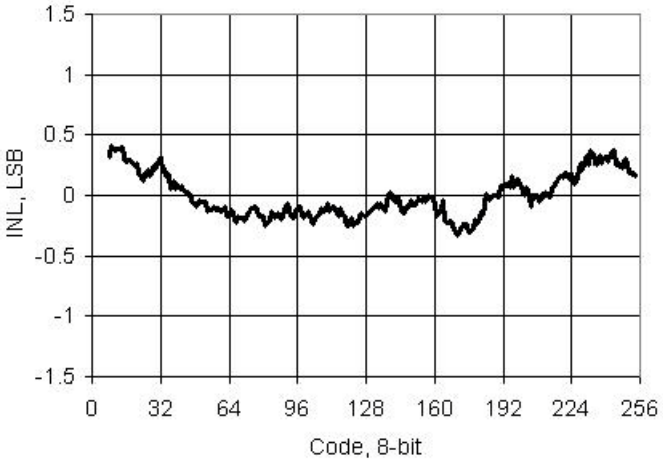


Figure 11-27. IDAC INL vs Input Code, Range = 255 µA, Sink Mode

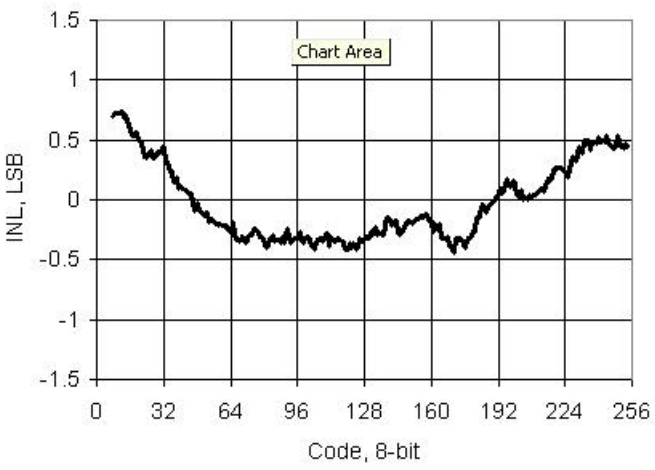


Table 11-27. IDAC AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
F_{DAC}	Update rate		–	–	8	Msps
T_{SETTLE}	Settling time to 0.5 LSB	Range = 31.875 µA or 255 µA, full scale transition, High speed mode, 600 Ω 15-pF load	–	–	125	ns
	Current noise	Range = 255 µA, source mode, High speed mode, V_{DDA} = 5 V, 10 kHz	–	340	–	pA/sqrtHz

Figure 11-36. IDAC Step Response, Codes 0x40 - 0xC0, 255 µA Mode, Source Mode, High speed mode, V_{DDA} = 5 V

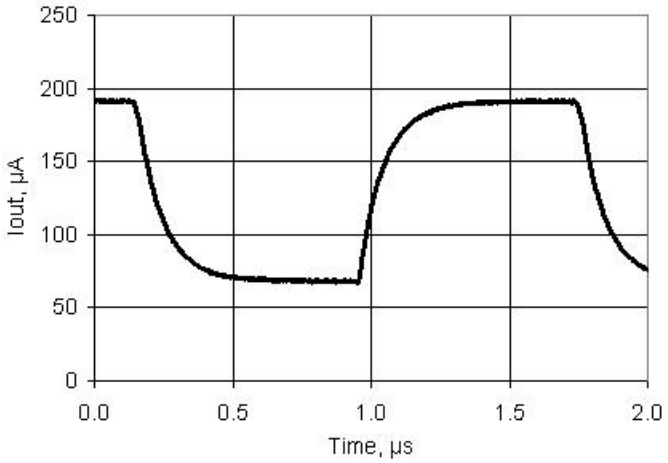


Figure 11-37. IDAC Glitch Response, Codes 0x7F - 0x80, 255 µA Mode, Source Mode, High speed mode, V_{DDA} = 5 V

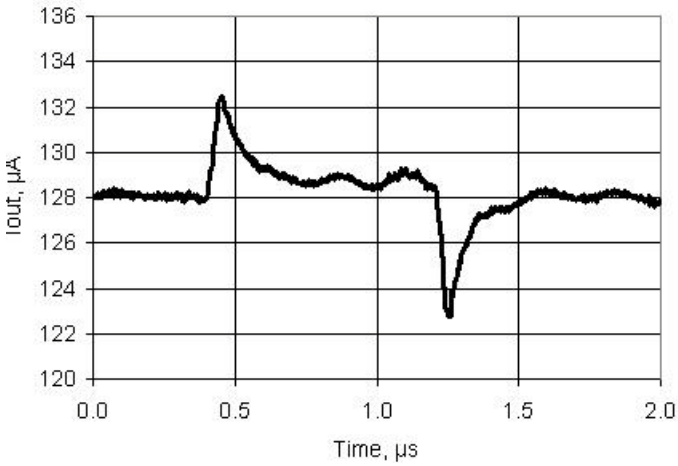


Figure 11-38. IDAC PSRR vs Frequency

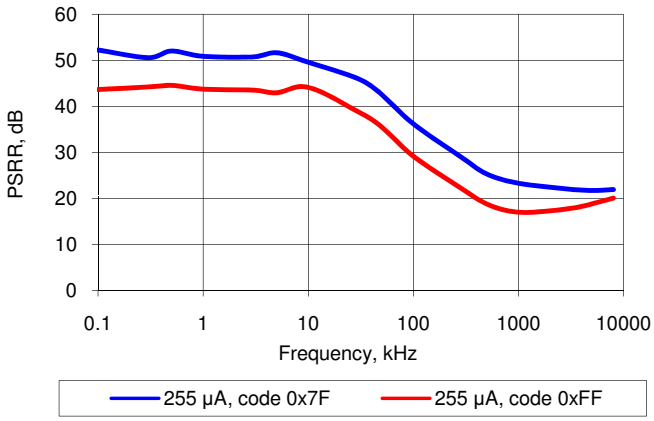


Figure 11-39. IDAC Current Noise, 255 µA Mode, Source Mode, High speed mode, V_{DDA} = 5 V

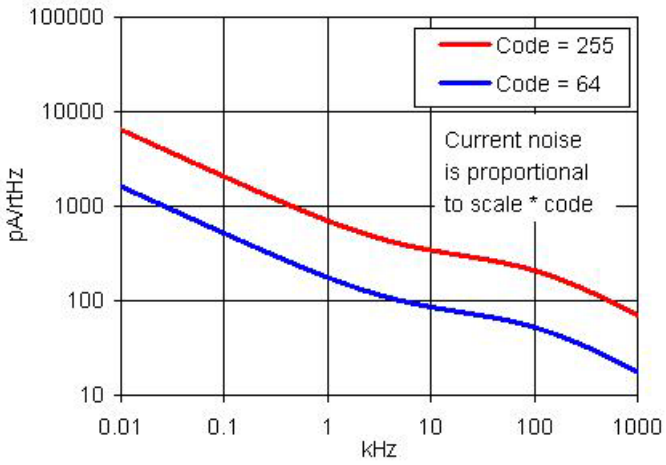


Figure 11-54. Synchronous Write and Read Cycle Timing, No Wait States

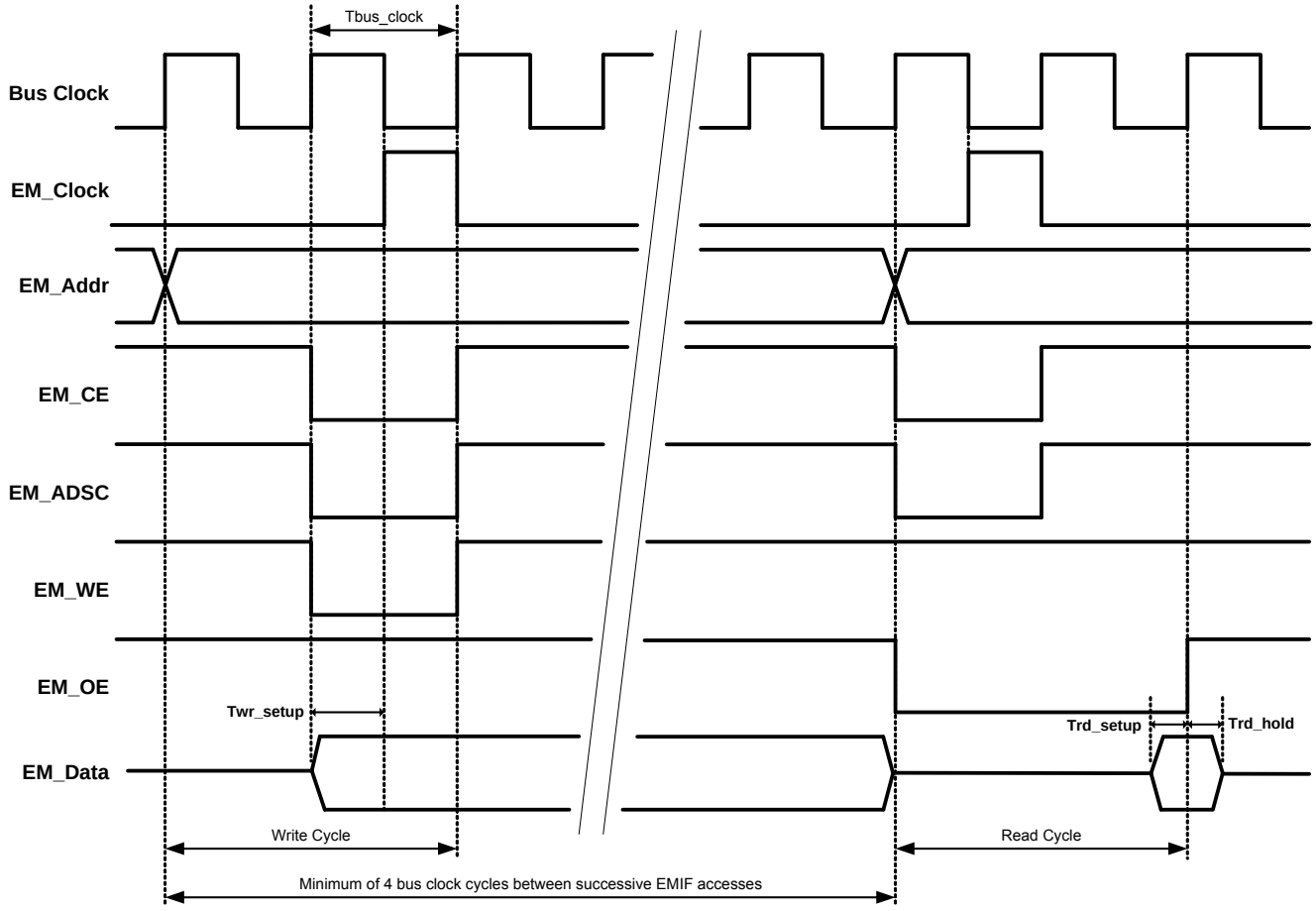


Table 11-54. Synchronous Write and Read Timing Specifications[59]

Parameter	Description	Conditions	Min	Typ	Max	Units
Fbus_clock	Bus clock frequency[60]		–	–	33	MHz
Tbus_clock	Bus clock period[61]		30.3	–	–	ns
Twr_Setup	Time from EM_data valid to rising edge of EM_Clock		Tbus_clock – 10	–	–	ns
Trd_setup	Time that EM_data must be valid before rising edge of EM_OE		5	–	–	ns
Trd_hold	Time that EM_data must be valid after rising edge of EM_OE		5	–	–	ns

Notes
59. Based on device characterization (Not production tested).
60. EMIF signal timings are limited by GPIO frequency limitations. See "GPIO" section on page 76.
61. EMIF output signals are generally synchronized to bus clock, so EMIF signal timings are dependent on bus clock frequency.

11.8.5 SWD Interface

Figure 11-58. SWD Interface Timing

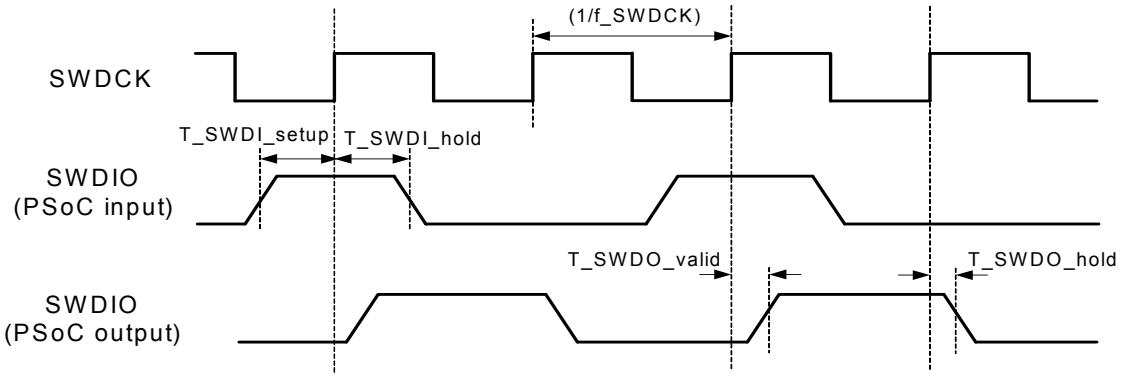


Table 11-63. SWD Interface AC Specifications[67]

Parameter	Description	Conditions	Min	Typ	Max	Units
f_SWDCK	SWDCLK frequency	3.3 V ≤ V_{DDD} ≤ 5 V	–	–	14[68]	MHz
		1.71 V ≤ V_{DDD} < 3.3 V	–	–	7[68]	MHz
		1.71 V ≤ V_{DDD} < 3.3 V, SWD over USBIO pins	–	–	5.5[68]	MHz
T_SWDI_setup	SWDIO input setup before SWDCK high	T = 1/f_SWDCK max	T/4	–	–	
T_SWDI_hold	SWDIO input hold after SWDCK high	T = 1/f_SWDCK max	T/4	–	–	
T_SWDO_valid	SWDCK high to SWDIO output	T = 1/f_SWDCK max	–	–	2T/5	

11.8.6 SWV Interface

Table 11-64. SWV Interface AC Specifications[30]

Parameter	Description	Conditions	Min	Typ	Max	Units
	SWV mode SWV bit rate		–	–	33	Mbit

11.9 Clocking

Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

11.9.1 Internal Main Oscillator

Table 11-65. IMO DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Supply current					
	24 MHz – USB mode	With oscillator locking to USB bus	–	–	500	µA
	24 MHz – non USB mode		–	–	300	µA
	12 MHz		–	–	200	µA
	6 MHz		–	–	180	µA
	3 MHz		–	–	150	µA

Notes
67. Based on device characterization (Not production tested).
68. f_SWDCK must also be no more than 1/3 CPU clock frequency.

11.9.4 kHz External Crystal Oscillator

Table 11-71. kHzECO DC Specifications[72]

Parameter	Description	Conditions	Min	Typ	Max	Units
I_{CC}	Operating current	Low-power mode; CL = 6 pF	–	0.25	1.0	µA
DL	Drive level		–	–	1	µW

Table 11-72. kHzECO AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
F	Frequency		–	32.768	–	kHz
T_{ON}	Startup time	High power mode	–	1	–	s

11.9.5 External Clock Reference

Table 11-73. External Clock Reference AC Specifications[72]

Parameter	Description	Conditions	Min	Typ	Max	Units
	External frequency range		0	–	33	MHz
	Input duty cycle range	Measured at $V_{DDIO}/2$	30	50	70	%
	Input edge rate	V_{IL} to V_{IH}	0.5	–	–	V/ns

11.9.6 Phase–Locked Loop

Table 11-74. PLL DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
I_{DD}	PLL operating current	In = 3 MHz, Out = 24 MHz	–	200	–	µA

Table 11-75. PLL AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Fpllin	PLL input frequency[73]		1	–	48	MHz
	PLL intermediate frequency[74]	Output of prescaler	1	–	3	MHz
Fpllout	PLL output frequency[73]		24	–	50	MHz
	Lock time at startup		–	–	250	µs
Jperiod-rms	Jitter (rms)[72]		–	–	250	ps

Notes
72. Based on device characterization (Not production tested).
73. This specification is guaranteed by testing the PLL across the specified range using the IMO as the source for the PLL.
74. PLL input divider, Q, must be set so that the input frequency is divided down to the intermediate frequency range. Value for Q ranges from 1 to 16.

Description Title: PSoC® 3: CY8C32 Family Data Sheet Programmable System-on-Chip (PSoC®) *(continued)* Document Number: 001-56955				
Revision	**ECN**	**Submission Date**	**Orig. of Change**	**Description of Change**
*D	2938381	05/27/10	MKEA	Replaced V_{DDIO} with V_{DDD} in USBIO diagram and specification tables, added text in USBIO section of Electrical Specifications. Added Table 13-2 (Package MSL) Modified Tstorag condition and changed max spec to 100 Added bullet (Pass) under ALU (section 7.2.2.2) Added figures for kHzECO and MHzECO in the External Oscillator section Updated Figure 6-1(Clocking Subsystem diagram) Removed CPUCLK_DIV in table 5-2, Deleted Clock Divider SFR subsection Updated PSoC Creator Framework image Updated SIO DC Specifications (V_{IH} and V_{IL} parameters) Updated bullets in Clocking System and Clocking Distribution sections Updated Figure 8-2 Updated Table 11-10 Updated PCB Layout and Schematic, updated as per MTRB review comments Updated Table 6-3 (power changed to current) In 32kHZ EC DC Specifications table, changed I_{CC} Max to 0.25 In IMO DC Specifications table, updated Supply Current values Updated GPIO DC Specs table Modified to support a maximum 50MHz CPU speed
*E	2958674	06/22/10	SHEA	Minor ECN to post datasheet to external website
*F	2989685	08/04/10	MKEA	Added USBIO 22 ohm DP and DM resistors to Simplified Block Diagram Added to Table 6-6 a footnote and references to same. Added sentences to the resistive pull-up and pull-down description bullets. Added sentence to Section 6.4.11, Adjustable Output Level. Updated section 5.5 External Memory Interface Updated Table 11-73 JTAG Interface AC Specifications Updated Table 11-74 SWD Interface AC Specifications
*G	3078568	11/04/10	MKEA	Updated "Current Digital-to-analog Converter (IDAC)" on page 87 Updated "Voltage Digital to Analog Converter (VDAC)" on page 92 Updated Table 11-2, "DC Specifications," on page 68
*H	3107314	12/10/2010	MKEA	Updated delta-sigma tables and graphs. Updated Flash AC specs Formatted table 11.2. Updated interrupt controller table Updated transimpedance amplifier section Updated SIO DC specs table Updated Voltage Monitors DC Specifications table Updated LCD Direct Drive DC specs table Updated ESD_{HBM} value. Updated IDAC and VDAC sections Removed ESO parts from ordering information Changed USBIO pins from NC to DNU and removed redundant USBIO pin description notes Updated POR with brown out DC and AC specs Updated 32 kHz External Crystal DC Specifications Updated XRES IO specs Updated Inductive boost regulator section Delta sigma ADC spec updates Updated comparator section Removed buzz mode from Power Mode Transition diagram
*I	3179219	02/22/2011	MKEA	Updated conditions for flash data retention time. Updated 100-pin TQFP package spec. Updated EEPROM AC specifications.