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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	50MHz
Connectivity	EBI/EMI, I ² C, LINbus, SPI, UART/USART
Peripherals	CapSense, DMA, POR, PWM, WDT
Number of I/O	25
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 16x12b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c3244lti-123

Figure 2-6. 100-pin TQFP Part Pinout

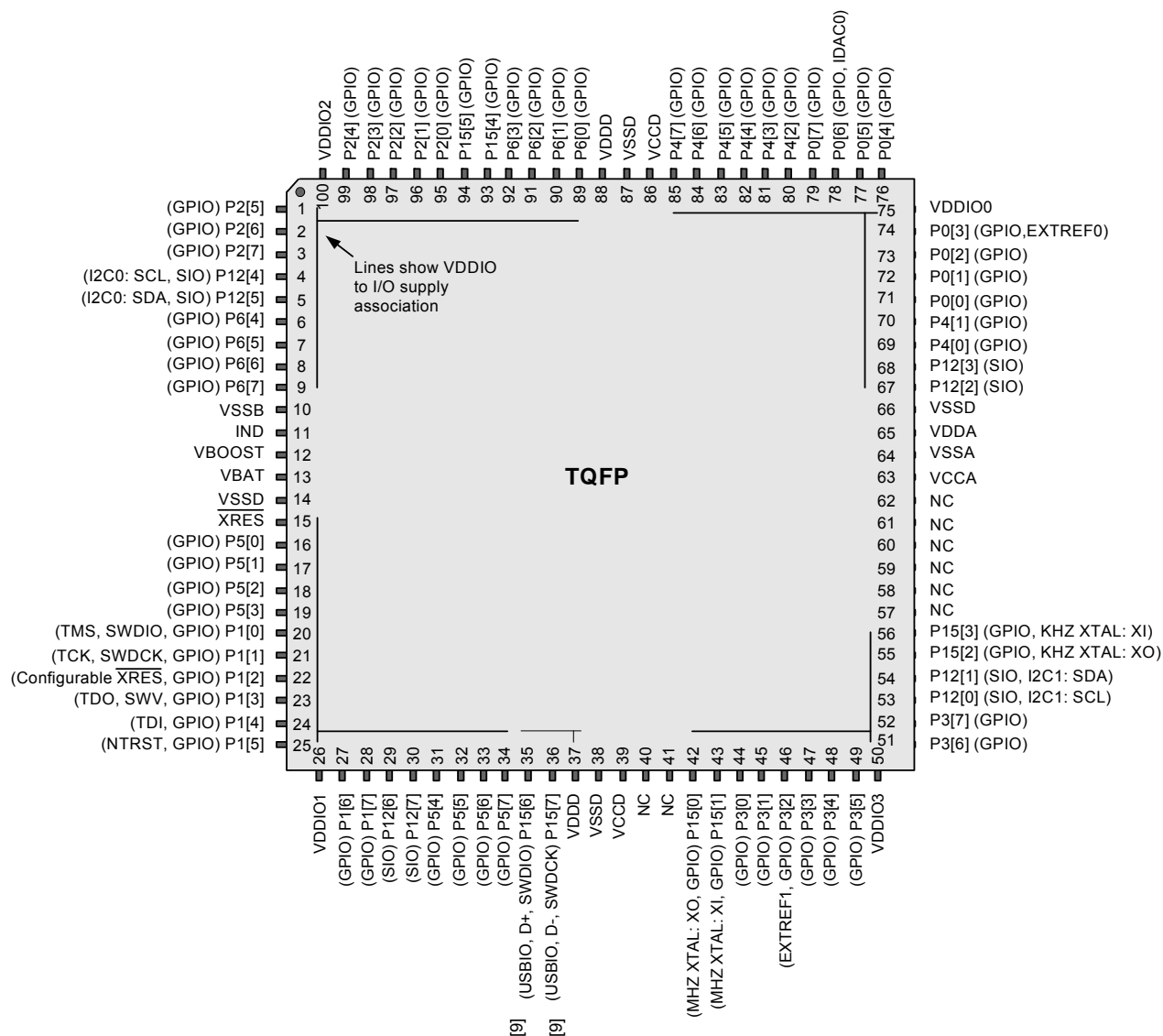


Table 2-1. VDDIO and Port Pin Associations

VDDIO	Port Pins
VDDIO0	P0[7:0], P4[7:0], P12[3:2]
VDDIO1	P1[7:0], P5[7:0], P12[7:6]
VDDIO2	P2[7:0], P6[7:0], P12[5:4], P15[5:4]
VDDIO3	P3[7:0], P12[1:0], P15[3:0]
VDDD	P15[7:6] (USB D+, D-)

Note

9. Pins are Do Not Use (DNU) on devices without USB. The pin must be left floating.

4.3 Instruction Set

The 8051 instruction set is highly optimized for 8-bit handling and Boolean operations. The types of instructions supported include:

- Arithmetic instructions
- Logical instructions
- Data transfer instructions
- Boolean instructions
- Program branching instructions

4.3.1 Instruction Set Summary

4.3.1.1 Arithmetic Instructions

Arithmetic instructions support the direct, indirect, register, immediate constant, and register-specific instructions. Arithmetic modes are used for addition, subtraction, multiplication, division, increment, and decrement operations. [Table 4-1](#) lists the different arithmetic instructions.

Table 4-1. Arithmetic Instructions

Mnemonic	Description	Bytes	Cycles
ADD A,Rn	Add register to accumulator	1	1
ADD A,Direct	Add direct byte to accumulator	2	2
ADD A,@Ri	Add indirect RAM to accumulator	1	2
ADD A,#data	Add immediate data to accumulator	2	2
ADDC A,Rn	Add register to accumulator with carry	1	1
ADDC A,Direct	Add direct byte to accumulator with carry	2	2
ADDC A,@Ri	Add indirect RAM to accumulator with carry	1	2
ADDC A,#data	Add immediate data to accumulator with carry	2	2
SUBB A,Rn	Subtract register from accumulator with borrow	1	1
SUBB A,Direct	Subtract direct byte from accumulator with borrow	2	2
SUBB A,@Ri	Subtract indirect RAM from accumulator with borrow	1	2
SUBB A,#data	Subtract immediate data from accumulator with borrow	2	2
INC A	Increment accumulator	1	1
INC Rn	Increment register	1	2
INC Direct	Increment direct byte	2	3
INC @Ri	Increment indirect RAM	1	3
DEC A	Decrement accumulator	1	1
DEC Rn	Decrement register	1	2
DEC Direct	Decrement direct byte	2	3
DEC @Ri	Decrement indirect RAM	1	3
INC DPTR	Increment data pointer	1	1
MUL	Multiply accumulator and B	1	2
DIV	Divide accumulator by B	1	6
DAA	Decimal adjust accumulator	1	3

4.3.1.3 Data Transfer Instructions

The data transfer instructions are of three types: the core RAM, xdata RAM, and the lookup tables. The core RAM transfer includes transfer between any two core RAM locations or SFRs. These instructions can use direct, indirect, register, and immediate addressing. The xdata RAM transfer includes only the transfer between the accumulator and the xdata RAM location. It can use only indirect addressing. The lookup tables involve nothing but the read of program memory using the Indexed

addressing mode. [Table 4-3](#) lists the various data transfer instructions available.

4.3.1.4 Boolean Instructions

The 8051 core has a separate bit-addressable memory location. It has 128 bits of bit addressable RAM and a set of SFRs that are bit addressable. The instruction set includes the whole menu of bit operations such as move, set, clear, toggle, OR, and AND instructions and the conditional jump instructions. [Table 4-4](#) on page 17 [Table 4-4](#) lists the available Boolean instructions.

Table 4-3. Data Transfer Instructions

Mnemonic	Description	Bytes	Cycles
MOV A,Rn	Move register to accumulator	1	1
MOV A,Direct	Move direct byte to accumulator	2	2
MOV A,@Ri	Move indirect RAM to accumulator	1	2
MOV A,#data	Move immediate data to accumulator	2	2
MOV Rn,A	Move accumulator to register	1	1
MOV Rn,Direct	Move direct byte to register	2	3
MOV Rn, #data	Move immediate data to register	2	2
MOV Direct, A	Move accumulator to direct byte	2	2
MOV Direct, Rn	Move register to direct byte	2	2
MOV Direct, Direct	Move direct byte to direct byte	3	3
MOV Direct, @Ri	Move indirect RAM to direct byte	2	3
MOV Direct, #data	Move immediate data to direct byte	3	3
MOV @Ri, A	Move accumulator to indirect RAM	1	2
MOV @Ri, Direct	Move direct byte to indirect RAM	2	3
MOV @Ri, #data	Move immediate data to indirect RAM	2	2
MOV DPTR, #data16	Load data pointer with 16-bit constant	3	3
MOVC A, @A+DPTR	Move code byte relative to DPTR to accumulator	1	5
MOVC A, @A + PC	Move code byte relative to PC to accumulator	1	4
MOVX A,@Ri	Move external RAM (8-bit) to accumulator	1	4
MOVX A, @DPTR	Move external RAM (16-bit) to accumulator	1	3
MOVX @Ri, A	Move accumulator to external RAM (8-bit)	1	5
MOVX @DPTR, A	Move accumulator to external RAM (16-bit)	1	4
PUSH Direct	Push direct byte onto stack	2	3
POP Direct	Pop direct byte from stack	2	2
XCH A, Rn	Exchange register with accumulator	1	2
XCH A, Direct	Exchange direct byte with accumulator	2	3
XCH A, @Ri	Exchange indirect RAM with accumulator	1	3
XCHD A, @Ri	Exchange low order indirect digit RAM with accumulator	1	3

4.4.2 DMA Features

- 24 DMA channels
- Each channel has one or more transaction descriptors (TDs) to configure channel behavior. Up to 128 total TDs can be defined
- TDs can be dynamically updated
- Eight levels of priority per channel
- Any digitally routable signal, the CPU, or another DMA channel, can trigger a transaction
- Each channel can generate up to two interrupts per transfer
- Transactions can be stalled or canceled
- Supports transaction size of infinite or 1 to 64k bytes
- TDs may be nested and/or chained for complex transactions

4.4.3 Priority Levels

The CPU always has higher priority than the DMA controller when their accesses require the same bus resources. Due to the system architecture, the CPU can never starve the DMA. DMA channels of higher priority (lower priority number) may interrupt current DMA transfers. In the case of an interrupt, the current transfer is allowed to complete its current transaction. To ensure latency limits when multiple DMA accesses are requested simultaneously, a fairness algorithm guarantees an interleaved minimum percentage of bus bandwidth for priority levels 2 through 7. Priority levels 0 and 1 do not take part in the fairness algorithm and may use 100 percent of the bus bandwidth. If a tie occurs on two DMA requests of the same priority level, a simple round robin method is used to evenly share the allocated bandwidth. The round robin allocation can be disabled for each DMA channel, allowing it to always be at the head of the line. Priority levels 2 to 7 are guaranteed the minimum bus bandwidth shown in [Table 4-7](#) after the CPU and DMA priority levels 0 and 1 have satisfied their requirements.

Table 4-7. Priority Levels

Priority Level	% Bus Bandwidth
0	100.0
1	100.0
2	50.0
3	25.0
4	12.5
5	6.2
6	3.1
7	1.5

When the fairness algorithm is disabled, DMA access is granted based solely on the priority level; no bus bandwidth guarantees are made.

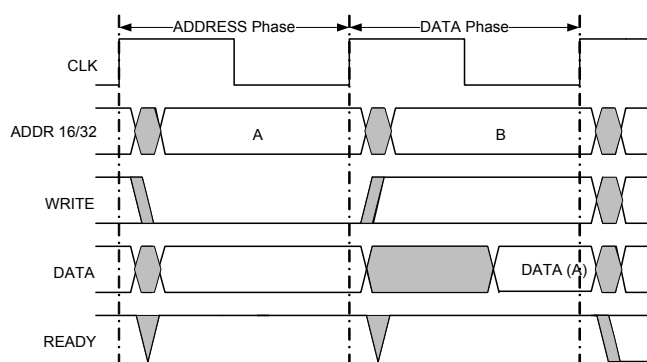
4.4.4 Transaction Modes Supported

The flexible configuration of each DMA channel and the ability to chain multiple channels allow the creation of both simple and complex use cases. General use cases include, but are not limited to:

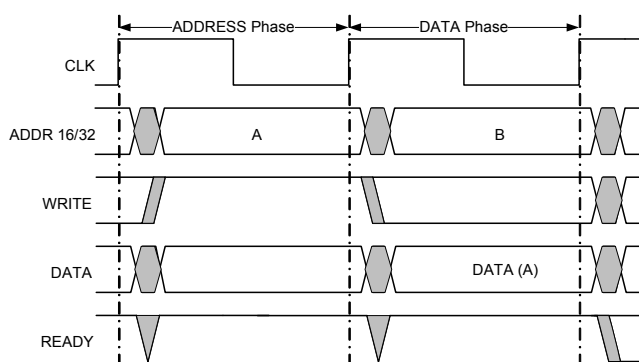
4.4.4.1 Simple DMA

In a simple DMA case, a single TD transfers data between a source and sink (peripherals or memory location). The basic timing diagrams of DMA read and write cycles are shown in [Figure 4-1](#). For more description on other transfer modes, refer to the Technical Reference Manual.

Figure 4-1. DMA Timing Diagram



Basic DMA Read Transfer without wait states



Basic DMA Write Transfer without wait states

4.4.4.2 Auto Repeat DMA

Auto repeat DMA is typically used when a static pattern is repetitively read from system memory and written to a peripheral. This is done with a single TD that chains to itself.

4.4.4.3 Ping Pong DMA

A ping pong DMA case uses double buffering to allow one buffer to be filled by one client while another client is consuming the

data previously received in the other buffer. In its simplest form, this is done by chaining two TDs together so that each TD calls the opposite TD when complete.

4.4.4.4 Circular DMA

Circular DMA is similar to ping pong DMA except it contains more than two buffers. In this case there are multiple TDs; after the last TD is complete it chains back to the first TD.

Figure 4-3. Interrupt Structure

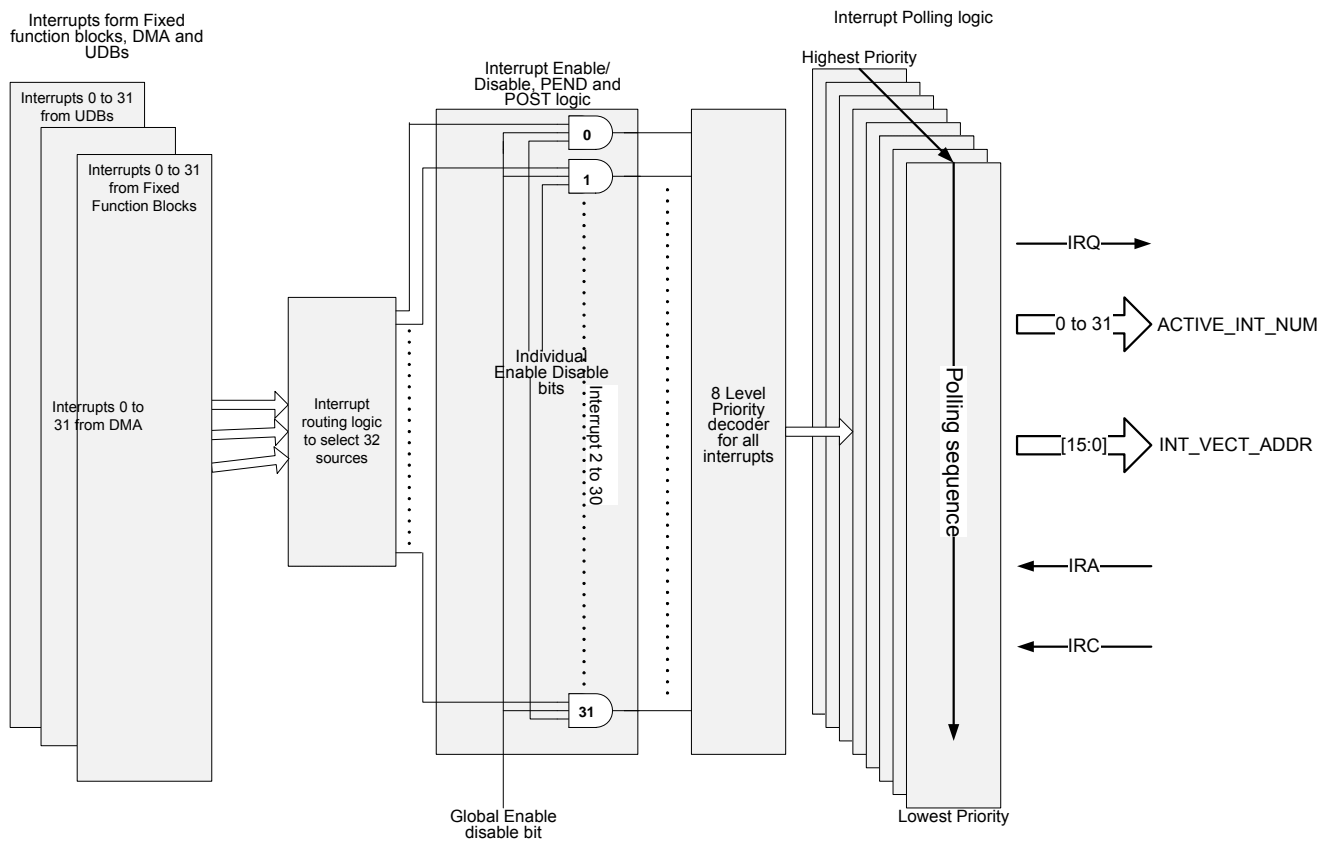


Table 4-8. Interrupt Vector Table

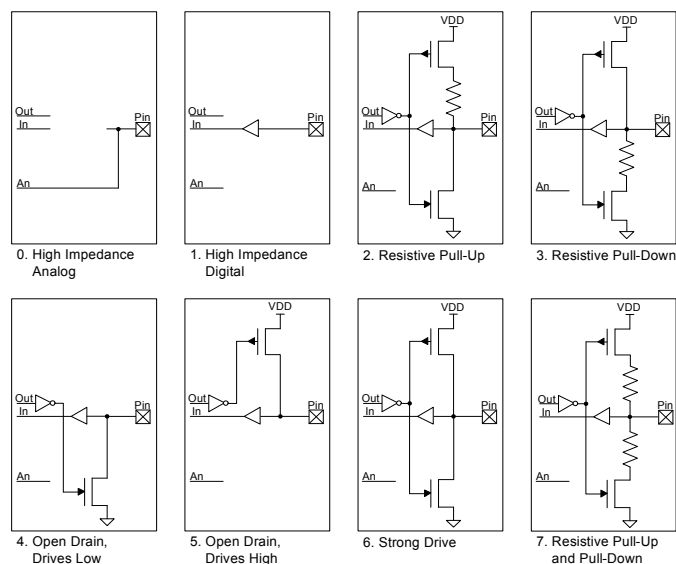
#	Fixed Function	DMA	UDB
0	LVD	phub_termout0[0]	udb_intr[0]
1	Cache/ECC	phub_termout0[1]	udb_intr[1]
2	Reserved	phub_termout0[2]	udb_intr[2]
3	Sleep (Pwr Mgr)	phub_termout0[3]	udb_intr[3]
4	PICU[0]	phub_termout0[4]	udb_intr[4]
5	PICU[1]	phub_termout0[5]	udb_intr[5]
6	PICU[2]	phub_termout0[6]	udb_intr[6]
7	PICU[3]	phub_termout0[7]	udb_intr[7]
8	PICU[4]	phub_termout0[8]	udb_intr[8]
9	PICU[5]	phub_termout0[9]	udb_intr[9]
10	PICU[6]	phub_termout0[10]	udb_intr[10]
11	PICU[12]	phub_termout0[11]	udb_intr[11]
12	PICU[15]	phub_termout0[12]	udb_intr[12]
13	Comparators Combined	phub_termout0[13]	udb_intr[13]
14	Reserved	phub_termout0[14]	udb_intr[14]
15	I ² C	phub_termout0[15]	udb_intr[15]
16	Reserved	phub_termout1[0]	udb_intr[16]
17	Timer/Counter0	phub_termout1[1]	udb_intr[17]
18	Timer/Counter1	phub_termout1[2]	udb_intr[18]
19	Timer/Counter2	phub_termout1[3]	udb_intr[19]
20	Timer/Counter3	phub_termout1[4]	udb_intr[20]
21	USB SOF Int	phub_termout1[5]	udb_intr[21]
22	USB Arb Int	phub_termout1[6]	udb_intr[22]
23	USB Bus Int	phub_termout1[7]	udb_intr[23]
24	USB Endpoint[0]	phub_termout1[8]	udb_intr[24]
25	USB Endpoint Data	phub_termout1[9]	udb_intr[25]
26	Reserved	phub_termout1[10]	udb_intr[26]
27	LCD	phub_termout1[11]	udb_intr[27]
28	Reserved	phub_termout1[12]	udb_intr[28]
29	Decimator Int	phub_termout1[13]	udb_intr[29]
30	PHUB Error Int	phub_termout1[14]	udb_intr[30]
31	EEPROM Fault Int	phub_termout1[15]	udb_intr[31]

- Input or output or both for CPU and DMA
- Eight drive modes
- Every pin can be an interrupt source configured as rising edge, falling edge or both edges. If required, level sensitive interrupts are supported through the DSI
- Dedicated port interrupt vector for each port
- Slew rate controlled digital output drive mode
- Access port control and configuration registers on either port basis or pin basis
- Separate port read (PS) and write (DR) data registers to avoid read modify write errors
- Special functionality on a pin by pin basis
- Additional features only provided on the GPIO pins:
 - LCD segment drive on LCD equipped devices
 - CapSense
 - Analog input and output capability
 - Continuous 100 μ A clamp current capability
- Standard drive strength down to 1.7 V
- Additional features only provided on SIO pins:
 - Higher drive strength than GPIO
 - Hot swap capability (5 V tolerance at any operating V_{DD})
 - Programmable and regulated high input and output drive levels down to 1.2 V
 - No analog input, CapSense, or LCD capability
 - Overvoltage tolerance up to 5.5 V
 - SIO can act as a general purpose analog comparator
- USBIO features:
 - Full speed USB 2.0 compliant I/O
 - Highest drive strength for general purpose use
 - Input, output, or both for CPU and DMA
 - Input, output, or both for digital peripherals
 - Digital output (CMOS) drive mode
 - Each pin can be an interrupt source configured as rising edge, falling edge, or both edges

6.4.1 Drive Modes

Each GPIO and SIO pin is individually configurable into one of the eight drive modes listed in Table 6-6. Three configuration bits are used for each pin (DM[2:0]) and set in the PRTxDM[2:0] registers. Figure 6-12 depicts a simplified pin view based on each of the eight drive modes. Table 6-6 shows the I/O pin's drive state based on the port data register value or digital array signal if bypass mode is selected. Note that the actual I/O pin voltage is determined by a combination of the selected drive mode and the load at the pin. For example, if a GPIO pin is configured for resistive pull-up mode and driven high while the pin is floating, the voltage measured at the pin is a high logic state. If the same GPIO pin is externally tied to ground then the voltage unmeasured at the pin is a low logic state.

Figure 6-12. Drive Mode



The 'Out' connection is driven from either the Digital System (when the Digital Output terminal is connected) or the Data Register (when HW connection is disabled).
The 'In' connection drives the Pin State register, and the Digital System if the Digital Input terminal is enabled and connected.
The 'An' connection connects to the Analog System.

Table 6-6. Drive Modes

Diagram	Drive Mode	PRTxDM2	PRTxDM1	PRTxDM0	PRTxDR = 1	PRTxDR = 0
0	High impedance analog	0	0	0	High Z	High Z
1	High Impedance digital	0	0	1	High Z	High Z
2	Resistive pull-up ^[12]	0	1	0	Res High (5K)	Strong Low
3	Resistive pull-down ^[12]	0	1	1	Strong High	Res Low (5K)
4	Open drain, drives low	1	0	0	High Z	Strong Low
5	Open drain, drive high	1	0	1	Strong High	High Z
6	Strong drive	1	1	0	Strong High	Strong Low
7	Resistive pull-up and pull-down ^[12]	1	1	1	Res High (5K)	Res Low (5K)

Note

¹². Resistive pull-up and pull-down are not available with SIO in regulated output mode.

6.4.5 Pin Interrupts

All GPIO and SIO pins are able to generate interrupts to the system. All eight pins in each port interface to their own Port Interrupt Control Unit (PICU) and associated interrupt vector. Each pin of the port is independently configurable to detect rising edge, falling edge, both edge interrupts, or to not generate an interrupt.

Depending on the configured mode for each pin, each time an interrupt event occurs on a pin, its corresponding status bit of the interrupt status register is set to “1” and an interrupt request is sent to the interrupt controller. Each PICU has its own interrupt vector in the interrupt controller and the pin status register providing easy determination of the interrupt source down to the pin level.

Port pin interrupts remain active in all sleep modes allowing the PSoC device to wake from an externally generated interrupt.

While level sensitive interrupts are not directly supported; Universal Digital Blocks (UDB) provide this functionality to the system when needed.

6.4.6 Input Buffer Mode

GPIO and SIO input buffers can be configured at the port level for the default CMOS input thresholds or the optional LVTTTL input thresholds. All input buffers incorporate Schmitt triggers for input hysteresis. Additionally, individual pin input buffers can be disabled in any drive mode.

6.4.7 I/O Power Supplies

Up to four I/O pin power supplies are provided depending on the device and package. Each I/O supply must be less than or equal to the voltage on the chip’s analog (VDDA) pin. This feature allows users to provide different I/O voltage levels for different pins on the device. Refer to the specific device package pinout to determine VDDIO capability for a given port and pin.

The SIO port pins support an additional regulated high output capability, as described in [Adjustable Output Level](#).

6.4.8 Analog Connections

These connections apply only to GPIO pins. All GPIO pins may be used as analog inputs or outputs. The analog voltage present on the pin must not exceed the VDDIO supply voltage to which the GPIO belongs. Each GPIO may connect to one of the analog global busses or to one of the analog mux buses to connect any pin to any internal analog resource such as ADC or comparators. In addition, one select pin provides direct connection to the high current DAC.

6.4.9 CapSense

This section applies only to GPIO pins. All GPIO pins may be used to create CapSense buttons and sliders. See the “[CapSense](#)” section on page 61 for more information.

6.4.10 LCD Segment Drive

This section applies only to GPIO pins. All GPIO pins may be used to generate Segment and Common drive signals for direct glass drive of LCD glass. See the “[LCD Direct Drive](#)” section on page 60 for details.

6.4.11 Adjustable Output Level

This section applies only to SIO pins. SIO port pins support the ability to provide a regulated high output level for interface to external signals that are lower in voltage than the SIO’s respective VDDIO. SIO pins are individually configurable to output either the standard VDDIO level or the regulated output, which is based on an internally generated reference. Typically the voltage DAC (VDAC) is used to generate the reference (see [Figure 6-13](#)). The “[DAC](#)” section on page 61 has more details on VDAC use and reference routing to the SIO pins. Resistive pull-up and pull-down drive modes are not available with SIO in regulated output mode.

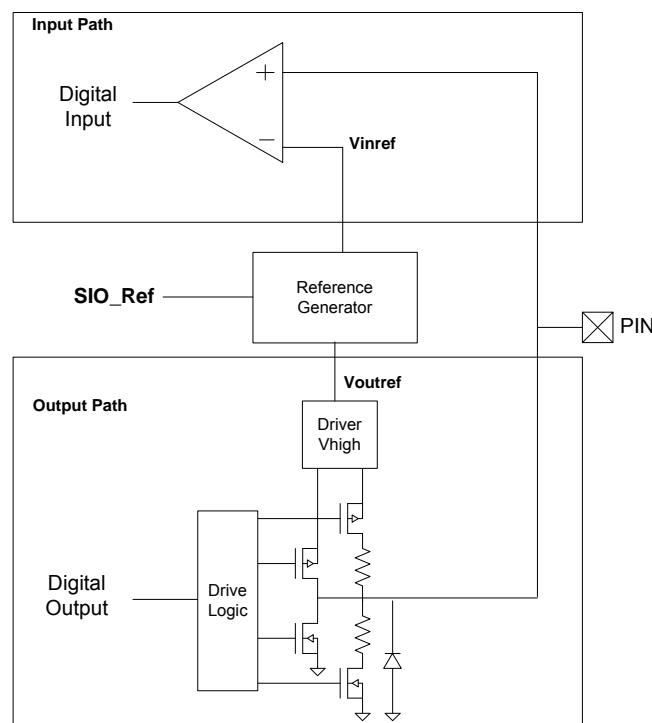
6.4.12 Adjustable Input Level

This section applies only to SIO pins. SIO pins by default support the standard CMOS and LVTTTL input levels but also support a differential mode with programmable levels. SIO pins are grouped into pairs. Each pair shares a reference generator block which, is used to set the digital input buffer reference level for interface to external signals that differ in voltage from VDDIO. The reference sets the pins voltage threshold for a high logic level (see [Figure 6-13](#)). Available input thresholds are:

- $0.5 \times VDDIO$
- $0.4 \times VDDIO$
- $0.5 \times VREF$
- $VREF$

Typically the voltage DAC (VDAC) generates the V_{REF} reference. The “[DAC](#)” section on page 61 has more details on VDAC use and reference routing to the SIO pins.

Figure 6-13. SIO Reference for Input and Output



6.4.13 SIO as Comparator

This section applies only to SIO pins. The adjustable input level feature of the SIOs as explained in the [Adjustable Input Level](#) section can be used to construct a comparator. The threshold for the comparator is provided by the SIO's reference generator. The reference generator has the option to set the analog signal routed through the analog global line as threshold for the comparator. Note that a pair of SIO pins share the same threshold.

The digital input path in [Figure 6-10](#) on page 40 illustrates this functionality. In the figure, 'Reference level' is the analog signal routed through the analog global. The hysteresis feature can also be enabled for the input buffer of the SIO, which increases noise immunity for the comparator.

6.4.14 Hot Swap

This section applies only to SIO pins. SIO pins support 'hot swap' capability to plug into an application without loading the signals that are connected to the SIO pins even when no power is applied to the PSoC device. This allows the unpowered PSoC to maintain a high impedance load to the external device while also preventing the PSoC from being powered through a SIO pin's protection diode.

Powering the device up or down while connected to an operational I²C bus may cause transient states on the SIO pins. The overall I²C bus design should take this into account.

6.4.15 Over Voltage Tolerance

All I/O pins provide an over voltage tolerance feature at any operating VDD.

- There are no current limitations for the SIO pins as they present a high impedance load to the external circuit where $V_{DDIO} < V_{IN} \leq 5.5 \text{ V}$.
- The GPIO pins must be limited to 100 μA using a current limiting resistor. GPIO pins clamp the pin voltage to approximately one diode above the VDDIO supply where $V_{DDIO} < V_{IN} < V_{DDA}$.
- In case of a GPIO pin configured for analog input/output, the analog voltage on the pin must not exceed the VDDIO supply voltage to which the GPIO belongs.

A common application for this feature is connection to a bus such as I²C where different devices are running from different supply voltages. In the I²C case, the PSoC chip is configured into the Open Drain, Drives Low mode for the SIO pin. This allows an external pull-up to pull the I²C bus voltage above the PSoC pin supply. For example, the PSoC chip could operate at 1.8 V, and an external device could run from 5 V. Note that the SIO pin's V_{IH} and V_{IL} levels are determined by the associated V_{DDIO} supply pin.

The SIO pin must be in one of the following modes: 0 (high impedance analog), 1 (high impedance digital), or 4 (open drain drives low). See [Figure 6-12](#) for details. Absolute maximum ratings for the device must be observed for all I/O pins.

6.4.16 Reset Configuration

While reset is active all I/Os are reset to and held in the High Impedance Analog state. After reset is released, the state can be reprogrammed on a port-by-port basis to pull-down or pull-up. To ensure correct reset operation, the port reset configuration data is stored in special nonvolatile registers. The stored reset data is automatically transferred to the port reset configuration registers at reset release.

6.4.17 Low-Power Functionality

In all low-power modes the I/O pins retain their state until the part is awakened and changed or reset. To awaken the part, use a pin interrupt, because the port interrupt logic continues to function in all low-power modes.

6.4.18 Special Pin Functionality

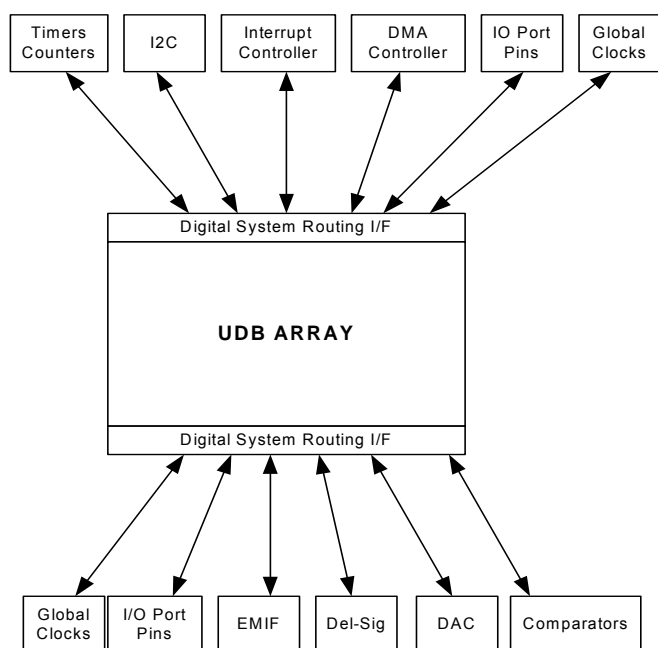
Some pins on the device include additional special functionality in addition to their GPIO or SIO functionality. The specific special function pins are listed in [Pinouts](#) on page 6. The special features are:

- Digital
 - 4- to 25- MHz crystal oscillator
 - 32.768-kHz crystal oscillator
 - Wake from sleep on I²C address match. Any pin can be used for I²C if wake from sleep is not required.
 - JTAG interface pins
 - SWD interface pins
 - SWV interface pins
 - External reset
- Analog
 - High current IDAC output
 - External reference inputs

6.4.19 JTAG Boundary Scan

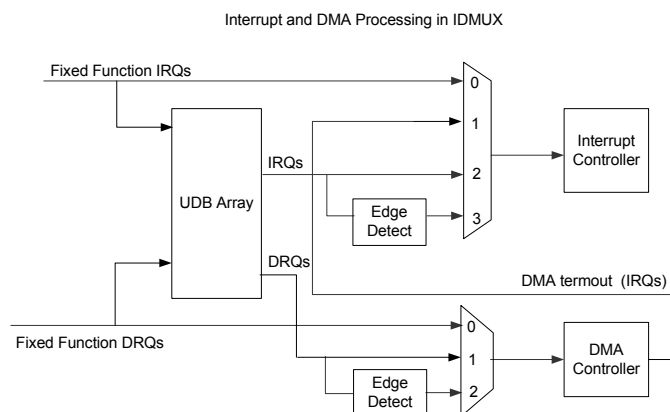
The device supports standard JTAG boundary scan chains on all I/O pins for board level test.

Figure 7-9. Digital System Interconnect



Interrupt and DMA routing is very flexible in the CY8C32 programmable architecture. In addition to the numerous fixed function peripherals that can generate interrupt requests, any data signal in the UDB array routing can also be used to generate a request. A single peripheral may generate multiple independent interrupt requests simplifying system and firmware design. Figure 7-10 shows the structure of the IDMUX (Interrupt/DMA Multiplexer).

Figure 7-10. Interrupt and DMA Processing in the IDMUX



7.4.1 I/O Port Routing

There are a total of 20 DSI routes to a typical 8-bit I/O port, 16 for data and four for drive strength control.

When an I/O pin is connected to the routing, there are two primary connections available, an input and an output. In

conjunction with drive strength control, this can implement a bidirectional I/O pin. A data output signal has the option to be single synchronized (pipelined) and a data input signal has the option to be double synchronized. The synchronization clock is the master clock (see Figure 6-1). Normally all inputs from pins are synchronized as this is required if the CPU interacts with the signal or any signal derived from it. Asynchronous inputs have rare uses. An example of this is a feed through of combinational PLD logic from input pins to output pins.

Figure 7-11. I/O Pin Synchronization Routing

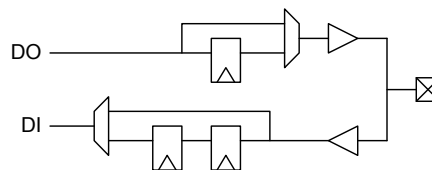
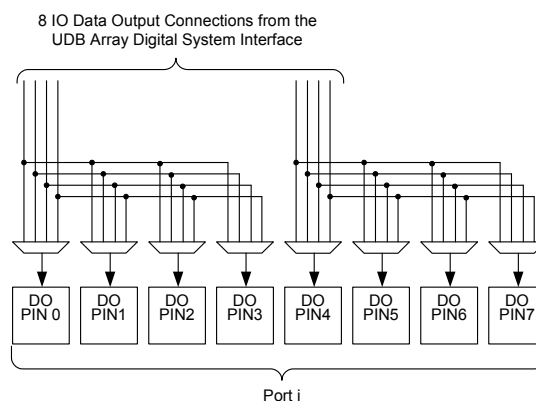
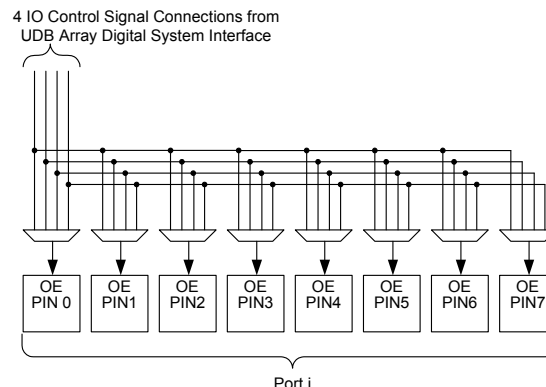


Figure 7-12. I/O Pin Output Connectivity



There are four more DSI connections to a given I/O port to implement dynamic output enable control of pins. This connectivity gives a range of options, from fully ganged 8-bits controlled by one signal, to up to four individually controlled pins. The output enable signal is useful for creating tri-state bidirectional pins and buses.

Figure 7-13. I/O Pin Output Enable Connectivity



7.7 I²C

PSoC includes a single fixed-function I²C peripheral. Additional I²C interfaces can be instantiated using Universal Digital Blocks (UDBs) in PSoC Creator, as required.

The I²C peripheral provides a synchronous two-wire interface designed to interface the PSoC device with a two-wire I²C serial communication bus. It is compatible^[13] with I²C Standard-mode, Fast-mode, and Fast-mode Plus devices as defined in the NXP I²C-bus specification and user manual (UM10204). The I²C bus I/O may be implemented with GPIO or SIO in open-drain modes.

To eliminate the need for excessive CPU intervention and overhead, I²C specific support is provided for status detection and generation of framing bits. I²C operates as a slave, a master, or multimaster (Slave and Master)^[14]. In slave mode, the unit always listens for a start condition to begin sending or receiving data. Master mode supplies the ability to generate the Start and Stop conditions and initiate transactions. Multimaster mode provides clock synchronization and arbitration to allow multiple masters on the same bus. If Master mode is enabled and Slave mode is not enabled, the block does not generate interrupts on externally generated Start conditions. I²C interfaces through the DSI routing and allows direct connections to any GPIO or SIO pins.

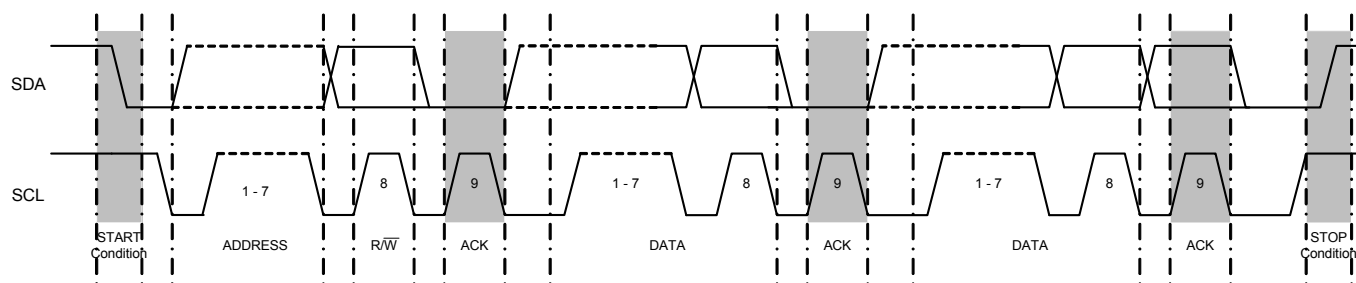
I²C provides hardware address detect of a 7-bit address without CPU intervention. Additionally the device can wake from low-power modes on a 7-bit hardware address match. If wakeup functionality is required, I²C pin connections are limited to one of two specific pairs of SIO pins. See descriptions of SCL and SDA pins in [Pin Descriptions](#) on page 12.

I²C features include:

- Slave and Master, Transmitter, and Receiver operation
- Byte processing for low CPU overhead
- Interrupt or polling CPU interface
- Support for bus speeds up to 1 Mbps
- 7 or 10-bit addressing (10-bit addressing requires firmware support)
- SMBus operation (through firmware support – SMBus supported in hardware in UDBs)
- 7-bit hardware address compare
- Wake from low-power modes on address match
- Glitch filtering (active and alternate-active modes only)

Data transfers follow the format shown in [Figure 7-16](#). After the START condition (S), a slave address is sent. This address is 7 bits long followed by an eighth bit which is a data direction bit (R/W) - a 'zero' indicates a transmission (WRITE), a 'one' indicates a request for data (READ). A data transfer is always terminated by a STOP condition (P) generated by the master.

Figure 7-16. I²C Complete Transfer Timing



7.7.1 External Electrical Connections

As [Figure 7-17](#) shows, the I²C bus requires external pull-up resistors (R_P). These resistors are primarily determined by the supply voltage, bus speed, and bus capacitance. For detailed

information on how to calculate the optimum pull-up resistor value for your design, we recommend using the UM10204 I²C-bus specification and user manual Rev 6, or newer, available from the NXP website at www.nxp.com.

Notes

13. The I²C peripheral is non-compliant with the NXP I²C specification in the following areas: analog glitch filter, I/O VOL/IOL, I/O hysteresis. The I²C Block has a digital glitch filter (not available in sleep mode). The Fast-mode minimum fall-time specification can be met by setting the I/Os to slow speed mode. See the I/O Electrical Specifications in "Inputs and Outputs" section on page 76 for details.

14. Fixed-block I²C does not support undefined bus conditions, nor does it support Repeated Start in Slave mode. These conditions should be avoided, or the UDB-based I²C component should be used instead.

8.3.2 LUT

The CY8C32 family of devices contains four LUTs. The LUT is a two input, one output lookup table that is driven by any one or two of the comparators in the chip. The output of any LUT is routed to the digital system interface of the UDB array. From the digital system interface of the UDB array, these signals can be connected to UDBs, DMA controller, I/O, or the interrupt controller.

The LUT control word written to a register sets the logic function on the output. The available LUT functions and the associated control word is shown in Table 8-2.

Table 8-2. LUT Function vs. Program Word and Inputs

Control Word	Output (A and B are LUT inputs)
0000b	FALSE ('0')
0001b	A AND B
0010b	A AND (NOT B)
0011b	A
0100b	(NOT A) AND B
0101b	B
0110b	A XOR B
0111b	A OR B
1000b	A NOR B
1001b	A XNOR B
1010b	NOT B
1011b	A OR (NOT B)
1100b	NOT A
1101b	(NOT A) OR B
1110b	A NAND B
1111b	TRUE ('1')

8.4 LCD Direct Drive

The PSoC Liquid Crystal Display (LCD) driver system is a highly configurable peripheral designed to allow PSoC to directly drive a broad range of LCD glass. All voltages are generated on chip, eliminating the need for external components. With a high multiplex ratio of up to 1/16, the CY8C32 family LCD driver system can drive a maximum of 736 segments. The PSoC LCD driver module was also designed with the conservative power budget of portable devices in mind, enabling different LCD drive modes and power down modes to conserve power.

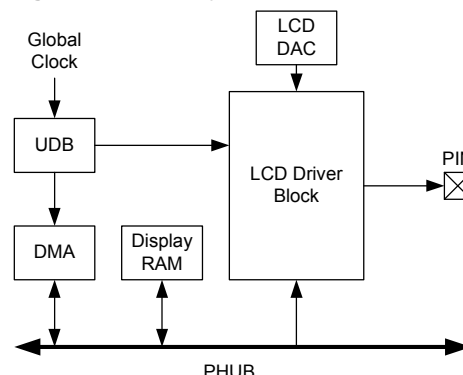
PSoC Creator provides an LCD segment drive component. The component wizard provides easy and flexible configuration of LCD resources. You can specify pins for segments and commons along with other options. The software configures the device to meet the required specifications. This is possible because of the programmability inherent to PSoC devices.

Key features of the PSoC LCD segment system are:

- LCD panel direct driving
- Type A (standard) and Type B (low-power) waveform support
- Wide operating voltage range support (2 V to 5 V) for LCD panels

- Static, 1/2, 1/3, 1/4, 1/5 bias voltage levels
- Internal bias voltage generation through internal resistor ladder
- Up to 62 total common and segment outputs
- Up to 1/16 multiplex for a maximum of 16 backplane/common outputs
- Up to 62 front plane/segment outputs for direct drive
- Drives up to 736 total segments (16 backplane × 46 front plane)
- Up to 64 levels of software controlled contrast
- Ability to move display data from memory buffer to LCD driver through DMA (without CPU intervention)
- Adjustable LCD refresh rate from 10 Hz to 150 Hz
- Ability to invert LCD display for negative image
- Three LCD driver drive modes, allowing power optimization

Figure 8-6. LCD System



8.4.1 LCD Segment Pin Driver

Each GPIO pin contains an LCD driver circuit. The LCD driver buffers the appropriate output of the LCD DAC to directly drive the glass of the LCD. A register setting determines whether the pin is a common or segment. The pin's LCD driver then selects one of the six bias voltages to drive the I/O pin, as appropriate for the display data.

8.4.2 Display Data Flow

The LCD segment driver system reads display data and generates the proper output voltages to the LCD glass to produce the desired image. Display data resides in a memory buffer in the system SRAM. Each time you need to change the common and segment driver voltages, the next set of pixel data moves from the memory buffer into the Port Data Registers via DMA.

8.4.3 UDB and LCD Segment Control

A UDB is configured to generate the global LCD control signals and clocking. This set of signals is routed to each LCD pin driver through a set of dedicated LCD global routing channels. In addition to generating the global LCD control signals, the UDB also produces a DMA request to initiate the transfer of the next frame of LCD data.

Figure 11-17. SIO Output High Voltage and Current, Unregulated Mode

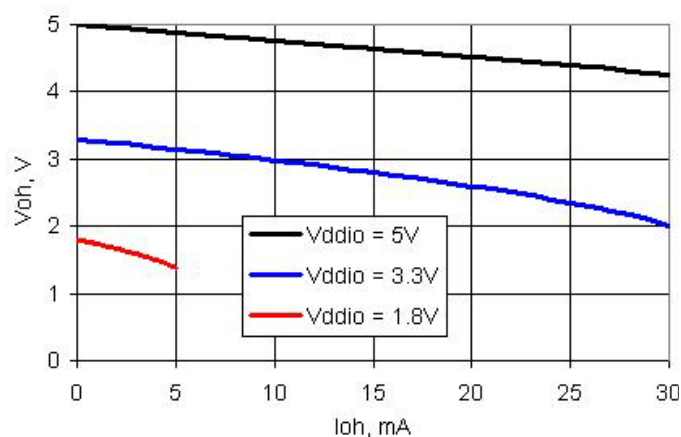


Figure 11-18. SIO Output Low Voltage and Current, Unregulated Mode

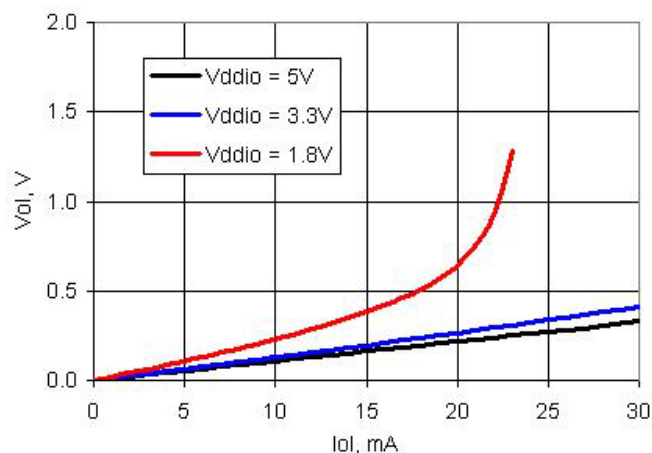


Figure 11-19. SIO Output High Voltage and Current, Regulated Mode

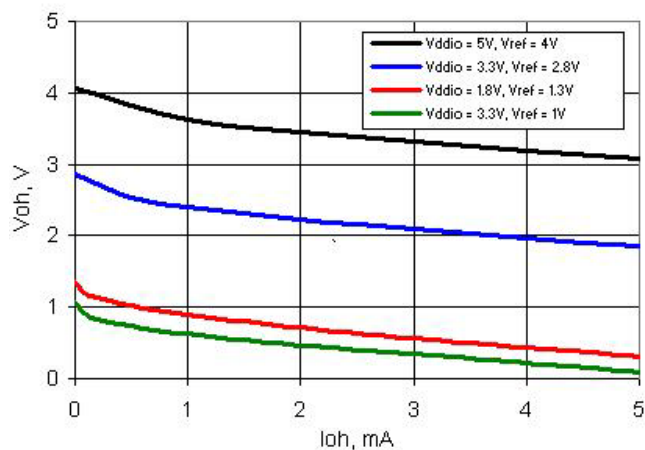


Table 11-12. SIO AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
TriseF	Rise time in Fast Strong Mode (90/10%) ^[41]	Cload = 25 pF, VDDIO = 3.3 V	–	–	12	ns
TfallF	Fall time in Fast Strong Mode (90/10%) ^[41]	Cload = 25 pF, VDDIO = 3.3 V	–	–	12	ns
TriseS	Rise time in Slow Strong Mode (90/10%) ^[41]	Cload = 25 pF, VDDIO = 3.0 V	–	–	75	ns
TfallS	Fall time in Slow Strong Mode (90/10%) ^[41]	Cload = 25 pF, VDDIO = 3.0 V	–	–	60	ns

Note

41. Based on device characterization (Not production tested).

$V_{DD} = 3.3\text{ V}$, 25 pF Load

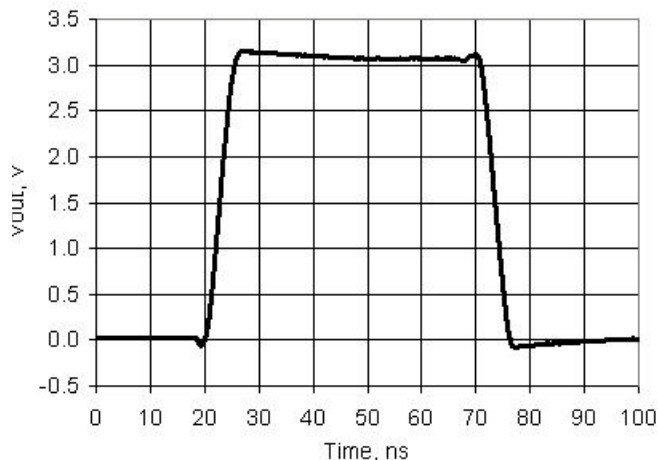


Table 11-16. USB Driver AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
T_r	Transition rise time		–	–	20	ns
T_f	Transition fall time		–	–	20	ns
TR	Rise/fall time matching	V_{USB_5} , $V_{USB_3.3}$, see USB DC Specifications on page 98	90%	–	111%	
Vcrs	Output signal crossover voltage		1.3	–	2	V

11.4.4 XRES

Table 11-17. XRES DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{IH}	Input voltage high threshold		$0.7 \times V_{DDIO}$	–	–	V
V_{IL}	Input voltage low threshold		–	–	$0.3 \times V_{DDIO}$	V
Rpullup	Pull-up resistor		3.5	5.6	8.5	k Ω
C_{IN}	Input capacitance ^[43]		–	3	–	pF
V_H	Input voltage hysteresis (Schmitt-Trigger) ^[43]		–	100	–	mV
I _{diode}	Current through protection diode to V_{DDIO} and V_{SSIO}		–	–	100	μ A

Table 11-18. XRES AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
T_{RESET}	Reset pulse width		1	–	–	μ s

Note

43. Based on device characterization (Not production tested).

11.5 Analog Peripherals

Specifications are valid for $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ and $T_J \leq 100\text{ }^{\circ}\text{C}$, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

11.5.1 Delta-sigma ADC

Unless otherwise specified, operating conditions are:

- Operation in continuous sample mode
- fclk = 6.144 MHz
- Reference = 1.024 V internal reference bypassed on P3.2 or P0.3
- Unless otherwise specified, all charts and graphs show typical values

Table 11-19. 12-bit Delta-sigma ADC DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Resolution		8	–	12	bits
	Number of channels, single ended		–	–	No. of GPIO	–
	Number of channels, differential	Differential pair is formed using a pair of GPIOs.	–	–	No. of GPIO/2	–
	Monotonic	Yes	–	–	–	–
Ge	Gain error	Buffered, buffer gain = 1, Range = $\pm 1.024\text{ V}$, $25\text{ }^{\circ}\text{C}$	–	–	± 0.2	%
Gd	Gain drift	Buffered, buffer gain = 1, Range = $\pm 1.024\text{ V}$	–	–	50	ppm/ $^{\circ}\text{C}$
Vos	Input offset voltage	Buffered, 12-bit mode	–	–	± 0.1	mV
TCVos	Temperature coefficient, input offset voltage	Buffer gain = 1, 12-bit, Range = $\pm 1.024\text{ V}$	–	–	1	$\mu\text{V}/^{\circ}\text{C}$
	Input voltage range, single ended ^[45]		V_{SSA}	–	V_{DDA}	V
	Input voltage range, differential unbuffered ^[45]		V_{SSA}	–	V_{DDA}	V
	Input voltage range, differential, buffered ^[45]		V_{SSA}	–	$V_{DDA} - 1$	V
INL12	Integral non linearity ^[45]	Range = $\pm 1.024\text{ V}$, unbuffered	–	–	± 1	LSB
DNL12	Differential non linearity ^[45]	Range = $\pm 1.024\text{ V}$, unbuffered	–	–	± 1	LSB
INL8	Integral non linearity ^[45]	Range = $\pm 1.024\text{ V}$, unbuffered	–	–	± 1	LSB
DNL8	Differential non linearity ^[45]	Range = $\pm 1.024\text{ V}$, unbuffered	–	–	± 1	LSB
Rin_Buff	ADC input resistance	Input buffer used	10	–	–	M Ω
Rin_ADC12	ADC input resistance	Input buffer bypassed, 12 bit, Range = $\pm 1.024\text{ V}$	–	148 ^[46]	–	k Ω
Rin_ExtRef	ADC external reference input resistance		–	70 ^[46, 47]	–	k Ω
Vextref	ADC external reference input voltage, see also internal reference in Voltage Reference on page 86	Pins P0[3], P3[2]	0.9	–	1.3	V
Current Consumption						
I _{DD_12}	I _{DDA} + I _{DDD} current consumption, 12 bit ^[45]	192 ksps, unbuffered	–	–	1.95	mA
I _{BUFF}	Buffer current consumption ^[45]		–	–	2.5	mA

Notes

45. Based on device characterization (not production tested).

46. By using switched capacitors at the ADC input an effective input resistance is created. Holding the gain and number of bits constant, the resistance is proportional to the inverse of the clock frequency. This value is calculated, not measured. For more information see the Technical Reference Manual.

47. Recommend an external reference device with an output impedance <100 Ω , for example, the LM185/285/385 family. A 1- μF capacitor is recommended. For more information, see [AN61290 - PSoC® 3 and PSoC 5LP Hardware Design Considerations](#).

11.8.5 SWD Interface

Figure 11-58. SWD Interface Timing

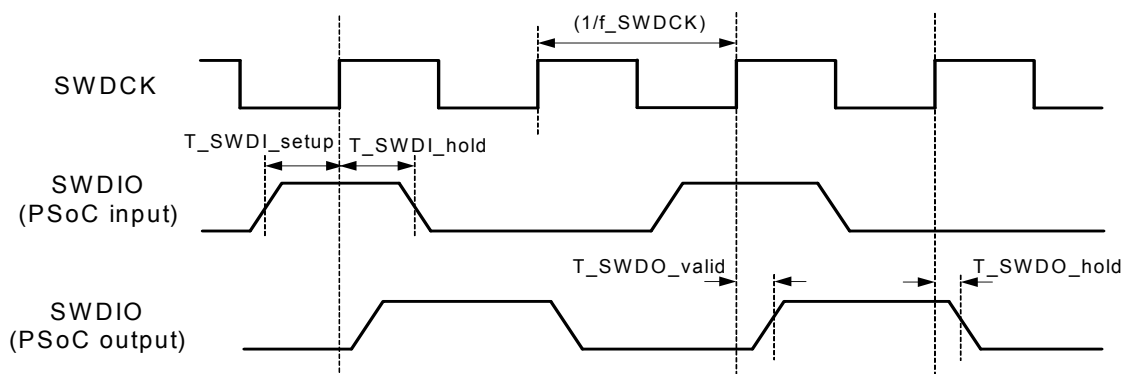


Table 11-63. SWD Interface AC Specifications^[67]

Parameter	Description	Conditions	Min	Typ	Max	Units
f_SWDCCK	SWDCLK frequency	3.3 V ≤ V _{DD} ≤ 5 V	–	–	14 ^[68]	MHz
		1.71 V ≤ V _{DD} < 3.3 V	–	–	7 ^[68]	MHz
		1.71 V ≤ V _{DD} < 3.3 V, SWD over USBIO pins	–	–	5.5 ^[68]	MHz
T_SWDI_setup	SWDIO input setup before SWDCK high	T = 1/f_SWDCCK max	T/4	–	–	
T_SWDI_hold	SWDIO input hold after SWDCK high	T = 1/f_SWDCCK max	T/4	–	–	
T_SWDO_valid	SWDCK high to SWDIO output	T = 1/f_SWDCCK max	–	–	2T/5	

11.8.6 SWV Interface

Table 11-64. SWV Interface AC Specifications^[30]

Parameter	Description	Conditions	Min	Typ	Max	Units
	SWV mode SWV bit rate		–	–	33	Mbit

11.9 Clocking

Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

11.9.1 Internal Main Oscillator

Table 11-65. IMO DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Supply current					
	24 MHz – USB mode	With oscillator locking to USB bus	–	–	500	μA
	24 MHz – non USB mode		–	–	300	μA
	12 MHz		–	–	200	μA
	6 MHz		–	–	180	μA
	3 MHz		–	–	150	μA

Notes

67. Based on device characterization (Not production tested).

68. f_SWDCCK must also be no more than 1/3 CPU clock frequency.

11.9.4 kHz External Crystal Oscillator

Table 11-71. kHzECO DC Specifications^[72]

Parameter	Description	Conditions	Min	Typ	Max	Units
I _{CC}	Operating current	Low-power mode; CL = 6 pF	–	0.25	1.0	μA
DL	Drive level		–	–	1	μW

Table 11-72. kHzECO AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
F	Frequency		–	32.768	–	kHz
T _{ON}	Startup time	High power mode	–	1	–	s

11.9.5 External Clock Reference

Table 11-73. External Clock Reference AC Specifications^[72]

Parameter	Description	Conditions	Min	Typ	Max	Units
	External frequency range		0	–	33	MHz
	Input duty cycle range	Measured at V _{DDIO} /2	30	50	70	%
	Input edge rate	V _{IL} to V _{IH}	0.5	–	–	V/ns

11.9.6 Phase-Locked Loop

Table 11-74. PLL DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
I _{DD}	PLL operating current	In = 3 MHz, Out = 24 MHz	–	200	–	μA

Table 11-75. PLL AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
F _{pllin}	PLL input frequency ^[73]		1	–	48	MHz
	PLL intermediate frequency ^[74]	Output of prescaler	1	–	3	MHz
F _{plout}	PLL output frequency ^[73]		24	–	50	MHz
	Lock time at startup		–	–	250	μs
J _{period-rms}	Jitter (rms) ^[72]		–	–	250	ps

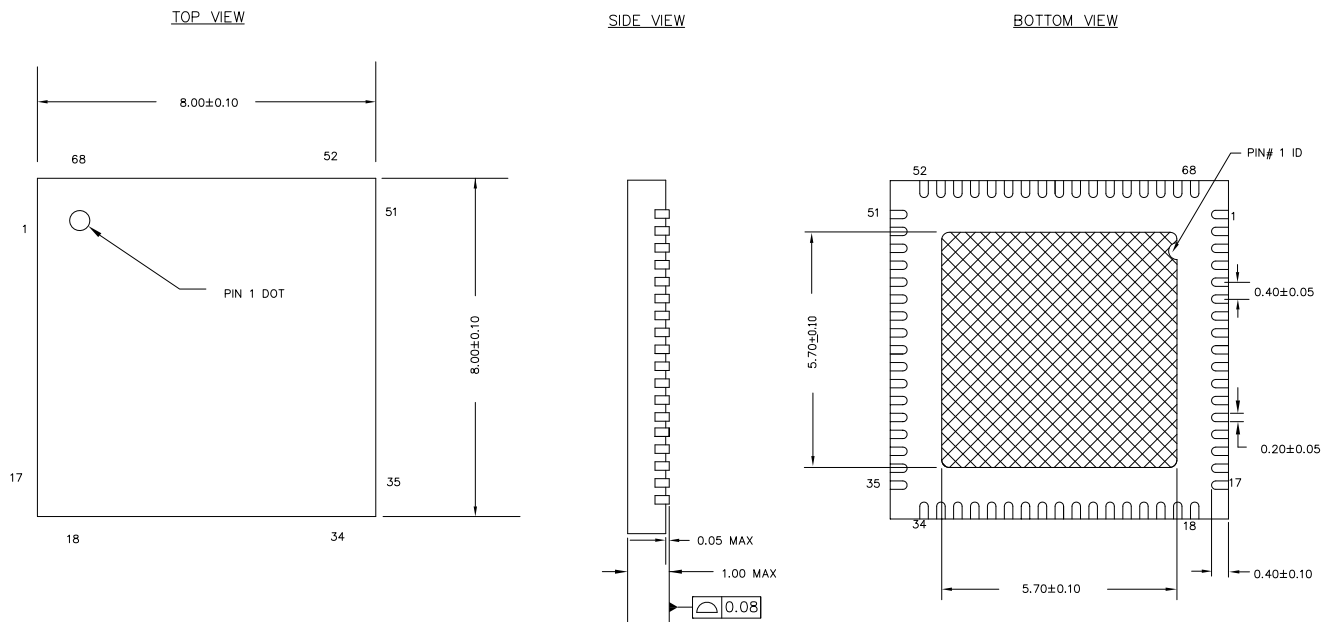
Notes

72. Based on device characterization (Not production tested).

73. This specification is guaranteed by testing the PLL across the specified range using the IMO as the source for the PLL.

74. PLL input divider, Q, must be set so that the input frequency is divided down to the intermediate frequency range. Value for Q ranges from 1 to 16.

Figure 13-3. 68-pin QFN 8x8 with 0.4 mm Pitch Package Outline (Sawn Version)

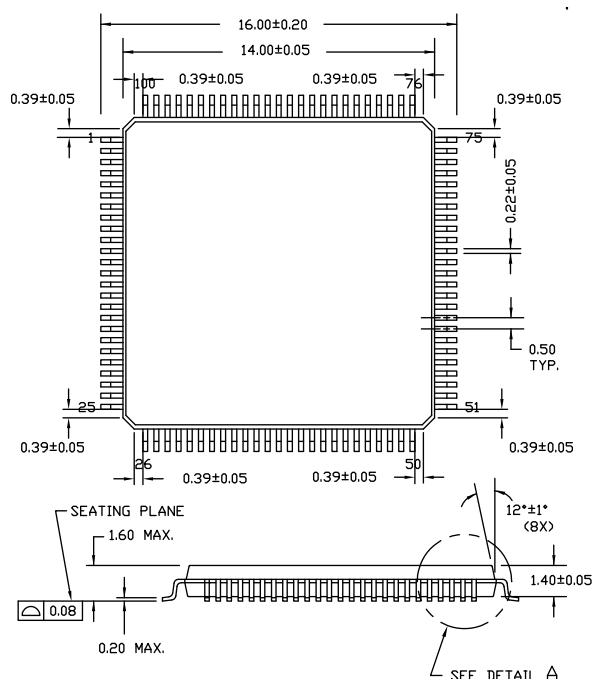


NOTES:

1. HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO-220
3. PACKAGE WEIGHT: 17 ± 2mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

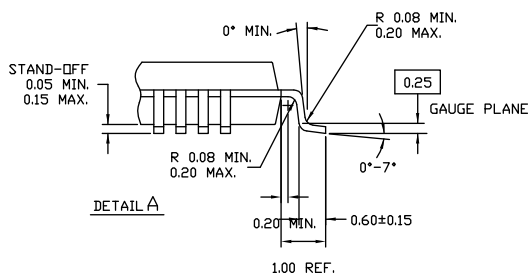
001-09618 *E

Figure 13-4. 100-pin TQFP (14 x 14 x 1.4 mm) Package Outline

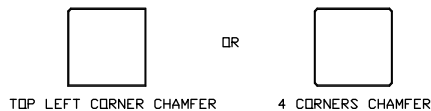


NOTE:

1. JEDEC STD REF MS-026
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH
MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.0098 in (0.25 mm) PER SIDE
BODY LENGTH DIMENSIONS ARE MAX PLASTIC BODY SIZE INCLUDING MOLD MISMATCH
3. DIMENSIONS IN MILLIMETERS



NOTE: PKG. CAN HAVE



51-85048 *J

Figure 13-5. WLCSP Package (4.25 × 4.98 × 0.60 mm)

