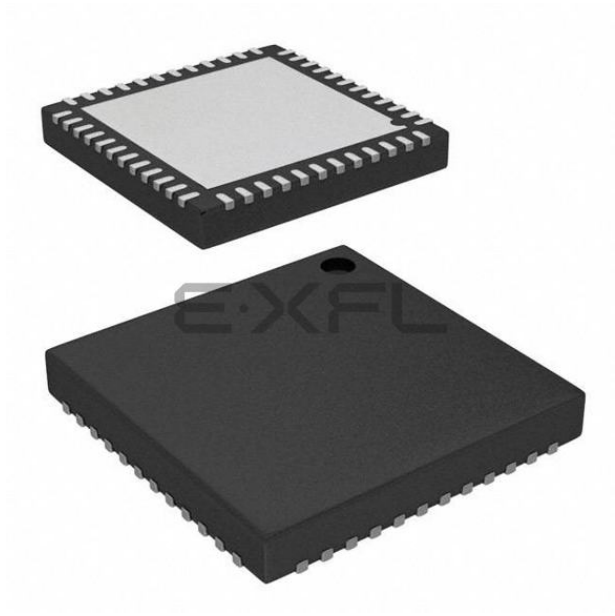


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	50MHz
Connectivity	EBI/EMI, I²C, LINbus, SPI, UART/USART
Peripherals	CapSense, DMA, POR, PWM, WDT
Number of I/O	25
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 16x12b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c3244lti-123t

4.4.4.5 Scatter Gather DMA

In the case of scatter gather DMA, there are multiple noncontiguous sources or destinations that are required to effectively carry out an overall DMA transaction. For example, a packet may need to be transmitted off of the device and the packet elements, including the header, payload, and trailer, exist in various noncontiguous locations in memory. Scatter gather DMA allows the segments to be concatenated together by using multiple TDs in a chain. The chain gathers the data from the multiple locations. A similar concept applies for the reception of data onto the device. Certain parts of the received data may need to be scattered to various locations in memory for software processing convenience. Each TD in the chain specifies the location for each discrete element in the chain.

4.4.4.6 Packet Queuing DMA

Packet queuing DMA is similar to scatter gather DMA but specifically refers to packet protocols. With these protocols, there may be separate configuration, data, and status phases associated with sending or receiving a packet.

For instance, to transmit a packet, a memory mapped configuration register can be written inside a peripheral, specifying the overall length of the ensuing data phase. The CPU can set up this configuration information anywhere in system memory and copy it with a simple TD to the peripheral. After the configuration phase, a data phase TD (or a series of data phase TDs) can begin (potentially using scatter gather). When the data phase TD(s) finish, a status phase TD can be invoked that reads some memory mapped status information from the peripheral and copies it to a location in system memory specified by the CPU for later inspection. Multiple sets of configuration, data, and status phase “subchains” can be strung together to create larger chains that transmit multiple packets in this way. A similar concept exists in the opposite direction to receive the packets.

4.4.4.7 Nested DMA

One TD may modify another TD, as the TD configuration space is memory mapped similar to any other peripheral. For example, a first TD loads a second TD’s configuration and then calls the second TD. The second TD moves data as required by the application. When complete, the second TD calls the first TD, which again updates the second TD’s configuration. This process repeats as often as necessary.

4.5 Interrupt Controller

The interrupt controller provides a mechanism for hardware resources to change program execution to a new address, independent of the current task being executed by the main code. The interrupt controller provides enhanced features not found on original 8051 interrupt controllers:

- Thirty two interrupt vectors
- Jumps directly to ISR anywhere in code space with dynamic vector addresses
- Multiple sources for each vector
- Flexible interrupt to vector matching
- Each interrupt vector is independently enabled or disabled
- Each interrupt can be dynamically assigned one of eight priorities
- Eight level nestable interrupts
- Multiple I/O interrupt vectors
- Software can send interrupts
- Software can clear pending interrupts

When an interrupt is pending, the current instruction is completed and the program counter is pushed onto the stack. Code execution then jumps to the program address provided by the vector. After the ISR is completed, a RETI instruction is executed and returns execution to the instruction following the previously interrupted instruction. To do this the RETI instruction pops the program counter from the stack.

If the same priority level is assigned to two or more interrupts, the interrupt with the lower vector number is executed first. Each interrupt vector may choose from three interrupt sources: Fixed Function, DMA, and UDB. The fixed function interrupts are direct connections to the most common interrupt sources and provide the lowest resource cost connection. The DMA interrupt sources provide direct connections to the two DMA interrupt sources provided per DMA channel. The third interrupt source for vectors is from the UDB digital routing array. This allows any digital signal available to the UDB array to be used as an interrupt source. Fixed function interrupts and all interrupt sources may be routed to any interrupt vector using the UDB interrupt source connections.

Figure 4-2 on page 21 represents typical flow of events when an interrupt triggered. Figure 4-3 on page 22 shows the interrupt structure and priority polling.

Table 4-8. Interrupt Vector Table

#	Fixed Function	DMA	UDB
0	LVD	phub_termout0[0]	udb_intr[0]
1	Cache/ECC	phub_termout0[1]	udb_intr[1]
2	Reserved	phub_termout0[2]	udb_intr[2]
3	Sleep (Pwr Mgr)	phub_termout0[3]	udb_intr[3]
4	PICU[0]	phub_termout0[4]	udb_intr[4]
5	PICU[1]	phub_termout0[5]	udb_intr[5]
6	PICU[2]	phub_termout0[6]	udb_intr[6]
7	PICU[3]	phub_termout0[7]	udb_intr[7]
8	PICU[4]	phub_termout0[8]	udb_intr[8]
9	PICU[5]	phub_termout0[9]	udb_intr[9]
10	PICU[6]	phub_termout0[10]	udb_intr[10]
11	PICU[12]	phub_termout0[11]	udb_intr[11]
12	PICU[15]	phub_termout0[12]	udb_intr[12]
13	Comparators Combined	phub_termout0[13]	udb_intr[13]
14	Reserved	phub_termout0[14]	udb_intr[14]
15	I^2C	phub_termout0[15]	udb_intr[15]
16	Reserved	phub_termout1[0]	udb_intr[16]
17	Timer/Counter0	phub_termout1[1]	udb_intr[17]
18	Timer/Counter1	phub_termout1[2]	udb_intr[18]
19	Timer/Counter2	phub_termout1[3]	udb_intr[19]
20	Timer/Counter3	phub_termout1[4]	udb_intr[20]
21	USB SOF Int	phub_termout1[5]	udb_intr[21]
22	USB Arb Int	phub_termout1[6]	udb_intr[22]
23	USB Bus Int	phub_termout1[7]	udb_intr[23]
24	USB Endpoint[0]	phub_termout1[8]	udb_intr[24]
25	USB Endpoint Data	phub_termout1[9]	udb_intr[25]
26	Reserved	phub_termout1[10]	udb_intr[26]
27	LCD	phub_termout1[11]	udb_intr[27]
28	Reserved	phub_termout1[12]	udb_intr[28]
29	Decimator Int	phub_termout1[13]	udb_intr[29]
30	PHUB Error Int	phub_termout1[14]	udb_intr[30]
31	EEPROM Fault Int	phub_termout1[15]	udb_intr[31]

5. Memory

5.1 Static RAM

CY8C32 Static RAM (SRAM) is used for temporary data storage. Up to 8 KB of SRAM is provided and can be accessed by the 8051 or the DMA controller. See Memory Map on page 26. Simultaneous access of SRAM by the 8051 and the DMA controller is possible if different 4-KB blocks are accessed.

5.2 Flash Program Memory

Flash memory in PSoC devices provides nonvolatile storage for user firmware, user configuration data, bulk data storage, and optional ECC data. The main flash memory area contains up to 64 KB of user program space.

Up to an additional 8 KB of flash space is available for Error Correcting Codes (ECC). If ECC is not used this space can store device configuration data and bulk user data. User code may not be run out of the ECC flash memory section. ECC can correct one bit error and detect two bit errors per 8 bytes of firmware memory; an interrupt can be generated when an error is detected.

The CPU reads instructions located in flash through a cache controller. This improves instruction execution rate and reduces system power consumption by requiring less frequent flash access. The cache has 8 lines at 64 bytes per line for a total of 512 bytes. It is fully associative, automatically controls flash power, and can be enabled or disabled. If ECC is enabled, the cache controller also performs error checking and correction, and interrupt generation.

Flash programming is performed through a special interface and preempts code execution out of flash. The flash programming interface performs flash erasing, programming and setting code protection levels. Flash in-system serial programming (ISSP), typically used for production programming, is possible through both the SWD and JTAG interfaces. In-system programming, typically used for bootloaders, is also possible using serial interfaces such as I^2C, USB, UART, and SPI, or any communications protocol.

5.3 Flash Security

All PSoC devices include a flexible flash-protection model that prevents access and visibility to on-chip flash memory. This prevents duplication or reverse engineering of proprietary code. Flash memory is organized in blocks, where each block contains 256 bytes of program or data and 32 bytes of ECC or configuration data. A total of up to 256 blocks is provided on 64-KB flash devices.

The device offers the ability to assign one of four protection levels to each row of flash. Table 5-1 lists the protection modes available. Flash protection levels can only be changed by performing a complete flash erase. The Full Protection and Field Upgrade settings disable external access (through a debugging tool such as PSoC Creator, for example). If your application requires code update through a boot loader, then use the Field Upgrade setting. Use the Unprotected setting only when no security is needed in your application. The PSoC device also offers an advanced security feature called Device Security which permanently disables all test, programming, and debug ports, protecting your application from external access (see the "Device Security" section on page 65). For more information about how to take full advantage of the security features in PSoC, see the PSoC 3 TRM.

Table 5-1. Flash Protection

Protection Setting	Allowed	Not Allowed
Unprotected	External read and write + internal read and write	–
Factory Upgrade	External write + internal read and write	External read
Field Upgrade	Internal read and write	External read and write
Full Protection	Internal read	External read and write + internal write

Disclaimer

Note the following details of the flash code protection features on Cypress devices.

Cypress products meet the specifications contained in their particular Cypress datasheets. Cypress believes that its family of products is one of the most secure families of its kind on the market today, regardless of how they are used. There may be methods, unknown to Cypress, that can breach the code protection features. Any of these methods, to our knowledge, would be dishonest and possibly illegal. Neither Cypress nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Cypress is willing to work with the customer who is concerned about the integrity of their code. Code protection is constantly evolving. We at Cypress are committed to continuously improving the code protection features of our products.

5.4 EEPROM

PSoC EEPROM memory is a byte-addressable nonvolatile memory. The CY8C32 has up to 2 KB of EEPROM memory to store user data. Reads from EEPROM are random access at the byte level. Reads are done directly; writes are done by sending write commands to an EEPROM programming interface. CPU code execution can continue from flash during EEPROM writes. EEPROM is erasable and writeable at the row level. The EEPROM is divided into 128 rows of 16 bytes each. The factory default values of all EEPROM bytes are 0.

Because the EEPROM is mapped to the 8051 xdata space, the CPU cannot execute out of EEPROM. There is no ECC hardware associated with EEPROM. If ECC is required it must be handled in firmware.

It can take as much as 20 milliseconds to write to EEPROM or flash. During this time the device should not be reset, or unexpected changes may be made to portions of EEPROM or flash. Reset sources (see *Section 6.3.1*) include XRES pin, software reset, and watchdog; care should be taken to make sure that these are not inadvertently activated. In addition, the low voltage detect circuits should be configured to generate an interrupt instead of a reset.

I/O ports are linked to the CPU through the PHUB and are also available in the SFRs. Using the SFRs allows faster access to a limited set of I/O port registers, while using the PHUB allows boot configuration and access to all I/O port registers.

Each SFR supported I/O port provides three SFRs:

- SFRPRTxDR sets the output data state of the port (where x is port number and includes ports 0 – 6, 12 and 15).
- The SFRPRTxSEL selects whether the PHUB PRTxDR register or the SFRPRTxDR controls each pin's output buffer within the port. If a SFRPRTxSEL[y] bit is high, the corresponding SFRPRTxDR[y] bit sets the output state for that pin. If a SFRPRTxSEL[y] bit is low, the corresponding PRTxDR[y] bit sets the output state of the pin (where y varies from 0 to 7).
- The SFRPRTxPS is a read only register that contains pin state values of the port pins.

5.7.4 xdata Space

The 8051 xdata space is 24-bit, or 16 MB in size. The majority of this space is not "external"—it is used by on-chip components. See Table 5-5. External, that is, off-chip, memory can be accessed using the EMIF. See External Memory Interface on page 26.

Table 5-5. XDATA Data Address Map

Address Range	Purpose
0×00 0000 – 0×00 1FFF	SRAM
0×00 4000 – 0×00 42FF	Clocking, PLLs, and oscillators
0×00 4300 – 0×00 43FF	Power management
0×00 4400 – 0×00 44FF	Interrupt controller
0×00 4500 – 0×00 45FF	Ports interrupt control
0×00 4700 – 0×00 47FF	Flash programming interface
0×00 4800 – 0×00 48FF	Cache controller
0×00 4900 – 0×00 49FF	I^2C controller
0×00 4E00 – 0×00 4EFF	Decimator
0×00 4F00 – 0×00 4FFF	Fixed timer/counter/PWMs
0×00 5000 – 0×00 51FF	I/O ports control
0×00 5400 – 0×00 54FF	External Memory Interface (EMIF) control registers
0×00 5800 – 0×00 5FFF	Analog Subsystem interface
0×00 6000 – 0×00 60FF	USB controller
0×00 6400 – 0×00 6FFF	UDB Working Registers
0×00 7000 – 0×00 7FFF	PHUB configuration
0×00 8000 – 0×00 8FFF	EEPROM
0×01 0000 – 0×01 FFFF	Digital Interconnect configuration
0×05 0220 – 0×05 02F0	Debug controller
0×08 0000 – 0×08 1FFF	Flash ECC bytes
0×80 0000 – 0×FF FFFF	External Memory Interface

6. System Integration

6.1 Clocking System

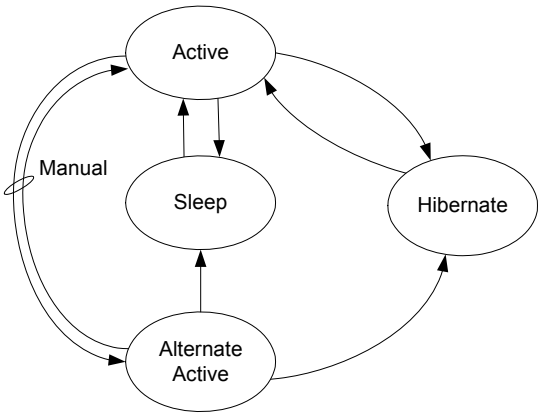
The clocking system generates, divides, and distributes clocks throughout the PSoC system. For the majority of systems, no external crystal is required. The IMO and PLL together can generate up to a 50 MHz clock, accurate to ±2 percent over voltage and temperature. Additional internal and external clock sources allow each design to optimize accuracy, power, and cost. Any of the clock sources can be used to generate other clock frequencies in the 16-bit clock dividers and UDBs for anything the user wants, for example a UART baud rate generator.

Clock generation and distribution is automatically configured through the PSoC Creator IDE graphical interface. This is based on the complete system's requirements. It greatly speeds the design process. PSoC Creator allows you to build clocking systems with minimal input. You can specify desired clock frequencies and accuracies, and the software locates or builds a clock that meets the required specifications. This is possible because of the programmability inherent in PSoC.

Key features of the clocking system include:

- Seven general purpose clock sources
  - 3- to 24-MHz IMO, ±2 percent at 3 MHz
  - 4- to 25-MHz external crystal oscillator (MHzECO)
  - Clock doubler provides a doubled clock frequency output for the USB block, see USB Clock Domain on page 31
  - DSI signal from an external I/O pin or other logic
  - 24- to 50- MHz fractional PLL sourced from IMO, MHzECO, or DSI
  - 1-kHz, 33-kHz, 100-kHz ILO for watchdog timer (WDT) and sleep timer
  - 32.768-kHz external crystal oscillator (kHzECO) for RTC
- IMO has a USB mode that auto locks to the USB bus clock requiring no external crystal for USB. (USB equipped parts only)
- Independently sourced clock in all clock dividers
- Eight 16-bit clock dividers for the digital system
- Four 16-bit clock dividers for the analog system
- Dedicated 16-bit divider for the bus clock
- Dedicated 4-bit divider for the CPU clock
- Automatic clock configuration in PSoC Creator

Figure 6-5. Power Mode Transitions



6.2.1.1 Active Mode

Active mode is the primary operating mode of the device. When in active mode, the active configuration template bits control which available resources are enabled or disabled. When a resource is disabled, the digital clocks are gated, analog bias currents are disabled, and leakage currents are reduced as appropriate. User firmware can dynamically control subsystem power by setting and clearing bits in the active configuration template. The CPU can disable itself, in which case the CPU is automatically reenabled at the next wakeup event.

When a wakeup event occurs, the global mode is always returned to active, and the CPU is automatically enabled, regardless of its template settings. Active mode is the default global power mode upon boot.

6.2.1.2 Alternate Active Mode

Alternate Active mode is very similar to Active mode. In alternate active mode, fewer subsystems are enabled, to reduce power consumption. One possible configuration is to turn off the CPU and flash, and run peripherals at full speed.

6.2.1.3 Sleep Mode

Sleep mode reduces power consumption when a resume time of 15 µs is acceptable. The wake time is used to ensure that the regulator outputs are stable enough to directly enter active mode.

6.2.1.4 Hibernate Mode

In hibernate mode nearly all of the internal functions are disabled. Internal voltages are reduced to the minimal level to keep vital systems alive. Configuration state is preserved in hibernate mode and SRAM memory is retained. GPIOs configured as digital outputs maintain their previous values and external GPIO pin interrupt settings are preserved. The device can only return from hibernate mode in response to an external I/O interrupt. The resume time from hibernate mode is less than 100 µs.

To achieve an extremely low current, the hibernate regulator has limited capacity. This limits the frequency of any signal present on the input pins - no GPIO should toggle at a rate greater than 10 kHz while in hibernate mode. If pins must be toggled at a high rate while in a low power mode, use sleep mode instead.

6.2.1.5 Wakeup Events

Wakeup events are configurable and can come from an interrupt or device reset. A wakeup event restores the system to active mode. Firmware enabled interrupt sources include internally generated interrupts, power supervisor, central timewheel, and I/O interrupts. Internal interrupt sources can come from a variety of peripherals, such as analog comparators and UDBs. The central timewheel provides periodic interrupts to allow the system to wake up, poll peripherals, or perform real-time functions. Reset event sources include the external reset I/O pin (XRES), WDT, and Precision Reset (PRES).

6.2.2 Boost Converter

Applications that use a supply voltage of less than 1.71 V, such as solar panels or single cell battery supplies, may use the on-chip boost converter to generate a minimum of 1.8 V supply voltage. The boost converter may also be used in any system that requires a higher operating voltage than the supply provides such as driving 5.0 V LCD glass in a 3.3 V system. With the addition of an inductor, Schottky diode, and capacitors, it produces a selectable output voltage sourcing enough current to operate the PSoC and other on-board components.

The boost converter accepts an input voltage V_{BAT} from 0.5 V to 3.6 V, and can start up with V_{BAT} as low as 0.5 V. The converter provides a user configurable output voltage of 1.8 to 5.0 V (V_{OUT}) in 100 mV increments. V_{BAT} is typically less than V_{OUT}; if V_{BAT} is greater than or equal to V_{OUT}, then V_{OUT} will be slightly less than V_{BAT} due to resistive losses in the boost converter. The block can deliver up to 50 mA (I_{BOOST}) depending on configuration to both the PSoC device and external components. The sum of all current sinks in the design including the PSoC device, PSoC I/O pin loads, and external component loads must be less than the I_{BOOST} specified maximum current.

Four pins are associated with the boost converter: VBAT, VSSB, VBOOST, and IND. The boosted output voltage is sensed at the VBOOST pin and must be connected directly to the chip's supply inputs, VDDA, VDDD, and VDDIO, if used to power the PSoC device.

The boost converter requires four components in addition to those required in a non-boost design, as shown in Figure 6-6 on page 35. A 22-µF capacitor (CBAT) is required close to the VBAT pin to provide local bulk storage of the battery voltage and provide regulator stability. A diode between the battery and VBAT pin should not be used for reverse polarity protection because the diodes forward voltage drop reduces the V_{BAT} voltage. Between the VBAT and IND pins, an inductor of 4.7 µH, 10 µH, or 22 µH is required. The inductor value can be optimized to increase the boost converter efficiency based on input voltage, output voltage, temperature, and current. Inductor size is determined by following the design guidance in this section and the electrical specifications. The inductor must be placed within 1 cm of the VBAT and IND pins and have a minimum saturation current of 750 mA. Between the IND and VBOOST pins, place a Schottky diode within 1 cm of the pins. This diode shall have a forward current rating of at least 1.0 A and a reverse voltage of at least 20 V. Connect a 22-µF bulk capacitor (CBOOST) close to VBOOST to provide regulator output stability. It is important to sum the total capacitance connected to the VBOOST pin and ensure the maximum CBOOST specification is not exceeded. All capacitors must be rated for a minimum of 10 V to minimize capacitive losses due to voltage de-rating.

boost typically draws 250 µA in active mode and 25 µA in standby mode. The boost operating modes must be used in conjunction with chip power modes to minimize total power consumption. Table 6-4 lists the boost power modes available in different chip power modes.

Table 6-4. Chip and Boost Power Modes Compatibility

Chip Power Modes	Boost Power Modes
Chip-active or alternate active mode	Boost must be operated in its active mode.
Chip-sleep mode	Boost can be operated in either active or standby mode. In boost standby mode, the chip must wake up periodically for boost active-mode refresh.
Chip-hibernate mode	Boost can be operated in its active mode. However, it is recommended not to use the boost in chip hibernate mode due to the higher current consumption in boost active mode.

6.2.2.1 Boost Firmware Requirements

To ensure boost inrush current is within specification at startup, the **Enable Fast IMO During Startup** value must be unchecked in the PSoC Creator IDE. The **Enable Fast IMO During Startup** option is found in PSoC Creator in the design wide resources (cydwr) file **System** tab. Un-checking this option configures the device to run at 12 MHz vs 48 MHz during startup while configuring the device. The slower clock speed results in reduced current draw through the boost circuit.

6.2.2.2 Boost Design Process

Correct operation of the boost converter requires specific component values determined for each designs unique operating conditions. The C_{BAT} capacitor, Inductor, Schottky diode, and C_{BOOST} capacitor components are required with the values specified in the electrical specifications, Table 11-7 on page 74. The only variable component value is the inductor L_{BOOST} which is primarily sized for correct operation of the boost across operating conditions and secondarily for efficiency. Additional operating region constraints exist for V_{OUT}, V_{BAT}, I_{OUT}, and T_A.

The following steps must be followed to determine boost converter operating parameters and L_{BOOST} value.

1. Choose desired V_{BAT}, V_{OUT}, T_A, and I_{OUT} operating condition ranges for the application.
2. Determine if V_{BAT} and V_{OUT} ranges fit the boost operating range based on the **T_A range over V_{BAT} and V_{OUT}** chart, Figure 11-8 on page 74. If the operating ranges are not met, modify the operating conditions or use an external boost regulator.
3. Determine if the desired ambient temperature (T_A) range fits the ambient temperature operating range based on the **T_A range over V_{BAT} and V_{OUT}** chart, Figure 11-8 on page 74. If the temperature range is not met, modify the operating conditions and return to step 2, or use an external boost regulator.
4. Determine if the desired output current (I_{OUT}) range fits the output current operating range based on the **I_{OUT} range over V_{BAT} and V_{OUT}** chart, Figure 11-9 on page 74. If the output current range is not met, modify the operating conditions and return to step 2, or use an external boost regulator.
5. Find the allowed inductor values based on the **L_{BOOST} values over V_{BAT} and V_{OUT}** chart, Figure 11-10 on page 74.
6. Based on the allowed inductor values, inductor dimensions, inductor cost, boost efficiency, and V_{RIPPLE} choose the optimum inductor value for the system. Boost efficiency and V_{RIPPLE} typical values are provided in the **Efficiency vs V_{BAT}** and **V_{RIPPLE} vs V_{BAT}** charts, Figure 11-11 on page 75 through Figure 11-14 on page 75. In general, if high efficiency and low V_{RIPPLE} are most important, then the highest allowed inductor value should be used. If low inductor cost or small inductor size are most important, then one of the smaller allowed inductor values should be used. If the allowed inductor(s) efficiency, V_{RIPPLE}, cost or dimensions are not acceptable for the application than an external boost regulator should be used.

6.3 Reset

CY8C32 has multiple internal and external reset sources available. The reset sources are:

- Power source monitoring – The analog and digital power voltages, VDDA, VDDD, VCCA, and VCCD are monitored in several different modes during power up, active mode, and sleep mode (buzzing). If any of the voltages goes outside predetermined ranges then a reset is generated. The monitors are programmable to generate an interrupt to the processor under certain conditions before reaching the reset thresholds.
- External – The device can be reset from an external source by pulling the reset pin (XRES) low. The XRES pin includes an internal pull-up to VDDIO1. VDDD, VDDA, and VDDIO1 must all have voltage applied before the part comes out of reset.
- Watchdog timer – A watchdog timer monitors the execution of instructions by the processor. If the watchdog timer is not reset by firmware within a certain period of time, the watchdog timer generates a reset.
- Software – The device can be reset under program control.

Figure 6-8. Resets

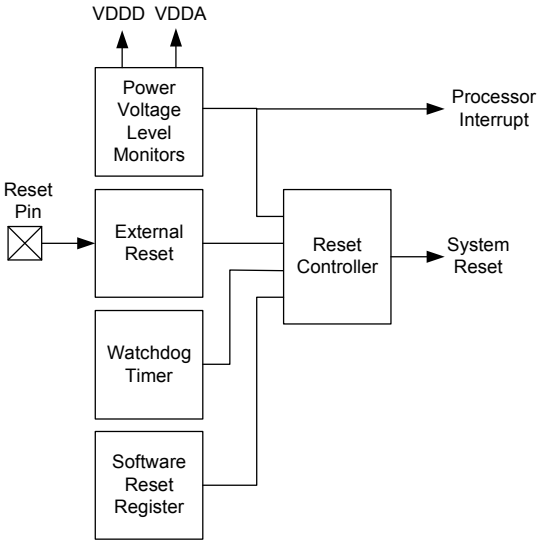
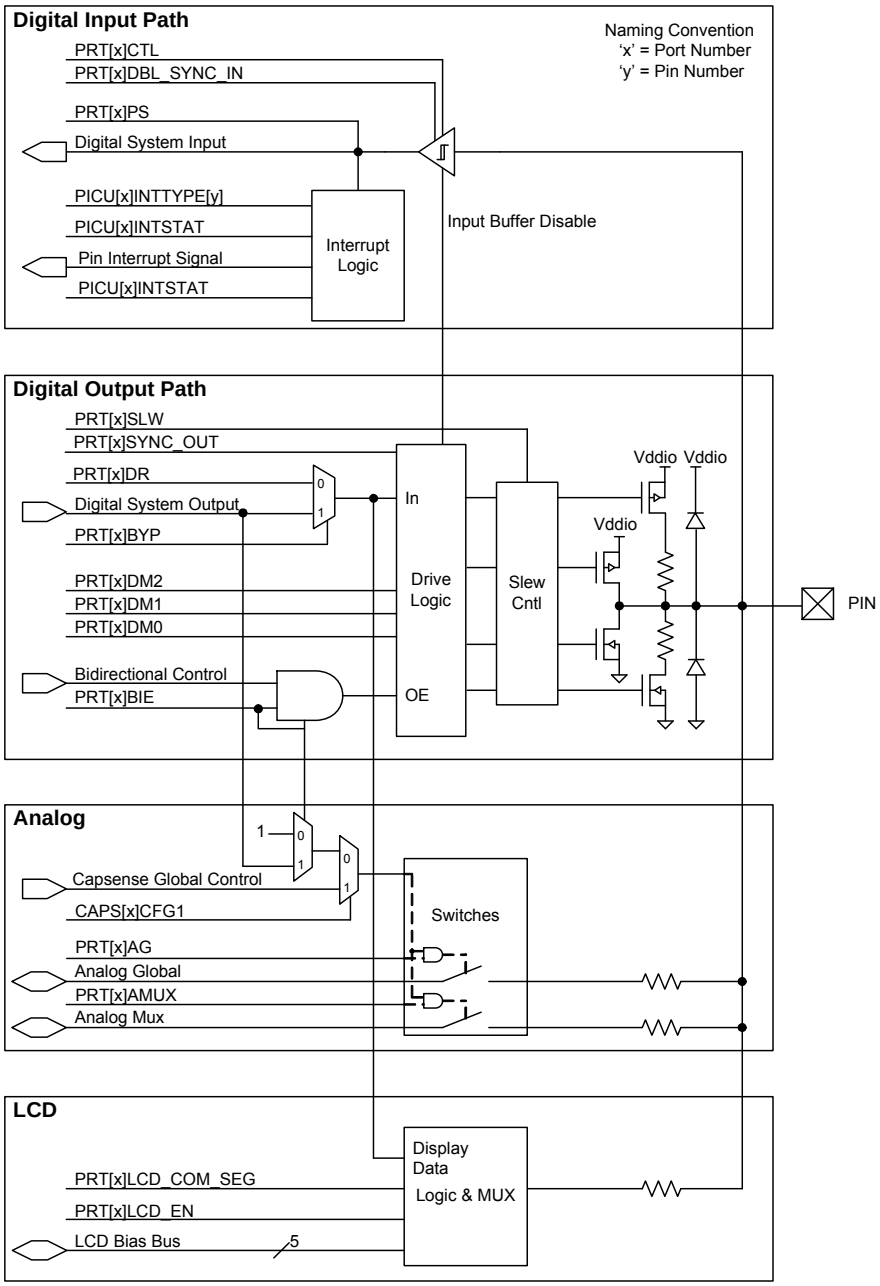


Figure 6-9. GPIO Block Diagram



7.1.4 Designing with PSoC Creator

7.1.4.1 More Than a Typical IDE

A successful design tool allows for the rapid development and deployment of both simple and complex designs. It reduces or eliminates any learning curve. It makes the integration of a new design into the production stream straightforward.

PSoC Creator is that design tool.

PSoC Creator is a full featured Integrated Development Environment (IDE) for hardware and software design. It is optimized specifically for PSoC devices and combines a modern, powerful software development platform with a sophisticated graphical design tool. This unique combination of tools makes PSoC Creator the most flexible embedded design platform available.

Graphical design entry simplifies the task of configuring a particular part. You can select the required functionality from an extensive catalog of components and place it in your design. All components are parameterized and have an editor dialog that allows you to tailor functionality to your needs.

PSoC Creator automatically configures clocks and routes the I/O to the selected pins and then generates APIs to give the application complete control over the hardware. Changing the PSoC device configuration is as simple as adding a new component, setting its parameters, and rebuilding the project.

At any stage of development you are free to change the hardware configuration and even the target processor. To retarget your application (hardware and software) to new devices, even from 8- to 32-bit families, just select the new device and rebuild.

You also have the ability to change the C compiler and evaluate an alternative. Components are designed for portability and are validated against all devices, from all families, and against all supported tool chains. Switching compilers is as easy as editing the from the project options and rebuilding the application with no errors from the generated APIs or boot code.

7.1.4.2 Component Catalog

The component catalog is a repository of reusable design elements that select device functionality and customize your PSoC device. It is populated with an impressive selection of content; from simple primitives such as logic gates and device registers, through the digital timers, counters and PWMs, plus analog components such as ADC and DAC, and communication protocols, such as I^2C, and USB. See Example Peripherals on page 45 for more details about available peripherals. All content is fully characterized and carefully documented in datasheets with code examples, AC/DC specifications, and user code ready APIs.

7.1.4.3 Design Reuse

The symbol editor gives you the ability to develop reusable components that can significantly reduce future design time. Just draw a symbol and associate that symbol with your proven design. PSoC Creator allows for the placement of the new symbol anywhere in the component catalog along with the content provided by Cypress. You can then reuse your content as many times as you want, and in any number of projects, without ever having to revisit the details of the implementation.

7.1.4.4 Software Development

Anchoring the tool is a modern, highly customizable user interface. It includes project management and integrated editors for C and assembler source code, as well the design entry tools.

Project build control leverages compiler technology from top commercial vendors such as ARM® Limited, Keil™, and CodeSourcery (GNU). Free versions of Keil C51 and GNU C Compiler (GCC) for ARM, with no restrictions on code size or end product distribution, are included with the tool distribution. Upgrading to more optimizing compilers is a snap with support for the professional Keil C51 product and ARM RealView™ compiler.

7.1.4.5 Nonintrusive Debugging

With JTAG (4-wire) and SWD (2-wire) debug connectivity available on all devices, the PSoC Creator debugger offers full control over the target device with minimum intrusion. Breakpoints and code execution commands are all readily available from toolbar buttons and an impressive lineup of windows—register, locals, watch, call stack, memory and peripherals—make for an unparalleled level of visibility into the system.

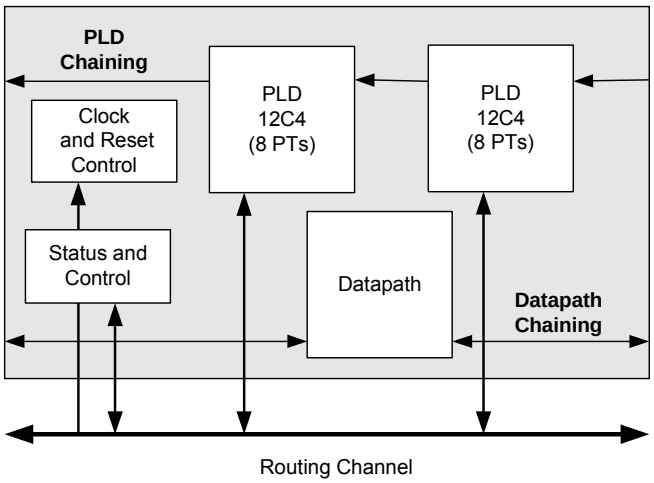
PSoC Creator contains all the tools necessary to complete a design, and then to maintain and extend that design for years to come. All steps of the design flow are carefully integrated and optimized for ease-of-use and to maximize productivity.

7.2 Universal Digital Block

The Universal Digital Block (UDB) represents an evolutionary step to the next generation of PSoC embedded digital peripheral functionality. The architecture in first generation PSoC digital blocks provides coarse programmability in which a few fixed functions with a small number of options are available. The new UDB architecture is the optimal balance between configuration granularity and efficient implementation. A cornerstone of this approach is to provide the ability to customize the devices digital operation to match application requirements.

To achieve this, UDBs consist of a combination of uncommitted logic (PLD), structured logic (Datapath), and a flexible routing scheme to provide interconnect between these elements, I/O connections, and other peripherals. UDB functionality ranges from simple self contained functions that are implemented in one UDB, or even a portion of a UDB (unused resources are available for other functions), to more complex functions that require multiple UDBs. Examples of basic functions are timers, counters, CRC generators, PWMs, dead band generators, and communications functions, such as UARTs, SPI, and I^2C. Also, the PLD blocks and connectivity provide full featured general purpose programmable logic within the limits of the available resources.

Figure 7-2. UDB Block Diagram



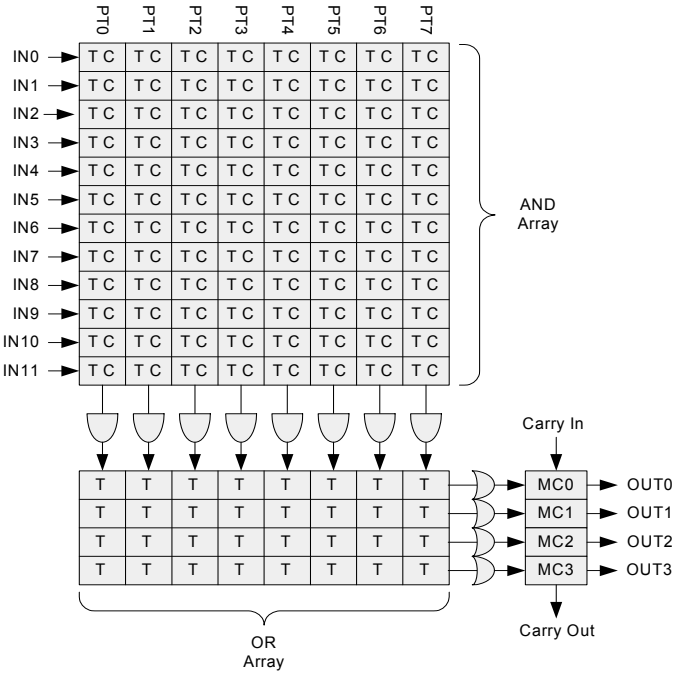
The main component blocks of the UDB are:

- PLD blocks – There are two small PLDs per UDB. These blocks take inputs from the routing array and form registered or combinational sum-of-products logic. PLDs are used to implement state machines, state bits, and combinational logic equations. PLD configuration is automatically generated from graphical primitives.
- Datapath Module – This 8-bit wide datapath contains structured logic to implement a dynamically configurable ALU, a variety of compare configurations and condition generation. This block also contains input/output FIFOs, which are the primary parallel data interface between the CPU/DMA system and the UDB.
- Status and Control Module – The primary role of this block is to provide a way for CPU firmware to interact and synchronize with UDB operation.
- Clock and Reset Module – This block provides the UDB clocks and reset selection and control.

7.2.1 PLD Module

The primary purpose of the PLD blocks is to implement logic expressions, state machines, sequencers, lookup tables, and decoders. In the simplest use model, consider the PLD blocks as a standalone resource onto which general purpose RTL is synthesized and mapped. The more common and efficient use model is to create digital functions from a combination of PLD and datapath blocks, where the PLD implements only the random logic and state portion of the function while the datapath (ALU) implements the more structured elements.

Figure 7-3. PLD 12C4 Structure



One 12C4 PLD block is shown in Figure 7-3. This PLD has 12 inputs, which feed across eight product terms. Each product term (AND function) can be from 1 to 12 inputs wide, and in a given product term, the true (T) or complement (C) of each input can be selected. The product terms are summed (OR function) to create the PLD outputs. A sum can be from 1 to 8 product terms wide. The 'C' in 12C4 indicates that the width of the OR gate (in this case 8) is constant across all outputs (rather than variable as in a 22V10 device). This PLA like structure gives maximum flexibility and insures that all inputs and outputs are permutable for ease of allocation by the software tools. There are two 12C4 PLDs in each UDB.

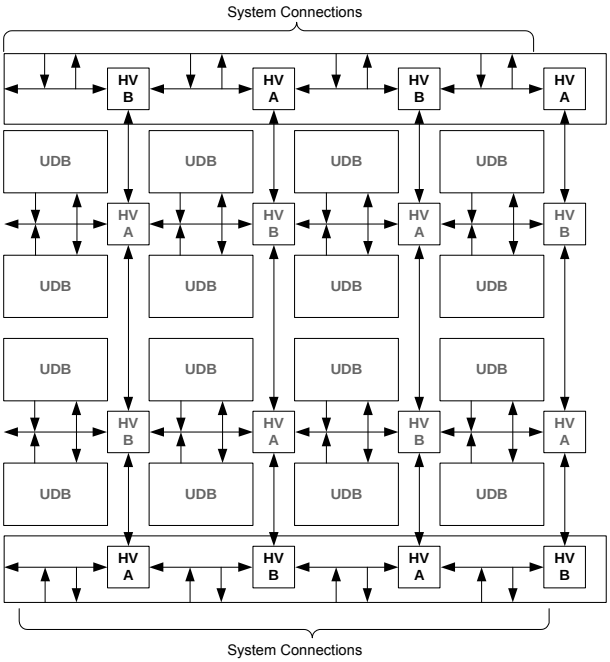
7.2.3.2 Clock Generation

Each subcomponent block of a UDB including the two PLDs, the datapath, and Status and Control, has a clock selection and control block. This promotes a fine granularity with respect to allocating clocking resources to UDB component blocks and allows unused UDB resources to be used by other functions for maximum system efficiency.

7.3 UDB Array Description

Figure 7-7 shows an example of a 16 UDB array. In addition to the array core, there are a DSI routing interfaces at the top and bottom of the array. Other interfaces that are not explicitly shown include the system interfaces for bus and clock distribution. The UDB array includes multiple horizontal and vertical routing channels each comprised of 96 wires. The wire connections to UDBs, at horizontal/vertical intersection and at the DSI interface are highly permutable providing efficient automatic routing in PSoC Creator. Additionally the routing allows wire by wire segmentation along the vertical and horizontal routing to further increase routing flexibility and capability.

Figure 7-7. Digital System Interface Structure

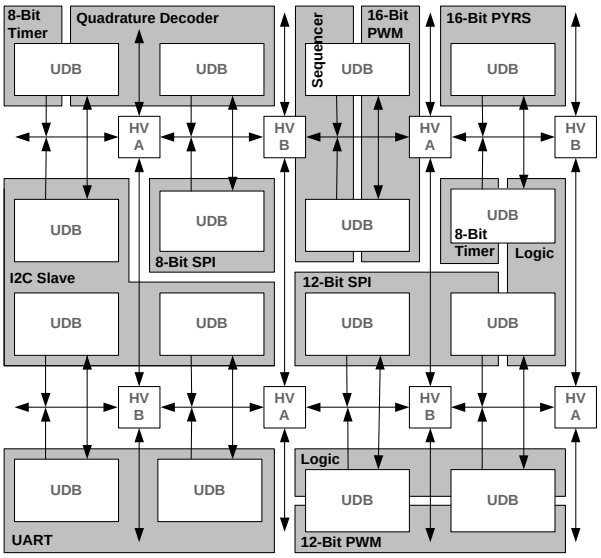


7.3.1 UDB Array Programmable Resources

Figure 7-8 shows an example of how functions are mapped into a bank of 16 UDBs. The primary programmable resources of the UDB are two PLDs, one datapath and one status/control register. These resources are allocated independently, because they have independently selectable clocks, and therefore unused blocks are allocated to other unrelated functions.

An example of this is the 8-bit Timer in the upper left corner of the array. This function only requires one datapath in the UDB, and therefore the PLD resources may be allocated to another function. A function such as a Quadrature Decoder may require more PLD logic than one UDB can supply and in this case can utilize the unused PLD blocks in the 8-bit Timer UDB. Programmable resources in the UDB array are generally homogeneous so functions can be mapped to arbitrary boundaries in the array.

Figure 7-8. Function Mapping Example in a Bank of UDBs



7.4 DSI Routing Interface Description

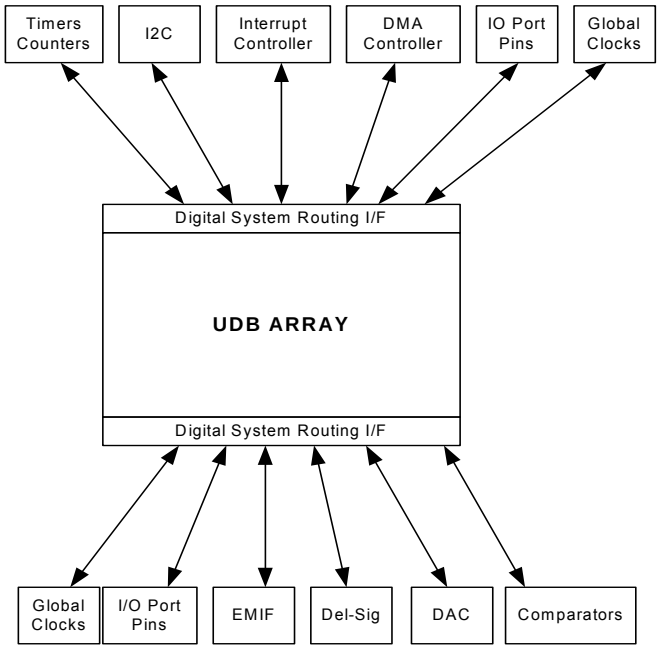
The DSI routing interface is a continuation of the horizontal and vertical routing channels at the top and bottom of the UDB array core. It provides general purpose programmable routing between device peripherals, including UDBs, I/Os, analog peripherals, interrupts, DMA and fixed function peripherals.

Figure 7-9 illustrates the concept of the digital system interconnect, which connects the UDB array routing matrix with other device peripherals. Any digital core or fixed function peripheral that needs programmable routing is connected to this interface.

Signals in this category include:

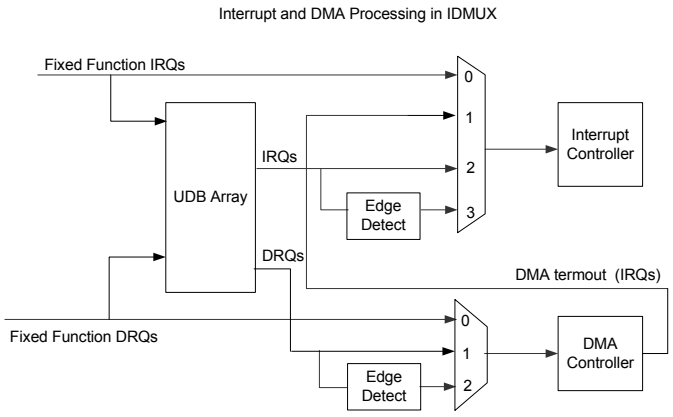
- Interrupt requests from all digital peripherals in the system.
- DMA requests from all digital peripherals in the system.
- Digital peripheral data signals that need flexible routing to I/Os.
- Digital peripheral data signals that need connections to UDBs.
- Connections to the interrupt and DMA controllers.
- Connection to I/O pins.
- Connection to analog system digital signals.

Figure 7-9. Digital System Interconnect



Interrupt and DMA routing is very flexible in the CY8C32 programmable architecture. In addition to the numerous fixed function peripherals that can generate interrupt requests, any data signal in the UDB array routing can also be used to generate a request. A single peripheral may generate multiple independent interrupt requests simplifying system and firmware design. Figure 7-10 shows the structure of the IDMUX (Interrupt/DMA Multiplexer).

Figure 7-10. Interrupt and DMA Processing in the IDMUX



7.4.1 I/O Port Routing

There are a total of 20 DSI routes to a typical 8-bit I/O port, 16 for data and four for drive strength control.

When an I/O pin is connected to the routing, there are two primary connections available, an input and an output. In conjunction with drive strength control, this can implement a bidirectional I/O pin. A data output signal has the option to be single synchronized (pipelined) and a data input signal has the option to be double synchronized. The synchronization clock is the master clock (see Figure 6-1). Normally all inputs from pins are synchronized as this is required if the CPU interacts with the signal or any signal derived from it. Asynchronous inputs have rare uses. An example of this is a feed through of combinational PLD logic from input pins to output pins.

Figure 7-11. I/O Pin Synchronization Routing

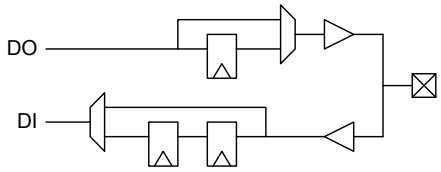
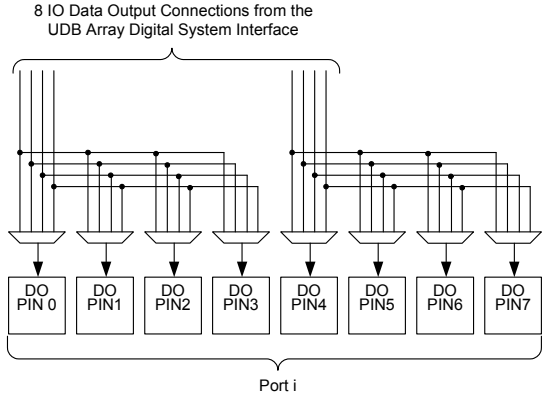
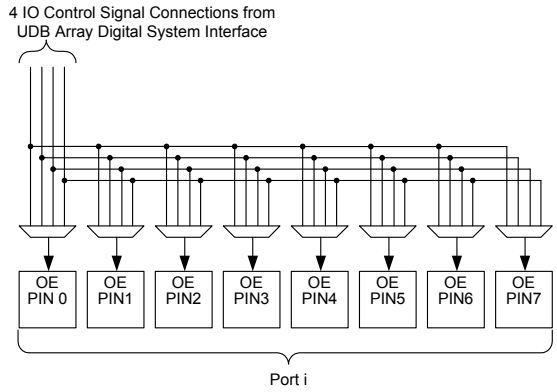


Figure 7-12. I/O Pin Output Connectivity



There are four more DSI connections to a given I/O port to implement dynamic output enable control of pins. This connectivity gives a range of options, from fully ganged 8-bits controlled by one signal, to up to four individually controlled pins. The output enable signal is useful for creating tri-state bidirectional pins and buses.

Figure 7-13. I/O Pin Output Enable Connectivity



7.7 I²C

PSoC includes a single fixed-function I²C peripheral. Additional I²C interfaces can be instantiated using Universal Digital Blocks (UDBs) in PSoC Creator, as required.

The I²C peripheral provides a synchronous two-wire interface designed to interface the PSoC device with a two-wire I²C serial communication bus. It is compatible[13] with I²C Standard-mode, Fast-mode, and Fast-mode Plus devices as defined in the NXP I2C-bus specification and user manual (UM10204). The I²C bus I/O may be implemented with GPIO or SIO in open-drain modes.

To eliminate the need for excessive CPU intervention and overhead, I²C specific support is provided for status detection and generation of framing bits. I²C operates as a slave, a master, or multimaster (Slave and Master)[14]. In slave mode, the unit always listens for a start condition to begin sending or receiving data. Master mode supplies the ability to generate the Start and Stop conditions and initiate transactions. Multimaster mode provides clock synchronization and arbitration to allow multiple masters on the same bus. If Master mode is enabled and Slave mode is not enabled, the block does not generate interrupts on externally generated Start conditions. I²C interfaces through the DSI routing and allows direct connections to any GPIO or SIO pins.

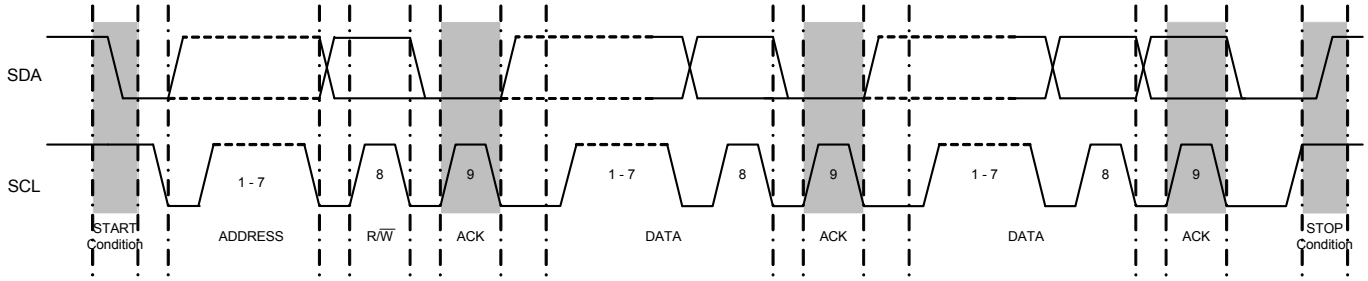
I²C provides hardware address detect of a 7-bit address without CPU intervention. Additionally the device can wake from low-power modes on a 7-bit hardware address match. If wakeup functionality is required, I2C pin connections are limited to one of two specific pairs of SIO pins. See descriptions of SCL and SDA pins in Pin Descriptions on page 12.

I²C features include:

- Slave and Master, Transmitter, and Receiver operation
- Byte processing for low CPU overhead
- Interrupt or polling CPU interface
- Support for bus speeds up to 1 Mbps
- 7 or 10-bit addressing (10-bit addressing requires firmware support)
- SMBus operation (through firmware support – SMBus supported in hardware in UDBs)
- 7-bit hardware address compare
- Wake from low-power modes on address match
- Glitch filtering (active and alternate-active modes only)

Data transfers follow the format shown in Figure 7-16. After the START condition (S), a slave address is sent. This address is 7 bits long followed by an eighth bit which is a data direction bit (R/W) - a 'zero' indicates a transmission (WRITE), a 'one' indicates a request for data (READ). A data transfer is always terminated by a STOP condition (P) generated by the master.

Figure 7-16. I²C Complete Transfer Timing



7.7.1 External Electrical Connections

As Figure 7-17 shows, the I²C bus requires external pull-up resistors (R_P). These resistors are primarily determined by the supply voltage, bus speed, and bus capacitance. For detailed information on how to calculate the optimum pull-up resistor value for your design, we recommend using the UM10204 I2C-bus specification and user manual Rev 6, or newer, available from the NXP website at www.nxp.com.

Notes

13. The I²C peripheral is non-compliant with the NXP I2C specification in the following areas: analog glitch filter, I/O VOL/IOL, I/O hysteresis. The I²C Block has a digital glitch filter (not available in sleep mode). The Fast-mode minimum fall-time specification can be met by setting the I/Os to slow speed mode. See the I/O Electrical Specifications in "Inputs and Outputs" section on page 76 for details.
14. Fixed-block I²C does not support undefined bus conditions, nor does it support Repeated Start in Slave mode. These conditions should be avoided, or the UDB-based I²C component should be used instead.

9.2 Serial Wire Debug Interface

The SWD interface is the preferred alternative to the JTAG interface. It requires only two pins instead of the four or five needed by JTAG. SWD provides all of the programming and debugging features of JTAG at the same speed. SWD does not provide access to scan chains or device chaining. The SWD clock frequency can be up to 1/3 of the CPU clock frequency.

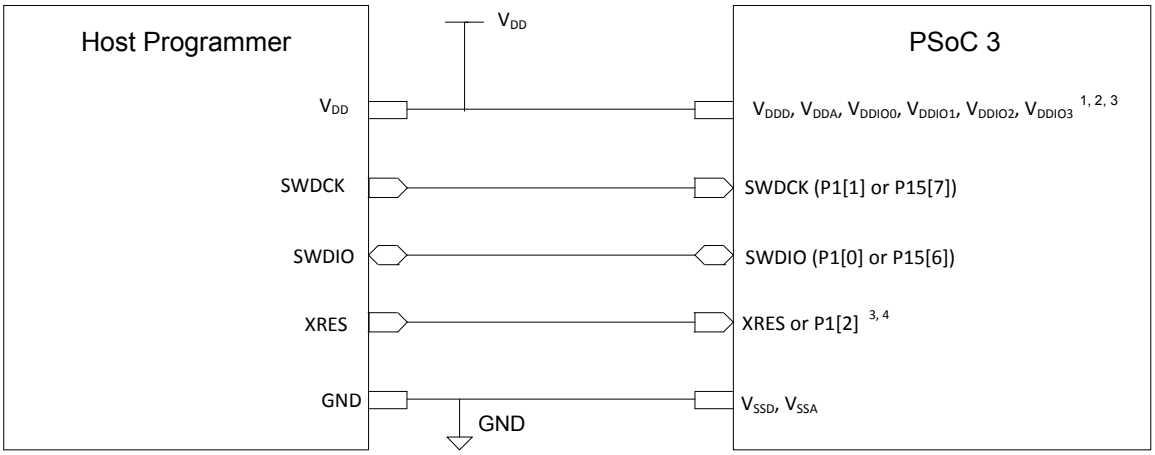
SWD uses two pins, either two of the JTAG pins (TMS and TCK) or the USBIO D+ and D– pins. The USBIO pins are useful for in system programming of USB solutions that would otherwise require a separate programming connector. One pin is used for the data clock and the other is used for data input and output.

SWD can be enabled on only one of the pin pairs at a time. This only happens if, within 8 µs (key window) after reset, that pin pair (JTAG or USB) receives a predetermined acquire sequence of 1s and 0s. If the NVL latches are set for SWD (see *Section 5.5*), this sequence need not be applied to the JTAG pin pair. The acquire sequence must always be applied to the USB pin pair.

SWD is used for debugging or for programming the flash memory.

The SWD interface can be enabled from the JTAG interface or disabled, allowing its pins to be used as GPIO. Unlike JTAG, the SWD interface can always be reacquired on any device during the key window. It can then be used to reenable the JTAG interface, if desired. When using SWD or JTAG pins as standard GPIO, make sure that the GPIO functionality and PCB circuits do not interfere with SWD or JTAG use.

Figure 9-2. SWD Interface Connections between PSoC 3 and Programmer



[1] The voltage levels of the Host Programmer and the PSoC 3 voltage domains involved in Programming should be the same. XRES pin (XRES_N or P1[2]) is powered by V_{DDIO1}. The USB SWD pins are powered by V_{DDD}. So for Programming using the USB SWD pins with XRES pin, the V_{DDD}, V_{DDIO1} of PSoC 3 should be at the same voltage level as Host V_{DD}. Rest of PSoC 3 voltage domains (V_{DDA}, V_{DDIO0}, V_{DDIO2}, V_{DDIO3}) need not be at the same voltage level as host Programmer. The Port 1 SWD pins are powered by V_{DDIO1}. So V_{DDIO1} of PSoC 3 should be at same voltage level as host V_{DD} for Port 1 SWD programming. Rest of PSoC 3 voltage domains (V_{DDD}, V_{DDA}, V_{DDIO0}, V_{DDIO2}, V_{DDIO3}) need not be at the same voltage level as host Programmer.

[2] Vdda must be greater than or equal to all other power supplies (Vddd, Vddio's) in PSoC 3.

[3] For Power cycle mode Programming, XRES pin is not required. But the Host programmer must have the capability to toggle power (Vddd, Vdda, All Vddio's) to PSoC 3. This may typically require external interface circuitry to toggle power which will depend on the programming setup. The power supplies can be brought up in any sequence, however, once stable, VDDA must be greater than or equal to all other supplies.

[4] P1[2] will be configured as XRES by default only for 48-pin devices (without dedicated XRES pin). For devices with dedicated XRES pin, P1[2] is GPIO pin by default. So use P1[2] as Reset pin only for 48-pin devices, but use dedicated XRES pin for rest of devices.

11.2 Device Level Specifications

Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

11.2.1 Device Level Specifications

Table 11-2. DC Specifications

Parameter	Description	Conditions		Min	Typ[22]	Max	Units
V_{DDA}	Analog supply voltage and input to analog core regulator	Analog core regulator enabled		1.8	–	5.5	V
V_{DDA}	Analog supply voltage, analog regulator bypassed	Analog core regulator disabled		1.71	1.8	1.89	V
V_{DDD}	Digital supply voltage relative to V_{SSD}	Digital core regulator enabled		1.8	–	V_{DDA}[18]	V
				–	–	V_{DDA} + 0.1[24]	
V_{DDD}	Digital supply voltage, digital regulator bypassed	Digital core regulator disabled		1.71	1.8	1.89	V
V_{DDIO}[19]	I/O supply voltage relative to V_{SSIO}			1.71	–	V_{DDA}[18]	V
				–	–	V_{DDA} + 0.1[24]	
V_{CCA}	Direct analog core voltage input (Analog regulator bypass)	Analog core regulator disabled		1.71	1.8	1.89	V
V_{CCD}	Direct digital core voltage input (Digital regulator bypass)	Digital core regulator disabled		1.71	1.8	1.89	V
I_{DD} [20, 21]	**Active Mode**						
	Only IMO and CPU clock enabled. CPU executing simple loop from instruction buffer.	V_{DDX} = 2.7 V – 5.5 V; F_{CPU} = 6 MHz[23]	T = –40 °C	–	1.2	2.9	mA
			T = 25 °C	–	1.2	3.1	
			T = 85 °C	–	4.9	7.7	
	IMO enabled, bus clock and CPU clock enabled. CPU executing program from flash.	V_{DDX} = 2.7 V – 5.5 V; F_{CPU} = 3 MHz[23]	T = –40 °C	–	1.3	2.9	
			T = 25 °C	–	1.6	3.2	
			T = 85 °C	–	4.8	7.5	
		V_{DDX} = 2.7 V – 5.5 V; F_{CPU} = 6 MHz	T = –40 °C	–	2.1	3.7	
			T = 25 °C	–	2.3	3.9	
			T = 85 °C	–	5.6	8.5	
		V_{DDX} = 2.7 V – 5.5 V; F_{CPU} = 12 MHz[23]	T = –40 °C	–	3.5	5.2	
			T = 25 °C	–	3.8	5.5	
			T = 85 °C	–	7.1	9.8	
		V_{DDX} = 2.7 V – 5.5 V; F_{CPU} = 24 MHz[23]	T = –40 °C	–	6.3	8.1	
			T = 25 °C	–	6.6	8.3	
			T = 85 °C	–	10	13	
		V_{DDX} = 2.7 V – 5.5 V; F_{CPU} = 48 MHz[23]	T = –40 °C	–	11.5	13.5	
			T = 25 °C	–	12	14	
			T = 85 °C	–	15.5	18.5	

Notes

18. The power supplies can be brought up in any sequence however once stable V_{DDA} must be greater than or equal to all other supplies.
19. The V_{DDIO} supply voltage must be greater than the maximum voltage on the associated GPIO pins. Maximum voltage on GPIO pin ≤ V_{DDIO} ≤ V_{DDA}.
20. Total current for all power domains: digital (I_{DDD}), analog (I_{DDA}), and I/Os ($I_{DDIO0, 1, 2, 3}$). Boost not included. All I/Os floating.
21. The current consumption of additional peripherals that are implemented only in programmed logic blocks can be found in their respective datasheets, available in PSoC Creator, the integrated design environment. To estimate total current, find the CPU current at the frequency of interest and add peripheral currents for your particular system from the device datasheet and component datasheets.
22. V_{DDX} = 3.3 V.
23. Based on device characterizations (Not production tested).
24. Guaranteed by design, not production tested.

Table 11-7. Recommended External Components for Boost Circuit

Parameter	Description	Conditions	Min	Typ	Max	Units
L_{BOOST}	Boost inductor	4.7 µH nominal	3.7	4.7	5.7	µH
		10 µH nominal	8.0	10.0	12.0	µH
		22 µH nominal	17.0	22.0	27.0	µH
C_{BOOST}	Total capacitance sum of V_{DDD}, V_{DDA}, V_{DDIO}[34]		17.0	26.0	31.0	µF
C_{BAT}	Battery filter capacitor		17.0	22.0	27.0	µF
I_F	Schottky diode average forward current		1.0	–	–	A
V_R	Schottky reverse voltage		20.0	–	–	V

Figure 11-8. T_A range over V_{BAT} and V_{OUT}

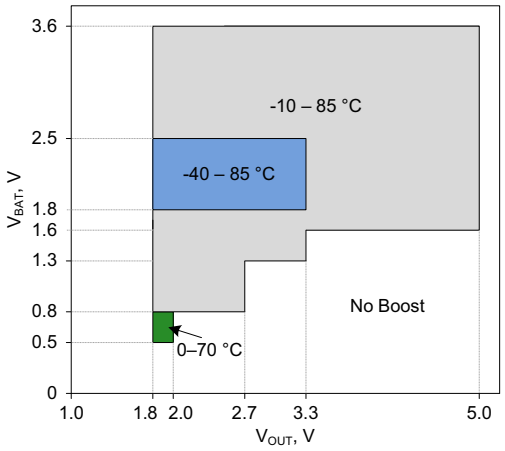


Figure 11-9. I_{OUT} range over V_{BAT} and V_{OUT}

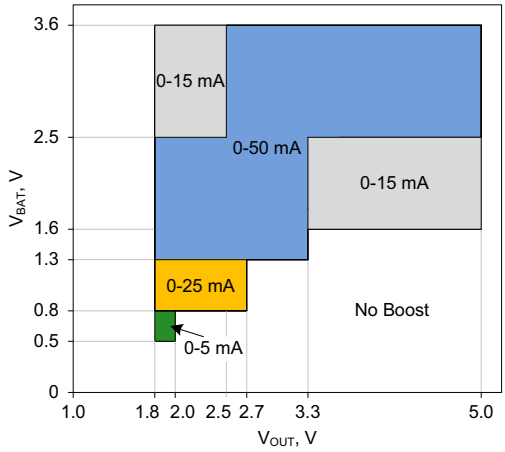
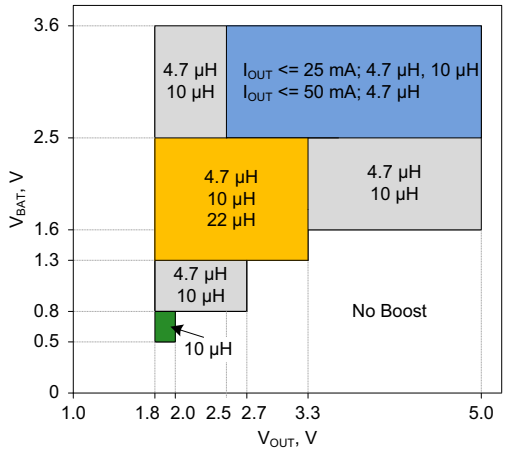


Figure 11-10. L_{BOOST} values over V_{BAT} and V_{OUT}



Note
34. Based on device characterization (Not production tested).

Table 11-12. SIO AC Specifications *(continued)*

Parameter	Description	Conditions	Min	Typ	Max	Units
Fsioout	SIO output operating frequency					
	2.7 V < V_{DDIO} < 5.5 V, Unregulated output (GPIO) mode, fast strong drive mode	90/10% V_{DDIO} into 25 pF	–	–	33	MHz
	1.71 V < V_{DDIO} < 2.7 V, Unregulated output (GPIO) mode, fast strong drive mode	90/10% V_{DDIO} into 25 pF	–	–	16	MHz
	3.3 V < V_{DDIO} < 5.5 V, Unregulated output (GPIO) mode, slow strong drive mode	90/10% V_{DDIO} into 25 pF	–	–	5	MHz
	1.71 V < V_{DDIO} < 3.3 V, Unregulated output (GPIO) mode, slow strong drive mode	90/10% V_{DDIO} into 25 pF	–	–	4	MHz
	2.7 V < V_{DDIO} < 5.5 V, Regulated output mode, fast strong drive mode	Output continuously switching into 25 pF	–	–	20	MHz
	1.71 V < V_{DDIO} < 2.7 V, Regulated output mode, fast strong drive mode	Output continuously switching into 25 pF	–	–	10	MHz
	1.71 V < V_{DDIO} < 5.5 V, Regulated output mode, slow strong drive mode	Output continuously switching into 25 pF	–	–	2.5	MHz
Fsioin	SIO input operating frequency					
	1.71 V ≤ V_{DDIO} ≤ 5.5 V	90/10% V_{DDIO}	–	–	33	MHz

Figure 11-20. SIO Output Rise and Fall Times, Fast Strong Mode, V_{DDIO} = 3.3 V, 25 pF Load

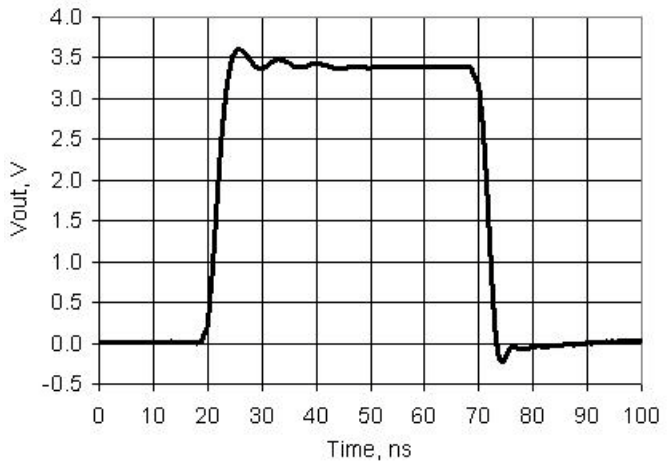


Figure 11-21. SIO Output Rise and Fall Times, Slow Strong Mode, V_{DDIO} = 3.3 V, 25 pF Load

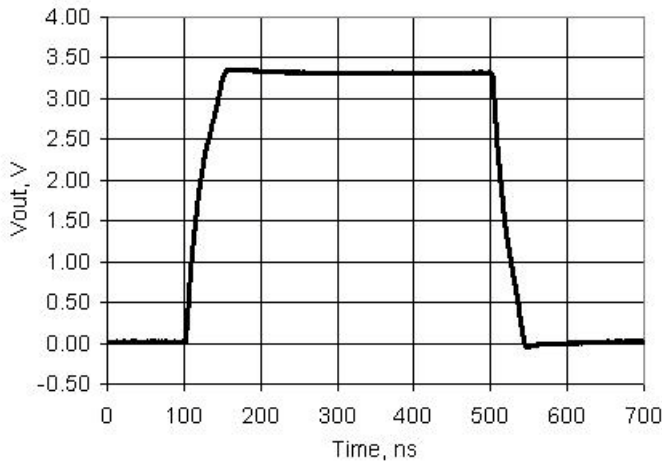


Table 11-13. SIO Comparator Specifications[42]

Parameter	Description	Conditions	Min	Typ	Max	Units
Vos	Offset voltage	V_{DDIO} = 2 V	–	–	68	mV
		V_{DDIO} = 2.7 V	–	–	72	
		V_{DDIO} = 5.5 V	–	–	82	
TCVos	Offset voltage drift with temp		–	–	250	µV/°C
CMRR	Common mode rejection ratio	V_{DDIO} = 2 V	30	–	–	dB
		V_{DDIO} = 2.7 V	35	–	–	
		V_{DDIO} = 5.5 V	40	–	–	
Tresp	Response time		–	–	30	ns

11.4.3 USBIO

For operation in GPIO mode, the standard range for V_{DDD} applies, see Device Level Specifications on page 68.

Table 11-14. USBIO DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Rusbi	USB D+ pull-up resistance	With idle bus	0.900	–	1.575	kΩ
Rusba	USB D+ pull-up resistance	While receiving traffic	1.425	–	3.090	kΩ
Vohusb	Static output high	15 kΩ ±5% to Vss, internal pull-up enabled	2.8	–	3.6	V
Volusb	Static output low	15 kΩ ±5% to Vss, internal pull-up enabled	–	–	0.3	V
Vohgpio	Output voltage high, GPIO mode	I_{OH} = 4 mA, $V_{DDD} \geq$ 3 V	2.4	–	–	V
Volgpio	Output voltage low, GPIO mode	I_{OL} = 4 mA, $V_{DDD} \geq$ 3 V	–	–	0.3	V
Vdi	Differential input sensitivity	|(D+)–(D–)|	–	–	0.2	V
Vcm	Differential input common mode range	–	0.8	–	2.5	V
Vse	Single ended receiver threshold	–	0.8	–	2	V
Rps2	PS/2 pull-up resistance	In PS/2 mode, with PS/2 pull-up enabled	3	–	7	kΩ
Rext	External USB series resistor	In series with each USB pin	21.78 (–1%)	22	22.22 (+1%)	Ω
Zo	USB driver output impedance	Including Rext	28	–	44	Ω
C_{IN}	USB transceiver input capacitance	–	–	–	20	pF
I_{IL}[42]	Input leakage current (absolute value)	25 °C, V_{DDD} = 3.0 V	–	–	2	nA

Note
42. Based on device characterization (Not production tested).

11.5 Analog Peripherals

Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

11.5.1 Delta-sigma ADC

Unless otherwise specified, operating conditions are:

- Operation in continuous sample mode
- fclk = 6.144 MHz
- Reference = 1.024 V internal reference bypassed on P3.2 or P0.3
- Unless otherwise specified, all charts and graphs show typical values

Table 11-19. 12-bit Delta-sigma ADC DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Resolution		8	–	12	bits
	Number of channels, single ended		–	–	No. of GPIO	–
	Number of channels, differential	Differential pair is formed using a pair of GPIOs.	–	–	No. of GPIO/2	–
	Monotonic	Yes	–	–	–	–
Ge	Gain error	Buffered, buffer gain = 1, Range = ±1.024 V, 25 °C	–	–	±0.2	%
Gd	Gain drift	Buffered, buffer gain = 1, Range = ±1.024 V	–	–	50	ppm/°C
Vos	Input offset voltage	Buffered, 12-bit mode	–	–	±0.1	mV
TCVos	Temperature coefficient, input offset voltage	Buffer gain = 1, 12-bit, Range = ±1.024 V	–	–	1	µV/°C
	Input voltage range, single ended[45]		V_{SSA}	–	V_{DDA}	V
	Input voltage range, differential unbuffered[45]		V_{SSA}	–	V_{DDA}	V
	Input voltage range, differential, buffered[45]		V_{SSA}	–	V_{DDA} – 1	V
INL12	Integral non linearity[45]	Range = ±1.024 V, unbuffered	–	–	±1	LSB
DNL12	Differential non linearity[45]	Range = ±1.024 V, unbuffered	–	–	±1	LSB
INL8	Integral non linearity[45]	Range = ±1.024 V, unbuffered	–	–	±1	LSB
DNL8	Differential non linearity[45]	Range = ±1.024 V, unbuffered	–	–	±1	LSB
Rin_Buff	ADC input resistance	Input buffer used	10	–	–	MΩ
Rin_ADC12	ADC input resistance	Input buffer bypassed, 12 bit, Range = ±1.024 V	–	148[46]	–	kΩ
Rin_ExtRef	ADC external reference input resistance		–	70[46, 47]	–	kΩ
Vextref	ADC external reference input voltage, see also internal reference in Voltage Reference on page 86	Pins P0[3], P3[2]	0.9	–	1.3	V
Current Consumption						
I_{DD_12}	I_{DDA} + I_{DDD} current consumption, 12 bit[45]	192 ksps, unbuffered	–	–	1.95	mA
I_{BUFF}	Buffer current consumption[45]		–	–	2.5	mA

Notes

45. Based on device characterization (not production tested).
46. By using switched capacitors at the ADC input an effective input resistance is created. Holding the gain and number of bits constant, the resistance is proportional to the inverse of the clock frequency. This value is calculated, not measured. For more information see the Technical Reference Manual.
47. Recommend an external reference device with an output impedance <100 Ω, for example, the LM185/285/385 family. A 1-µF capacitor is recommended. For more information, see AN61290 - PSoC® 3 and PSoC 5LP Hardware Design Considerations.

Table 11-26. IDAC DC Specifications *(continued)*

Parameter	Description	Conditions	Min	Typ	Max	Units
I_{DD}	Operating current, code = 0	Low speed mode, source mode, range = 31.875 µA	–	44	100	µA
		Low speed mode, source mode, range = 255 µA,	–	33	100	µA
		Low speed mode, source mode, range = 2.04 mA	–	33	100	µA
		Low speed mode, sink mode, range = 31.875 µA	–	36	100	µA
		Low speed mode, sink mode, range = 255 µA	–	33	100	µA
		Low speed mode, sink mode, range = 2.04 mA	–	33	100	µA
		High speed mode, source mode, range = 31.875 µA	–	310	500	µA
		High speed mode, source mode, range = 255 µA	–	305	500	µA
		High speed mode, source mode, range = 2.04 mA	–	305	500	µA
		High speed mode, sink mode, range = 31.875 µA	–	310	500	µA
		High speed mode, sink mode, range = 255 µA	–	300	500	µA
		High speed mode, sink mode, range = 2.04 mA	–	300	500	µA

Figure 11-26. IDAC INL vs Input Code, Range = 255 µA, Source Mode

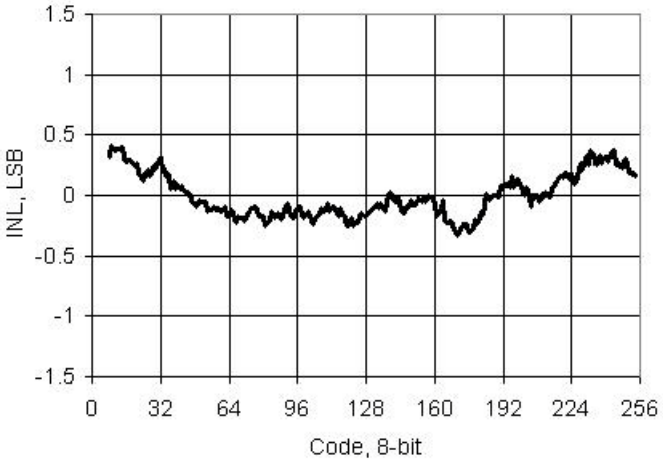


Figure 11-27. IDAC INL vs Input Code, Range = 255 µA, Sink Mode

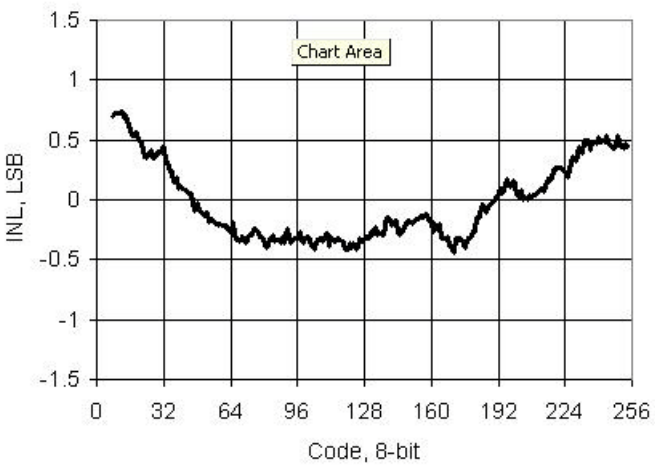


Table 11-27. IDAC AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
F_{DAC}	Update rate		–	–	8	Msps
T_{SETTLE}	Settling time to 0.5 LSB	Range = 31.875 µA or 255 µA, full scale transition, High speed mode, 600 Ω 15-pF load	–	–	125	ns
	Current noise	Range = 255 µA, source mode, High speed mode, V_{DDA} = 5 V, 10 kHz	–	340	–	pA/sqrtHz

Figure 11-36. IDAC Step Response, Codes 0x40 - 0xC0, 255 µA Mode, Source Mode, High speed mode, V_{DDA} = 5 V

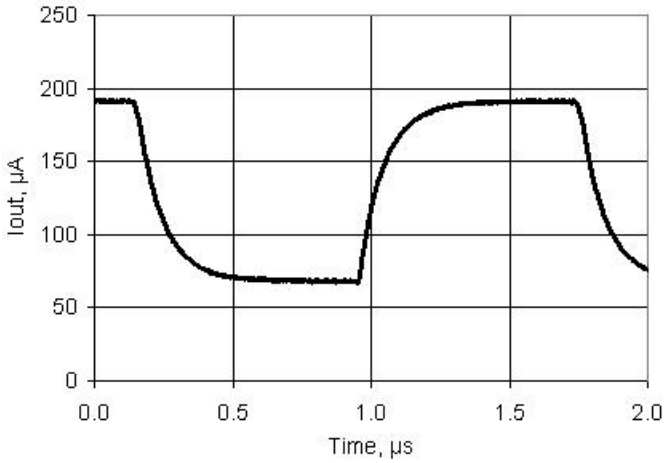


Figure 11-37. IDAC Glitch Response, Codes 0x7F - 0x80, 255 µA Mode, Source Mode, High speed mode, V_{DDA} = 5 V

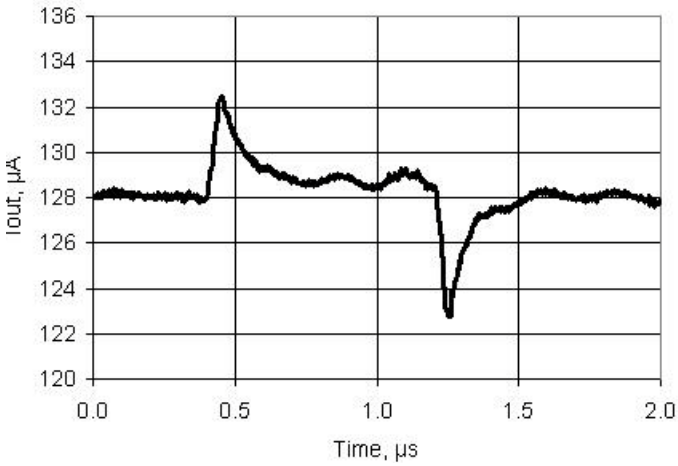


Figure 11-38. IDAC PSRR vs Frequency

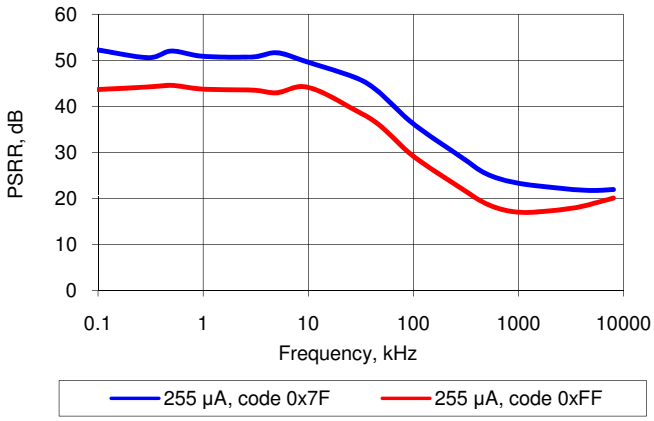


Figure 11-39. IDAC Current Noise, 255 µA Mode, Source Mode, High speed mode, V_{DDA} = 5 V