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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | 8051 |
| Core Size | 8-Bit |
| Speed | 50MHz |
| Connectivity | EBI/EMI, I²C, LINbus, SPI, UART/USART |
| Peripherals | CapSense, DMA, LCD, POR, PWM, WDT |
| Number of I/O | 25 |
| Program Memory Size | 16KB (16K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 512 x 8 |
| RAM Size | 2K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.71V ~ 5.5V |
| Data Converters | A/D 16x12b; D/A 1x8b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 48-BSSOP (0.295", 7.50mm Width) |
| Supplier Device Package | 48-SSOP |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/cy8c3244pvi-133 |

## More Information

Cypress provides a wealth of data at www.cypress.com to help you to select the right PSoC device for your design, and to help you to quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the knowledge base article KBA86521, How to Design with PSoC 3, PSoC 4, and PSoC 5LP. Following is an abbreviated list for PSoC 3:

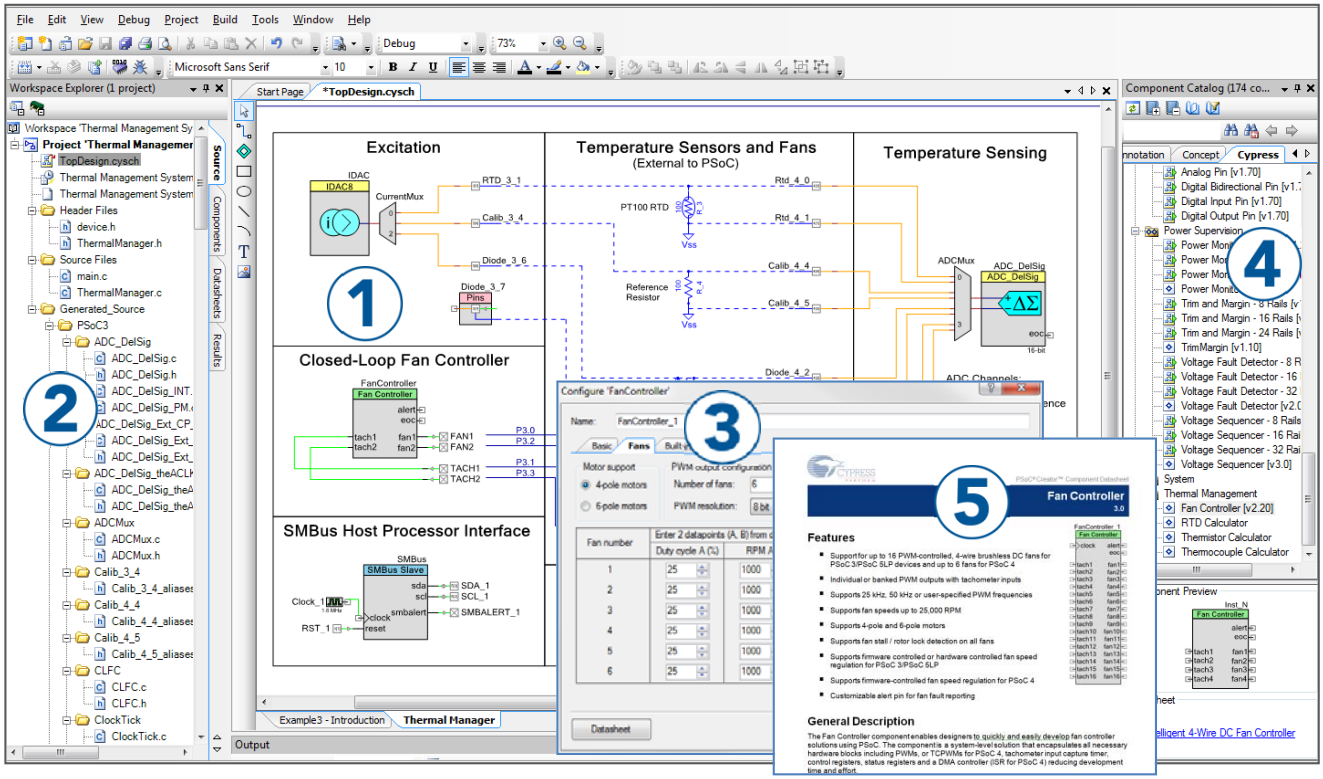
- Overview: PSoC Portfolio, PSoC Roadmap
- Product Selectors: PSoC 1, PSoC 3, PSoC 4, PSoC 5LP
  In addition, PSoC Creator includes a device selection tool.
- Application notes: Cypress offers a large number of PSoC application notes and code examples covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with PSoC 3 are:
  - AN54181: Getting Started With PSoC 3
  - AN61290: Hardware Design Considerations
  - AN57821: Mixed Signal Circuit Board Layout
  - AN58304: Pin Selection for Analog Designs
  - AN81623: Digital Design Best Practices
  - AN73854: Introduction To Bootloaders
- Development Kits:
  - CY8CKIT-030 is designed for analog performance, for developing high-precision analog, low-power, and low-voltage applications.
  - CY8CKIT-001 provides a common development platform for any one of the PSoC 1, PSoC 3, PSoC 4, or PSoC 5LP families of devices.
  - The MiniProg3 device provides an interface for flash programming and debug.
- Technical Reference Manuals (TRM)
  - Architecture TRM
  - Registers TRM
  - Programming Specification

## PSoC Creator

PSoC Creator is a free Windows-based Integrated Design Environment (IDE). It enables concurrent hardware and firmware design of PSoC 3, PSoC 4, and PSoC 5LP based systems. Create designs using classic, familiar schematic capture supported by over 100 pre-verified, production-ready PSoC Components; see the list of component datasheets. With PSoC Creator, you can:

1. Drag and drop component icons to build your hardware system design in the main design workspace
2. Codesign your application firmware with the PSoC hardware, using the PSoC Creator IDE C compiler
3. Configure components using the configuration tools
4. Explore the library of 100+ components
5. Review component datasheets

**Figure 1. Multiple-Sensor Example Project in PSoC Creator**



This enables the device to be powered directly from a single battery or solar cell. In addition, you can use the boost converter to generate other voltages required by the device, such as a 3.3-V supply for LCD glass drive. The boost's output is available on the $V_{BOOST}$ pin, allowing other devices in the application to be powered from the PSoC.

PSoC supports a wide range of low-power modes. These include a 200-nA hibernate mode with RAM retention and a 1-µA sleep mode with RTC. In the second mode the optional 32.768-kHz watch crystal runs continuously and maintains an accurate RTC.

Power to all major functional blocks, including the programmable digital and analog peripherals, can be controlled independently by firmware. This allows low-power background processing when some peripherals are not in use. This, in turn, provides a total device current of only 1.2 mA when the CPU is running at 6 MHz, or 0.8 mA running at 3 MHz.

The details of the PSoC power modes are covered in the "Power System" section on page 31 of this datasheet.

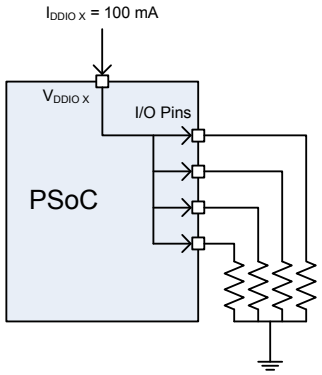
PSoC uses JTAG (4-wire) or SWD (2-wire) interfaces for programming, debug, and test. The 1-wire SWV may also be used for "printf" style debugging. By combining SWD and SWV, you can implement a full debugging interface with just three pins. Using these standard interfaces enables you to debug or program the PSoC with a variety of hardware solutions from Cypress or third party vendors. PSoC supports on-chip break points and 4-KB instruction and data race memory for debug. Details of the programming, test, and debugging interfaces are discussed in the "Programming, Debug Interfaces, Resources" section on page 62 of this datasheet.

## 2. Pinouts

Each VDDIO pin powers a specific set of I/O pins. (The USBIOs are powered from VDDD.) Using the VDDIO pins, a single PSoC can support multiple voltage levels, reducing the need for off-chip level shifters. The black lines drawn on the pinout diagrams in Figure 2-3 through Figure 2-6, as well as Table 2-1, show the pins that are powered by each VDDIO.

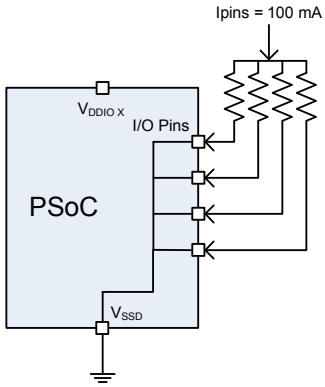
Each VDDIO may source up to 100 mA total to its associated I/O pins, as shown in Figure 2-1.

**Figure 2-1. VDDIO Current Limit**



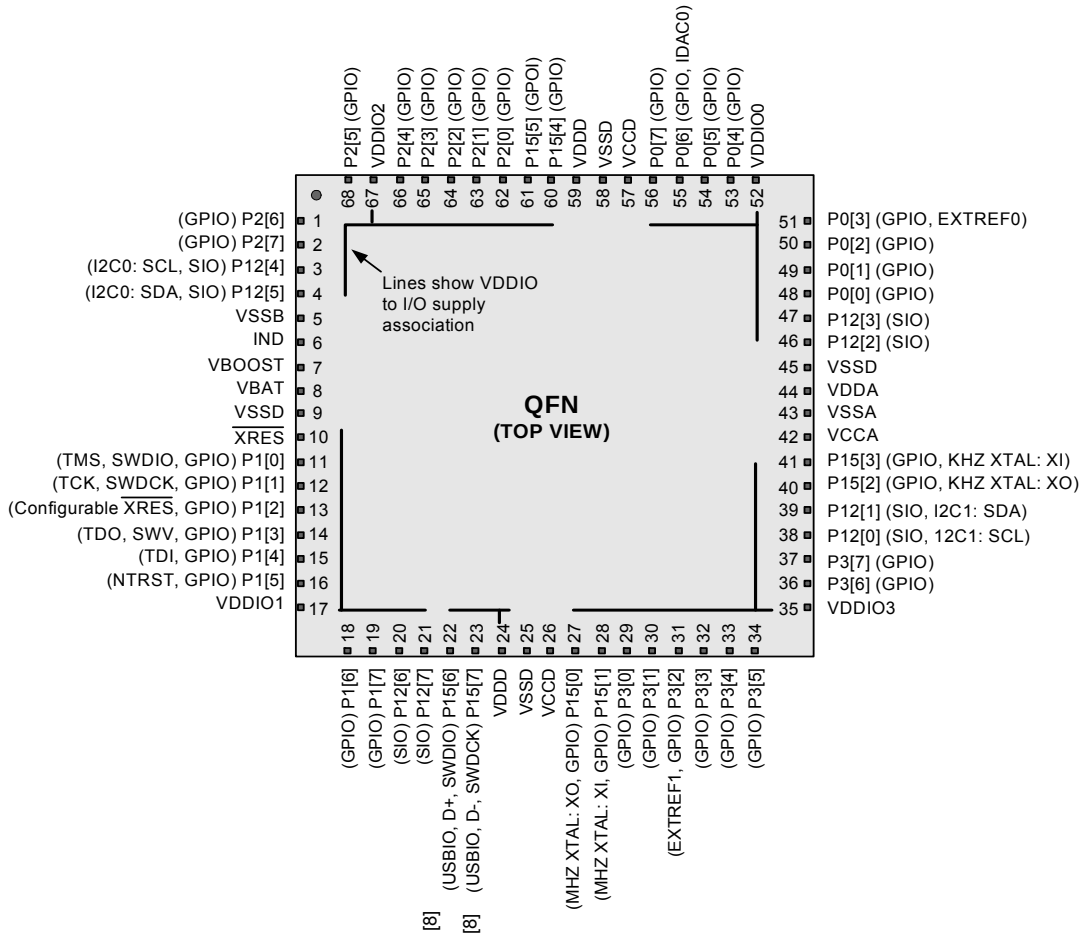

Conversely, for the 100-pin and 68-pin devices, the set of I/O pins associated with any VDDIO may sink up to 100 mA total, as shown in Figure 2-2.

**Figure 2-2. I/O Pins Current Limit**




For the 48-pin devices, the set of I/O pins associated with VDDIO0 plus VDDIO2 may sink up to 100 mA total. The set of I/O pins associated with VDDIO1 plus VDDIO3 may sink up to a total of 100 mA.

**Figure 2-5. 68-pin QFN Part Pinout**[7]




**Notes**

7. The center pad on the QFN package should be connected to digital ground (VSSD) for best mechanical, thermal, and electrical performance. If not connected to ground, it should be electrically floated and not connected to any other signal. For more information, see AN72845, Design Guidelines for QFN Devices.
8. Pins are Do Not Use (DNU) on devices without USB. The pin must be left floating.

**Figure 2-6. 100-pin TQFP Part Pinout**

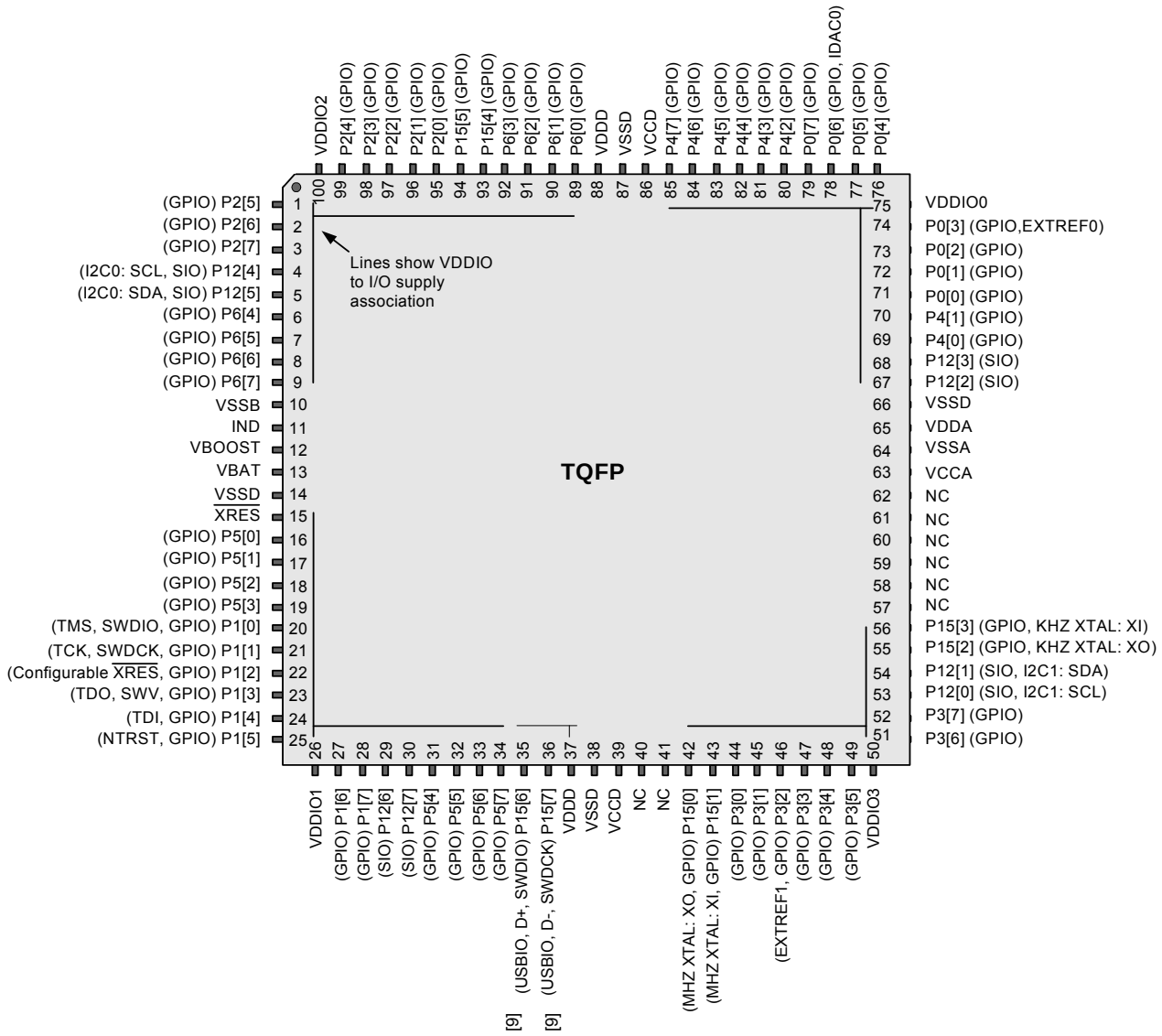
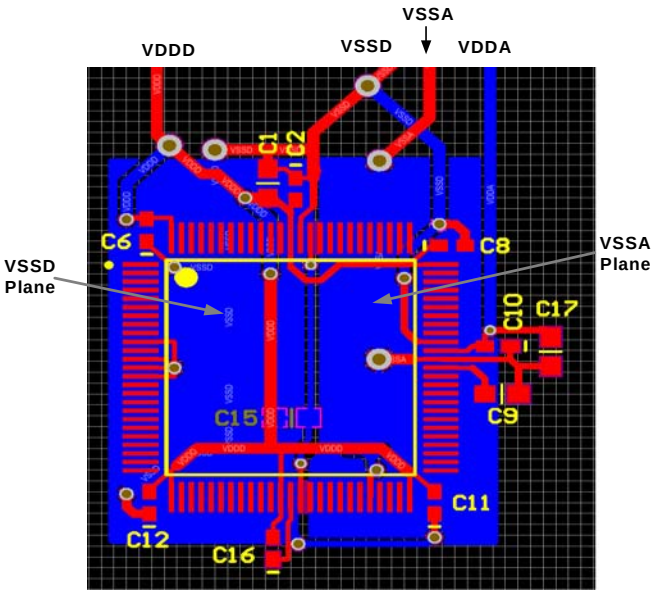



**Table 2-1. VDDIO and Port Pin Associations**

| VDDIO | Port Pins |
|---|---|
| VDDIO0 | P0[7:0], P4[7:0], P12[3:2] |
| VDDIO1 | P1[7:0], P5[7:0], P12[7:6] |
| VDDIO2 | P2[7:0], P6[7:0], P12[5:4], P15[5:4] |
| VDDIO3 | P3[7:0], P12[1:0], P15[3:0] |
| VDDD | P15[7:6] (USB D+, D-) |

**Note**
9. Pins are Do Not Use (DNU) on devices without USB. The pin must be left floating.

**Figure 2-8. Example PCB Layout for 100-pin TQFP Part for Optimal Analog Performance**




## 3. Pin Descriptions

**IDAC0**

Low resistance output pin for high current DAC (IDAC).

**Extref0, Extref1**

External reference input to the analog system.

**GPIO**

General purpose I/O pin provides interfaces to the CPU, digital peripherals, analog peripherals, interrupts, LCD segment drive, and CapSense.

**I2C0: SCL, I2C1: SCL**

$I^2C$ SCL line providing wake from sleep on an address match. Any I/O pin can be used for $I^2C$ SCL if wake from sleep is not required.

**I2C0: SDA, I2C1: SDA**

$I^2C$ SDA line providing wake from sleep on an address match. Any I/O pin can be used for $I^2C$ SDA if wake from sleep is not required.

**Ind**

Inductor connection to boost pump.

**kHz XTAL: Xo, kHz XTAL: Xi**

32.768-kHz crystal oscillator pin.

**MHz XTAL: Xo, MHz XTAL: Xi**

4- to 25- MHz crystal oscillator pin.

**nTRST**

Optional JTAG test reset programming and debug port connection to reset the JTAG connection.

**SIO**

Special I/O provides interfaces to the CPU, digital peripherals and interrupts with a programmable high threshold voltage, analog comparator, high sink current, and high impedance state when the device is unpowered.

**SWDCK**

Serial wire debug clock programming and debug port connection.

**SWDIO**

Serial wire debug input and output programming and debug port connection.

**SWV.**

Single wire viewer debug output.

**TCK**

JTAG test clock programming and debug port connection.

**TDI**

JTAG test data in programming and debug port connection.

**TDO**

JTAG test data out programming and debug port connection.

**TMS**

JTAG test mode select programming and debug port connection.

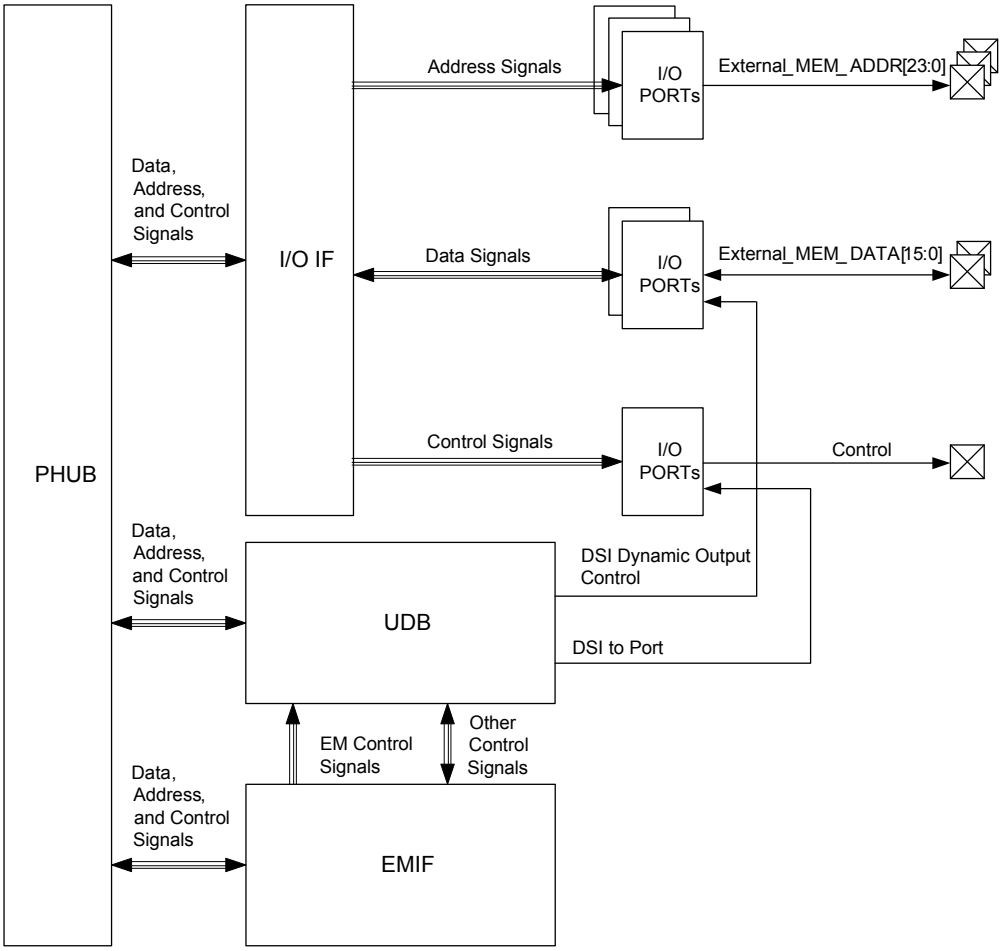
## 5.6 External Memory Interface

CY8C32 provides an external memory interface (EMIF) for connecting to external memory devices. The connection allows read and write accesses to external memories. The EMIF operates in conjunction with UDBs, I/O ports, and other hardware to generate external memory address and control signals. At 33 MHz, each memory access cycle takes four bus clock cycles.

Figure 5-1 is the EMIF block diagram. The EMIF supports synchronous and asynchronous memories. The CY8C32 supports only one type of external memory device at a time.

External memory can be accessed via the 8051 xdata space; up to 24 address bits can be used. See "xdata Space" section on page 28. The memory can be 8 or 16 bits wide.

**Figure 5-1. EMIF Block Diagram**




## 5.7 Memory Map

The CY8C32 8051 memory map is very similar to the MCS-51 memory map.

### *5.7.1 Code Space*

The CY8C32 8051 code space is 64 KB. Only main flash exists in this space. See the "Flash Program Memory" section on page 24.

### *5.7.2 Internal Data Space*

The CY8C32 8051 internal data space is 384 bytes, compressed within a 256-byte space. This space consists of 256 bytes of RAM (in addition to the SRAM mentioned in Static RAM on page 24) and a 128-byte space for Special Function Registers (SFRs). See Figure 5-2. The lowest 32 bytes are used for 4 banks of registers R0-R7. The next 16 bytes are bit-addressable.

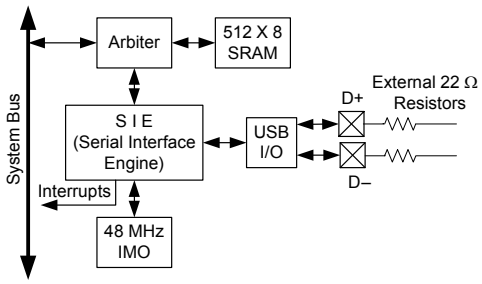
## 7.5 USB

PSoC includes a dedicated Full-Speed (12 Mbps) USB 2.0 transceiver supporting all four USB transfer types: control, interrupt, bulk, and isochronous. PSoC Creator provides full configuration support. USB interfaces to hosts through two dedicated USBIO pins, which are detailed in the "I/O System and Routing" section on page 37.

USB includes the following features:

- Eight unidirectional data endpoints
- One bidirectional control endpoint 0 (EP0)
- Shared 512-byte buffer for the eight data endpoints
- Dedicated 8-byte buffer for EP0
- Three memory modes
  - Manual Memory Management with No DMA Access
  - Manual Memory Management with Manual DMA Access
  - Automatic Memory Management with Automatic DMA Access
- Internal 3.3 V regulator for transceiver
- Internal 48 MHz main oscillator mode that auto locks to USB bus clock, requiring no external crystal for USB (USB equipped parts only)
- Interrupts on bus and each endpoint event, with device wakeup
- USB Reset, Suspend, and Resume operations
- Bus powered and self powered modes

**Figure 7-14. USB**




## 7.6 Timers, Counters, and PWMs

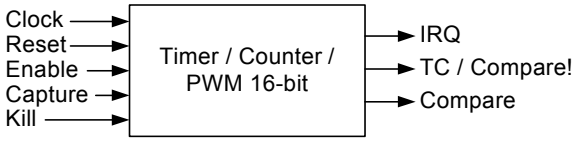
The Timer/Counter/PWM peripheral is a 16-bit dedicated peripheral providing three of the most common embedded peripheral features. As almost all embedded systems use some combination of timers, counters, and PWMs. Four of them have been included on this PSoC device family. Additional and more advanced functionality timers, counters, and PWMs can also be instantiated in Universal Digital Blocks (UDBs) as required. PSoC Creator allows you to choose the timer, counter, and PWM features that they require. The tool set utilizes the most optimal resources available.

The Timer/Counter/PWM peripheral can select from multiple clock sources, with input and output signals connected through the DSI routing. DSI routing allows input and output connections to any device pin and any internal digital signal accessible through the DSI. Each of the four instances has a compare output, terminal count output (optional complementary compare output), and programmable interrupt request line. The Timer/Counter/PWMs are configurable as free running, one shot, or Enable input controlled. The peripheral has timer reset and capture inputs, and a kill input for control of the comparator outputs. The peripheral supports full 16-bit capture.

Timer/Counter/PWM features include:

- 16-bit Timer/Counter/PWM (down count only)
- Selectable clock source
- PWM comparator (configurable for LT, LTE, EQ, GTE, GT)
- Period reload on start, reset, and terminal count
- Interrupt on terminal count, compare true, or capture
- Dynamic counter reads
- Timer capture mode
- Count while enable signal is asserted mode
- Free run mode
- One Shot mode (stop at end of period)
- Complementary PWM outputs with deadband
- PWM output kill

**Figure 7-15. Timer/Counter/PWM**



# 9. Programming, Debug Interfaces, Resources

PSoC devices include extensive support for programming, testing, debugging, and tracing both hardware and firmware. Three interfaces are available: JTAG, SWD, and SWV. JTAG and SWD support all programming and debug features of the device. JTAG also supports standard JTAG scan chains for board level test and chaining multiple JTAG devices to a single JTAG connection.

For more information on PSoC 3 Programming, refer to the PSoC® 3 Device Programming Specifications.

Complete Debug on Chip (DoC) functionality enables full device debugging in the final system using the standard production device. It does not require special interfaces, debugging pods, simulators, or emulators. Only the standard programming connections are required to fully support debug.

The PSoC Creator IDE software provides fully integrated programming and debug support for PSoC devices. The low cost MiniProg3 programmer and debugger is designed to provide full programming and debug support of PSoC devices in conjunction with the PSoC Creator IDE. PSoC JTAG, SWD, and SWV interfaces are fully compatible with industry standard third party tools.

All DOC circuits are disabled by default and can only be enabled in firmware. If not enabled, the only way to reenable them is to erase the entire device, clear flash protection, and reprogram the device with new firmware that enables DOC. Disabling DOC features, robust flash protection, and hiding custom analog and digital functionality inside the PSoC device provide a level of security not possible with multichip application solutions. Additionally, all device interfaces can be permanently disabled (Device Security) for applications concerned about phishing attacks due to a maliciously reprogrammed device. Permanently disabling interfaces is not recommended in most applications because you cannot access the device later. Because all programming, debug, and test interfaces are disabled when Device Security is enabled, PSoCs with Device Security enabled may not be returned for failure analysis.

**Table 9-1. Debug Configurations**

| Debug and Trace Configuration | GPIO Pins Used |
|---|---|
| All debug and trace disabled | 0 |
| JTAG | 4 or 5 |
| SWD | 2 |
| SWV | 1 |
| SWD + SWV | 3 |

## 9.1 JTAG Interface

The IEEE 1149.1 compliant JTAG interface exists on four or five pins (the nTRST pin is optional). The JTAG interface is used for programming the flash memory, debugging, I/O scan chains, and JTAG device chaining.

PSoC 3 has certain timing requirements to be met for entering programming mode through the JTAG interface. Due to these timing requirements, not all standard JTAG programmers, or standard JTAG file formats such as SVF or STAPL, can support PSoC 3 programming. The list of programmers that support PSoC 3 programming is available at http://www.cypress.com/go/programming.

The JTAG clock frequency can be up to 14 MHz, or 1/3 of the CPU clock frequency for 8 and 16-bit transfers, or 1/5 of the CPU clock frequency for 32-bit transfers. By default, the JTAG pins are enabled on new devices but the JTAG interface can be disabled, allowing these pins to be used as GPIO instead.

## 9.2 Serial Wire Debug Interface

The SWD interface is the preferred alternative to the JTAG interface. It requires only two pins instead of the four or five needed by JTAG. SWD provides all of the programming and debugging features of JTAG at the same speed. SWD does not provide access to scan chains or device chaining. The SWD clock frequency can be up to 1/3 of the CPU clock frequency.

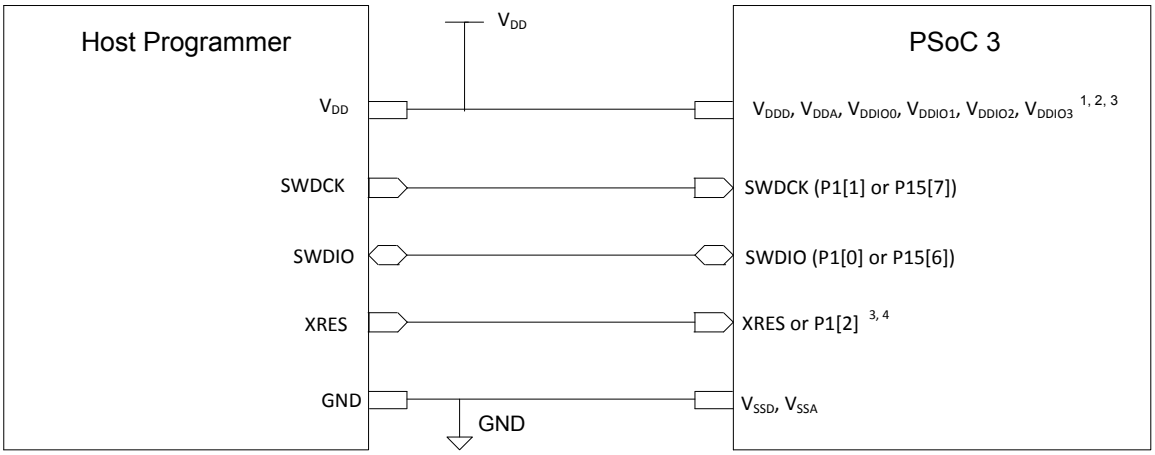
SWD uses two pins, either two of the JTAG pins (TMS and TCK) or the USBIO D+ and D– pins. The USBIO pins are useful for in system programming of USB solutions that would otherwise require a separate programming connector. One pin is used for the data clock and the other is used for data input and output.

SWD can be enabled on only one of the pin pairs at a time. This only happens if, within 8 µs (key window) after reset, that pin pair (JTAG or USB) receives a predetermined acquire sequence of 1s and 0s. If the NVL latches are set for SWD (see *Section 5.5*), this sequence need not be applied to the JTAG pin pair. The acquire sequence must always be applied to the USB pin pair.

SWD is used for debugging or for programming the flash memory.

The SWD interface can be enabled from the JTAG interface or disabled, allowing its pins to be used as GPIO. Unlike JTAG, the SWD interface can always be reacquired on any device during the key window. It can then be used to reenable the JTAG interface, if desired. When using SWD or JTAG pins as standard GPIO, make sure that the GPIO functionality and PCB circuits do not interfere with SWD or JTAG use.

**Figure 9-2. SWD Interface Connections between PSoC 3 and Programmer**




[1] The voltage levels of the Host Programmer and the PSoC 3 voltage domains involved in Programming should be the same. XRES pin (XRES_N or P1[2]) is powered by $V_{DDIO1}$. The USB SWD pins are powered by $V_{DDD}$. So for Programming using the USB SWD pins with XRES pin, the $V_{DDD}$, $V_{DDIO1}$ of PSoC 3 should be at the same voltage level as Host $V_{DD}$. Rest of PSoC 3 voltage domains ( $V_{DDA}$, $V_{DDIO0}$, $V_{DDIO2}$, $V_{DDIO3}$) need not be at the same voltage level as host Programmer. The Port 1 SWD pins are powered by $V_{DDIO1}$. So $V_{DDIO1}$ of PSoC 3 should be at same voltage level as host $V_{DD}$ for Port 1 SWD programming. Rest of PSoC 3 voltage domains ( $V_{DDD}$, $V_{DDA}$, $V_{DDIO0}$, $V_{DDIO2}$, $V_{DDIO3}$) need not be at the same voltage level as host Programmer.

[2] Vdda must be greater than or equal to all other power supplies (Vddd, Vddio's) in PSoC 3.

[3] For Power cycle mode Programming, XRES pin is not required. But the Host programmer must have the capability to toggle power (Vddd, Vdda, All Vddio's) to PSoC 3. This may typically require external interface circuitry to toggle power which will depend on the programming setup. The power supplies can be brought up in any sequence, however, once stable, VDDA must be greater than or equal to all other supplies.

[4] P1[2] will be configured as XRES by default only for 48-pin devices (without dedicated XRES pin). For devices with dedicated XRES pin, P1[2] is GPIO pin by default. So use P1[2] as Reset pin only for 48-pin devices, but use dedicated XRES pin for rest of devices.

## 9.3 Debug Features

Using the JTAG or SWD interface, the CY8C32 supports the following debug features:

- Halt and single-step the CPU
- View and change CPU and peripheral registers, and RAM addresses
- Eight program address breakpoints
- One memory access breakpoint—break on reading or writing any memory address and data value
- Break on a sequence of breakpoints (non recursive)
- Debugging at the full speed of the CPU
- Compatible with PSoC Creator and MiniProg3 programmer and debugger
- Standard JTAG programming and debugging interfaces make CY8C32 compatible with other popular third-party tools (for example, ARM / Keil)

## 9.4 Trace Features

The CY8C32 supports the following trace features when using JTAG or SWD:

- Trace the 8051 program counter (PC), accumulator register (ACC), and one SFR / 8051 core RAM register
- Trace depth up to 1000 instructions if all registers are traced, or 2000 instructions if only the PC is traced (on devices that include trace memory)
- Program address trigger to start tracing
- Trace windowing, that is, only trace when the PC is within a given range
- Two modes for handling trace buffer full: continuous (overwriting the oldest trace data) or break when trace buffer is full

## 9.5 Single Wire Viewer Interface

The SWV interface is closely associated with SWD but can also be used independently. SWV data is output on the JTAG interface's TDO pin. If using SWV, you must configure the device for SWD, not JTAG. SWV is not supported with the JTAG interface.

SWV is ideal for application debug where it is helpful for the firmware to output data similar to 'printf' debugging on PCs. The SWV is ideal for data monitoring, because it requires only a single pin and can output data in standard UART format or Manchester encoded format. For example, it can be used to tune a PID control loop in which the output and graphing of the three error terms greatly simplifies coefficient tuning.

The following features are supported in SWV:

- 32 virtual channels, each 32 bits long
- Simple, efficient packing and serializing protocol
- Supports standard UART format (N81)

## 9.6 Programming Features

The JTAG and SWD interfaces provide full programming support. The entire device can be erased, programmed, and verified. You can increase flash protection levels to protect firmware IP. Flash protection can only be reset after a full device erase. Individual flash blocks can be erased, programmed, and verified, if block security settings permit.

## 9.7 Device Security

PSoC 3 offers an advanced security feature called device security, which permanently disables all test, programming, and debug ports, protecting your application from external access. The device security is activated by programming a 32-bit key (0×50536F43) to a Write Once Latch (WOL).

The Write Once Latch is a type of nonvolatile latch (NVL). The cell itself is an NVL with additional logic wrapped around it. Each WOL device contains four bytes (32 bits) of data. The wrapper outputs a '1' if a super-majority (28 of 32) of its bits match a pre-determined pattern (0×50536F43); it outputs a '0' if this majority is not reached. When the output is 1, the Write Once NV latch locks the part out of Debug and Test modes; it also permanently gates off the ability to erase or alter the contents of the latch. Matching all bits is intentionally not required, so that single (or few) bit failures do not deassert the WOL output. The state of the NVL bits after wafer processing is truly random with no tendency toward 1 or 0.

The WOL only locks the part after the correct 32-bit key (0×50536F43) is loaded into the NVL's volatile memory, programmed into the NVL's nonvolatile cells, and the part is reset. The output of the WOL is only sampled on reset and used to disable the access. This precaution prevents anyone from reading, erasing, or altering the contents of the internal memory.

The user can write the key into the WOL to lock out external access only if no flash protection is set (see "Flash Security" on page 24). However, after setting the values in the WOL, a user still has access to the part until it is reset. Therefore, a user can write the key into the WOL, program the flash protection data, and then reset the part to lock it.

If the device is protected with a WOL setting, Cypress cannot perform failure analysis and, therefore, cannot accept RMAs from customers. The WOL can be read out via SWD port to electrically identify protected parts. The user can write the key in WOL to lock out external access only if no flash protection is set. For more information on how to take full advantage of the security features in PSoC see the PSoC 3 TRM.

**Disclaimer**

Note the following details of the flash code protection features on Cypress devices.

Cypress products meet the specifications contained in their particular Cypress datasheets. Cypress believes that its family of products is one of the most secure families of its kind on the market today, regardless of how they are used. There may be methods, unknown to Cypress, that can breach the code protection features. Any of these methods, to our knowledge, would be dishonest and possibly illegal. Neither Cypress nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Cypress is willing to work with the customer who is concerned about the integrity of their code. Code protection is constantly evolving. We at Cypress are committed to continuously improving the code protection features of our products.

## 11.2 Device Level Specifications

Specifications are valid for –40 °C ≤ $T_A$ ≤ 85 °C and $T_J$ ≤ 100 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

### *11.2.1 Device Level Specifications*

**Table 11-2. DC Specifications**

| Parameter | Description | Conditions | | Min | Typ[22] | Max | Units |
|---|---|---|---|---|---|---|---|
| $V_{DDA}$ | Analog supply voltage and input to analog core regulator | Analog core regulator enabled | | 1.8 | – | 5.5 | V |
| $V_{DDA}$ | Analog supply voltage, analog regulator bypassed | Analog core regulator disabled | | 1.71 | 1.8 | 1.89 | V |
| $V_{DDD}$ | Digital supply voltage relative to $V_{SSD}$ | Digital core regulator enabled | | 1.8 | – | $V_{DDA}$[18] | V |
| | | | | – | – | $V_{DDA}$ + 0.1[24] | |
| $V_{DDD}$ | Digital supply voltage, digital regulator bypassed | Digital core regulator disabled | | 1.71 | 1.8 | 1.89 | V |
| $V_{DDIO}$[19] | I/O supply voltage relative to $V_{SSIO}$ | | | 1.71 | – | $V_{DDA}$[18] | V |
| | | | | – | – | $V_{DDA}$ + 0.1[24] | |
| $V_{CCA}$ | Direct analog core voltage input (Analog regulator bypass) | Analog core regulator disabled | | 1.71 | 1.8 | 1.89 | V |
| $V_{CCD}$ | Direct digital core voltage input (Digital regulator bypass) | Digital core regulator disabled | | 1.71 | 1.8 | 1.89 | V |
| $I_{DD}$ [20, 21] | **Active Mode** | | | | | | |
| | Only IMO and CPU clock enabled. CPU executing simple loop from instruction buffer. | $V_{DDX}$ = 2.7 V – 5.5 V; $F_{CPU}$ = 6 MHz[23] | T = –40 °C | – | 1.2 | 2.9 | mA |
| | | | T = 25 °C | – | 1.2 | 3.1 | |
| | | | T = 85 °C | – | 4.9 | 7.7 | |
| | IMO enabled, bus clock and CPU clock enabled. CPU executing program from flash. | $V_{DDX}$ = 2.7 V – 5.5 V; $F_{CPU}$ = 3 MHz[23] | T = –40 °C | – | 1.3 | 2.9 | |
| | | | T = 25 °C | – | 1.6 | 3.2 | |
| | | | T = 85 °C | – | 4.8 | 7.5 | |
| | | $V_{DDX}$ = 2.7 V – 5.5 V; $F_{CPU}$ = 6 MHz | T = –40 °C | – | 2.1 | 3.7 | |
| | | | T = 25 °C | – | 2.3 | 3.9 | |
| | | | T = 85 °C | – | 5.6 | 8.5 | |
| | | $V_{DDX}$ = 2.7 V – 5.5 V; $F_{CPU}$ = 12 MHz[23] | T = –40 °C | – | 3.5 | 5.2 | |
| | | | T = 25 °C | – | 3.8 | 5.5 | |
| | | | T = 85 °C | – | 7.1 | 9.8 | |
| | | $V_{DDX}$ = 2.7 V – 5.5 V; $F_{CPU}$ = 24 MHz[23] | T = –40 °C | – | 6.3 | 8.1 | |
| | | | T = 25 °C | – | 6.6 | 8.3 | |
| | | | T = 85 °C | – | 10 | 13 | |
| | | $V_{DDX}$ = 2.7 V – 5.5 V; $F_{CPU}$ = 48 MHz[23] | T = –40 °C | – | 11.5 | 13.5 | |
| | | | T = 25 °C | – | 12 | 14 | |
| | | | T = 85 °C | – | 15.5 | 18.5 | |

**Notes**

18. The power supplies can be brought up in any sequence however once stable $V_{DDA}$ must be greater than or equal to all other supplies.
19. The $V_{DDIO}$ supply voltage must be greater than the maximum voltage on the associated GPIO pins. Maximum voltage on GPIO pin ≤ $V_{DDIO}$ ≤ $V_{DDA}$.
20. Total current for all power domains: digital ($I_{DDD}$), analog ($I_{DDA}$), and I/Os ($I_{DDIO0, 1, 2, 3}$). Boost not included. All I/Os floating.
21. The current consumption of additional peripherals that are implemented only in programmed logic blocks can be found in their respective datasheets, available in PSoC Creator, the integrated design environment. To estimate total current, find the CPU current at the frequency of interest and add peripheral currents for your particular system from the device datasheet and component datasheets.
22. $V_{DDX}$ = 3.3 V.
23. Based on device characterizations (Not production tested).
24. Guaranteed by design, not production tested.

**Table 11-2. DC Specifications** *(continued)*

| Parameter | Description | Conditions | | Min | Typ[22] | Max | Units |
|---|---|---|---|---|---|---|---|
| | **Sleep Mode**[25] | | | | | | |
| | CPU = OFF<br>RTC = ON (= ECO32K ON, in low-power mode)<br>Sleep timer = ON (= ILO ON at 1 kHz)[26]<br>WDT = OFF<br>$I^2C$ Wake = OFF<br>Comparator = OFF<br>POR = ON<br>Boost = OFF<br>SIO pins in single ended input, unregulated output mode | $V_{DD} = V_{DDIO}$ = 4.5 V - 5.5 V | T = –40 °C | – | 1.1 | 2.3 | µA |
| | | | T = 25 °C | – | 1.1 | 2.2 | |
| | | | T = 85 °C | – | 15 | 30 | |
| | | $V_{DD} = V_{DDIO}$ = 2.7 V – 3.6 V | T = –40 °C | – | 1 | 2.2 | |
| | | | T = 25 °C | – | 1 | 2.1 | |
| | | | T = 85 °C | – | 12 | 28 | |
| | | $V_{DD} = V_{DDIO}$ = 1.71 V – 1.95 V[27] | T = 25 °C | – | 2.2 | 4.2 | |
| | Comparator = ON<br>CPU = OFF<br>RTC = OFF<br>Sleep timer = OFF<br>WDT = OFF<br>$I^2C$ Wake = OFF<br>POR = ON<br>Boost = OFF<br>SIO pins in single ended input, unregulated output mode | $V_{DD} = V_{DDIO}$ = 2.7 V – 3.6 V[28] | T = 25 °C | – | 2.2 | 2.7 | |
| | $I^2C$ Wake = ON<br>CPU = OFF<br>RTC = OFF<br>Sleep timer = OFF<br>WDT = OFF<br>Comparator = OFF<br>POR = ON<br>Boost = OFF<br>SIO pins in single ended input, unregulated output mode | $V_{DD} = V_{DDIO}$ = 2.7 V – 3.6 V[28] | T = 25 °C | – | 2.2 | 2.8 | |
| | **Hibernate Mode**[25] | | | | | | |
| | Hibernate mode current<br>All regulators and oscillators off<br>SRAM retention<br>GPIO interrupts are active<br>Boost = OFF<br>SIO pins in single ended input, unregulated output<br>mode | $V_{DD} = V_{DDIO}$ = 4.5 V - 5.5 V | T = –40 °C | – | 0.2 | 1.5 | µA |
| | | | T = 25 °C | – | 0.5 | 1.5 | |
| | | | T = 85 °C | – | 4.1 | 5.3 | |
| | | $V_{DD} = V_{DDIO}$ = 2.7 V – 3.6 V | T = –40 °C | – | 0.2 | 1.5 | |
| | | | T = 25 °C | – | 0.2 | 1.5 | |
| | | | T = 85 °C | – | 3.2 | 4.2 | |
| | | $V_{DD} = V_{DDIO}$ = 1.71 V – 1.95 V[27] | T = –40 °C | – | 0.2 | 1.5 | |
| | | | T = 25 °C | – | 0.3 | 1.5 | |
| | | | T = 85 °C | – | 3.3 | 4.3 | |
| $I_{DDAR}$ | Analog current consumption while device is reset[29] | $V_{DDA} \leq 3.6$ V | | – | 0.3 | 0.6 | mA |
| | | $V_{DDA} > 3.6$ V | | – | 1.4 | 3.3 | mA |
| $I_{DDDR}$ | Digital current consumption while device is reset[29] | $V_{DDD} \leq 3.6$ V | | – | 1.1 | 3.1 | mA |
| | | $V_{DDD} > 3.6$ V | | – | 0.7 | 3.1 | mA |

**$V_{DDD}$ = 3.3 V, 25 pF Load**

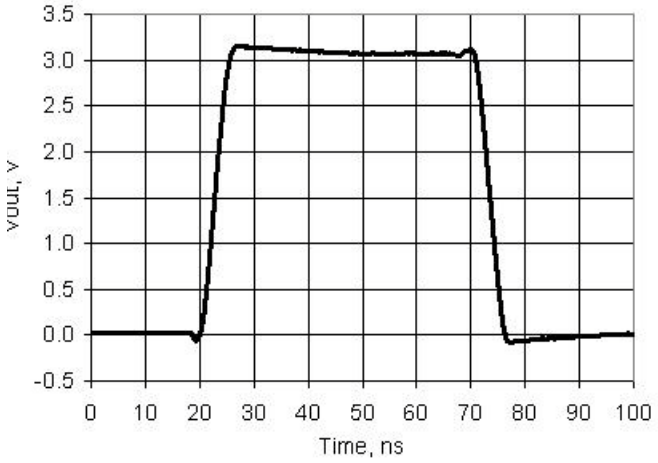



**Table 11-16. USB Driver AC Specifications**

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Tr | Transition rise time | | – | – | 20 | ns |
| Tf | Transition fall time | | – | – | 20 | ns |
| TR | Rise/fall time matching | $V_{USB\_5}$, $V_{USB\_3.3}$, see USB DC Specifications on page 98 | 90% | – | 111% | |
| Vcrs | Output signal crossover voltage | | 1.3 | – | 2 | V |

*11.4.4 XRES*

**Table 11-17. XRES DC Specifications**

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input voltage high threshold | | 0.7 × $V_{DDIO}$ | – | – | V |
| $V_{IL}$ | Input voltage low threshold | | – | – | 0.3 × $V_{DDIO}$ | V |
| Rpullup | Pull-up resistor | | 3.5 | 5.6 | 8.5 | kΩ |
| $C_{IN}$ | Input capacitance[43] | | – | 3 | – | pF |
| $V_H$ | Input voltage hysteresis (Schmitt-Trigger)[43] | | – | 100 | – | mV |
| Idiode | Current through protection diode to $V_{DDIO}$ and $V_{SSIO}$ | | – | – | 100 | µA |

**Table 11-18. XRES AC Specifications**

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $T_{RESET}$ | Reset pulse width | | 1 | – | – | µs |

**Note**
43. Based on device characterization (Not production tested).

**Figure 11-28. IDAC DNL vs Input Code, Range = 255 µA, Source Mode**

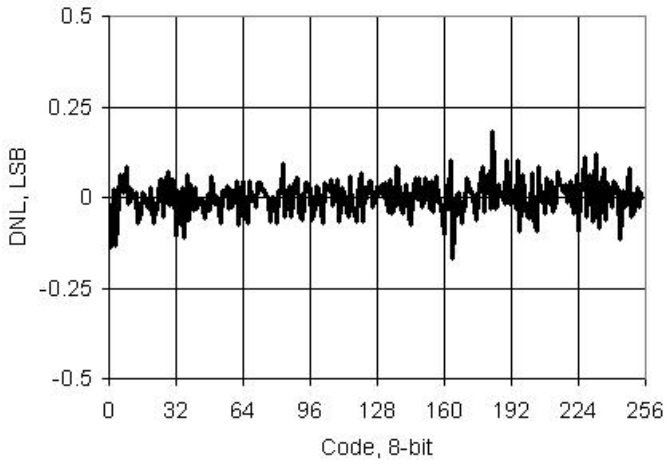



**Figure 11-29. IDAC DNL vs Input Code, Range = 255 µA, Sink Mode**

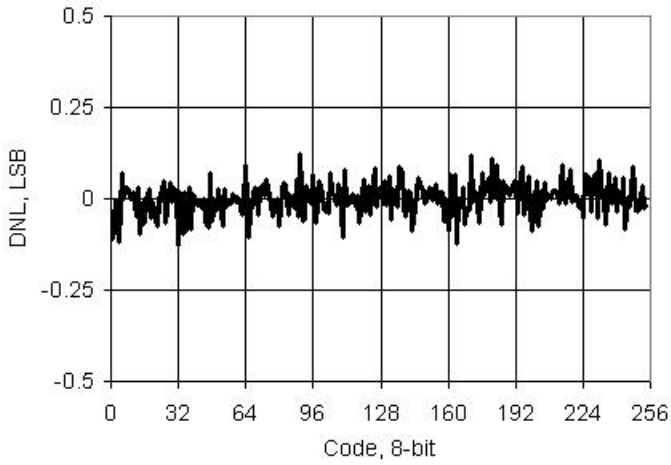



**Figure 11-30. IDAC INL vs Temperature, Range = 255 µA, High speed mode**

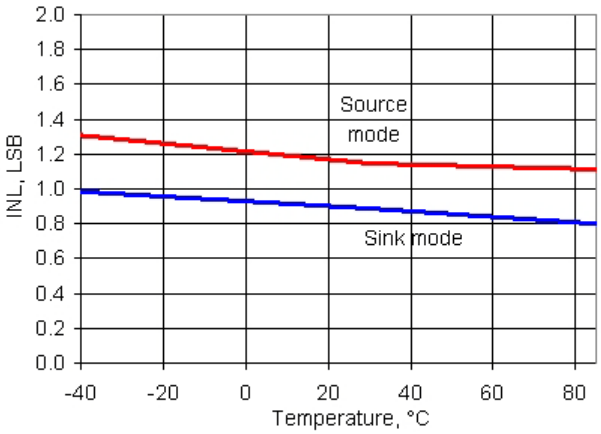



**Figure 11-31. IDAC DNL vs Temperature, Range = 255 µA, High speed mode**

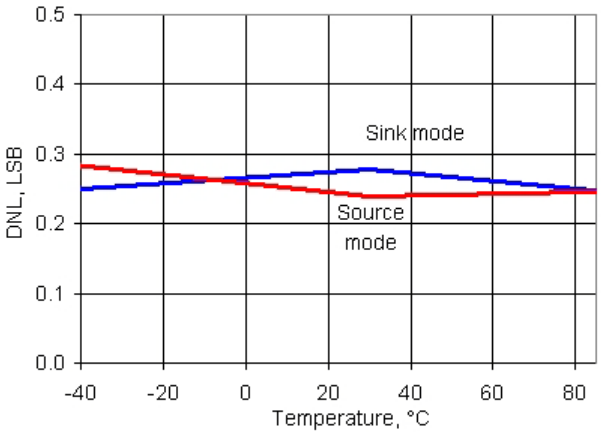


**Figure 11-32. IDAC Full Scale Error vs Temperature, Range = 255 µA, Source Mode**

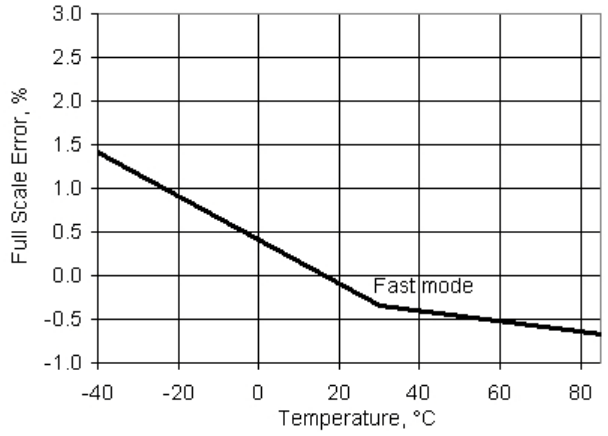



**Figure 11-33. IDAC Full Scale Error vs Temperature, Range = 255 µA, Sink Mode**

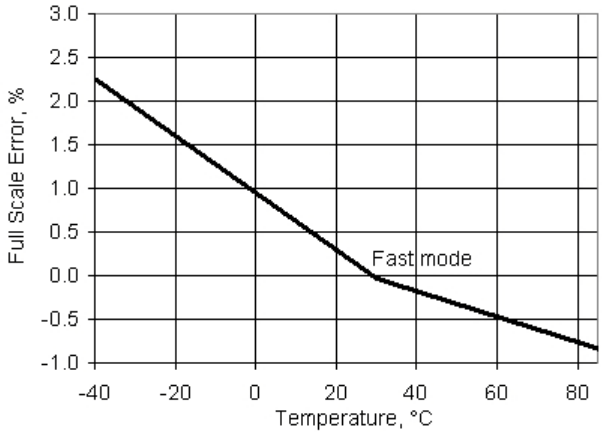



**Figure 11-34. IDAC Operating Current vs Temperature, Range = 255 µA, Code = 0, Source Mode**

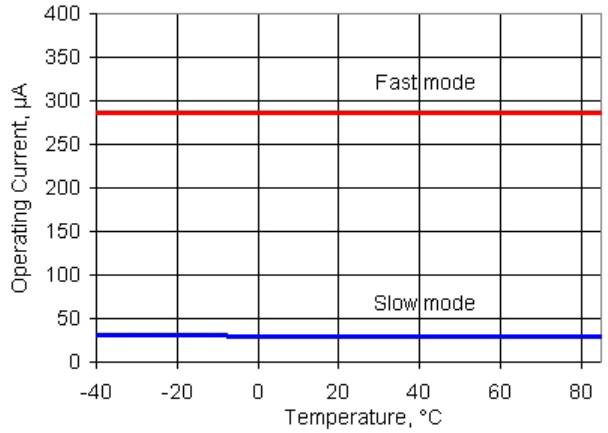
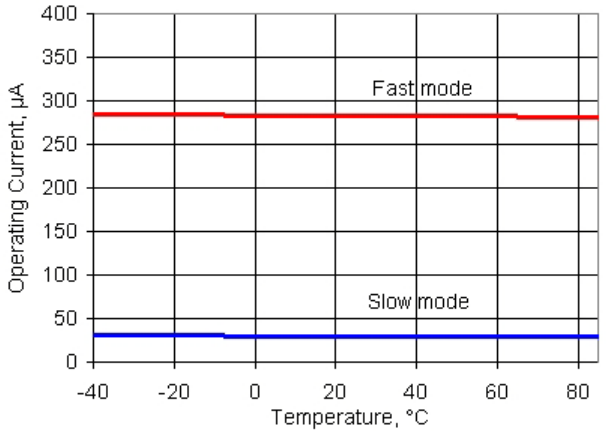



**Figure 11-35. IDAC Operating Current vs Temperature, Range = 255 µA, Code = 0, Sink Mode**



### *11.5.6 Voltage Digital to Analog Converter (VDAC)*

See the VDAC component datasheet in PSoC Creator for full electrical specifications and APIs.

Unless otherwise specified, all charts and graphs show typical values.

**Table 11-28. VDAC DC Specifications**

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| | Resolution | | – | 8 | – | bits |
| INL1 | Integral nonlinearity | 1 V scale | – | ±2.1 | ±2.5 | LSB |
| INL4 | Integral nonlinearity[52] | 4 V scale | – | ±2.1 | ±2.5 | LSB |
| DNL1 | Differential nonlinearity | 1 V scale | – | ±0.3 | ±1 | LSB |
| DNL4 | Differential nonlinearity[52] | 4 V scale | – | ±0.3 | ±1 | LSB |
| Rout | Output resistance | 1 V scale | – | 4 | – | kΩ |
| | | 4 V scale | – | 16 | – | kΩ |
| $V_{OUT}$ | Output voltage range, code = 255 | 1 V scale | – | 1.02 | – | V |
| | | 4 V scale, $V_{DDA}$ = 5 V | – | 4.08 | – | V |
| | Monotonicity | | – | – | Yes | – |
| $V_{OS}$ | Zero scale error | | – | 0 | ±0.9 | LSB |
| Eg | Gain error | 1 V scale | – | – | ±2.5 | % |
| | | 4 V scale | – | – | ±2.5 | % |
| TC_Eg | Temperature coefficient, gain error | 1 V scale | – | – | 0.03 | %FSR / °C |
| | | 4 V scale | – | – | 0.03 | %FSR / °C |
| $I_{DD}$ | Operating current | Low speed mode | – | – | 100 | µA |
| | | High speed mode | – | – | 500 | µA |

**Figure 11-40. VDAC INL vs Input Code, 1 V Mode**

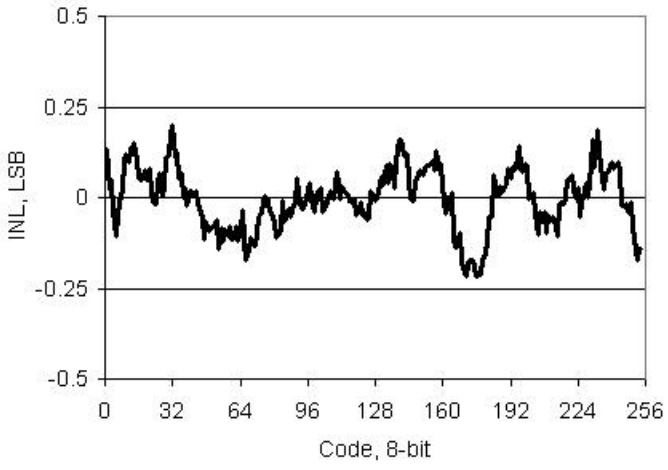
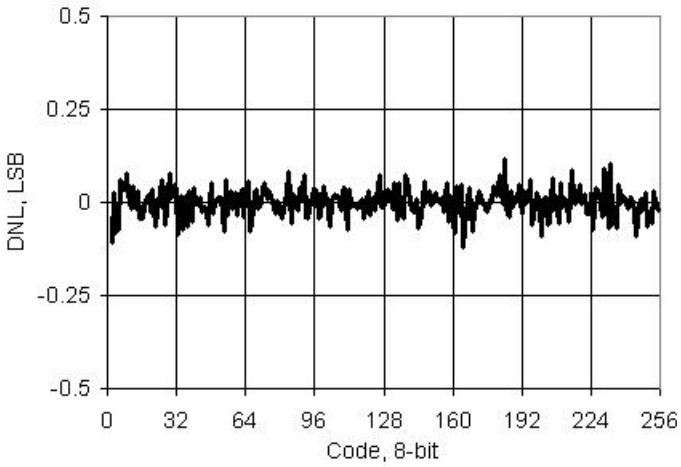



**Figure 11-41. VDAC DNL vs Input Code, 1 V Mode**




**Note**
52. Based on device characterization (Not production tested).

### 11.5.7 Temperature Sensor

**Table 11-30. Temperature Sensor Specifications**

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| | Temp sensor accuracy | Range: –40 °C to +85 °C | – | ±5 | – | °C |

### 11.5.8 LCD Direct Drive

**Table 11-31. LCD Direct Drive DC Specifications**

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $I_{CC}$ | LCD system operating current | Device sleep mode with wakeup at 400-Hz rate to refresh LCDs, bus clock = 3 MHz, $V_{DDIO} = V_{DDA} = 3$ V, 4 commons, 16 segments, 1/4 duty cycle, 50 Hz frame rate, no glass connected | – | 38 | – | µA |
| $I_{CC\_SEG}$ | Current per segment driver | Strong drive mode | – | 260 | – | µA |
| $V_{BIAS}$ | LCD bias range ($V_{BIAS}$ refers to the main output voltage(V0) of LCD DAC) | $V_{DDA} \geq 3$ V and $V_{DDA} \geq V_{BIAS}$ | 2 | – | 5 | V |
| | LCD bias step size | $V_{DDA} \geq 3$ V and $V_{DDA} \geq V_{BIAS}$ | – | 9.1 × $V_{DDA}$ | – | mV |
| | LCD capacitance per segment/common driver | Drivers may be combined | – | 500 | 5000 | pF |
| | Long term segment offset | | – | – | 20 | mV |
| $I_{OUT}$ | Output drive current per segment driver) | $V_{DDIO}$ = 5.5V, strong drive mode | 355 | – | 710 | µA |

**Table 11-32. LCD Direct Drive AC Specifications**

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $f_{LCD}$ | LCD frame rate | | 10 | 50 | 150 | Hz |

# 13. Packaging

**Table 13-1. Package Characteristics**

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $T_A$ | Operating ambient temperature | | –40 | 25.00 | 85 | °C |
| $T_J$ | Operating junction temperature | | –40 | – | 100 | °C |
| $T_{JA}$ | Package $\theta_{JA}$ (48-pin SSOP) | | – | 49 | – | °C/Watt |
| $T_{JA}$ | Package $\theta_{JA}$ (48-pin QFN) | | – | 14 | – | °C/Watt |
| $T_{JA}$ | Package $\theta_{JA}$ (68-pin QFN) | | – | 15 | – | °C/Watt |
| $T_{JA}$ | Package $\theta_{JA}$ (100-pin TQFP) | | – | 34 | – | °C/Watt |
| $T_{JC}$ | Package $\theta_{JC}$ (48-pin SSOP) | | – | 24 | – | °C/Watt |
| $T_{JC}$ | Package $\theta_{JC}$ (48-pin QFN) | | – | 15 | – | °C/Watt |
| $T_{JC}$ | Package $\theta_{JC}$ (68-pin QFN) | | – | 13 | – | °C/Watt |
| $T_{JC}$ | Package $\theta_{JC}$ (100-pin TQFP) | | – | 10 | – | °C/Watt |
| $T_{JA}$ | Package $\theta_{JA}$ (72-pin CSP) | | – | 18 | – | °C/Watt |
| $T_{JC}$ | Package $\theta_{JC}$ (72-pin CSP) | | – | 0.13 | – | °C/Watt |

**Table 13-2. Solder Reflow Peak Temperature**

| Package | Maximum Peak Temperature | Maximum Time at Peak Temperature |
|---|---|---|
| 48-pin SSOP | 260 °C | 30 seconds |
| 48-pin QFN | 260 °C | 30 seconds |
| 68-pin QFN | 260 °C | 30 seconds |
| 100-pin TQFP | 260 °C | 30 seconds |
| 72-pin CSP | 260 °C | 30 seconds |

**Table 13-3. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2**

| Package | MSL |
|---|---|
| 48-pin SSOP | MSL 3 |
| 48-pin QFN | MSL 3 |
| 68-pin QFN | MSL 3 |
| 100-pin TQFP | MSL 3 |
| 72-pin CSP | MSL 1 |

| Description Title: PSoC® 3: CY8C32 Family Data Sheet Programmable System-on-Chip (PSoC®) *(continued)*<br>Document Number: 001-56955 | | | | |
|---|---|---|---|---|
| **Revision** | **ECN** | **Submission Date** | **Orig. of Change** | **Description of Change** |
| *C | 2903576 | 04/01/10 | MKEA | Updated Vb pin in PCB Schematic.<br>Updated Tstartup parameter in AC Specifications table.<br>Added Load regulation and Line regulation parameters to Inductive Boost Regulator DC Specifications table.<br>Updated $I_{CC}$ parameter in LCD Direct Drive DC Specs table.<br>In page 1, updated internal oscillator range under Prescision programmable clocking to start from 3 MHz.<br>Updated $I_{OUT}$ parameter in LCD Direct Drive DC Specs table.<br>Updated Table 6-2 and Table 6-3.<br>Added bullets on CapSense in page 1; added CapSense column in Section 12<br>Removed some references to footnote [1].<br>Changed INC_Rn cycles from 3 to 2 (Table 4-1).<br>Added footnote in PLL AC Specification table.<br>Added PLL intermediate frequency row with footnote in PLL AC Specs table.<br>Added UDBs subsection under 11.6 Digital Peripherals.<br>Updated Figure 2-6 (PCB Layout).<br>Updated Pin Descriptions section and modified Figures 6-6, 6-8, 6-9.<br>Updated LVD in Tables 6-2 and 6-3; modified Low-power modes bullet in page 1.<br>Added note to Figures 2-5 and 6-2; Updated Figure 6-2 to add capacitors for $V_{DDA}$ and $V_{DDD}$ pins.<br>Updated boost converter section (6.2.2).<br>Updated Tstartup values in Table 11-3.<br>Removed IPOR rows from Table 11-53. Updated 6.3.1.1, Power Voltage Level Monitors.<br>Updated section 5.2 and Table 11-2 to correct suggestion of execution from flash.<br>Updated IMO max frequency in Figure 6-1, Table 11-63, and Table 11-64.<br>Updated $V_{REF}$ specs in Table 11-19.<br>Updated IDAC uncompensated gain error in Table 11-23.<br>Updated Delay from Interrupt signal input to ISR code execution from ISR code in Table-71. Removed other line in table.<br>Added sentence to last paragraph of section 6.1.1.3.<br>Updated Tresp, high and low-power modes, in Table 11-22.<br>Updated f_TCK values in Table 11-58 and f_SWDCK values in Table 11-59.<br>Updated SNR condition in Table 11-18.<br>Updated sleep wakeup time in Table 6-3 and Tsleep in Table 11-3.<br>Added 1.71 V <= $V_{DDD}$ < 3.3 V, SWD over USBIO pins value to Table 11-59.<br>Removed mention of hibernate reset (HRES) from page 1 features, Table 6-3, Section 6.2.1.4, Section 6.3, and Section 6.3.1.1. Change PPOR/PRES to TBDs in Section 6.3.1.1, Section 6.4.1.6 (changed PPOR to reset), Table 11-3 (changed PPOR to PRES), Table 11-53 (changed title, values TBD), and Table 11-54 (changed PPOR_TR to PRES_TR).<br>Added sentence saying that LVD circuits can generate a reset to Section 6.3.1.1.<br>Changed $I_{DD}$ values on page 1, page 5, and Table 11-2.<br>Changed resume time value in Section 6.2.1.3.<br>Changed ESD HBM value in Table 11-1.<br>Changed sample rate row in Table 11-18.<br>Removed $V_{DDA}$ = 1.65 V rows and changed BWag value in Table 11-20.<br>Changed Vioff values and changed CMRR value in Table 11-21.<br>Changed INL max value in Table 11-25.<br>Changed occurrences of “Block” to “Row” and deleted the “ECC not included” footnote in Table 11-41.<br>Changed max response time value in Tables 11-54 and 11-56.<br>Change the Startup time in Table 11-64.<br>Added condition to intermediate frequency row in Table 11-70.<br>Added row to Table 11-54.<br>Added brown out note to Section 11.8.1. |

# 18. Sales, Solutions, and Legal Information

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