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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	50MHz
Connectivity	EBI/EMI, I <sup>2</sup> C, LINbus, SPI, UART/USART
Peripherals	CapSense, DMA, LCD, POR, PWM, WDT
Number of I/O	25
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 16x12b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-BSSOP (0.295", 7.50mm Width)
Supplier Device Package	48-SSOP
Purchase URL	<a href="https://www.e-xfl.com/product-detail/infineon-technologies/cy8c3244pvi-133t">https://www.e-xfl.com/product-detail/infineon-technologies/cy8c3244pvi-133t</a>

## More Information

Cypress provides a wealth of data at [www.cypress.com](http://www.cypress.com) to help you to select the right PSoC device for your design, and to help you to quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the knowledge base article [KBA86521, How to Design with PSoC 3, PSoC 4, and PSoC 5LP](#). Following is an abbreviated list for PSoC 3:

### ■ Overview: [PSoC Portfolio](#), [PSoC Roadmap](#)

### ■ Product Selectors: [PSoC 1](#), [PSoC 3](#), [PSoC 4](#), [PSoC 5LP](#) In addition, PSoC Creator includes a device selection tool.

### ■ Application notes: Cypress offers a large number of PSoC application notes and [code examples](#) covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with PSoC 3 are:

- [AN54181](#): Getting Started With PSoC 3
- [AN61290](#): Hardware Design Considerations
- [AN57821](#): Mixed Signal Circuit Board Layout
- [AN58304](#): Pin Selection for Analog Designs
- [AN81623](#): Digital Design Best Practices
- [AN73854](#): Introduction To Bootloaders

### ■ Development Kits:

- [CY8CKIT-030](#) is designed for analog performance, for developing high-precision analog, low-power, and low-voltage applications.
- [CY8CKIT-001](#) provides a common development platform for any one of the PSoC 1, PSoC 3, PSoC 4, or PSoC 5LP families of devices.
- The [MiniProg3](#) device provides an interface for flash programming and debug.

### ■ Technical Reference Manuals (TRM)

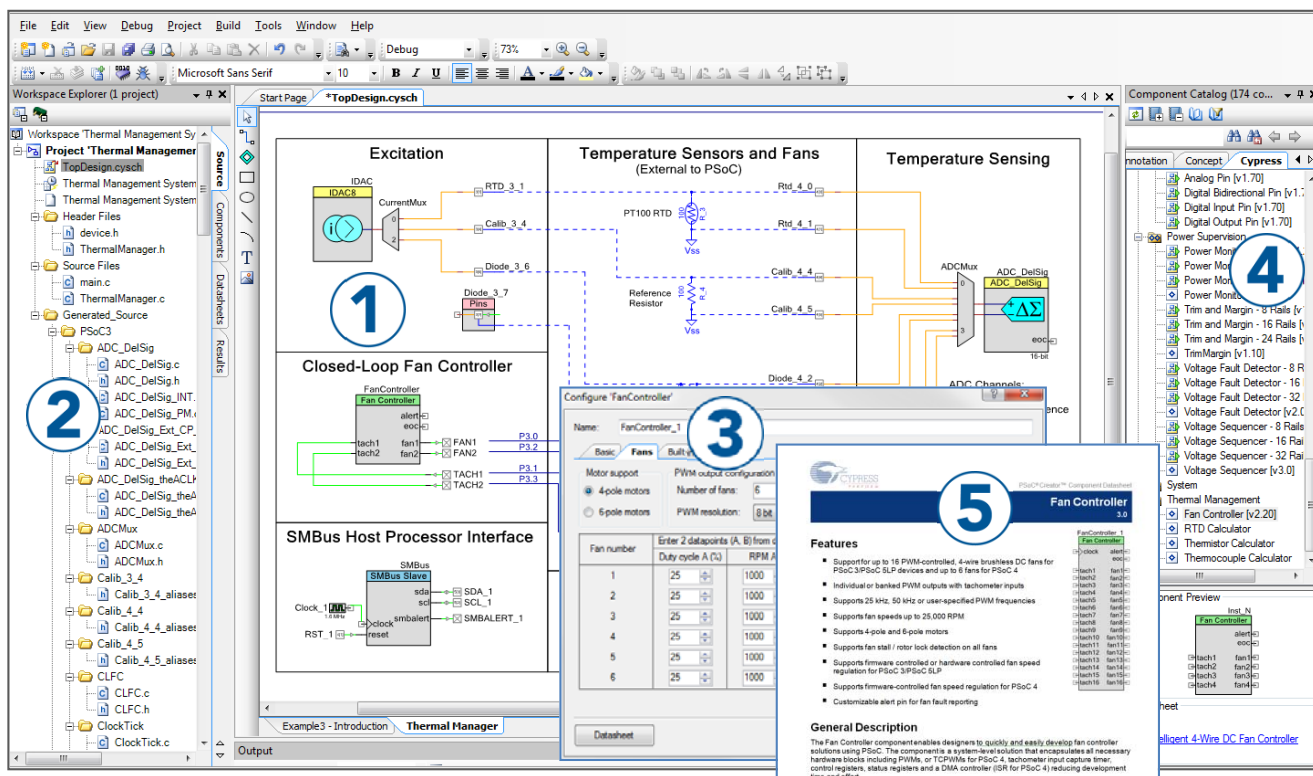
- [Architecture TRM](#)
- [Registers TRM](#)
- [Programming Specification](#)

## PSoC Creator

[PSoC Creator](#) is a free Windows-based Integrated Design Environment (IDE). It enables concurrent hardware and firmware design of PSoC 3, PSoC 4, and PSoC 5LP based systems. Create designs using classic, familiar schematic capture supported by over 100 pre-verified, production-ready PSoC Components; see the [list of component datasheets](#). With PSoC Creator, you can:

1. Drag and drop component icons to build your hardware system design in the main design workspace
2. Codesign your application firmware with the PSoC hardware, using the PSoC Creator IDE C compiler
3. Configure components using the configuration tools
4. Explore the library of 100+ components
5. Review component datasheets

**Figure 1. Multiple-Sensor Example Project in PSoC Creator**



## 1. Architectural Overview

Introducing the CY8C32 family of ultra low-power, flash Programmable System-on-Chip (PSoC®) devices, part of a scalable 8-bit PSoC 3 and 32-bit PSoC 5 platform. The CY8C32 family provides configurable blocks of analog, digital, and interconnect circuitry around a CPU subsystem. The combination of a CPU with a flexible analog subsystem, digital subsystem, routing, and I/O enables a high level of integration in a wide variety of consumer, industrial, and medical applications.

**Figure 1-1. Simplified Block Diagram**

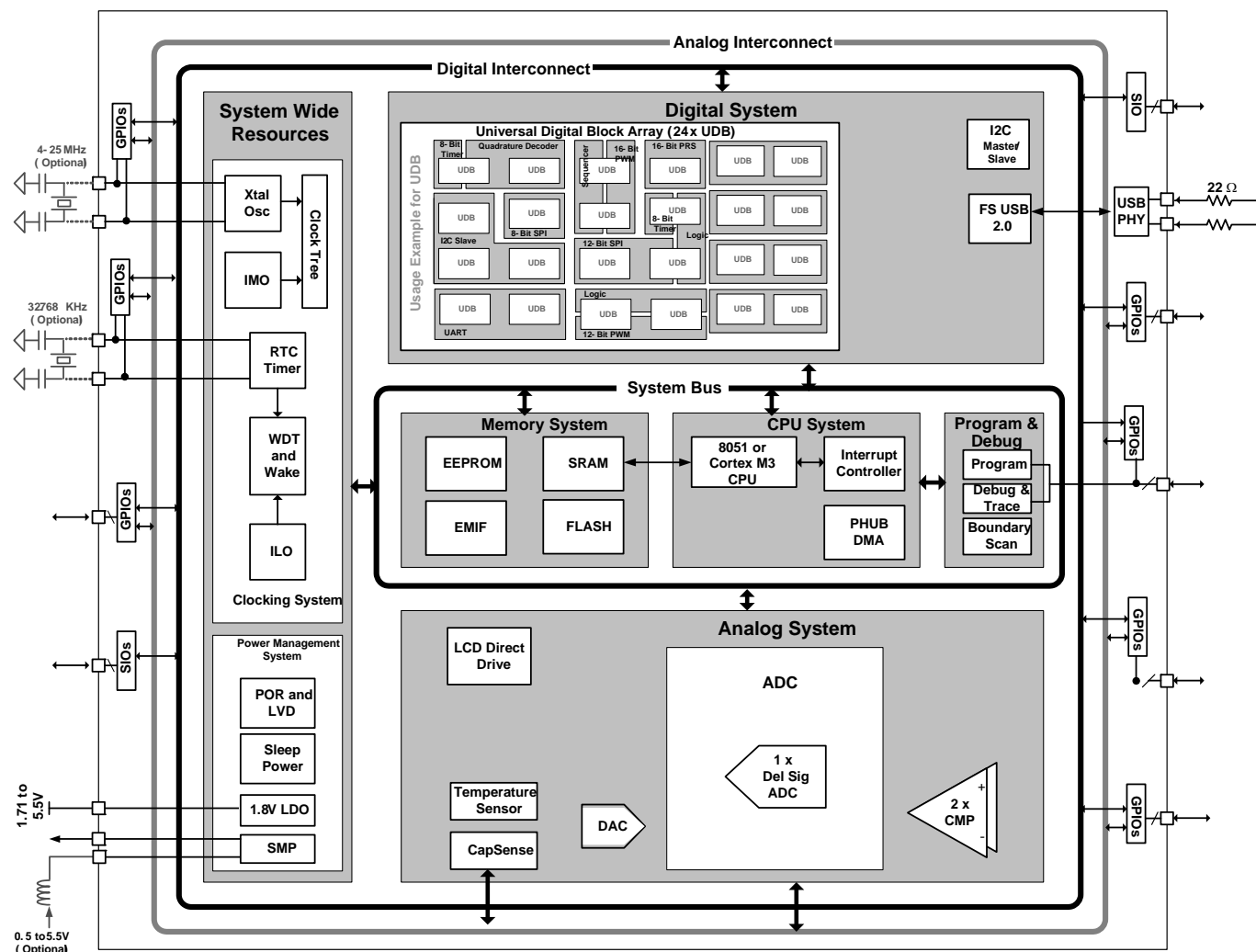


Figure 1-1 illustrates the major components of the CY8C32 family. They are:

- 8051 CPU subsystem
- Nonvolatile subsystem
- Programming, debug, and test subsystem
- Inputs and outputs
- Clocking
- Power
- Digital subsystem
- Analog subsystem

PSoC's digital subsystem provides half of its unique configurability. It connects a digital signal from any peripheral to any pin through the Digital System Interconnect (DSI). It also provides functional flexibility through an array of small, fast, low-power UDBs. PSoC Creator provides a library of prebuilt and tested standard digital peripherals (UART, SPI, LIN, PRS, CRC, timer, counter, PWM, AND, OR, and so on) that are mapped to the UDB array. You can also easily create a digital circuit using boolean primitives by means of graphical design entry. Each UDB contains programmable array logic (PAL)/programmable logic device (PLD) functionality, together with a small state machine engine to support a wide variety of peripherals.

Figure 2-3. 48-pin SSOP Part Pinout

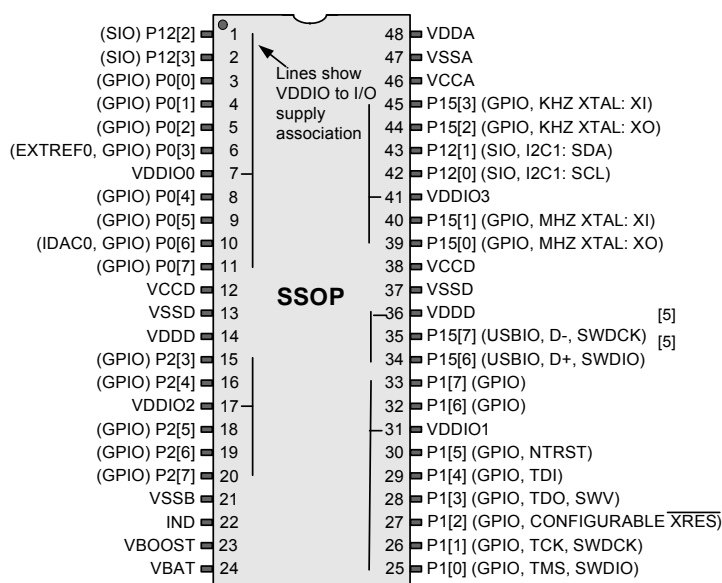
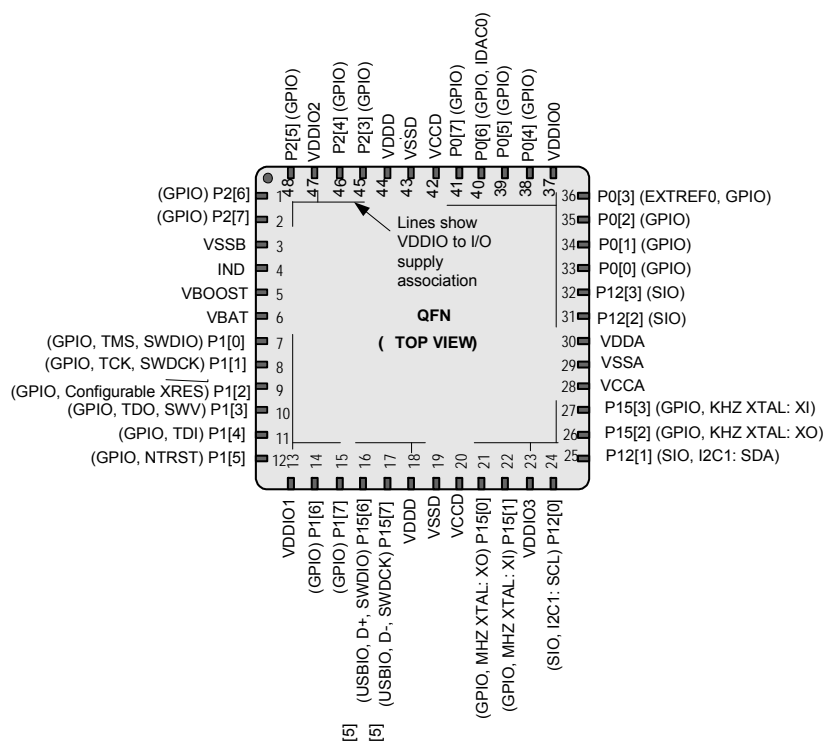


Figure 2-4. 48-pin QFN Part Pinout<sup>[6]</sup>



## Notes

- Pins are Do Not Use (DNU) on devices without USB. The pin must be left floating.
- The center pad on the QFN package should be connected to digital ground (VSSD) for best mechanical, thermal, and electrical performance. If not connected to ground, it should be electrically floated and not connected to any other signal. For more information, see [AN72845](#), Design Guidelines for QFN Devices.

**Table 4-4. Boolean Instructions**

<b>Mnemonic</b>	<b>Description</b>	<b>Bytes</b>	<b>Cycles</b>
CLR C	Clear carry	1	1
CLR bit	Clear direct bit	2	3
SETB C	Set carry	1	1
SETB bit	Set direct bit	2	3
CPL C	Complement carry	1	1
CPL bit	Complement direct bit	2	3
ANL C, bit	AND direct bit to carry	2	2
ANL C, /bit	AND complement of direct bit to carry	2	2
ORL C, bit	OR direct bit to carry	2	2
ORL C, /bit	OR complement of direct bit to carry	2	2
MOV C, bit	Move direct bit to carry	2	2
MOV bit, C	Move carry to direct bit	2	3
JC rel	Jump if carry is set	2	3
JNC rel	Jump if no carry is set	2	3
JB bit, rel	Jump if direct bit is set	3	5
JNB bit, rel	Jump if direct bit is not set	3	5
JBC bit, rel	Jump if direct bit is set and clear bit	3	5

## 4.3.1.5 Program Branching Instructions

The 8051 supports a set of conditional and unconditional jump instructions that help to modify the program execution flow. [Table 4-5](#) shows the list of jump instructions.

**Table 4-5. Jump Instructions**

Mnemonic	Description	Bytes	Cycles
ACALL addr11	Absolute subroutine call	2	4
LCALL addr16	Long subroutine call	3	4
RET	Return from subroutine	1	4
RETI	Return from interrupt	1	4
AJMP addr11	Absolute jump	2	3
LJMP addr16	Long jump	3	4
SJMP rel	Short jump (relative address)	2	3
JMP @A + DPTR	Jump indirect relative to DPTR	1	5
JZ rel	Jump if accumulator is zero	2	4
JNZ rel	Jump if accumulator is nonzero	2	4
CJNE A, Direct, rel	Compare direct byte to accumulator and jump if not equal	3	5
CJNE A, #data, rel	Compare immediate data to accumulator and jump if not equal	3	4
CJNE Rn, #data, rel	Compare immediate data to register and jump if not equal	3	4
CJNE @Ri, #data, rel	Compare immediate data to indirect RAM and jump if not equal	3	5
DJNZ Rn, rel	Decrement register and jump if not zero	2	4
DJNZ Direct, rel	Decrement direct byte and jump if not zero	3	5
NOP	No operation	1	1

## 4.4 DMA and PHUB

The PHUB and the DMA controller are responsible for data transfer between the CPU and peripherals, and also data transfers between peripherals. The PHUB and DMA also control device configuration during boot. The PHUB consists of:

- A central hub that includes the DMA controller, arbiter, and router
- Multiple spokes that radiate outward from the hub to most peripherals

There are two PHUB masters: the CPU and the DMA controller. Both masters may initiate transactions on the bus. The DMA channels can handle peripheral communication without CPU intervention. The arbiter in the central hub determines which DMA channel is the highest priority if there are multiple requests.

### 4.4.1 PHUB Features

- CPU and DMA controller are both bus masters to the PHUB
- Eight Multi-layer AHB Bus parallel access paths (spokes) for peripheral access

- Simultaneous CPU and DMA access to peripherals located on different spokes
- Simultaneous DMA source and destination burst transactions on different spokes
- Supports 8, 16, 24, and 32-bit addressing and data

**Table 4-6. PHUB Spokes and Peripherals**

PHUB Spokes	Peripherals
0	SRAM
1	IOs, PICU, EMIF
2	PHUB local configuration, Power manager, Clocks, IC, SWV, EEPROM, Flash programming interface
3	Analog interface and trim, Decimator
4	USB, USB, I <sup>2</sup> C, Timers, Counters, and PWMs
5	Reserved
6	UDBs group 1
7	UDBs group 2

## 4.4.4.5 Scatter Gather DMA

In the case of scatter gather DMA, there are multiple noncontiguous sources or destinations that are required to effectively carry out an overall DMA transaction. For example, a packet may need to be transmitted off of the device and the packet elements, including the header, payload, and trailer, exist in various noncontiguous locations in memory. Scatter gather DMA allows the segments to be concatenated together by using multiple TDs in a chain. The chain gathers the data from the multiple locations. A similar concept applies for the reception of data onto the device. Certain parts of the received data may need to be scattered to various locations in memory for software processing convenience. Each TD in the chain specifies the location for each discrete element in the chain.

## 4.4.4.6 Packet Queuing DMA

Packet queuing DMA is similar to scatter gather DMA but specifically refers to packet protocols. With these protocols, there may be separate configuration, data, and status phases associated with sending or receiving a packet.

For instance, to transmit a packet, a memory mapped configuration register can be written inside a peripheral, specifying the overall length of the ensuing data phase. The CPU can set up this configuration information anywhere in system memory and copy it with a simple TD to the peripheral. After the configuration phase, a data phase TD (or a series of data phase TDs) can begin (potentially using scatter gather). When the data phase TD(s) finish, a status phase TD can be invoked that reads some memory mapped status information from the peripheral and copies it to a location in system memory specified by the CPU for later inspection. Multiple sets of configuration, data, and status phase "subchains" can be strung together to create larger chains that transmit multiple packets in this way. A similar concept exists in the opposite direction to receive the packets.

## 4.4.4.7 Nested DMA

One TD may modify another TD, as the TD configuration space is memory mapped similar to any other peripheral. For example, a first TD loads a second TD's configuration and then calls the second TD. The second TD moves data as required by the application. When complete, the second TD calls the first TD, which again updates the second TD's configuration. This process repeats as often as necessary.

## 4.5 Interrupt Controller

The interrupt controller provides a mechanism for hardware resources to change program execution to a new address, independent of the current task being executed by the main code. The interrupt controller provides enhanced features not found on original 8051 interrupt controllers:

- Thirty two interrupt vectors
- Jumps directly to ISR anywhere in code space with dynamic vector addresses
- Multiple sources for each vector
- Flexible interrupt to vector matching
- Each interrupt vector is independently enabled or disabled
- Each interrupt can be dynamically assigned one of eight priorities
- Eight level nestable interrupts
- Multiple I/O interrupt vectors
- Software can send interrupts
- Software can clear pending interrupts

When an interrupt is pending, the current instruction is completed and the program counter is pushed onto the stack. Code execution then jumps to the program address provided by the vector. After the ISR is completed, a RETI instruction is executed and returns execution to the instruction following the previously interrupted instruction. To do this the RETI instruction pops the program counter from the stack.

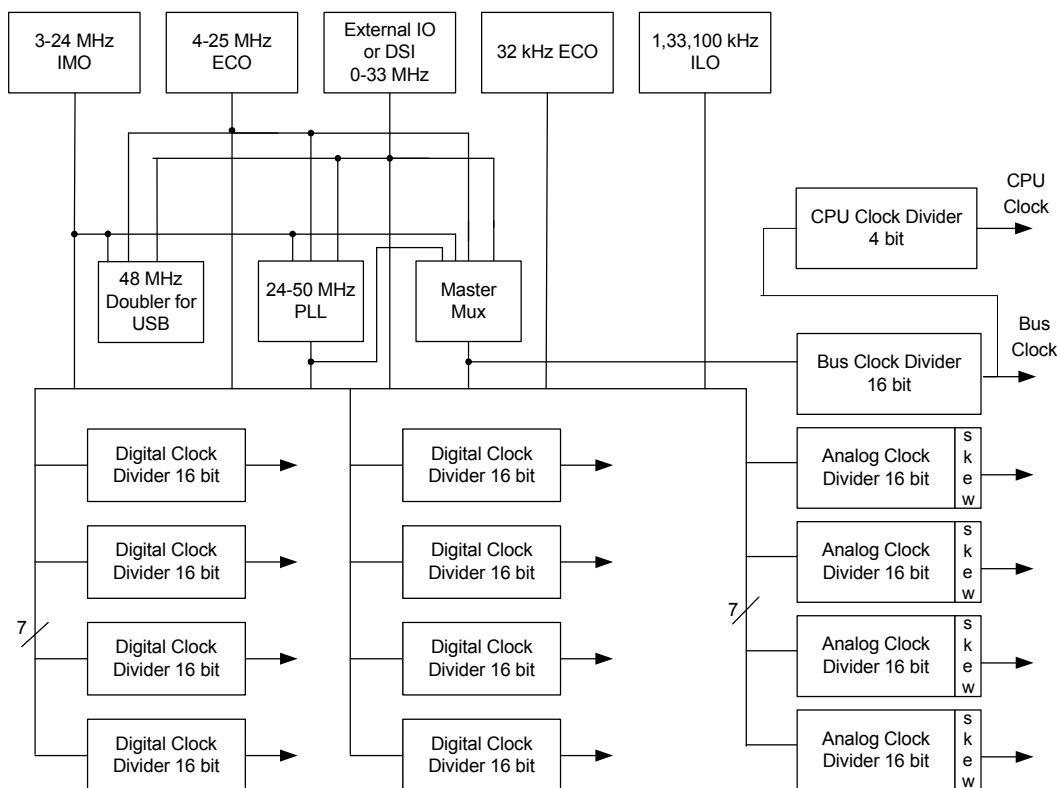
If the same priority level is assigned to two or more interrupts, the interrupt with the lower vector number is executed first. Each interrupt vector may choose from three interrupt sources: Fixed Function, DMA, and UDB. The fixed function interrupts are direct connections to the most common interrupt sources and provide the lowest resource cost connection. The DMA interrupt sources provide direct connections to the two DMA interrupt sources provided per DMA channel. The third interrupt source for vectors is from the UDB digital routing array. This allows any digital signal available to the UDB array to be used as an interrupt source. Fixed function interrupts and all interrupt sources may be routed to any interrupt vector using the UDB interrupt source connections.

Figure 4-2 on page 21 represents typical flow of events when an interrupt triggered. Figure 4-3 on page 22 shows the interrupt structure and priority polling.

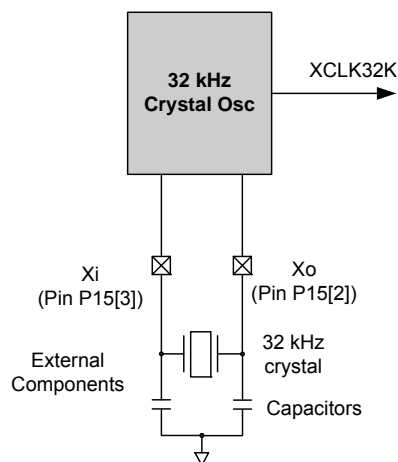
**Table 6-1. Oscillator Summary**

Source	Fmin	Tolerance at Fmin	Fmax	Tolerance at Fmax	Startup Time
IMO	3 MHz	±2% over voltage and temperature	24 MHz	±4%	13-µs max
MHzECO	4 MHz	Crystal dependent	25 MHz	Crystal dependent	5 ms typ, max is crystal dependent
DSI	0 MHz	Input dependent	33 MHz	Input dependent	Input dependent
PLL	24 MHz	Input dependent	50 MHz	Input dependent	250 µs max
Doubler	48 MHz	Input dependent	48 MHz	Input dependent	1 µs max
ILO	1 kHz	-50%, +100%	100 kHz	-55%, +100%	15 ms max in lowest power mode
kHzECO	32 kHz	Crystal dependent	32 kHz	Crystal dependent	500 ms typ, max is crystal dependent

**Figure 6-1. Clocking Subsystem**



**Figure 6-3. 32kHzECO Block Diagram**



It is recommended that the external 32.768-kHz watch crystal have a load capacitance (CL) of 6 pF or 12.5 pF. Check the crystal manufacturer's datasheet. The two external capacitors, CL1 and CL2, are typically of the same value, and their total capacitance,  $CL1CL2 / (CL1 + CL2)$ , including pin and trace capacitance, should equal the crystal CL value. For more information, refer to application note [AN54439: PSoC 3 and PSoC 5 External Oscillators](#). See also pin capacitance specifications in the "GPIO" section on page 76.

### 6.1.2.3 Digital System Interconnect

The DSI provides routing for clocks taken from external clock oscillators connected to I/O. The oscillators can also be generated within the device in the digital system and Universal Digital Blocks.

While the primary DSI clock input provides access to all clocking resources, up to eight other DSI clocks (internally or externally generated) may be routed directly to the eight digital clock dividers. This is only possible if there are multiple precision clock sources.

### 6.1.3 Clock Distribution

All seven clock sources are inputs to the central clock distribution system. The distribution system is designed to create multiple high precision clocks. These clocks are customized for the design's requirements and eliminate the common problems found with limited resolution prescalers attached to peripherals. The clock distribution system generates several types of clock trees.

- The master clock is used to select and supply the fastest clock in the system for general clock requirements and clock synchronization of the PSoC device.

- Bus Clock 16-bit divider uses the master clock to generate the bus clock used for data transfers. Bus clock is the source clock for the CPU clock divider.
- Eight fully programmable 16-bit clock dividers generate digital system clocks for general use in the digital system, as configured by the design's requirements. Digital system clocks can generate custom clocks derived from any of the seven clock sources for any purpose. Examples include baud rate generators, accurate PWM periods, and timer clocks, and many others. If more than eight digital clock dividers are required, the Universal Digital Blocks (UDBs) and fixed function Timer/Counter/PWMs can also generate clocks.
- Four 16-bit clock dividers generate clocks for the analog system components that require clocking, such as ADC. The analog clock dividers include skew control to ensure that critical analog events do not occur simultaneously with digital switching events. This is done to reduce analog system noise.

Each clock divider consists of an 8-input multiplexer, a 16-bit clock divider (divide by 2 and higher) that generates ~50 percent duty cycle clocks, master clock resynchronization logic, and deglitch logic. The outputs from each digital clock tree can be routed into the digital system interconnect and then brought back into the clock system as an input, allowing clock chaining of up to 32 bits.

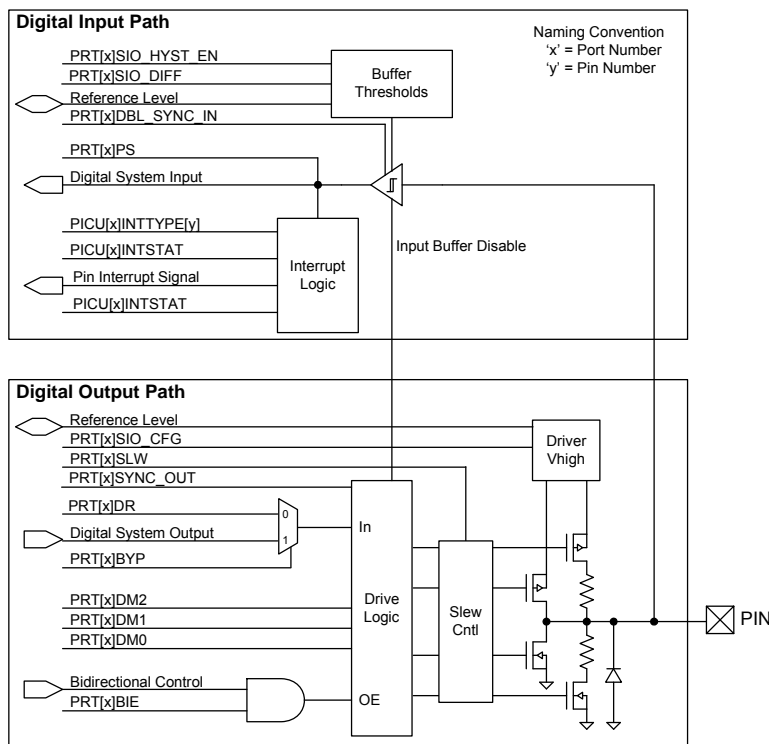
### 6.1.4 USB Clock Domain

The USB clock domain is unique in that it operates largely asynchronously from the main clock network. The USB logic contains a synchronous bus interface to the chip, while running on an asynchronous clock to process USB data. The USB logic requires a 48 MHz frequency. This frequency can be generated from different sources, including DSI clock at 48 MHz or doubled value of 24 MHz from internal oscillator, DSI signal, or crystal oscillator.

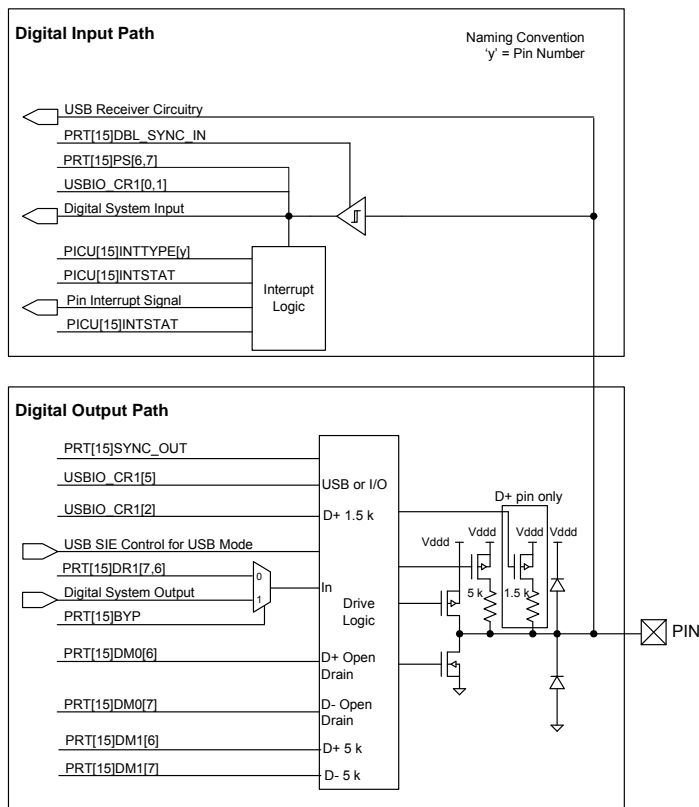
## 6.2 Power System

The power system consists of separate analog, digital, and I/O supply pins, labeled VDDA, VDDD, and VDDIOX, respectively. It also includes two internal 1.8 V regulators that provide the digital (VCCD) and analog (VCCA) supplies for the internal core logic. The output pins of the regulators (VCCD and VCCA) and the VDDIO pins must have capacitors connected as shown in [Figure 6-4](#). The two VCCD pins must be shorted together, with as short a trace as possible, and connected to a 1-μF ±10-percent X5R capacitor. The power system also contains a sleep regulator, an I<sup>2</sup>C regulator, and a hibernate regulator.

**Figure 6-10. SIO Input/Output Block Diagram**



**Figure 6-11. USBIO Block Diagram**



The USBIO pins (P15[7] and P15[6]), when enabled for I/O mode, have limited drive mode control. The drive mode is set using the PRT15.DM0[7, 6] register. A resistive pull option is also available at the USBIO pins, which can be enabled using the PRT15.DM1[7, 6] register. When enabled for USB mode, the drive mode control has no impact on the configuration of the USB pins. Unlike the GPIO and SIO configurations, the port wide configuration registers do not configure the USB drive mode bits. Table 6-7 shows the drive mode configuration for the USBIO pins.

**Table 6-7. USBIO Drive Modes (P15[7] and P15[6])**

PRT15.DM1[7,6] Pull up enable	PRT15.DM0[7,6] Drive Mode enable	PRT15.DR[7,6] = 1	PRT15.DR[7,6] = 0	Description
0	0	High Z	Strong Low	Open Drain, Strong Low
0	1	Strong High	Strong Low	Strong Outputs
1	0	Res High (5k)	Strong Low	Resistive Pull Up, Strong Low
1	1	Strong High	Strong Low	Strong Outputs

## ■ High Impedance Analog

The default reset state with both the output driver and digital input buffer turned off. This prevents any current from flowing in the I/O's digital input buffer due to a floating voltage. This state is recommended for pins that are floating or that support an analog voltage. High impedance analog pins do not provide digital input functionality.

To achieve the lowest chip current in sleep modes, all I/Os must either be configured to the high impedance analog mode, or have their pins driven to a power supply rail by the PSoC device or by external circuitry.

## ■ High Impedance Digital

The input buffer is enabled for digital signal input. This is the standard high impedance (HiZ) state recommended for digital inputs.

## ■ Resistive pull-up or resistive pull-down

Resistive pull-up or pull-down, respectively, provides a series resistance in one of the data states and strong drive in the other. Pins can be used for digital input and output in these modes. Interfacing to mechanical switches is a common application for these modes. Resistive pull-up and pull-down are not available with SIO in regulated output mode.

## ■ Open Drain, Drives High and Open Drain, Drives Low

Open drain modes provide high impedance in one of the data states and strong drive in the other. Pins can be used for digital input and output in these modes. A common application for these modes is driving the I<sup>2</sup>C bus signal lines.

## ■ Strong Drive

Provides a strong CMOS output drive in either high or low state. This is the standard output mode for pins. Strong Drive mode pins must not be used as inputs under normal circumstances. This mode is often used to drive digital output signals or external FETs.

## ■ Resistive pull-up and pull-down

Similar to the resistive pull-up and resistive pull-down modes except the pin is always in series with a resistor. The high data state is pull-up while the low data state is pull-down. This mode is most often used when other signals that may cause shorts can drive the bus. Resistive pull-up and pull-down are not available with SIO in regulated output mode.

### 6.4.2 Pin Registers

Registers to configure and interact with pins come in two forms that may be used interchangeably.

All I/O registers are available in the standard port form, where each bit of the register corresponds to one of the port pins. This register form is efficient for quickly reconfiguring multiple port pins at the same time.

I/O registers are also available in pin form, which combines the eight most commonly used port register bits into a single register for each pin. This enables very fast configuration changes to individual pins with a single register write.

### 6.4.3 Bidirectional Mode

High-speed bidirectional capability allows pins to provide both the high impedance digital drive mode for input signals and a second user selected drive mode such as strong drive (set using PRT×DM[2:0] registers) for output signals on the same pin, based on the state of an auxiliary control bus signal. The bidirectional capability is useful for processor busses and communications interfaces such as the SPI Slave MISO pin that requires dynamic hardware control of the output buffer.

The auxiliary control bus routes up to 16 UDB or digital peripheral generated output enable signals to one or more pins.

### 6.4.4 Slew Rate Limited Mode

GPIO and SIO pins have fast and slow output slew rate options for strong and open drain drive modes, not resistive drive modes. Because it results in reduced EMI, the slow edge rate option is recommended for signals that are not speed critical, generally less than 1 MHz. The fast slew rate is for signals between 1 MHz and 33 MHz. The slew rate is individually configurable for each pin, and is set by the PRT×SLW registers.

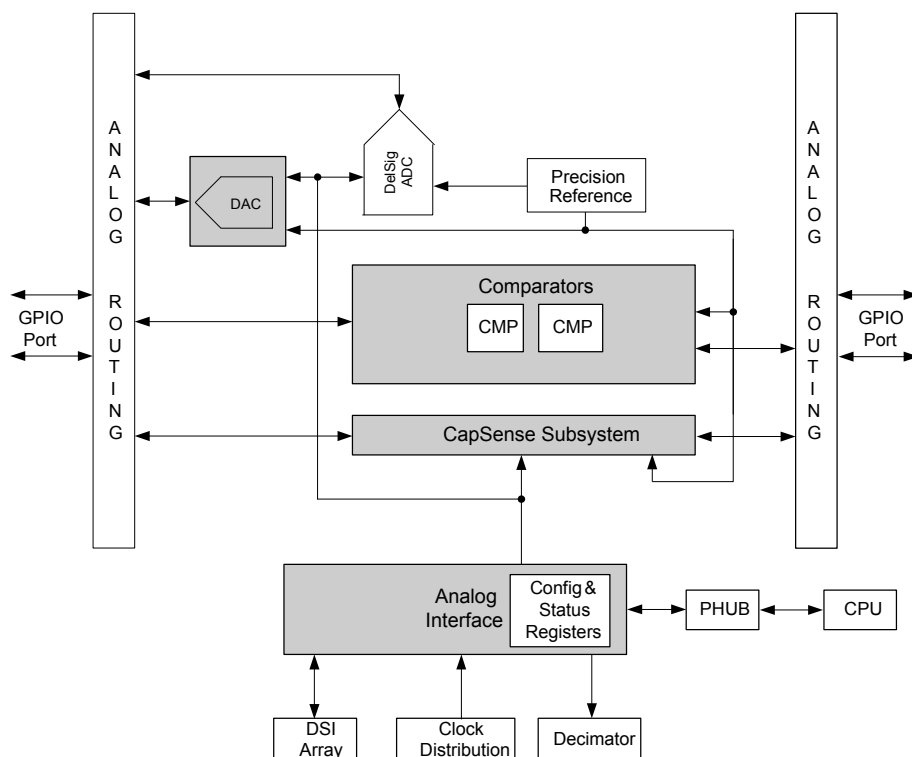
## 8. Analog Subsystem

The analog programmable system creates application specific combinations of both standard and advanced analog signal processing blocks. These blocks are then interconnected to each other and also to any pin on the device, providing a high level of design flexibility and IP security. The features of the analog subsystem are outlined here to provide an overview of capabilities and architecture.

- Flexible, configurable analog routing architecture provided by analog globals, analog mux bus, and analog local buses.

- High resolution delta-sigma ADC.
- One 8-bit DAC that provides either voltage or current output.
- Two comparators with optional connection to configurable LUT outputs.
- CapSense subsystem to enable capacitive touch sensing.
- Precision reference for generating an accurate analog voltage for internal analog blocks.

**Figure 8-1. Analog Subsystem Block Diagram**



The PSoC Creator software program provides a user friendly interface to configure the analog connections between the GPIO and various analog resources and connections from one analog resource to another. PSoC Creator also provides component libraries that allow you to configure the various analog blocks to perform application specific functions. The tool also generates API interface libraries that allow you to write firmware that allows the communication between the analog peripheral and CPU/Memory.

## 11. Electrical Specifications

Specifications are valid for  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$  and  $T_J \leq 100\text{ }^{\circ}\text{C}$ , except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted. The unique flexibility of the PSoC UDBs and analog blocks enable many functions to be implemented in PSoC Creator components, see the component datasheets for full AC/DC specifications of individual functions. See the [“Example Peripherals”](#) section on page 45 for further explanation of PSoC Creator components.

### 11.1 Absolute Maximum Ratings

**Table 11-1. Absolute Maximum Ratings DC Specifications<sup>[15]</sup>**

Parameter	Description	Conditions	Min	Typ	Max	Units
V <sub>DDA</sub>	Analog supply voltage relative to V <sub>SSA</sub>		-0.5	–	6	V
V <sub>DDD</sub>	Digital supply voltage relative to V <sub>SSD</sub>		-0.5	–	6	V
V <sub>DDIO</sub>	I/O supply voltage relative to V <sub>SSD</sub>		-0.5	–	6	V
V <sub>CCA</sub>	Direct analog core voltage input		-0.5	–	1.95	V
V <sub>CCD</sub>	Direct digital core voltage input		-0.5	–	1.95	V
V <sub>SSA</sub>	Analog ground voltage		V <sub>SSD</sub> - 0.5	–	V <sub>SSD</sub> + 0.5	V
V <sub>GPIO</sub> <sup>[16]</sup>	DC input voltage on GPIO	Includes signals sourced by V <sub>DDA</sub> and routed internal to the pin	V <sub>SSD</sub> - 0.5	–	V <sub>DDIO</sub> + 0.5	V
V <sub>SIO</sub>	DC input voltage on SIO	Output disabled	V <sub>SSD</sub> - 0.5	–	7	V
		Output enabled	V <sub>SSD</sub> - 0.5	–	6	V
V <sub>IND</sub>	Voltage at boost converter input		0.5	–	5.5	V
V <sub>BAT</sub>	Boost converter supply		V <sub>SSD</sub> - 0.5	–	5.5	V
I <sub>VDDIO</sub>	Current per V <sub>DDIO</sub> supply pin		–	–	100	mA
I <sub>GPIO</sub>	GPIO current		-30	–	41	mA
I <sub>SIO</sub>	SIO current		-49	–	28	mA
I <sub>USBIO</sub>	USBIO current		-56	–	59	mA
VEXTREF	ADC external reference inputs	Pins P0[3], P3[2]	–	–	2	V
LU	Latch up current <sup>[17]</sup>		-140	–	140	mA
ESD <sub>HBM</sub>	Electrostatic discharge voltage, Human body model	V <sub>SSA</sub> tied to V <sub>SSD</sub>	2200	–	–	V
		V <sub>SSA</sub> not tied to V <sub>SSD</sub>	750	–	–	V
ESD <sub>CDM</sub>	Electrostatic discharge voltage, Charge device model		500	–	–	V

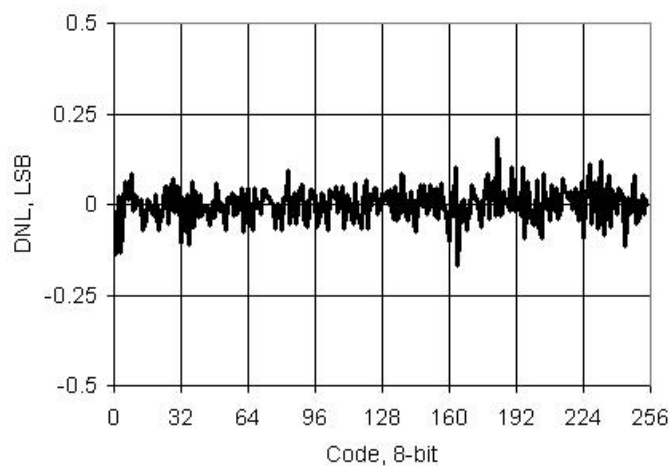
#### Notes

15. Usage above the absolute maximum conditions listed in [Table 11-1](#) may cause permanent damage to the device. Exposure to Absolute Maximum conditions for extended periods of time may affect device reliability. The Maximum Storage Temperature is 150 °C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below Absolute Maximum conditions but above normal operating conditions, the device may not operate to specification.

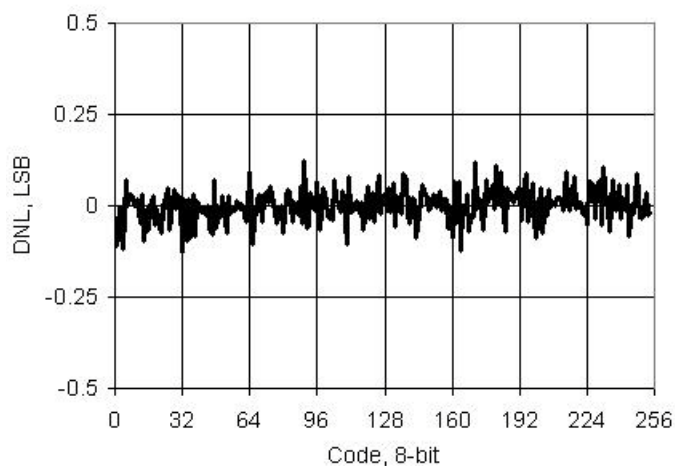
16. The V<sub>DDIO</sub> supply voltage must be greater than the maximum voltage on the associated GPIO pins. Maximum voltage on GPIO pin  $\leq V_{DDIO} \leq V_{DDA}$ .

17. Meets or exceeds JEDEC Spec EIA/JESD78 IC Latch-up Test.

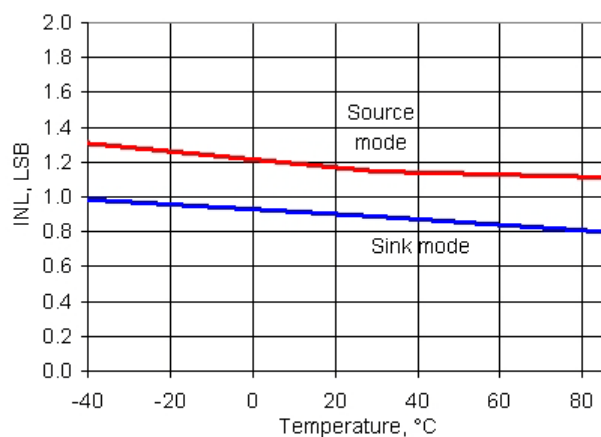
**Figure 11-28. IDAC DNL vs Input Code, Range = 255  $\mu$ A, Source Mode**



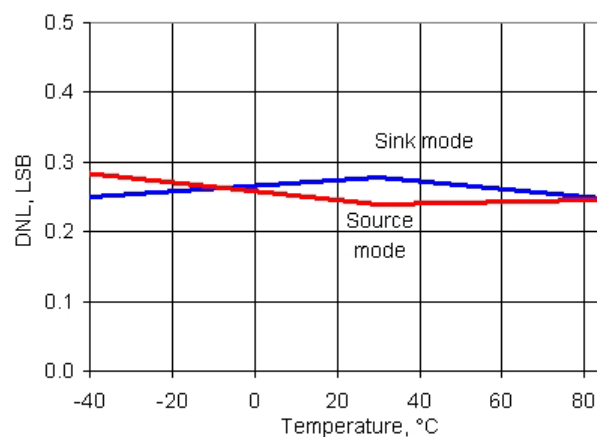
**Figure 11-29. IDAC DNL vs Input Code, Range = 255  $\mu$ A, Sink Mode**



**Figure 11-30. IDAC INL vs Temperature, Range = 255  $\mu$ A, High speed mode**



**Figure 11-31. IDAC DNL vs Temperature, Range = 255  $\mu$ A, High speed mode**



## 11.5.6 Voltage Digital to Analog Converter (VDAC)

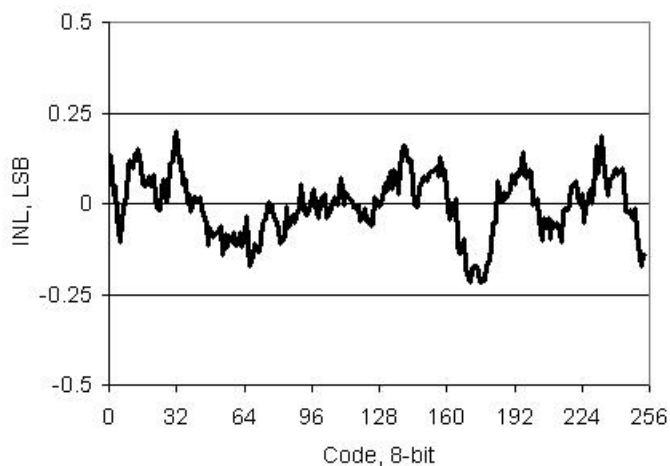
See the VDAC component datasheet in PSoC Creator for full electrical specifications and APIs.

Unless otherwise specified, all charts and graphs show typical values.

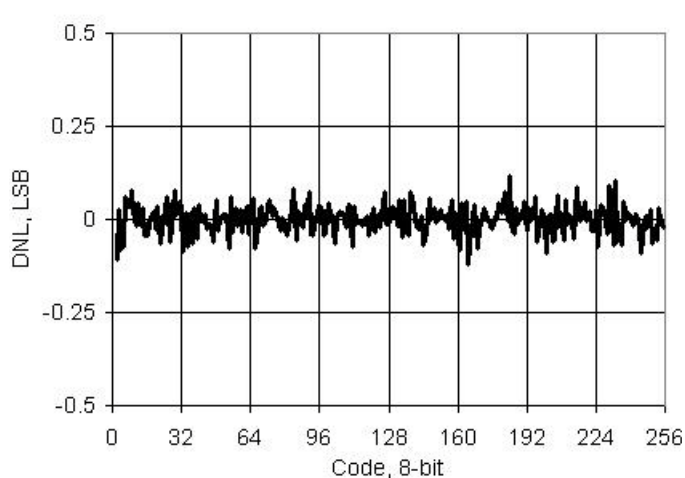
**Table 11-28. VDAC DC Specifications**

Parameter	Description	Conditions	Min	Typ	Max	Units
	Resolution		–	8	–	bits
INL1	Integral nonlinearity	1 V scale	–	±2.1	±2.5	LSB
INL4	Integral nonlinearity <sup>[52]</sup>	4 V scale	–	±2.1	±2.5	LSB
DNL1	Differential nonlinearity	1 V scale	–	±0.3	±1	LSB
DNL4	Differential nonlinearity <sup>[52]</sup>	4 V scale	–	±0.3	±1	LSB
Rout	Output resistance	1 V scale	–	4	–	kΩ
		4 V scale	–	16	–	kΩ
V <sub>OUT</sub>	Output voltage range, code = 255	1 V scale	–	1.02	–	V
		4 V scale, V <sub>DDA</sub> = 5 V	–	4.08	–	V
	Monotonicity		–	–	Yes	–
V <sub>OS</sub>	Zero scale error		–	0	±0.9	LSB
Eg	Gain error	1 V scale	–	–	±2.5	%
		4 V scale	–	–	±2.5	%
TC_Eg	Temperature coefficient, gain error	1 V scale	–	–	0.03	%FSR / °C
		4 V scale	–	–	0.03	%FSR / °C
I <sub>DD</sub>	Operating current	Low speed mode	–	–	100	μA
		High speed mode	–	–	500	μA

**Figure 11-40. VDAC INL vs Input Code, 1 V Mode**



**Figure 11-41. VDAC DNL vs Input Code, 1 V Mode**



**Note**

52. Based on device characterization (Not production tested).

## 11.5.7 Temperature Sensor

**Table 11-30. Temperature Sensor Specifications**

Parameter	Description	Conditions	Min	Typ	Max	Units
	Temp sensor accuracy	Range: -40 °C to +85 °C	–	±5	–	°C

## 11.5.8 LCD Direct Drive

**Table 11-31. LCD Direct Drive DC Specifications**

Parameter	Description	Conditions	Min	Typ	Max	Units
$I_{CC}$	LCD system operating current	Device sleep mode with wakeup at 400-Hz rate to refresh LCDs, bus clock = 3 MHz, $V_{DDIO} = V_{DDA} = 3\text{ V}$ , 4 commons, 16 segments, 1/4 duty cycle, 50 Hz frame rate, no glass connected	–	38	–	μA
$I_{CC\_SEG}$	Current per segment driver	Strong drive mode	–	260	–	μA
$V_{BIAS}$	LCD bias range ( $V_{BIAS}$ refers to the main output voltage( $V_0$ ) of LCD DAC)	$V_{DDA} \geq 3\text{ V}$ and $V_{DDA} \geq V_{BIAS}$	2	–	5	V
	LCD bias step size	$V_{DDA} \geq 3\text{ V}$ and $V_{DDA} \geq V_{BIAS}$	–	$9.1 \times V_{DDA}$	–	mV
	LCD capacitance per segment/common driver	Drivers may be combined	–	500	5000	pF
	Long term segment offset		–	–	20	mV
$I_{OUT}$	Output drive current per segment driver)	$V_{DDIO} = 5.5\text{V}$ , strong drive mode	355	–	710	μA

**Table 11-32. LCD Direct Drive AC Specifications**

Parameter	Description	Conditions	Min	Typ	Max	Units
$f_{LCD}$	LCD frame rate		10	50	150	Hz

## 11.6.3 Pulse Width Modulation

The following specifications apply to the Timer/Counter/PWM peripheral, in PWM mode. PWM components can also be implemented in UDBs; for more information, see the PWM component datasheet in PSoC Creator.

**Table 11-37. PWM DC Specifications**

Parameter	Description	Conditions	Min	Typ	Max	Units
	Block current consumption	16-bit PWM, at listed input clock frequency	–	–	–	μA
	3 MHz		–	15	–	μA
	12 MHz		–	60	–	μA
	50 MHz		–	260	–	μA

**Table 11-38. Pulse Width Modulation (PWM) AC Specifications**

Parameter	Description	Conditions	Min	Typ	Max	Units
	Operating frequency		DC	–	50.01	MHz
	Pulse width		21	–	–	ns
	Pulse width (external)		42	–	–	ns
	Kill pulse width		21	–	–	ns
	Kill pulse width (external)		42	–	–	ns
	Enable pulse width		21	–	–	ns
	Enable pulse width (external)		42	–	–	ns
	Reset pulse width		21	–	–	ns
	Reset pulse width (external)		42	–	–	ns

## 11.6.4 I<sup>2</sup>C

**Table 11-39. Fixed I<sup>2</sup>C DC Specifications**

Parameter	Description	Conditions	Min	Typ	Max	Units
	Block current consumption	Enabled, configured for 100 kbps	–	–	250	μA
		Enabled, configured for 400 kbps	–	–	260	μA
		Wake from sleep mode	–	–	30	μA

**Table 11-40. Fixed I<sup>2</sup>C AC Specifications**

Parameter	Description	Conditions	Min	Typ	Max	Units
	Bit rate		–	–	1	Mbps

## 11.6.5 Controller Area Network

**Table 11-41. CAN DC Specifications<sup>[53]</sup>**

Parameter	Description	Conditions	Min	Typ	Max	Units
I <sub>DD</sub>	Block current consumption		–	–	200	μA

**Table 11-42. CAN AC Specifications<sup>[53]</sup>**

Parameter	Description	Conditions	Min	Typ	Max	Units
	Bit rate	Minimum 8 MHz clock	–	–	1	Mbit

### Note

53. Refer to ISO 11898 specification for details.

## 11.7.2 EEPROM

**Table 11-47. EEPROM DC Specifications**

Parameter	Description	Conditions	Min	Typ	Max	Units
	Erase and program voltage		1.71	–	5.5	V

**Table 11-48. EEPROM AC Specifications**

Parameter	Description	Conditions	Min	Typ	Max	Units
$T_{WRITE}$	Single row erase/write cycle time		–	10	20	ms
	EEPROM data retention time, retention period measured from last erase cycle	Average ambient temp, $T_A \leq 25^\circ\text{C}$ , 1M erase/program cycles	20	–	–	years
		Average ambient temp, $T_A \leq 55^\circ\text{C}$ , 100 K erase/program cycles	20	–	–	
		Average ambient temp. $T_A \leq 85^\circ\text{C}$ , 10 K erase/program cycles	10	–	–	

## 11.7.3 Nonvolatile Latches (NVL)

**Table 11-49. NVL DC Specifications**

Parameter	Description	Conditions	Min	Typ	Max	Units
	Erase and program voltage	$V_{DDD}$ pin	1.71	–	5.5	V

**Table 11-50. NVL AC Specifications**

Parameter	Description	Conditions	Min	Typ	Max	Units
	NVL endurance	Programmed at $25^\circ\text{C}$	1K	–	–	program/erase cycles
		Programmed at $0^\circ\text{C}$ to $70^\circ\text{C}$	100	–	–	program/erase cycles
	NVL data retention time	Average ambient temp. $T_A \leq 55^\circ\text{C}$	20	–	–	years
		Average ambient temp. $T_A \leq 85^\circ\text{C}$	10	–	–	years

## 11.7.4 SRAM

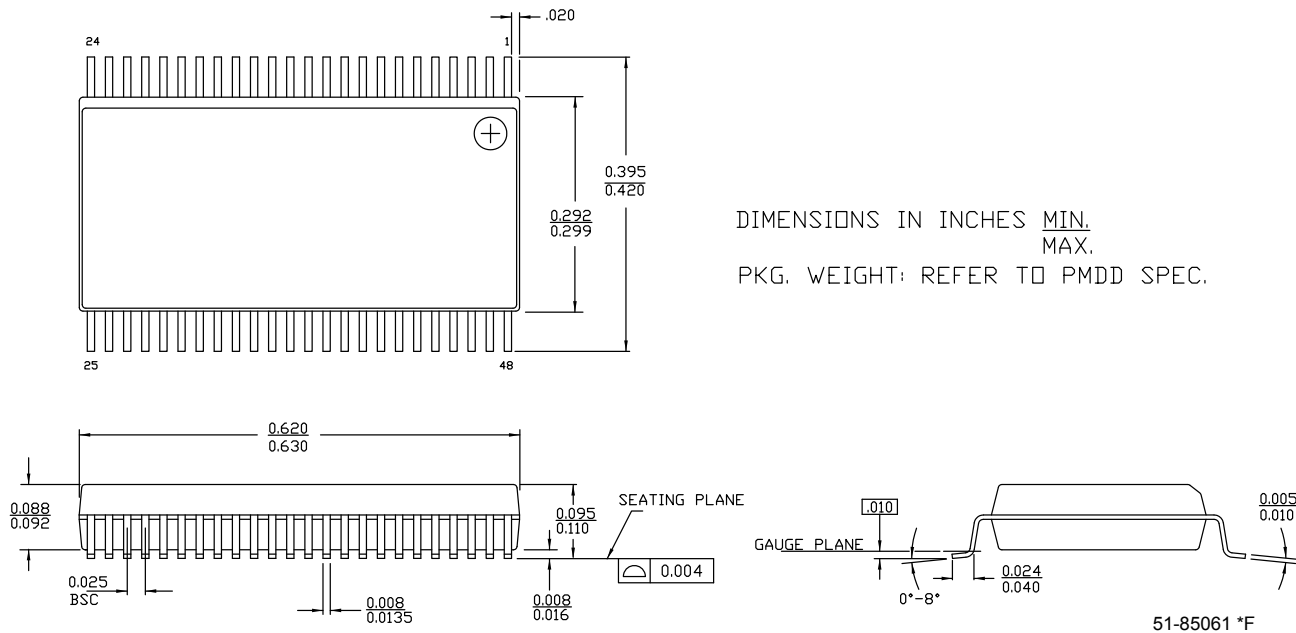
**Table 11-51. SRAM DC Specifications**

Parameter	Description	Conditions	Min	Typ	Max	Units
$V_{SRAM}$	SRAM retention voltage		1.2	–	–	V

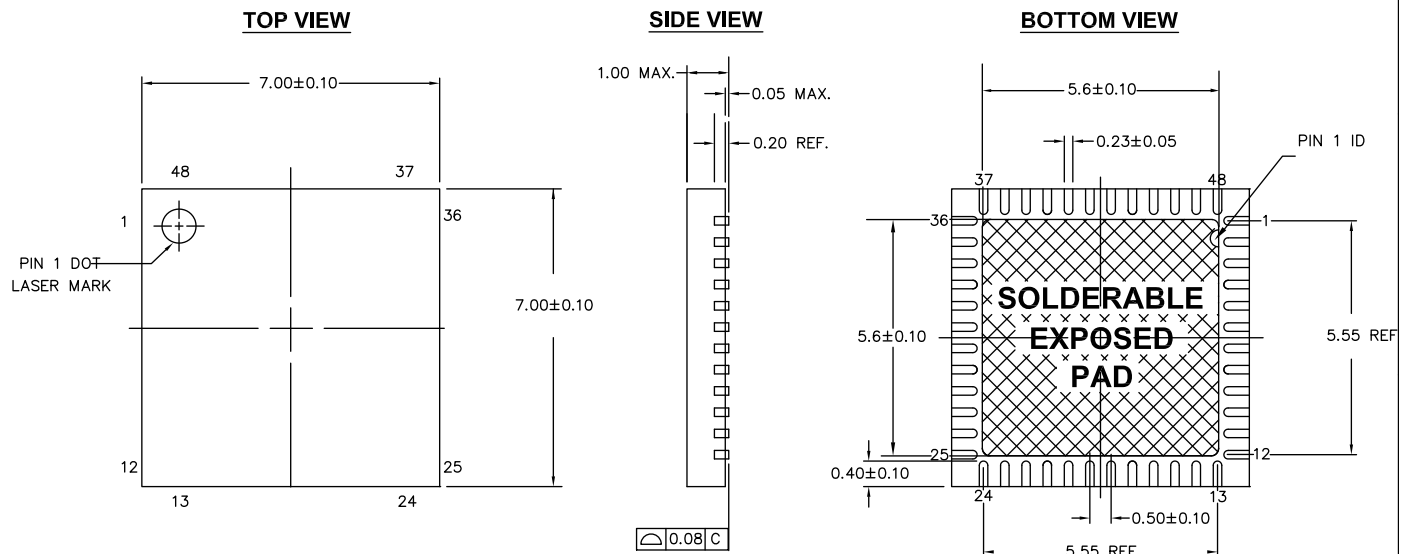
**Table 11-52. SRAM AC Specifications**

Parameter	Description	Conditions	Min	Typ	Max	Units
$F_{SRAM}$	SRAM operating frequency		DC	–	50.01	MHz


**Figure 13-1. 48-pin (300 mil) SSOP Package Outline**



**Figure 13-2. 48-pin QFN Package Outline**



**NOTES:**

1.  HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO-220
3. PACKAGE WEIGHT: REFER TO PMDD SPEC.
4. ALL DIMENSIONS ARE IN MM [MIN/MAX]
5. PACKAGE CODE

PART #	DESCRIPTION
LT48D	LEAD FREE

001-45616 \*E

**Table 14-1. Acronyms Used in this Document** *(continued)*

Acronym	Description
PHUB	peripheral hub
PHY	physical layer
PICU	port interrupt control unit
PLA	programmable logic array
PLD	programmable logic device, see also PAL
PLL	phase-locked loop
PMDD	package material declaration datasheet
POR	power-on reset
PRES	precise low-voltage reset
PRS	pseudo random sequence
PS	port read data register
PSoC®	Programmable System-on-Chip™
PSRR	power supply rejection ratio
PWM	pulse-width modulator
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RTL	register transfer language
RTR	remote transmission request
RX	receive
SAR	successive approximation register
SC/CT	switched capacitor/continuous time
SCL	I <sup>2</sup> C serial clock
SDA	I <sup>2</sup> C serial data
S/H	sample and hold
SINAD	signal to noise and distortion ratio
SIO	special input/output, GPIO with advanced features. See GPIO.
SOC	start of conversion

**Table 14-1. Acronyms Used in this Document** *(continued)*

Acronym	Description
SOF	start of frame
SPI	Serial Peripheral Interface, a communications protocol
SR	slew rate
SRAM	static random access memory
SRES	software reset
SWD	serial wire debug, a test protocol
SWV	single-wire viewer
TD	transaction descriptor, see also DMA
THD	total harmonic distortion
TIA	transimpedance amplifier
TRM	technical reference manual
TTL	transistor-transistor logic
TX	transmit
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
UDB	universal digital block
USB	Universal Serial Bus
USBIO	USB input/output, PSoC pins used to connect to a USB port
VDAC	voltage DAC, see also DAC, IDAC
WDT	watchdog timer
WOL	write once latch, see also NVL
WRES	watchdog timer reset
XRES	external reset I/O pin
XTAL	crystal

## 15. Reference Documents

[PSoC® 3, PSoC® 5 Architecture TRM](#)

[PSoC® 3 Registers TRM](#)

**Description Title: PSoC® 3: CY8C32 Family Data Sheet Programmable System-on-Chip (PSoC®) (continued)**  
**Document Number: 001-56955**

Revision	ECN	Submission Date	Orig. of Change	Description of Change
*L	3464258	12/14/2011	MKEA	<p>Updated Analog Global specs</p> <p>Updated IDAC range</p> <p>Modified VDDIO description in Section 3</p> <p>Added note on Sleep and Hibernate modes in the Power Modes section</p> <p>Updated Boost Converter section</p> <p>Updated conditions for Inductive boost AC specs</p> <p>Added VDAC/IDAC noise graphs and specs</p> <p>Added pin capacitance specs for ECO pins</p> <p>Removed <math>C_L</math> from 32 kHz External Crystal DC Specs table.</p> <p>Added reference to AN54439 in Section 6.1.2.2</p> <p>Deleted T_SWDO_hold row from the SWD Interface AC Specifications table</p> <p>Removed Pin 46 connections in "Example Schematic for 100-pin TQFP Part with Power Connections"</p> <p>Updated Active Mode IDD description in Table 11-2.</p> <p>Added I_DDDR and I_DDAR specs in Table 11-2.</p> <p>Replaced "total device program time" with T_PROG in Flash AC specs table</p> <p>Added I_GPIO, I_SIO and I_USBIO specs in Absolute Maximum Ratings</p> <p>Added conditions to I_CC spec in 32 kHz External Crystal DC Specs table.</p> <p>Updated TCV_OS value</p> <p>Removed Boost Efficiency vs V_OUT graph</p> <p>Updated boost graphs</p> <p>Updated min value of GPIO input edge rate</p> <p>Removed 3.4 Mbps in UDBs from I2C section</p> <p>Updated USBIO Block diagram; added USBIO drive mode description</p> <p>Updated Analog Interconnect diagram</p> <p>Changed max IMO startup time to 12 <math>\mu</math>s</p> <p>Added note for I_IL spec in USBIO DC specs table</p> <p>Updated GPIO Block diagram</p> <p>Updated voltage reference specs</p> <p>Added text explaining power supply ramp up in Section 11-4.</p>