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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	50MHz
Connectivity	EBI/EMI, I ² C, LINbus, SPI, UART/USART
Peripherals	CapSense, DMA, LCD, POR, PWM, WDT
Number of I/O	38
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 16x12b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	68-VFQFN Exposed Pad
Supplier Device Package	68-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c3245lti-163

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



1. Architectural Overview

Introducing the CY8C32 family of ultra low-power, flash Programmable System-on-Chip (PSoC[®]) devices, part of a scalable 8-bit PSoC 3 and 32-bit PSoC 5 platform. The CY8C32 family provides configurable blocks of analog, digital, and interconnect circuitry around a CPU subsystem. The combination of a CPU with a flexible analog subsystem, digital subsystem, routing, and I/O enables a high level of integration in a wide variety of consumer, industrial, and medical applications.



Figure 1-1. Simplified Block Diagram

Figure 1-1 illustrates the major components of the CY8C32 family. They are:

- 8051 CPU subsystem
- Nonvolatile subsystem
- Programming, debug, and test subsystem
- Inputs and outputs
- Clocking
- Power
- Digital subsystem
- Analog subsystem

PSoC's digital subsystem provides half of its unique configurability. It connects a digital signal from any peripheral to any pin through the Digital System Interconnect (DSI). It also provides functional flexibility through an array of small, fast, low-power UDBs. PSoC Creator provides a library of prebuilt and tested standard digital peripherals (UART, SPI, LIN, PRS, CRC, timer, counter, PWM, AND, OR, and so on) that are mapped to the UDB array. You can also easily create a digital circuit using boolean primitives by means of graphical design entry. Each UDB contains programmable array logic (PAL)/programmable logic device (PLD) functionality, together with a small state machine engine to support a wide variety of peripherals.





This enables the device to be powered directly from a single battery or solar cell. In addition, you can use the boost converter to generate other voltages required by the device, such as a 3.3-V supply for LCD glass drive. The boost's output is available on the V_{BOOST} pin, allowing other devices in the application to be powered from the PSoC.

PSoC supports a wide range of low-power modes. These include a 200-nA hibernate mode with RAM retention and a $1-\mu$ A sleep mode with RTC. In the second mode the optional 32.768-kHz watch crystal runs continuously and maintains an accurate RTC.

Power to all major functional blocks, including the programmable digital and analog peripherals, can be controlled independently by firmware. This allows low-power background processing when some peripherals are not in use. This, in turn, provides a total device current of only 1.2 mA when the CPU is running at 6 MHz, or 0.8 mA running at 3 MHz.

The details of the PSoC power modes are covered in the "Power System" section on page 31 of this datasheet.

PSoC uses JTAG (4-wire) or SWD (2-wire) interfaces for programming, debug, and test. The 1-wire SWV may also be used for "printf" style debugging. By combining SWD and SWV, you can implement a full debugging interface with just three pins. Using these standard interfaces enables you to debug or program the PSoC with a variety of hardware solutions from Cypress or third party vendors. PSoC supports on-chip break points and 4-KB instruction and data race memory for debug. Details of the programming, test, and debugging interfaces are discussed in the "Programming, Debug Interfaces, Resources" section on page 62 of this datasheet.

2. Pinouts

Each VDDIO pin powers a specific set of I/O pins. (The USBIOs are powered from VDDD.) Using the VDDIO pins, a single PSoC can support multiple voltage levels, reducing the need for off-chip level shifters. The black lines drawn on the pinout diagrams in Figure 2-3 through Figure 2-6, as well as Table 2-1, show the pins that are powered by each VDDIO.

Each VDDIO may source up to 100 mA total to its associated I/O pins, as shown in Figure 2-1.

Figure 2-1. VDDIO Current Limit



Conversely, for the 100-pin and 68-pin devices, the set of I/O pins associated with any VDDIO may sink up to 100 mA total, as shown in Figure 2-2.

Figure 2-2. I/O Pins Current Limit



For the 48-pin devices, the set of I/O pins associated with VDDIO0 plus VDDIO2 may sink up to 100 mA total. The set of I/O pins associated with VDDIO1 plus VDDIO3 may sink up to a total of 100 mA.





Figure 2-8. Example PCB Layout for 100-pin TQFP Part for Optimal Analog Performance

3. Pin Descriptions

IDAC0

Low resistance output pin for high current DAC (IDAC).

Extref0, Extref1

External reference input to the analog system.

GPIO

General purpose I/O pin provides interfaces to the CPU, digital peripherals, analog peripherals, interrupts, LCD segment drive, and CapSense.

12C0: SCL, 12C1: SCL

 I^2C SCL line providing wake from sleep on an address match. Any I/O pin can be used for I^2C SCL if wake from sleep is not required.

12C0: SDA, 12C1: SDA

 $\rm I^2C$ SDA line providing wake from sleep on an address match. Any I/O pin can be used for $\rm I^2C$ SDA if wake from sleep is not required.

Ind

Inductor connection to boost pump.

kHz XTAL: Xo, kHz XTAL: Xi

32.768-kHz crystal oscillator pin.

MHz XTAL: Xo, MHz XTAL: Xi

4- to 25- MHz crystal oscillator pin.

nTRST

Optional JTAG test reset programming and debug port connection to reset the JTAG connection.

SIO

Special I/O provides interfaces to the CPU, digital peripherals and interrupts with a programmable high threshold voltage, analog comparator, high sink current, and high impedance state when the device is unpowered.

SWDCK

Serial wire debug clock programming and debug port connection.

SWDIO

Serial wire debug input and output programming and debug port connection.

SWV.

Single wire viewer debug output.

тск

JTAG test clock programming and debug port connection.

TDI

JTAG test data in programming and debug port connection.

TDO

JTAG test data out programming and debug port connection.

TMS

JTAG test mode select programming and debug port connection.



4.3 Instruction Set

The 8051 instruction set is highly optimized for 8-bit handling and Boolean operations. The types of instructions supported include:

- Arithmetic instructions
- Logical instructions
- Data transfer instructions
- Boolean instructions
- Program branching instructions

Table 4-1. Arithmetic Instructions

4.3.1 Instruction Set Summary

4.3.1.1 Arithmetic Instructions

Arithmetic instructions support the direct, indirect, register, immediate constant, and register-specific instructions. Arithmetic modes are used for addition, subtraction, multiplication, division, increment, and decrement operations. Table 4-1 lists the different arithmetic instructions.

Mnemonic	Description	Bytes	Cycles
ADD A,Rn	Add register to accumulator	1	1
ADD A,Direct	Add direct byte to accumulator	2	2
ADD A,@Ri	Add indirect RAM to accumulator	1	2
ADD A,#data	Add immediate data to accumulator	2	2
ADDC A,Rn	Add register to accumulator with carry	1	1
ADDC A, Direct	Add direct byte to accumulator with carry	2	2
ADDC A,@Ri	Add indirect RAM to accumulator with carry	1	2
ADDC A,#data	Add immediate data to accumulator with carry	2	2
SUBB A,Rn	Subtract register from accumulator with borrow	1	1
SUBB A, Direct	Subtract direct byte from accumulator with borrow	2	2
SUBB A,@Ri	Subtract indirect RAM from accumulator with borrow	1	2
SUBB A,#data	Subtract immediate data from accumulator with borrow	2	2
INC A	Increment accumulator	1	1
INC Rn	Increment register	1	2
INC Direct	Increment direct byte	2	3
INC @Ri	Increment indirect RAM	1	3
DEC A	Decrement accumulator	1	1
DEC Rn	Decrement register	1	2
DEC Direct	Decrement direct byte	2	3
DEC @Ri	Decrement indirect RAM	1	3
INC DPTR	Increment data pointer	1	1
MUL	Multiply accumulator and B	1	2
DIV	Divide accumulator by B	1	6
DAA	Decimal adjust accumulator	1	3





Figure 4-2. Interrupt Processing Timing Diagram

Notes

- 1: Interrupt triggered asynchronous to the clock
- 2: The PEND bit is set on next active clock edge to indicate the interrupt arrival
- 3: POST bit is set following the PEND bit
- 4: Interrupt request and the interrupt number sent to CPU core after evaluation priority (Takes 3 clocks)
- 5: ISR address is posted to CPU core for branching
- 6: CPU acknowledges the interrupt request
- 7: ISR address is read by CPU for branching
- 8, 9: PEND and POST bits are cleared respectively after receiving the IRA from core
- 10: IRA bit is cleared after completing the current instruction and starting the instruction execution from ISR location (Takes 7 cycles)
- 11: IRC is set to indicate the completion of ISR, Active int. status is restored with previous status

The total interrupt latency (ISR execution)

- = POST + PEND + IRQ + IRA + Completing current instruction and branching
- = 1+1+1+2+7 cycles
- = 12 cycles



Figure 4-3. Interrupt Structure







Notes

- The two VCCD pins must be connected together with as short a trace as possible. A trace under the device is recommended, as shown in Figure 2-8 on page 12.
- It is good practice to check the datasheets for your bypass capacitors, specifically the working voltage and the DC bias specifications. With some capacitors, the actual capacitance can decrease considerably when the DC bias (VDDX or VCCX in Figure 6-4) is a significant percentage of the rated working voltage.
- You can power the device in internally regulated mode, where the voltage applied to the VDDx pins is as high as 5.5 V, and the internal regulators provide the core voltages. In this mode, do not apply power to the VCCx pins, and do not tie the VDDx pins to the VCCx pins.
- You can also power the device in externally regulated mode, that is, by directly powering the VCCD and VCCA pins. In this configuration, the VDDD pins should be shorted to the VCCD pins and the VDDA pin should be shorted to the VCCA pin. The allowed supply range in this configuration is 1.71 V to 1.89 V. After power up in this configuration, the internal regulators are on by default, and should be disabled to reduce power consumption.



The term **device reset** indicates that the processor as well as analog and digital peripherals and registers are reset.

A reset status register shows some of the resets or power voltage monitoring interrupts. The program may examine this register to detect and report certain exception conditions. This register is cleared after a power-on reset. For details see the Technical Reference Manual.

6.3.1 Reset Sources

- 6.3.1.1 Power Voltage Level Monitors
- IPOR Initial Power-on Reset

At initial power on, IPOR monitors the power voltages VDDD, VDDA, VCCD, and VCCA. The trip level is not precise. It is set to approximately 1 volt, which is below the lowest specified operating voltage but high enough for the internal circuits to be reset and to hold their reset state. The monitor generates a reset pulse that is at least 150 ns wide. It may be much wider if one or more of the voltages ramps up slowly.

After boot, the IPOR circuit is disabled and voltage supervision is handed off to the precise low-voltage reset (PRES) circuit.

PRES – Precise Low Voltage Reset

This circuit monitors the outputs of the analog and digital internal regulators after power up. The regulator outputs are compared to a precise reference voltage. The response to a PRES trip is identical to an IPOR reset.

In normal operating mode, the program cannot disable the digital PRES circuit. The analog regulator can be disabled, which also disables the analog portion of the PRES. The PRES circuit is disabled automatically during sleep and hibernate modes, with one exception: During sleep mode the regulators are periodically activated (buzzed) to provide supervisory services and to reduce wakeup time. At these times the PRES circuit is also buzzed to allow periodic voltage monitoring.

ALVI, DLVI, AHVI – Analog/Digital Low Voltage Interrupt, Analog High Voltage Interrupt

Interrupt circuits are available to detect when VDDA and VDDD go outside a voltage range. For AHVI, VDDA is compared to a fixed trip level. For ALVI and DLVI, VDDA and VDDD are compared to trip levels that are programmable, as listed in Table 6-5. ALVI and DLVI can also be configured to generate a device reset instead of an interrupt.

Table 6-5. Analog/Digital Low Voltage Interrupt, Analog High Voltage Interrupt

Interrupt	Supply	Normal Voltage Range	Available Trip Settings
DLVI	VDDD	1.71 V – 5.5 V	1.70 V – 5.45 V in 250 mV increments
ALVI	VDDA	1.71 V – 5.5 V	1.70 V – 5.45 V in 250 mV increments
AHVI	VDDA	1.71 V – 5.5 V	5.75 V

The monitors are disabled until after IPOR. During sleep mode these circuits are periodically activated (buzzed). If an interrupt occurs during buzzing then the system first enters its wake up sequence. The interrupt is then recognized and may be serviced. The buzz frequency is adjustable, and should be set to be less than the minimum time that any voltage is expected to be out of range. For details on how to adjust the buzz frequency, see the TRM.

6.3.1.2 Other Reset Sources

XRES – External Reset

PSoC 3 has either a single GPIO pin that is configured as an external reset or a dedicated XRES pin. Either the dedicated XRES pin or the GPIO pin, if configured, holds the part in reset while held active (low). The response to an XRES is the same as to an IPOR reset.

After XRES has been deasserted, at least 10 μs must elapse before it can be reasserted.

The external reset is active low. It includes an internal pull-up resistor. XRES is active during sleep and hibernate modes.

SRES – Software Reset

A reset can be commanded under program control by setting a bit in the software reset register. This is done either directly by the program or indirectly by DMA access. The response to a SRES is the same as after an IPOR reset.

Another register bit exists to disable this function.

WRES – Watchdog Timer Reset

The watchdog reset detects when the software program is no longer being executed correctly. To indicate to the watchdog timer that it is running correctly, the program must periodically reset the timer. If the timer is not reset before a user-specified amount of time, then a reset is generated.

Note IPOR disables the watchdog function. The program must enable the watchdog function at an appropriate point in the code by setting a register bit. When this bit is set, it cannot be cleared again except by an IPOR power-on reset event.

6.4 I/O System and Routing

PSoC I/Os are extremely flexible. Every GPIO has analog and digital I/O capability. All I/Os have a large number of drive modes, which are set at POR. PSoC also provides up to four individual I/O voltage domains through the VDDIO pins.

There are two types of I/O pins on every device; those with USB provide a third type. Both GPIO and Special I/O (SIO) provide similar digital functionality. The primary differences are their analog capability and drive strength. Devices that include USB also provide two USBIO pins that support specific USB functionality as well as limited GPIO capability.

All I/O pins are available for use as digital inputs and outputs for both the CPU and digital peripherals. In addition, all I/O pins can generate an interrupt. The flexible and advanced capabilities of the PSoC I/O, combined with any signal to any pin routability, greatly simplify circuit design and board layout. All GPIO pins can be used for analog input, CapSense, and LCD segment drive, while SIO pins are used for voltages in excess of VDDA and for programmable output voltages.

- Features supported by both GPIO and SIO:
 - User programmable port reset state
- Separate I/O supplies and voltages for up to four groups of I/O
- Digital peripherals use DSI to connect the pins





Figure 6-10. SIO Input/Output Block Diagram

Figure 6-11. USBIO Block Diagram





7.5 USB

PSoC includes a dedicated Full-Speed (12 Mbps) USB 2.0 transceiver supporting all four USB transfer types: control, interrupt, bulk, and isochronous. PSoC Creator provides full configuration support. USB interfaces to hosts through two dedicated USBIO pins, which are detailed in the "I/O System and Routing" section on page 37.

USB includes the following features:

- Eight unidirectional data endpoints
- One bidirectional control endpoint 0 (EP0)
- Shared 512-byte buffer for the eight data endpoints
- Dedicated 8-byte buffer for EP0
- Three memory modes
 - Manual Memory Management with No DMA Access
- Manual Memory Management with Manual DMA Access
 Automatic Memory Management with Automatic DMA Access
- Internal 3.3 V regulator for transceiver
- Internal 48 MHz main oscillator mode that auto locks to USB bus clock, requiring no external crystal for USB (USB equipped parts only)
- Interrupts on bus and each endpoint event, with device wakeup
- USB Reset, Suspend, and Resume operations
- Bus powered and self powered modes

Figure 7-14. USB



7.6 Timers, Counters, and PWMs

The Timer/Counter/PWM peripheral is a 16-bit dedicated peripheral providing three of the most common embedded peripheral features. As almost all embedded systems use some combination of timers, counters, and PWMs. Four of them have been included on this PSoC device family. Additional and more advanced functionality timers, counters, and PWMs can also be instantiated in Universal Digital Blocks (UDBs) as required. PSoC Creator allows you to choose the timer, counter, and PWM features that they require. The tool set utilizes the most optimal resources available.

The Timer/Counter/PWM peripheral can select from multiple clock sources, with input and output signals connected through the DSI routing. DSI routing allows input and output connections to any device pin and any internal digital signal accessible through the DSI. Each of the four instances has a compare output, terminal count output (optional complementary compare output), and programmable interrupt request line. The Timer/Counter/PWMs are configurable as free running, one shot, or Enable input controlled. The peripheral has timer reset and capture inputs, and a kill input for control of the comparator outputs. The peripheral supports full 16-bit capture.

Timer/Counter/PWM features include:

- 16-bit Timer/Counter/PWM (down count only)
- Selectable clock source
- PWM comparator (configurable for LT, LTE, EQ, GTE, GT)
- Period reload on start, reset, and terminal count
- Interrupt on terminal count, compare true, or capture
- Dynamic counter reads
- Timer capture mode
- Count while enable signal is asserted mode
- Free run mode
- One Shot mode (stop at end of period)
- Complementary PWM outputs with deadband
- PWM output kill

Figure 7-15. Timer/Counter/PWM





Figure 7-17. Connection of Devices to the I²C Bus



For most designs, the default values in Table 7-2 will provide excellent performance without any calculations. The default values were chosen to use standard resistor values between the minimum and maximum limits. The values in Table 7-2 work for designs with 1.8 V to 5.0V V_{DD}, less than 200-pF bus capacitance (C_B), up to 25 μ A of total input leakage (I_{IL}), up to 0.4 V output voltage level (V_{OL}), and a max V_{IH} of 0.7 * V_{DD}. Standard Mode and Fast Mode can use either GPIO or SIO PSoC pins. Fast Mode Plus requires use of SIO pins to meet the V_{OL} spec at 20 mA. Calculation of custom pull-up resistor values is required; if your design does not meet the default assumptions, you use series resistor value for low power consumption.

Table 7-2. Recommended default Pull-up Resistor Values

	R _P	Units
Standard Mode – 100 kbps	4.7 k, 5%	Ω
Fast Mode – 400 kbps	1.74 k, 1%	Ω
Fast Mode Plus – 1 Mbps	620, 5%	Ω

Calculation of the ideal pull-up resistor value involves finding a value between the limits set by three equations detailed in the NXP I^2C specification. These equations are:

Equation 1:

$$R_{PMIN} = (V_{DD}(max) - V_{OL}(max))/(I_{OL}(min))$$

Equation 2:

$$R_{PMAX} = T_R(max)/0.8473 \times C_R(max)$$

Equation 3:

 $R_{PMAX} = V_{DD}(min) - V_{IH}(min) + V_{NH}(min) / I_{IH}(max)$

Equation parameters:

 V_{DD} = Nominal supply voltage for I²C bus

V_{OL} = Maximum output low voltage of bus devices.

 I_{OI} = Low-level output current from I²C specification

 T_R = Rise Time of bus from I²C specification

C_B = Capacitance of each bus line including pins and PCB traces

V_{IH} = Minimum high-level input voltage of all bus devices

 V_{NH} = Minimum high-level input noise margin from I^2C specification

I_{IH} = Total input leakage current of all devices on the bus

The supply voltage (V_{DD}) limits the minimum pull-up resistor value due to bus devices maximum low output voltage (V_{DL}) specifications. Lower pull-up resistance increases current through the pins and can, therefore, exceed the spec conditions of V_{OL}. Equation 1 is derived using Ohm's law to determine the minimum resistance that will still meet the V_{OL} specification at 3 mA for standard and fast modes, and 20 mA for fast mode plus at the given V_{DD}.

Equation 2 determines the maximum pull-up resistance due to bus capacitance. Total bus capacitance is comprised of all pin, wire, and trace capacitance on the bus. The higher the bus capacitance, the lower the pull-up resistance required to meet the specified bus speeds rise time due to RC delays. Choosing a pull-up resistance higher than allowed can result in failing timing requirements resulting in communication errors. Most designs with five or less I^2C devices and up to 20 centimeters of bus trace length have less than 100 pF of bus capacitance.

A secondary effect that limits the maximum pull-up resistor value is total bus leakage calculated in Equation 3. The primary source of leakage is I/O pins connected to the bus. If leakage is too high, the pull-ups will have difficulty maintaining an acceptable V_{IH} level causing communication errors. Most designs with five or less I²C devices on the bus have less than 10 µA of total leakage current.



8.1 Analog Routing

The CY8C32 family of devices has a flexible analog routing architecture that provides the capability to connect GPIOs and different analog blocks, and also route signals between different analog blocks. One of the strong points of this flexible routing architecture is that it allows dynamic routing of input and output connections to the different analog blocks.

For information on how to make pin selections for optimal analog routing, refer to the application note, AN58304 - PSoC® 3 and PSoC® 5 - Pin Selection for Analog Designs.

- 8.1.1 Features
- Flexible, configurable analog routing architecture
- 16 analog globals (AG) and two analog mux buses (AMUXBUS) to connect GPIOs and the analog blocks
- Each GPIO is connected to one analog global and one analog mux bus

- Eight analog local buses (abus) to route signals between the different analog blocks
- Multiplexers and switches for input and output selection of the analog blocks

8.1.2 Functional Description

Analog globals (AGs) and analog mux buses (AMUXBUS) provide analog connectivity between GPIOs and the various analog blocks. There are 16 AGs in the CY8C32 family. The analog routing architecture is divided into four quadrants as shown in Figure 8-2. Each quadrant has four analog globals (AGL[0..3], AGL[4..7], AGR[0..3], AGR[4..7]). Each GPIO is connected to the corresponding AG through an analog switch. The analog mux bus is a shared routing resource that connects to every GPIO through an analog switch. There are two AMUXBUS routes in CY8C32, one in the left half (AMUXBUSL) and one in the right half (AMUXBUSR), as shown in Figure 8-2.



Table 11-12. SIO AC Specifications (continued)

Parameter	Description	Conditions	Min	Тур	Max	Units
	SIO output operating frequency					
	2.7 V < V _{DDIO} < 5.5 V, Unregu- lated output (GPIO) mode, fast strong drive mode	90/10% V _{DDIO} into 25 pF	-	-	33	MHz
	1.71 V < V _{DDIO} < 2.7 V, Unregu- lated output (GPIO) mode, fast strong drive mode	90/10% V _{DDIO} into 25 pF	_	-	16	MHz
	3.3 V < V _{DDIO} < 5.5 V, Unregu- lated output (GPIO) mode, slow strong drive mode	90/10% V _{DDIO} into 25 pF	-	-	5	MHz
Fsioout	1.71 V < V _{DDIO} < 3.3 V, Unregu- lated output (GPIO) mode, slow strong drive mode	90/10% V _{DDIO} into 25 pF	_	-	4	MHz
	$2.7 V < V_{DDIO} < 5.5 V$, Regulated output mode, fast strong drive mode	Output continuously switching into 25 pF	_	-	20	MHz
	1.71 V < V _{DDIO} < 2.7 V, Regulated output mode, fast strong drive mode	Output continuously switching into 25 pF	-	-	10	MHz
	1.71 V < V _{DDIO} < 5.5 V, Regulated output mode, slow strong drive mode	Output continuously switching into 25 pF	_	-	2.5	MHz
Esioin	SIO input operating frequency					
1 3011	$1.71 \text{ V} \leq \text{V}_{\text{DDIO}} \leq 5.5 \text{ V}$	90/10% V _{DDIO}	_	-	33	MHz

Figure 11-20. SIO Output Rise and Fall Times, Fast Strong Mode, V_{DDIO} = 3.3 V, 25 pF Load



Figure 11-21. SIO Output Rise and Fall Times, Slow Strong Mode, $V_{\mbox{DDIO}}$ = 3.3 V, 25 pF Load





Figure 11-22. USBIO Output High Voltage and Current, GPIO Mode







Table 11-15. USBIO AC Specifications

Parameter	Description	Conditions	Min	Тур	Max	Units
Tdrate	Full-speed data rate average bit rate		12 – 0.25%	12	12 + 0.25%	MHz
Tjr1	Receiver data jitter tolerance to next transition		-8	-	8	ns
Tjr2	Receiver data jitter tolerance to pair transition		-5	_	5	ns
Tdj1	Driver differential jitter to next transition		-3.5	-	3.5	ns
Tdj2	Driver differential jitter to pair transition		-4	-	4	ns
Tfdeop	Source jitter for differential transition to SE0 transition		-2	-	5	ns
Tfeopt	Source SE0 interval of EOP		160	-	175	ns
Tfeopr	Receiver SE0 interval of EOP		82	_	_	ns
Tfst	Width of SE0 interval during differ- ential transition		-	-	14	ns
Fgpio_out	GPIO mode output operating	$3 \text{ V} \leq \text{V}_{\text{DDD}} \leq 5.5 \text{ V}$	-	_	20	MHz
	frequency	V _{DDD} = 1.71 V	-	_	6	MHz
Tr_gpio	Rise time, GPIO mode, 10%/90%	V _{DDD} > 3 V, 25 pF load	_	-	12	ns
	V _{DDD}	V _{DDD} = 1.71 V, 25 pF load	_	-	40	ns
Tf_gpio	Fall time, GPIO mode, 90%/10% V _{DDD}	V _{DDD} > 3 V, 25 pF load	_	_	12	ns
		V _{DDD} = 1.71 V, 25 pF load	_	_	40	ns

Figure 11-24. USBIO Output Rise and Fall Times, GPIO Mode,







Figure 11-34. IDAC Operating Current vs Temperature, Range = 255μ A, Code = 0, Source Mode



Figure 11-33. IDAC Full Scale Error vs Temperature, Range = 255μ A, Sink Mode



Figure 11-35. IDAC Operating Current vs Temperature, Range = 255 μ A, Code = 0, Sink Mode





Figure 11-52. Clock to Output Performance



11.7 Memory

Specifications are valid for –40 °C \leq T_A \leq 85 °C and T_J \leq 100 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

11.7.1 Flash

Table 11-45. Flash DC Specifications

Parameter	Description	Conditions	Min	Тур	Max	Units
	Erase and program voltage	V _{DDD} pin	1.71	-	5.5	V

Table 11-46. Flash AC Specifications

Parameter	Description	Conditions	Min	Тур	Max	Units
T _{WRITE}	Row write time (erase + program)		-	15	20	ms
T _{ERASE}	Row erase time		-	10	13	ms
	Row program time		-	5	7	ms
T _{BULK}	Bulk erase time (16 KB to 64 KB)		-	-	35	ms
	Sector erase time (8 KB to 16 KB)		-	-	15	ms
T _{PROG}	Total device programming time	No overhead ^[55]	-	1.5	2	seconds
	Flash data retention time, retention period measured from last erase cycle	Average ambient temp. $T_A \le 55$ °C, 100 K erase/program cycles	20	-	_	years
		Average ambient temp. $T_A \le 85$ °C, 10 K erase/program cycles	10	_	-	



11.8.3 Interrupt Controller

Table 11-61. Interrupt Controller AC Specifications

Parameter	Description	Conditions	Min	Тур	Max	Units
	Delay from interrupt signal input to ISR code execution from ISR code	Includes worse case completion of longest instruction DIV with 6 cycles	-	-	25	Tcy CPU

11.8.4 JTAG Interface





|--|

Parameter	Description	Conditions	Min	Тур	Max	Units
f_TCK	TCK frequency	$3.3 \text{ V} \leq \text{V}_{DDD} \leq 5 \text{ V}$	-	-	14 ^[66]	MHz
		$1.71 \text{ V} \le \text{V}_{\text{DDD}} < 3.3 \text{ V}$	-	-	7 ^[66]	MHz
T_TDI_setup	TDI setup before TCK high		(T/10)-5	-	-	ns
T_TMS_setup	TMS setup before TCK high		T/4	_	-	
T_TDI_hold	TDI, TMS hold after TCK high	T = 1/f_TCK max	T/4	_	-	
T_TDO_valid	TCK low to TDO valid	T = 1/f_TCK max	-	-	2T/5	
T_TDO_hold	TDO hold after TCK high	T = 1/f_TCK max	T/4	-	_	

Notes

65. Based on device characterization (Not production tested).
 66. f_TCK must also be no more than 1/3 CPU clock frequency.





Figure 13-1. 48-pin (300 mil) SSOP Package Outline

Figure 13-2. 48-pin QFN Package Outline



- 2. REFERENCE JEDEC#: MO-220
- 3. PACKAGE WEIGHT: REFER TO PMDD SPEC.
- 4. ALL DIMENSIONS ARE IN MM [MIN/MAX]
- 5. PACKAGE CODE

PART #	DESCRIPTION
LT48D	LEAD FREE

001-45616 *E









17. Revision History

Description Title: PSoC [®] 3: CY8C32 Family Data Sheet Programmable System-on-Chip (PSoC [®]) Document Number: 001-56955				
Revision	ECN	Submission Date	Orig. of Change	Description of Change
**	2796903	11/04/09	MKEA	New datasheet
*A	2824546	12/09/09	MKEA	Updated I2C section to reflect 1 Mbps. Updated Table 11-6 and 11-7 (Boost AC and DC specs); also added Shottky Diode specs. Changed current for sleep/hibernate mode to include SIO; Added footnote to analog global specs. Updated Figures 1-1, 6-2, 7-14, and 8-1. Updated Table 6-2 and Table 6-3 (Hibernate and Sleep rows) and Power Modes section. Updated GPIO and SIO AC specifications. Updated Gain error in IDAC and VDAC specifications. Updated description of V _{DDA} spec in Table 11-1 and removed GPIO Clamp Current parameter. Updated number of UDBs on page 1. Moved FILO from ILO DC to AC table. Added PCB Layout and PCB Schematic diagrams. Updated Fgpioout spec (Table 11-9). Added duty cycle frequency in PLL AC spec table. Added note for Sleep and Hibernate modes and Active Mode specs in Table 11-2. Linked URL in Section 10.3 to PSoC Creator site. Updated Ja and Jc values in Table 13-1. Updated Single Sample Mode and Fast FIR Mode sections. Updated Input Resistance specification in Del-Sig ADC table. Added Tio_init parameter. Updated PGA and UGB AC Specs. Removed SPC ADC. Updated Boost Converter section. Added section 'SIO as Comparator'; updated Hysteresis spec (differential mode) in Table 11-10. Updated V _{BAT} condition and deleted Vstart parameter in Table 11-6. Added 'Bytes' column for Tables 4-1 to 4-5.
*В	2873322	02/04/10	MKEA	Changed maximum value of PPOR_TR to '1'. Updated V _{BIAS} specification. Updated PCB Schematic. Updated Figure 8-1 and Figure 6-3. Updated Interrupt Vector table, Updated Sales links. Updated JTAG and SWD specifications. Removed Jp-p and Jperiod from ECO AC Spec table. Added note on sleep timer in Table 11-2. Updated ILO AC and DC specifications. Added Resolution parameter in VDAC and IDAC tables. Updated I _{OUT} typical and maximum values. Changed Temperature Sensor range to -40 °C to +85 °C. Removed Latchup specification from Table 11-1. Updated DAC details