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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	50MHz
Connectivity	EBI/EMI, I²C, LINbus, SPI, UART/USART, USB
Peripherals	CapSense, DMA, LCD, POR, PWM, WDT
Number of I/O	25
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	1K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 16x12b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-BSSOP (0.295", 7.50mm Width)
Supplier Device Package	48-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c3245pvi-150

1. Architectural Overview

Introducing the CY8C32 family of ultra low-power, flash Programmable System-on-Chip (PSoC®) devices, part of a scalable 8-bit PSoC 3 and 32-bit PSoC 5 platform. The CY8C32 family provides configurable blocks of analog, digital, and interconnect circuitry around a CPU subsystem. The combination of a CPU with a flexible analog subsystem, digital subsystem, routing, and I/O enables a high level of integration in a wide variety of consumer, industrial, and medical applications.

Figure 1-1. Simplified Block Diagram

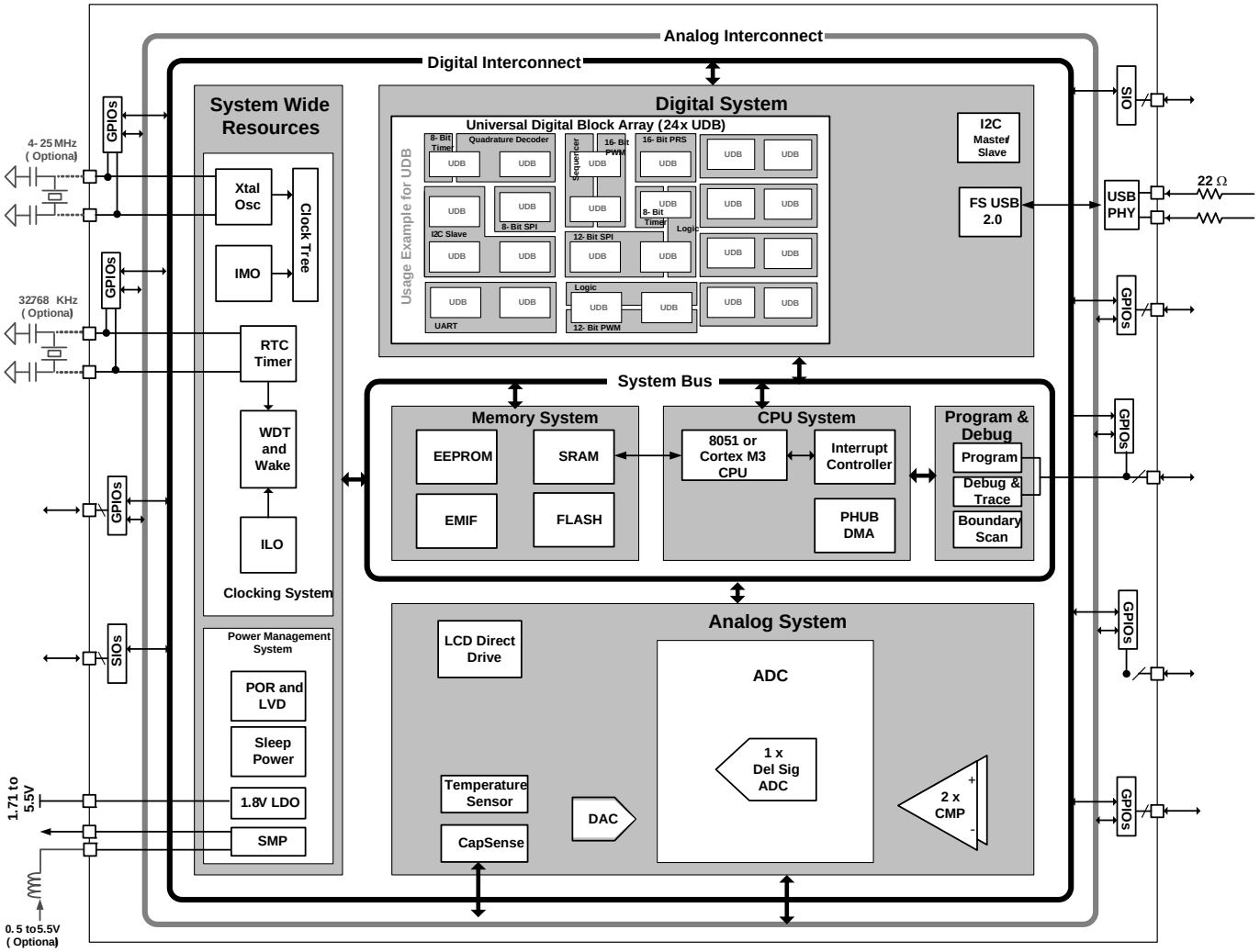
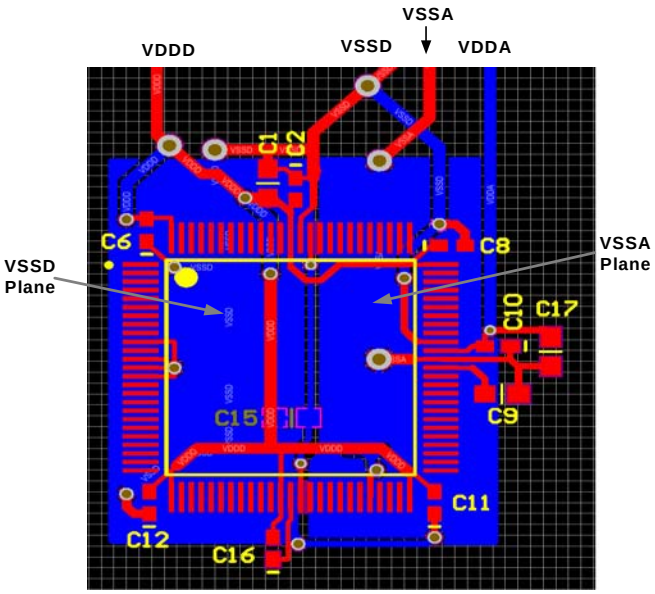


Figure 1-1 illustrates the major components of the CY8C32 family. They are:

- 8051 CPU subsystem
- Nonvolatile subsystem
- Programming, debug, and test subsystem
- Inputs and outputs
- Clocking
- Power
- Digital subsystem
- Analog subsystem

PSoC's digital subsystem provides half of its unique configurability. It connects a digital signal from any peripheral to any pin through the Digital System Interconnect (DSI). It also provides functional flexibility through an array of small, fast, low-power UDBs. PSoC Creator provides a library of prebuilt and tested standard digital peripherals (UART, SPI, LIN, PRS, CRC, timer, counter, PWM, AND, OR, and so on) that are mapped to the UDB array. You can also easily create a digital circuit using boolean primitives by means of graphical design entry. Each UDB contains programmable array logic (PAL)/programmable logic device (PLD) functionality, together with a small state machine engine to support a wide variety of peripherals.

Figure 2-8. Example PCB Layout for 100-pin TQFP Part for Optimal Analog Performance



3. Pin Descriptions

IDAC0

Low resistance output pin for high current DAC (IDAC).

Extref0, Extref1

External reference input to the analog system.

GPIO

General purpose I/O pin provides interfaces to the CPU, digital peripherals, analog peripherals, interrupts, LCD segment drive, and CapSense.

I2C0: SCL, I2C1: SCL

I^2C SCL line providing wake from sleep on an address match. Any I/O pin can be used for I^2C SCL if wake from sleep is not required.

I2C0: SDA, I2C1: SDA

I^2C SDA line providing wake from sleep on an address match. Any I/O pin can be used for I^2C SDA if wake from sleep is not required.

Ind

Inductor connection to boost pump.

kHz XTAL: Xo, kHz XTAL: Xi

32.768-kHz crystal oscillator pin.

MHz XTAL: Xo, MHz XTAL: Xi

4- to 25- MHz crystal oscillator pin.

nTRST

Optional JTAG test reset programming and debug port connection to reset the JTAG connection.

SIO

Special I/O provides interfaces to the CPU, digital peripherals and interrupts with a programmable high threshold voltage, analog comparator, high sink current, and high impedance state when the device is unpowered.

SWDCK

Serial wire debug clock programming and debug port connection.

SWDIO

Serial wire debug input and output programming and debug port connection.

SWV.

Single wire viewer debug output.

TCK

JTAG test clock programming and debug port connection.

TDI

JTAG test data in programming and debug port connection.

TDO

JTAG test data out programming and debug port connection.

TMS

JTAG test mode select programming and debug port connection.

4.3.1.3 Data Transfer Instructions

The data transfer instructions are of three types: the core RAM, xdata RAM, and the lookup tables. The core RAM transfer includes transfer between any two core RAM locations or SFRs. These instructions can use direct, indirect, register, and immediate addressing. The xdata RAM transfer includes only the transfer between the accumulator and the xdata RAM location. It can use only indirect addressing. The lookup tables involve nothing but the read of program memory using the Indexed addressing mode. Table 4-3 lists the various data transfer instructions available.

4.3.1.4 Boolean Instructions

The 8051 core has a separate bit-addressable memory location. It has 128 bits of bit addressable RAM and a set of SFRs that are bit addressable. The instruction set includes the whole menu of bit operations such as move, set, clear, toggle, OR, and AND instructions and the conditional jump instructions. Table 4-4 on page 17Table 4-4 lists the available Boolean instructions.

Table 4-3. Data Transfer Instructions

Mnemonic	Description	Bytes	Cycles
MOV A,Rn	Move register to accumulator	1	1
MOV A,Direct	Move direct byte to accumulator	2	2
MOV A,@Ri	Move indirect RAM to accumulator	1	2
MOV A,#data	Move immediate data to accumulator	2	2
MOV Rn,A	Move accumulator to register	1	1
MOV Rn,Direct	Move direct byte to register	2	3
MOV Rn, #data	Move immediate data to register	2	2
MOV Direct, A	Move accumulator to direct byte	2	2
MOV Direct, Rn	Move register to direct byte	2	2
MOV Direct, Direct	Move direct byte to direct byte	3	3
MOV Direct, @Ri	Move indirect RAM to direct byte	2	3
MOV Direct, #data	Move immediate data to direct byte	3	3
MOV @Ri, A	Move accumulator to indirect RAM	1	2
MOV @Ri, Direct	Move direct byte to indirect RAM	2	3
MOV @Ri, #data	Move immediate data to indirect RAM	2	2
MOV DPTR, #data16	Load data pointer with 16-bit constant	3	3
MOVC A, @A+DPTR	Move code byte relative to DPTR to accumulator	1	5
MOVC A, @A + PC	Move code byte relative to PC to accumulator	1	4
MOVX A,@Ri	Move external RAM (8-bit) to accumulator	1	4
MOVX A, @DPTR	Move external RAM (16-bit) to accumulator	1	3
MOVX @Ri, A	Move accumulator to external RAM (8-bit)	1	5
MOVX @DPTR, A	Move accumulator to external RAM (16-bit)	1	4
PUSH Direct	Push direct byte onto stack	2	3
POP Direct	Pop direct byte from stack	2	2
XCH A, Rn	Exchange register with accumulator	1	2
XCH A, Direct	Exchange direct byte with accumulator	2	3
XCH A, @Ri	Exchange indirect RAM with accumulator	1	3
XCHD A, @Ri	Exchange low order indirect digit RAM with accumulator	1	3

Table 4-4. Boolean Instructions

Mnemonic	Description	Bytes	Cycles
CLR C	Clear carry	1	1
CLR bit	Clear direct bit	2	3
SETB C	Set carry	1	1
SETB bit	Set direct bit	2	3
CPL C	Complement carry	1	1
CPL bit	Complement direct bit	2	3
ANL C, bit	AND direct bit to carry	2	2
ANL C, /bit	AND complement of direct bit to carry	2	2
ORL C, bit	OR direct bit to carry	2	2
ORL C, /bit	OR complement of direct bit to carry	2	2
MOV C, bit	Move direct bit to carry	2	2
MOV bit, C	Move carry to direct bit	2	3
JC rel	Jump if carry is set	2	3
JNC rel	Jump if no carry is set	2	3
JB bit, rel	Jump if direct bit is set	3	5
JNB bit, rel	Jump if direct bit is not set	3	5
JBC bit, rel	Jump if direct bit is set and clear bit	3	5

4.3.1.5 Program Branching Instructions

The 8051 supports a set of conditional and unconditional jump instructions that help to modify the program execution flow. Table 4-5 shows the list of jump instructions.

Table 4-5. Jump Instructions

Mnemonic	Description	Bytes	Cycles
ACALL addr11	Absolute subroutine call	2	4
LCALL addr16	Long subroutine call	3	4
RET	Return from subroutine	1	4
RETI	Return from interrupt	1	4
AJMP addr11	Absolute jump	2	3
LJMP addr16	Long jump	3	4
SJMP rel	Short jump (relative address)	2	3
JMP @A + DPTR	Jump indirect relative to DPTR	1	5
JZ rel	Jump if accumulator is zero	2	4
JNZ rel	Jump if accumulator is nonzero	2	4
CJNE A,Direct, rel	Compare direct byte to accumulator and jump if not equal	3	5
CJNE A, #data, rel	Compare immediate data to accumulator and jump if not equal	3	4
CJNE Rn, #data, rel	Compare immediate data to register and jump if not equal	3	4
CJNE @Ri, #data, rel	Compare immediate data to indirect RAM and jump if not equal	3	5
DJNZ Rn,rel	Decrement register and jump if not zero	2	4
DJNZ Direct, rel	Decrement direct byte and jump if not zero	3	5
NOP	No operation	1	1

4.4 DMA and PHUB

The PHUB and the DMA controller are responsible for data transfer between the CPU and peripherals, and also data transfers between peripherals. The PHUB and DMA also control device configuration during boot. The PHUB consists of:

- A central hub that includes the DMA controller, arbiter, and router
- Multiple spokes that radiate outward from the hub to most peripherals

There are two PHUB masters: the CPU and the DMA controller. Both masters may initiate transactions on the bus. The DMA channels can handle peripheral communication without CPU intervention. The arbiter in the central hub determines which DMA channel is the highest priority if there are multiple requests.

4.4.1 PHUB Features

- CPU and DMA controller are both bus masters to the PHUB
- Eight Multi-layer AHB Bus parallel access paths (spokes) for peripheral access
- Simultaneous CPU and DMA access to peripherals located on different spokes
- Simultaneous DMA source and destination burst transactions on different spokes
- Supports 8, 16, 24, and 32-bit addressing and data

Table 4-6. PHUB Spokes and Peripherals

PHUB Spokes	Peripherals
0	SRAM
1	IOs, PICU, EMIF
2	PHUB local configuration, Power manager, Clocks, IC, SWV, EEPROM, Flash programming interface
3	Analog interface and trim, Decimator
4	USB, USB, I^2C, Timers, Counters, and PWMs
5	Reserved
6	UDBs group 1
7	UDBs group 2

7. Digital Subsystem

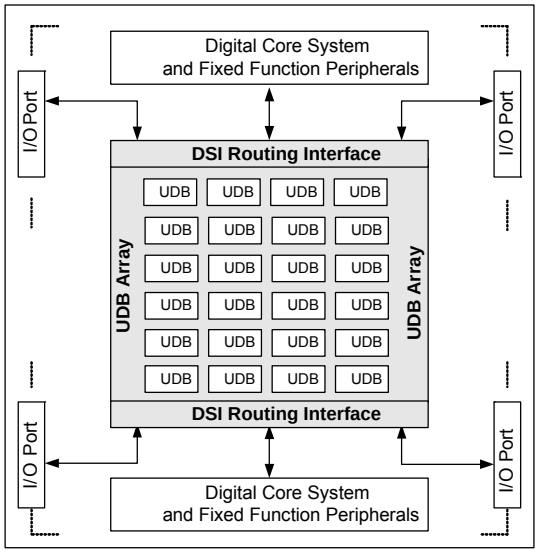
The digital programmable system creates application specific combinations of both standard and advanced digital peripherals and custom logic functions. These peripherals and logic are then interconnected to each other and to any pin on the device, providing a high level of design flexibility and IP security.

The features of the digital programmable system are outlined here to provide an overview of capabilities and architecture. You do not need to interact directly with the programmable digital system at the hardware and register level. PSoC Creator provides a high level schematic capture graphical interface to automatically place and route resources similar to PLDs.

The main components of the digital programmable system are:

- Universal Digital Blocks (UDB) – These form the core functionality of the digital programmable system. UDBs are a collection of uncommitted logic (PLD) and structural logic (Datapath) optimized to create all common embedded peripherals and customized functionality that are application or design specific.
- Universal Digital Block Array – UDB blocks are arrayed within a matrix of programmable interconnect. The UDB array structure is homogeneous and allows for flexible mapping of digital functions onto the array. The array supports extensive and flexible routing interconnects between UDBs and the Digital System Interconnect.
- Digital System Interconnect (DSI) – Digital signals from Universal Digital Blocks (UDBs), fixed function peripherals, I/O pins, interrupts, DMA, and other system core signals are attached to the Digital System Interconnect to implement full featured device connectivity. The DSI allows any digital function to any pin or other feature routability when used with the Universal Digital Block Array.

Figure 7-1. CY8C32 Digital Programmable Architecture



7.1 Example Peripherals

The flexibility of the CY8C32 family's Universal Digital Blocks (UDBs) and Analog Blocks allow the user to create a wide range of components (peripherals). The most common peripherals were built and characterized by Cypress and are shown in the PSoC Creator component catalog, however, users may also create their own custom components using PSoC Creator. Using PSoC Creator, users may also create their own components for reuse within their organization, for example sensor interfaces, proprietary algorithms, and display interfaces.

The number of components available through PSoC Creator is too numerous to list in the datasheet, and the list is always growing. An example of a component available for use in CY8C32 family, but, not explicitly called out in this datasheet is the UART component.

7.1.1 Example Digital Components

The following is a sample of the digital components available in PSoC Creator for the CY8C32 family. The exact amount of hardware resources (UDBs, routing, RAM, flash) used by a component varies with the features selected in PSoC Creator for the component.

- Communications
  - I^2C
  - UART
  - SPI
- Functions
  - EMIF
  - PWMs
  - Timers
  - Counters
- Logic
  - NOT
  - OR
  - XOR
  - AND

7.1.2 Example Analog Components

The following is a sample of the analog components available in PSoC Creator for the CY8C32 family. The exact amount of hardware resources (routing, RAM, flash) used by a component varies with the features selected in PSoC Creator for the component.

- ADC
  - Delta-sigma
- DACs
  - Current
  - Voltage
  - PWM
- Comparators

7.1.3 Example System Function Components

The following is a sample of the system function components available in PSoC Creator for the CY8C32 family. The exact amount of hardware resources (UDBs, routing, RAM, flash) used by a component varies with the features selected in PSoC Creator for the component.

- CapSense
- LCD Drive
- LCD Control

11. Electrical Specifications

Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted. The unique flexibility of the PSoC UDBs and analog blocks enable many functions to be implemented in PSoC Creator components, see the component datasheets for full AC/DC specifications of individual functions. See the "Example Peripherals" section on page 45 for further explanation of PSoC Creator components.

11.1 Absolute Maximum Ratings

Table 11-1. Absolute Maximum Ratings DC Specifications[15]

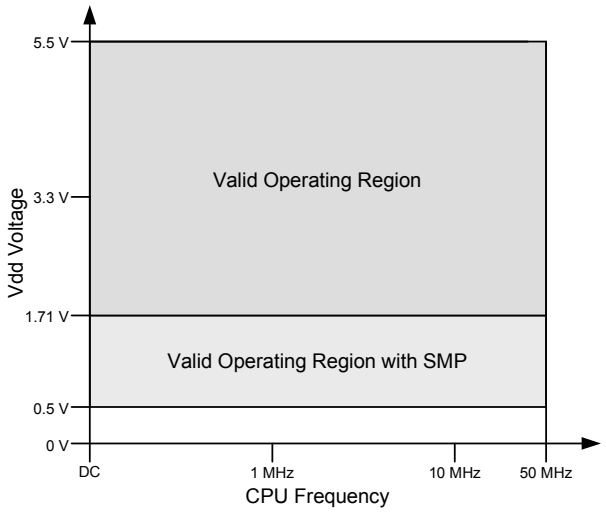
Parameter	Description	Conditions	Min	Typ	Max	Units
V_{DDA}	Analog supply voltage relative to V_{SSA}		–0.5	–	6	V
V_{DDD}	Digital supply voltage relative to V_{SSD}		–0.5	–	6	V
V_{DDIO}	I/O supply voltage relative to V_{SSD}		–0.5	–	6	V
V_{CCA}	Direct analog core voltage input		–0.5	–	1.95	V
V_{CCD}	Direct digital core voltage input		–0.5	–	1.95	V
V_{SSA}	Analog ground voltage		V_{SSD} –0.5	–	V_{SSD} + 0.5	V
V_{GPIO}[16]	DC input voltage on GPIO	Includes signals sourced by V_{DDA} and routed internal to the pin	V_{SSD} –0.5	–	V_{DDIO} + 0.5	V
V_{SIO}	DC input voltage on SIO	Output disabled	V_{SSD} –0.5	–	7	V
		Output enabled	V_{SSD} –0.5	–	6	V
V_{IND}	Voltage at boost converter input		0.5	–	5.5	V
V_{BAT}	Boost converter supply		V_{SSD} –0.5	–	5.5	V
I_{VDDIO}	Current per V_{DDIO} supply pin		–	–	100	mA
I_{GPIO}	GPIO current		–30	–	41	mA
I_{SIO}	SIO current		–49	–	28	mA
I_{USBIO}	USBIO current		–56	–	59	mA
VEXTREF	ADC external reference inputs	Pins P0[3], P3[2]	–	–	2	V
LU	Latch up current[17]		–140	–	140	mA
ESD_{HBM}	Electrostatic discharge voltage, Human body model	V_{SSA} tied to V_{SSD}	2200	–	–	V
		V_{SSA} not tied to V_{SSD}	750	–	–	V
ESD_{CDM}	Electrostatic discharge voltage, Charge device model		500	–	–	V

Notes
15. Usage above the absolute maximum conditions listed in Table 11-1 may cause permanent damage to the device. Exposure to Absolute Maximum conditions for extended periods of time may affect device reliability. The Maximum Storage Temperature is 150 °C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below Absolute Maximum conditions but above normal operating conditions, the device may not operate to specification.
16. The V_{DDIO} supply voltage must be greater than the maximum voltage on the associated GPIO pins. Maximum voltage on GPIO pin ≤ V_{DDIO} ≤ V_{DDA}.
17. Meets or exceeds JEDEC Spec EIA/JESD78 IC Latch-up Test.

Table 11-3. AC Specifications[30]

Parameter	Description	Conditions	Min	Typ	Max	Units
F_{CPU}	CPU frequency	1.71 V ≤ V_{DDD} ≤ 5.5 V	DC	–	50.01	MHz
F_{BUSCLK}	Bus frequency	1.71 V ≤ V_{DDD} ≤ 5.5 V	DC	–	50.01	MHz
Svdd	V_{DD} ramp rate		–	–	0.066	V/µs
T_{IO_INIT}	Time from V_{DDD}/V_{DDA}/V_{CCD}/V_{CCA} ≥ IPOR to I/O ports set to their reset states		–	–	10	µs
$T_{STARTUP}$	Time from V_{DDD}/V_{DDA}/V_{CCD}/V_{CCA} ≥ PRES to CPU executing code at reset vector	V_{CCA}/V_{CCD} = regulated from V_{DDA}/V_{DDD}, no PLL used, IMO boot mode (12 MHz typ.)	–	–	74	µs
T_{SLEEP}	Wakeup from sleep mode – Application of non-LVD interrupt to beginning of execution of next CPU instruction		–	–	15	µs
$T_{HIBERNATE}$	Wakeup from hibernate mode – Application of external interrupt to beginning of execution of next CPU instruction		–	–	100	µs

Figure 11-4. F_{CPU} vs. V_{DD}



Note
30. Based on device characterization (Not production tested).

11.3 Power Regulators

Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

11.3.1 Digital Core Regulator

Table 11-4. Digital Core Regulator DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{DDD}	Input voltage		1.8	–	5.5	V
V_{CCD}	Output voltage		–	1.80	–	V
	Regulator output capacitor	±10%, X5R ceramic or better. The two V_{CCD} pins must be shorted together, with as short a trace as possible, see Power System on page 31	0.9	1	1.1	µF

Figure 11-5. Regulators V_{CC} vs V_{DD}

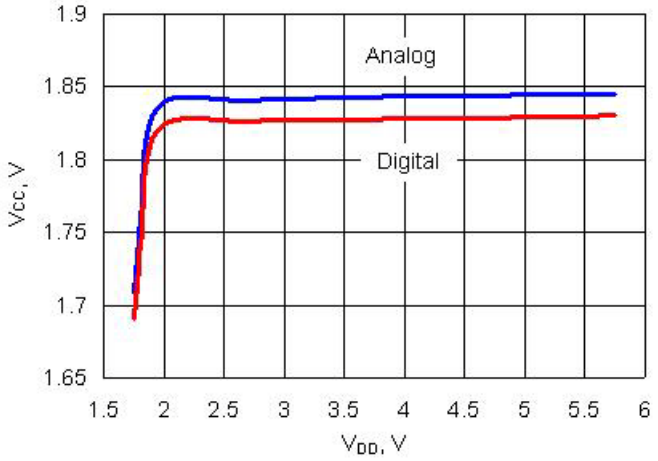
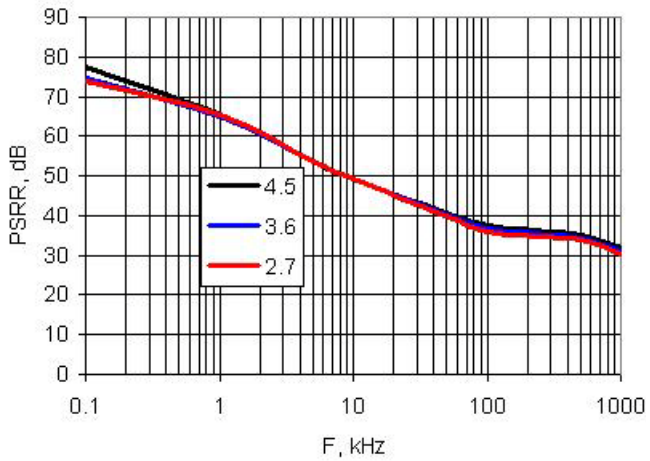


Figure 11-6. Digital Regulator PSRR vs Frequency and V_{DD}

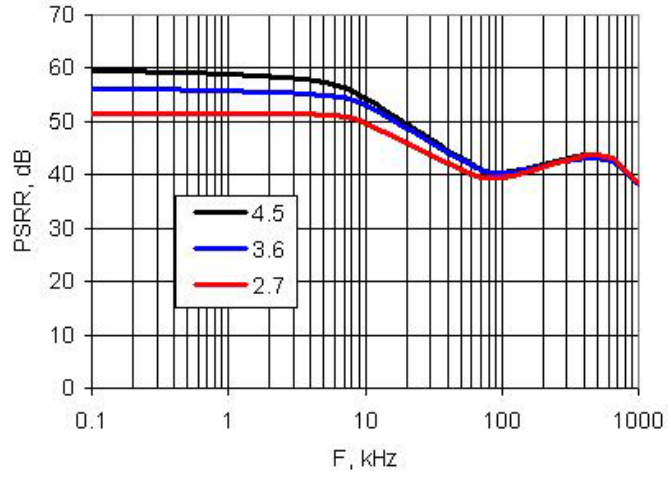


11.3.2 Analog Core Regulator

Table 11-5. Analog Core Regulator DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{DDA}	Input voltage		1.8	–	5.5	V
V_{CCA}	Output voltage		–	1.80	–	V
	Regulator output capacitor	±10%, X5R ceramic or better	0.9	1	1.1	µF

Figure 11-7. Analog Regulator PSRR vs Frequency and V_{DD}



11.3.3 Inductive Boost Regulator

Unless otherwise specified, operating conditions are: V_{BAT} = 0.5 V–3.6 V, V_{OUT} = 1.8 V–5.0 V, I_{OUT} = 0 mA–50 mA, L_{BOOST} = 4.7 µH–22 µH, C_{BOOST} = 22 µF || 3 × 1.0 µF || 3 × 0.1 µF, C_{BAT} = 22 µF, I_F = 1.0 A. Unless otherwise specified, all charts and graphs show typical values.

Table 11-6. Inductive Boost Regulator DC Specifications

Parameter	Description	Conditions		Min	Typ	Max	Units
V_{OUT}	Boost output voltage[31]	vsel = 1.8 V in register BOOST_CR0		1.71	1.8	1.89	V
		vsel = 1.9 V in register BOOST_CR0		1.81	1.90	2.00	V
		vsel = 2.0 V in register BOOST_CR0		1.90	2.00	2.10	V
		vsel = 2.4 V in register BOOST_CR0		2.16	2.40	2.64	V
		vsel = 2.7 V in register BOOST_CR0		2.43	2.70	2.97	V
		vsel = 3.0 V in register BOOST_CR0		2.70	3.00	3.30	V
		vsel = 3.3 V in register BOOST_CR0		2.97	3.30	3.63	V
		vsel = 3.6 V in register BOOST_CR0		3.24	3.60	3.96	V
		vsel = 5.0 V in register BOOST_CR0		4.50	5.00	5.50	V
V_{BAT}	Input voltage to boost[32]	I_{OUT} = 0 mA–5 mA	vsel = 1.8 V–2.0 V, T_A = 0 °C–70 °C	0.5	–	0.8	V
		I_{OUT} = 0 mA–15 mA	vsel = 1.8 V–5.0 V[33], T_A = –10 °C–85 °C	1.6	–	3.6	V
		I_{OUT} = 0 mA–25 mA	vsel = 1.8 V–2.7 V, T_A = –10 °C–85 °C	0.8	–	1.6	V
		I_{OUT} = 0 mA–50 mA	vsel = 1.8 V–3.3 V[33], T_A = –40 °C–85 °C	1.8	–	2.5	V
			vsel = 1.8 V–3.3 V[33], T_A = –10 °C–85 °C	1.3	–	2.5	V
			vsel = 2.5 V–5.0 V[33], T_A = –10 °C–85 °C	2.5	–	3.6	V
I_{OUT}	Output current	T_A = 0 °C–70 °C	V_{BAT} = 0.5 V–0.8 V	0	–	5	mA
		T_A = –10 °C–85 °C	V_{BAT} = 1.6 V–3.6 V	0	–	15	mA
			V_{BAT} = 0.8 V–1.6 V	0	–	25	mA
			V_{BAT} = 1.3 V–2.5 V	0	–	50	mA
			V_{BAT} = 2.5 V–3.6 V	0	–	50	mA
		T_A = –40 °C–85 °C	V_{BAT} = 1.8 V–2.5 V	0	–	50	mA
I_{LPK}	Inductor peak current			–	–	700	mA
I_Q	Quiescent current	Boost active mode		–	250	–	µA
		Boost sleep mode, I_{OUT} < 1 µA		–	25	–	µA
Reg_{LOAD}	Load regulation			–	–	10	%
Reg_{LINE}	Line regulation			–	–	10	%

Notes
31. Listed vsel options are characterized. Additional vsel options are valid and guaranteed by design.
32. The boost will start at all valid V_{BAT} conditions including down to V_{BAT} = 0.5 V.
33. If V_{BAT} is greater than or equal to V_{OUT} boost setting, then V_{OUT} will be less than V_{BAT} due to resistive losses in the boost circuit.

Figure 11-11. Efficiency vs V_{BAT}, L_{BOOST} = 4.7 µH [35]

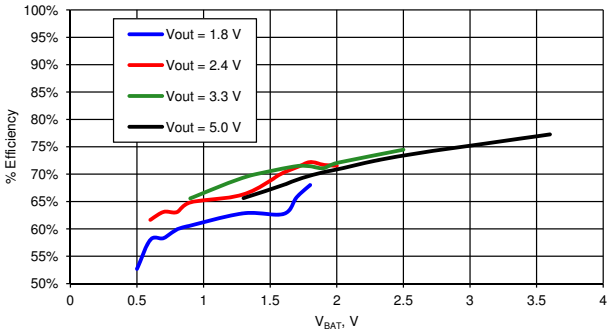


Figure 11-12. Efficiency vs V_{BAT}, L_{BOOST} = 10 µH [35]

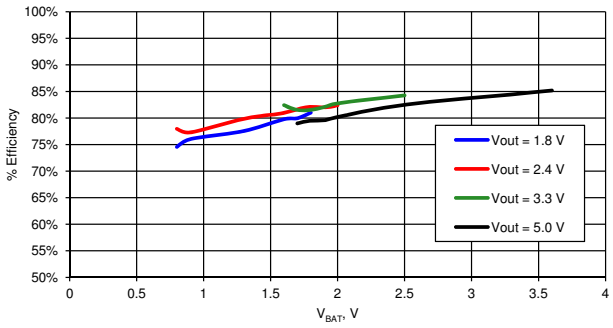


Figure 11-13. Efficiency vs V_{BAT}, L_{BOOST} = 22 µH [35]

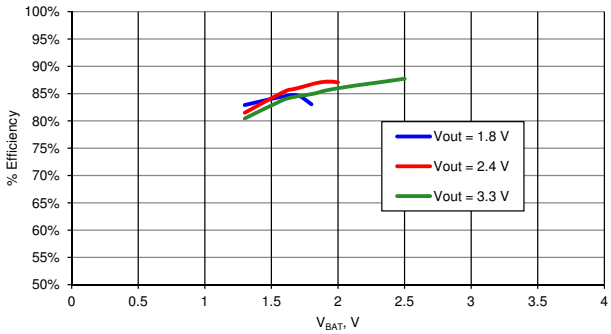
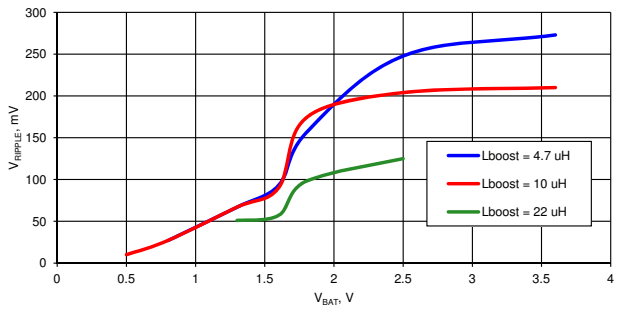


Figure 11-14. V_{RIPPLE} vs V_{BAT} [35]



Note
35. Typical example. Actual values may vary depending on external component selection, PCB layout, and other design parameters.

Figure 11-15. GPIO Output High Voltage and Current

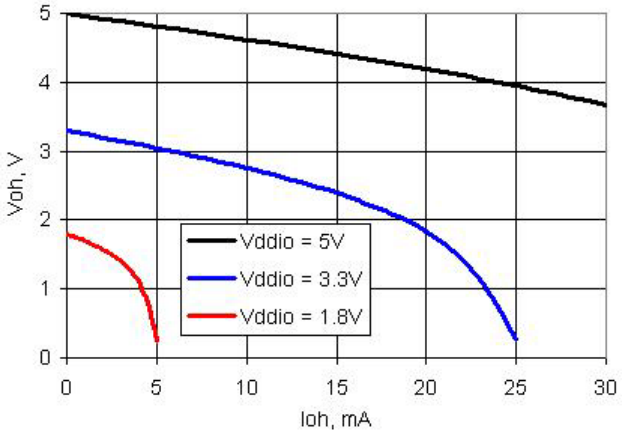


Figure 11-16. GPIO Output Low Voltage and Current

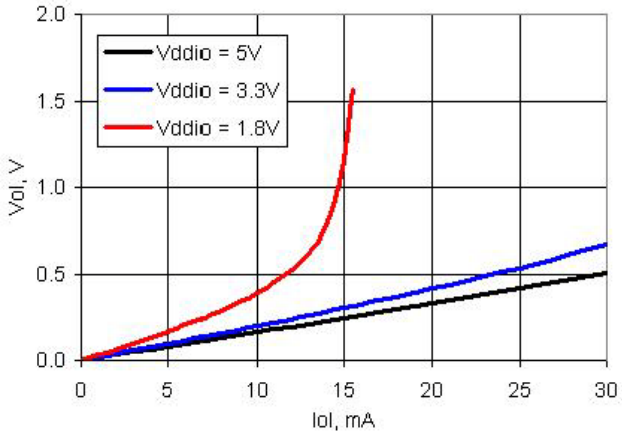


Table 11-10. GPIO AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
TriseF	Rise time in Fast Strong Mode[38]	3.3 V V_{DDIO} Cload = 25 pF	–	–	6	ns
TfallF	Fall time in Fast Strong Mode[38]	3.3 V V_{DDIO} Cload = 25 pF	–	–	6	ns
TriseS	Rise time in Slow Strong Mode[38]	3.3 V V_{DDIO} Cload = 25 pF	–	–	60	ns
TfallS	Fall time in Slow Strong Mode[38]	3.3 V V_{DDIO} Cload = 25 pF	–	–	60	ns
Fgpioout	GPIO output operating frequency					
	2.7 V ≤ V_{DDIO} ≤ 5.5 V, fast strong drive mode	90/10% V_{DDIO} into 25 pF	–	–	33	MHz
	1.71 V ≤ V_{DDIO} < 2.7 V, fast strong drive mode	90/10% V_{DDIO} into 25 pF	–	–	20	MHz
	3.3 V ≤ V_{DDIO} ≤ 5.5 V, slow strong drive mode	90/10% V_{DDIO} into 25 pF	–	–	7	MHz
	1.71 V ≤ V_{DDIO} < 3.3 V, slow strong drive mode	90/10% V_{DDIO} into 25 pF	–	–	3.5	MHz
Fgpioin	GPIO input operating frequency					
	1.71 V ≤ V_{DDIO} ≤ 5.5 V	90/10% V_{DDIO}	–	–	33	MHz

Note
38. Based on device characterization (Not production tested).

Figure 11-22. USBIO Output High Voltage and Current, GPIO Mode

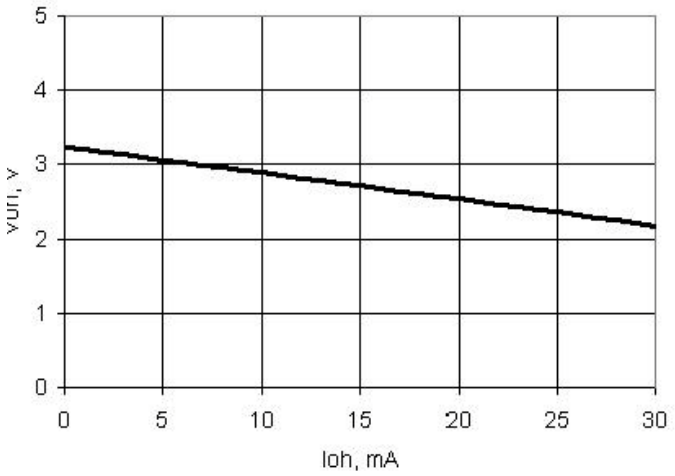


Figure 11-23. USBIO Output Low Voltage and Current, GPIO Mode

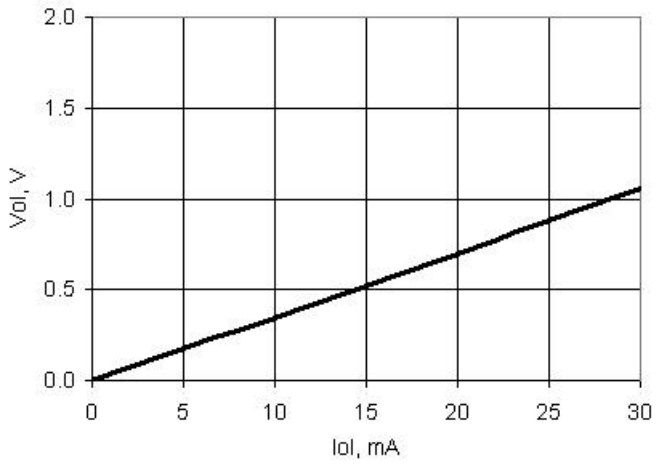


Table 11-15. USBIO AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Tdrate	Full-speed data rate average bit rate		12 – 0.25%	12	12 + 0.25%	MHz
Tjr1	Receiver data jitter tolerance to next transition		–8	–	8	ns
Tjr2	Receiver data jitter tolerance to pair transition		–5	–	5	ns
Tdj1	Driver differential jitter to next transition		–3.5	–	3.5	ns
Tdj2	Driver differential jitter to pair transition		–4	–	4	ns
Tfdeop	Source jitter for differential transition to SE0 transition		–2	–	5	ns
Tfeopt	Source SE0 interval of EOP		160	–	175	ns
Tfeopr	Receiver SE0 interval of EOP		82	–	–	ns
Tfst	Width of SE0 interval during differential transition		–	–	14	ns
Fgpio_out	GPIO mode output operating frequency	3 V ≤ V_{DDD} ≤ 5.5 V	–	–	20	MHz
		V_{DDD} = 1.71 V	–	–	6	MHz
Tr_gpio	Rise time, GPIO mode, 10%/90% V_{DDD}	V_{DDD} > 3 V, 25 pF load	–	–	12	ns
		V_{DDD} = 1.71 V, 25 pF load	–	–	40	ns
Tf_gpio	Fall time, GPIO mode, 90%/10% V_{DDD}	V_{DDD} > 3 V, 25 pF load	–	–	12	ns
		V_{DDD} = 1.71 V, 25 pF load	–	–	40	ns

Figure 11-24. USBIO Output Rise and Fall Times, GPIO Mode,

Table 11-27. IDAC AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
F_{DAC}	Update rate		–	–	8	Msps
T_{SETTLE}	Settling time to 0.5 LSB	Range = 31.875 µA or 255 µA, full scale transition, High speed mode, 600 Ω 15-pF load	–	–	125	ns
	Current noise	Range = 255 µA, source mode, High speed mode, V_{DDA} = 5 V, 10 kHz	–	340	–	pA/sqrtHz

Figure 11-36. IDAC Step Response, Codes 0x40 - 0xC0, 255 µA Mode, Source Mode, High speed mode, V_{DDA} = 5 V

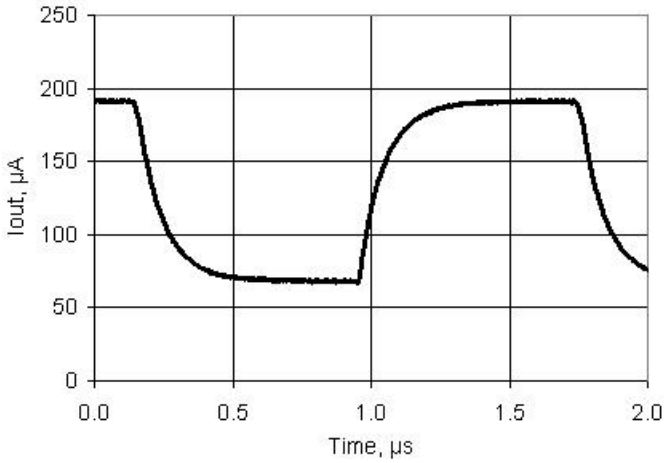


Figure 11-37. IDAC Glitch Response, Codes 0x7F - 0x80, 255 µA Mode, Source Mode, High speed mode, V_{DDA} = 5 V

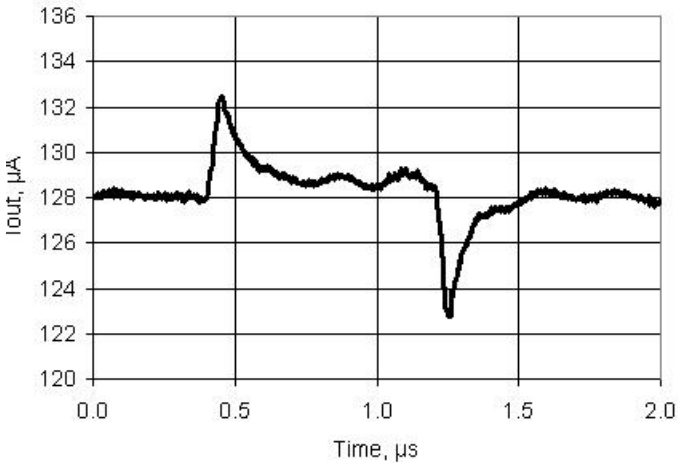


Figure 11-38. IDAC PSRR vs Frequency

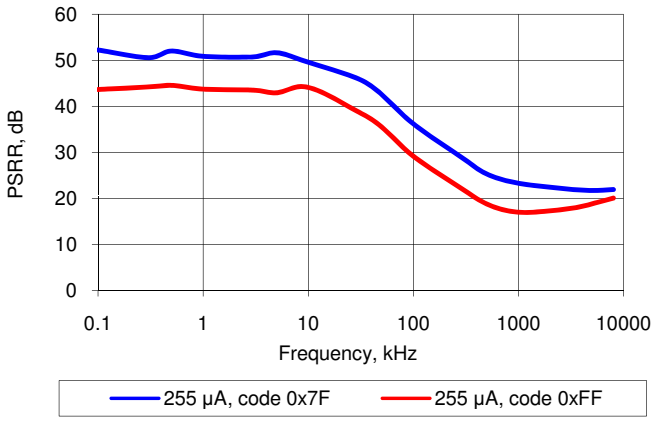
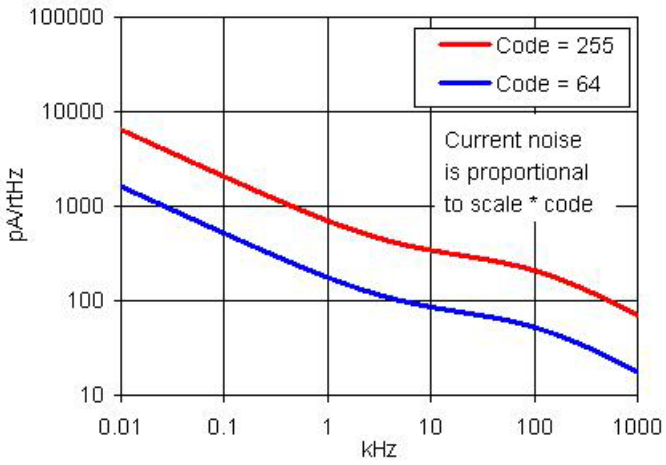


Figure 11-39. IDAC Current Noise, 255 µA Mode, Source Mode, High speed mode, V_{DDA} = 5 V



12. Ordering Information

In addition to the features listed in Table 12-1, every CY8C32 device includes: a precision on-chip voltage reference, precision oscillators, flash, ECC, DMA, a fixed function I²C, 4 KB trace RAM, JTAG/SWD programming and debug, external memory interface, and more. In addition to these features, the flexible UDBs and analog subsection support a wide range of peripherals. To assist you in selecting the ideal part, PSoC Creator makes a part recommendation after you choose the components required by your application. All CY8C32 derivatives incorporate device and flash security in user-selectable security levels; see the TRM for details.

Table 12-1. CY8C32 Family with Single Cycle 8051

Part Number	MCU Core				Analog								Digital				I/O[76]				Package	JTAG ID[77]
	CPU Speed (MHz)	Flash (KB)	SRAM (KB)	EEPROM (KB)	LCD Segment Drive	ADC	DAC	Comparator	SC/CT Analog Blocks	Opamps	DFB	CapSense	UDBs[75]	16-bit Timer/PWM	FS USB	CAN 2.0b	Total I/O	GPIO	SIO	USBIO		
16 KB Flash																						
CY8C3244AXI-153	50	16	2	0.5	✔	12-bit Del-Sig	1	2	0	0	–	✔	16	4	–	–	70	62	8	0	100-pin TQFP	0×1E099069
CY8C3244LTI-130	50	16	2	0.5	✔	12-bit Del-Sig	1	2	0	0	–	✔	16	4	–	–	46	38	8	0	68-pin QFN	0×1E082069
CY8C3244LTI-123	50	16	2	0.5	✔	12-bit Del-Sig	1	2	0	0	–	✔	16	4	–	–	29	25	4	0	48-pin QFN	0×1E07B069
CY8C3244PVI-133	50	16	2	0.5	✔	12-bit Del-Sig	1	2	0	0	–	✔	16	4	–	–	29	25	4	0	48-pin SSOP	0×1E085069
32 KB Flash																						
CY8C3245AXI-158	50	32	4	1	✔	12-bit Del-Sig	1	2	0	0	–	✔	20	4	–	–	70	62	8	0	100-pin TQFP	0×1E09E069
CY8C3245LTI-163	50	32	4	1	✔	12-bit Del-Sig	1	2	0	0	–	✔	20	4	–	–	46	38	8	0	68-pin QFN	0×1E0A3069
CY8C3245LTI-139	50	32	4	1	✔	12-bit Del-Sig	1	2	0	0	–	✔	20	4	–	–	29	25	4	0	48-pin QFN	0×1E08B069
CY8C3245PVI-134	50	32	4	1	✔	12-bit Del-Sig	1	2	0	0	–	✔	20	4	–	–	29	25	4	0	48-pin SSOP	0×1E086069
CY8C3245AXI-166	50	32	4	1	✔	12-bit Del-Sig	1	2	0	0	–	✔	20	4	✔	–	72	62	8	2	100-pin TQFP	0×1E0A6069
CY8C3245LTI-144	50	32	4	1	✔	12-bit Del-Sig	1	2	0	0	–	✔	20	4	✔	–	31	25	4	2	48-pin QFN	0×1E090069
CY8C3245PVI-150	50	32	4	1	✔	12-bit Del-Sig	1	2	0	0	–	✔	20	4	✔	–	31	25	4	2	48-pin SSOP	0×1E096069
CY8C3245FNI-212	50	32	4	1	✔	12-bit Del-Sig	1	2	0	0	–	✔	20	4	–	–	46	38	8	0	72-pin WLCSP	0x1E0D4069
64 KB Flash																						
CY8C3246LTI-149	50	64	8	2	✔	12-bit Del-Sig	1	2	0	0	–	✔	24	4	–	–	46	38	8	0	68-pin QFN	0×1E095069
CY8C3246PVI-147	50	64	8	2	✔	12-bit Del-Sig	1	2	0	0	–	✔	24	4	✔	–	31	25	4	2	48-pin SSOP	0×1E093069
CY8C3246AXI-131	50	64	8	2	✔	12-bit Del-Sig	1	2	0	0	–	✔	24	4	–	–	70	62	8	0	100-pin TQFP	0×1E083069
CY8C3246LTI-162	50	64	8	2	✔	12-bit Del-Sig	1	2	0	0	–	✔	24	4	–	–	29	25	4	0	48-pin QFN	0×1E0A2069
CY8C3246PVI-122	50	64	8	2	✔	12-bit Del-Sig	1	2	0	0	–	✔	24	4	–	–	29	25	4	0	48-pin SSOP	0×1E07A069
CY8C3246AXI-138	50	64	8	2	✔	12-bit Del-Sig	1	2	0	0	–	✔	24	4	✔	–	72	62	8	2	100-pin TQFP	0×1E08A069
CY8C3246LTI-128	50	64	8	2	✔	12-bit Del-Sig	1	2	0	0	–	✔	24	4	✔	–	48	38	8	2	68-pin QFN	0×1E080069
CY8C3246LTI-125	50	64	8	2	✔	12-bit Del-Sig	1	2	0	0	–	✔	24	4	✔	–	31	25	4	2	48-pin QFN	0×1E07D069
CY8C3246FNI-213	50	64	8	2	✔	12-bit Del-Sig	1	2	–	–	–	✔	24	4	–	–	46	38	8	–	72-pin WLCSP	0x1E0D5069

Notes

75. UDBs support a wide variety of functionality including SPI, LIN, UART, timer, counter, PWM, PRS, and others. Individual functions may use a fraction of a UDB or multiple UDBs. Multiple functions can share a single UDB. See the Example Peripherals on page 45 for more information on how UDBs can be used.
76. The I/O Count includes all types of digital I/O: GPIO, SIO, and the two USB I/O. See the I/O System and Routing on page 37 for details on the functionality of each of these types of I/O.
77. The JTAG ID has three major fields. The most significant nibble (left digit) is the version, followed by a 2 byte part number and a 3 nibble manufacturer ID.

13. Packaging

Table 13-1. Package Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Units
T_A	Operating ambient temperature		–40	25.00	85	°C
T_J	Operating junction temperature		–40	–	100	°C
T_{JA}	Package θ_{JA} (48-pin SSOP)		–	49	–	°C/Watt
T_{JA}	Package θ_{JA} (48-pin QFN)		–	14	–	°C/Watt
T_{JA}	Package θ_{JA} (68-pin QFN)		–	15	–	°C/Watt
T_{JA}	Package θ_{JA} (100-pin TQFP)		–	34	–	°C/Watt
T_{JC}	Package θ_{JC} (48-pin SSOP)		–	24	–	°C/Watt
T_{JC}	Package θ_{JC} (48-pin QFN)		–	15	–	°C/Watt
T_{JC}	Package θ_{JC} (68-pin QFN)		–	13	–	°C/Watt
T_{JC}	Package θ_{JC} (100-pin TQFP)		–	10	–	°C/Watt
T_{JA}	Package θ_{JA} (72-pin CSP)		–	18	–	°C/Watt
T_{JC}	Package θ_{JC} (72-pin CSP)		–	0.13	–	°C/Watt

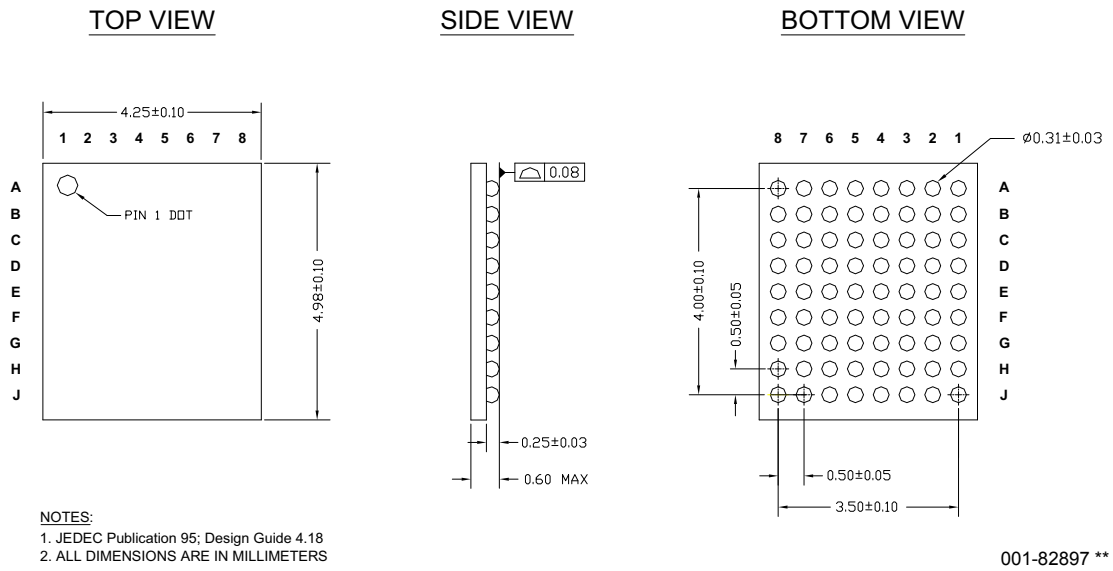
Table 13-2. Solder Reflow Peak Temperature

Package	Maximum Peak Temperature	Maximum Time at Peak Temperature
48-pin SSOP	260 °C	30 seconds
48-pin QFN	260 °C	30 seconds
68-pin QFN	260 °C	30 seconds
100-pin TQFP	260 °C	30 seconds
72-pin CSP	260 °C	30 seconds

Table 13-3. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2

Package	MSL
48-pin SSOP	MSL 3
48-pin QFN	MSL 3
68-pin QFN	MSL 3
100-pin TQFP	MSL 3
72-pin CSP	MSL 1

Figure 13-5. WLCSP Package (4.25 × 4.98 × 0.60 mm)



NOTES:
1. JEDEC Publication 95; Design Guide 4.18
2. ALL DIMENSIONS ARE IN MILLIMETERS

001-82897 **

17. Revision History

Description Title: PSoC® 3: CY8C32 Family Data Sheet Programmable System-on-Chip (PSoC®) Document Number: 001-56955				
Revision	**ECN**	**Submission Date**	**Orig. of Change**	**Description of Change**
**	2796903	11/04/09	MKEA	New datasheet
*A	2824546	12/09/09	MKEA	Updated I2C section to reflect 1 Mbps. Updated Table 11-6 and 11- 7 (Boost AC and DC specs); also added Shottky Diode specs. Changed current for sleep/hibernate mode to include SIO; Added footnote to analog global specs. Updated Figures 1-1, 6-2, 7-14, and 8-1. Updated Table 6-2 and Table 6-3 (Hibernate and Sleep rows) and Power Modes section. Updated GPIO and SIO AC specifications. Updated Gain error in IDAC and VDAC specifications. Updated description of V_{DDA} spec in Table 11-1 and removed GPIO Clamp Current parameter. Updated number of UDBs on page 1. Moved FILO from ILO DC to AC table. Added PCB Layout and PCB Schematic diagrams. Updated Fgpioout spec (Table 11-9). Added duty cycle frequency in PLL AC spec table. Added note for Sleep and Hibernate modes and Active Mode specs in Table 11-2. Linked URL in Section 10.3 to PSoC Creator site. Updated Ja and Jc values in Table 13-1. Updated Single Sample Mode and Fast FIR Mode sections. Updated Input Resistance specification in Del-Sig ADC table. Added Tio_init parameter. Updated PGA and UGB AC Specs. Removed SPC ADC. Updated Boost Converter section. Added section 'SIO as Comparator'; updated Hysteresis spec (differential mode) in Table 11-10. Updated V_{BAT} condition and deleted Vstart parameter in Table 11-6. Added 'Bytes' column for Tables 4-1 to 4-5.
*B	2873322	02/04/10	MKEA	Changed maximum value of PPOR_TR to '1'. Updated V_{BIAS} specification. Updated PCB Schematic. Updated Figure 8-1 and Figure 6-3. Updated Interrupt Vector table, Updated Sales links. Updated JTAG and SWD specifications. Removed Jp-p and Jperiod from ECO AC Spec table. Added note on sleep timer in Table 11-2. Updated ILO AC and DC specifications. Added Resolution parameter in VDAC and IDAC tables. Updated I_{OUT} typical and maximum values. Changed Temperature Sensor range to –40 °C to +85 °C. Removed Latchup specification from Table 11-1. Updated DAC details

Description Title: PSoC® 3: CY8C32 Family Data Sheet Programmable System-on-Chip (PSoC®) *(continued)* Document Number: 001-56955				
Revision	**ECN**	**Submission Date**	**Orig. of Change**	**Description of Change**
*D	2938381	05/27/10	MKEA	Replaced V_{DDIO} with V_{DDD} in USBIO diagram and specification tables, added text in USBIO section of Electrical Specifications. Added Table 13-2 (Package MSL) Modified Tstorag condition and changed max spec to 100 Added bullet (Pass) under ALU (section 7.2.2.2) Added figures for kHzECO and MHzECO in the External Oscillator section Updated Figure 6-1(Clocking Subsystem diagram) Removed CPUCLK_DIV in table 5-2, Deleted Clock Divider SFR subsection Updated PSoC Creator Framework image Updated SIO DC Specifications (V_{IH} and V_{IL} parameters) Updated bullets in Clocking System and Clocking Distribution sections Updated Figure 8-2 Updated Table 11-10 Updated PCB Layout and Schematic, updated as per MTRB review comments Updated Table 6-3 (power changed to current) In 32kHZ EC DC Specifications table, changed I_{CC} Max to 0.25 In IMO DC Specifications table, updated Supply Current values Updated GPIO DC Specs table Modified to support a maximum 50MHz CPU speed
*E	2958674	06/22/10	SHEA	Minor ECN to post datasheet to external website
*F	2989685	08/04/10	MKEA	Added USBIO 22 ohm DP and DM resistors to Simplified Block Diagram Added to Table 6-6 a footnote and references to same. Added sentences to the resistive pull-up and pull-down description bullets. Added sentence to Section 6.4.11, Adjustable Output Level. Updated section 5.5 External Memory Interface Updated Table 11-73 JTAG Interface AC Specifications Updated Table 11-74 SWD Interface AC Specifications
*G	3078568	11/04/10	MKEA	Updated "Current Digital-to-analog Converter (IDAC)" on page 87 Updated "Voltage Digital to Analog Converter (VDAC)" on page 92 Updated Table 11-2, "DC Specifications," on page 68
*H	3107314	12/10/2010	MKEA	Updated delta-sigma tables and graphs. Updated Flash AC specs Formatted table 11.2. Updated interrupt controller table Updated transimpedance amplifier section Updated SIO DC specs table Updated Voltage Monitors DC Specifications table Updated LCD Direct Drive DC specs table Updated ESD_{HBM} value. Updated IDAC and VDAC sections Removed ESO parts from ordering information Changed USBIO pins from NC to DNU and removed redundant USBIO pin description notes Updated POR with brown out DC and AC specs Updated 32 kHz External Crystal DC Specifications Updated XRES IO specs Updated Inductive boost regulator section Delta sigma ADC spec updates Updated comparator section Removed buzz mode from Power Mode Transition diagram
*I	3179219	02/22/2011	MKEA	Updated conditions for flash data retention time. Updated 100-pin TQFP package spec. Updated EEPROM AC specifications.

Description Title: PSoC® 3: CY8C32 Family Data Sheet Programmable System-on-Chip (PSoC®) *(continued)* Document Number: 001-56955				
Revision	**ECN**	**Submission Date**	**Orig. of Change**	**Description of Change**
*O	3732521	09/03/2012	MKEA	Replaced I_{DDDR} and I_{DDAR} specs in Table 11-2, “DC Specifications,” on page 68 that were dropped out in *M revision. Updated Table 11-19, “12-bit Delta-sigma ADC DC Specifications,” on page 84, I_{DD_12} Max value from 1.4 to 1.95 mA Replaced PSoC® 3 Programming AN62391 with TRM in footnote #55 and Section Table 9., “Programming, Debug Interfaces, Resources,” on page 62 Removed Figure 11-8 (Efficiency vs Vout) Removed 62-MHz sub-row in Table 11-2, “DC Specifications,” on page 68 Updated conditions for Storage Temperature in Table 11-1, “Absolute Maximum Ratings DC Specifications[15],” on page 67 Updated conditions and min values for NVL data retention time in Table 11-50, “NVL AC Specifications,” on page 100 Updated Table 11-67, “ILO DC Specifications,” on page 109. Removed the pruned part CY8C3245LTI-129 from the “Ordering Information” section on page 111. Updated PSoC 3 boost circuit value throughout the document. Updated package diagram 51-85061 to *F revision.
*P	3922905	03/06/2013	MKEA	Updated I_{DD_XX} parameters under Table 11-19, “12-bit Delta-sigma ADC DC Specifications,” on page 84. Updated I2C section and updated GPIO and SIO DC specification tables.
*Q	4064707	07/18/2013	MKEA	Added USB test ID in Features. Updated schematic in *Section 2.*. Added paragraph for device reset warning in *Section 5.4*. Added NVL bit for DEBUG_EN in *Section 5.5*. Updated UDB PLD array diagram in *Section 7.2.1*. Changed Tstartup specs in *Section 11.2.1*. Changed GPIO rise and fall time specs in *Section 11.4*. Added IMO spec condition: pre-assembly in *Section 11.9.1*. Added Appendix for CSP package (preliminary)
*R	4118845	09/10/2013	MKEA	Removed T_{STG} spec and added note clarifying the maximum storage temperature range in Table 11-1. Updated Vos spec conditions and TCVos in Table 11-19. Updated 100-TQFP package diagram.
*S	4188568	11/14/2013	MKEA	Updated delta-sigma Vos spec conditions. Added SIO Comparator specifications.
*T	4218210	12/12/2013	MKEA	Integrated 72-pin CSP package information in the datasheet.
*U	4385782	05/21/2014	MKEA	Updated General Description and Features. Added More Information and PSoC Creator sections. Updated 100-pin TQFP package diagram.
*V	4708125	03/31/2015	MKEA	Added INL4 and DNL4 specs in VDAC DC specs. Updated Fig 6-11. Added second note after Fig 6-4. Added a reference to Fig 6-1 in *Section 6.1.1* and *Section 6.1.2* Updated *Section 6.2.2*. Added *Section 7.7.1*. Updated Boost specifications.
*W	4807497	06/23/2015	MKEA	Added reference to code examples in More Information. Updated typ value of T_{WRITE} from 2 to 10 in EEPROM AC specs table. Changed “Device supply for USB operation" to "Device supply (VDDD) for USB operation" in USB DC Specifications. Clarified power supply sequencing and margin for VDDA and VDDD. Updated Serial Wire Debug Interface with limitations of debugging on Port 15. Updated Section 11.7.5. Updated Delta-sigma ADC DC Specifications.