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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	50MHz
Connectivity	EBI/EMI, I <sup>2</sup> C, LINbus, SPI, UART/USART, USB
Peripherals	CapSense, DMA, POR, PWM, WDT
Number of I/O	62
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 16x12b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/infineon-technologies/cy8c3246axa-140">https://www.e-xfl.com/product-detail/infineon-technologies/cy8c3246axa-140</a>

This enables the device to be powered directly from a single battery or solar cell. In addition, you can use the boost converter to generate other voltages required by the device, such as a 3.3-V supply for LCD glass drive. The boost's output is available on the  $V_{BOOST}$  pin, allowing other devices in the application to be powered from the PSoC.

PSoC supports a wide range of low-power modes. These include a 200-nA hibernate mode with RAM retention and a 1- $\mu$ A sleep mode with RTC. In the second mode the optional 32.768-kHz watch crystal runs continuously and maintains an accurate RTC.

Power to all major functional blocks, including the programmable digital and analog peripherals, can be controlled independently by firmware. This allows low-power background processing when some peripherals are not in use. This, in turn, provides a total device current of only 1.2 mA when the CPU is running at 6 MHz, or 0.8 mA running at 3 MHz.

The details of the PSoC power modes are covered in the “Power System” section on page 31 of this datasheet.

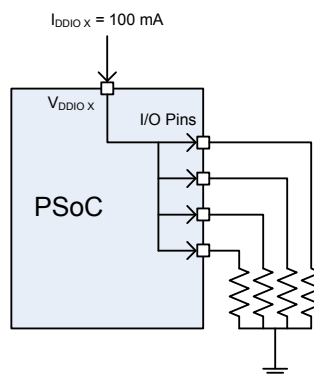
PSoC uses JTAG (4-wire) or SWD (2-wire) interfaces for programming, debug, and test. The 1-wire SWV may also be used for “printf” style debugging. By combining SWD and SWV, you can implement a full debugging interface with just three pins. Using these standard interfaces enables you to debug or program the PSoC with a variety of hardware solutions from Cypress or third party vendors. PSoC supports on-chip break points and 4-KB instruction and data cache memory for debug. Details of the programming, test, and debugging interfaces are discussed in the “Programming, Debug Interfaces, Resources” section on page 62 of this datasheet.

## 2. Pinouts

Each VDDIO pin powers a specific set of I/O pins. (The USBIOs are powered from VDDD.) Using the VDDIO pins, a single PSoC can support multiple voltage levels, reducing the need for off-chip level shifters. The black lines drawn on the pinout diagrams in Figure 2-3 through Figure 2-6, as well as Table 2-1, show the pins that are powered by each VDDIO.

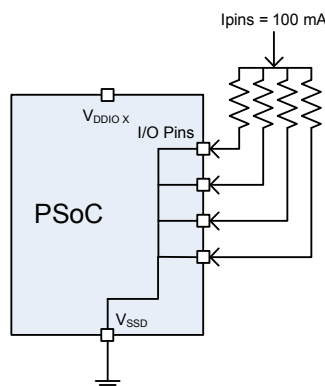
Each VDDIO may source up to 100 mA total to its associated I/O pins, as shown in Figure 2-1.

**Figure 2-1. VDDIO Current Limit**



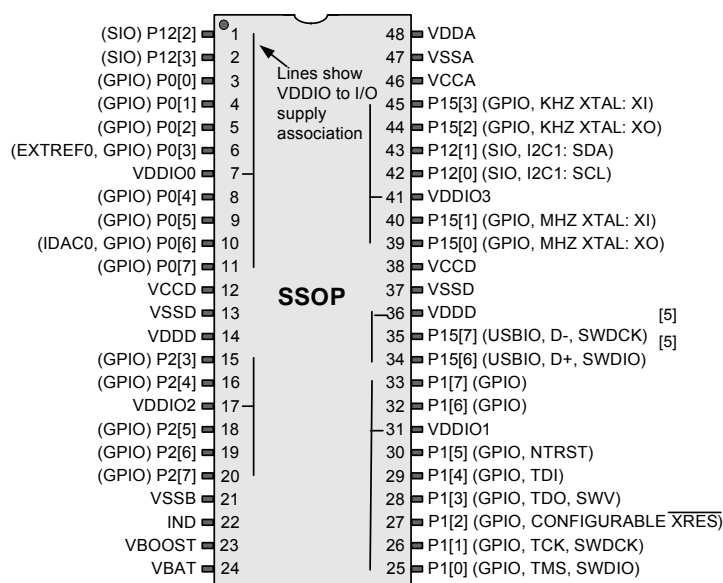
Conversely, for the 100-pin and 68-pin devices, the set of I/O pins associated with any VDDIO may sink up to 100 mA total, as shown in Figure 2-2.

**Figure 2-2. I/O Pins Current Limit**

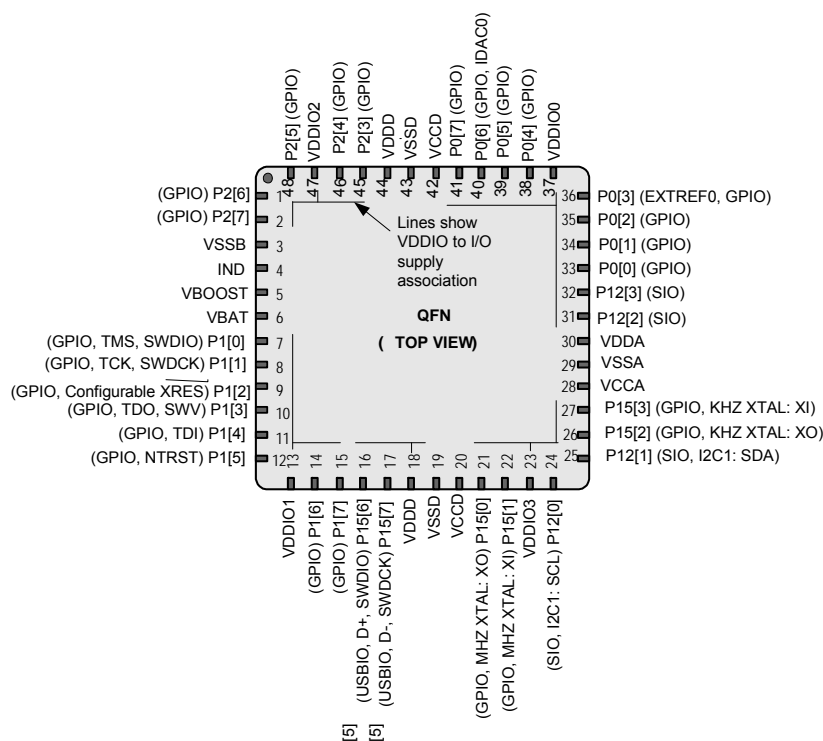


For the 48-pin devices, the set of I/O pins associated with VDDIO0 plus VDDIO2 may sink up to 100 mA total. The set of I/O pins associated with VDDIO1 plus VDDIO3 may sink up to a total of 100 mA.

**Figure 2-3. 48-pin SSOP Part Pinout**



**Figure 2-4. 48-pin QFN Part Pinout<sup>[6]</sup>**



## Notes

- Pins are Do Not Use (DNU) on devices without USB. The pin must be left floating.
- The center pad on the QFN package should be connected to digital ground (VSSD) for best mechanical, thermal, and electrical performance. If not connected to ground, it should be electrically floated and not connected to any other signal. For more information, see [AN72845](#), Design Guidelines for QFN Devices.

## USBIO, D+

Provides D+ connection directly to a USB 2.0 bus. May be used as a digital I/O pin. Pins are Do Not Use (DNU) on devices without USB.

## USBIO, D-

Provides D- connection directly to a USB 2.0 bus. May be used as a digital I/O pin. Pins are No Connect (NC) on devices without USB.

## VBOOST

Power sense connection to boost pump.

## VBAT

Battery supply to boost pump.

## VCCA.

**Output of the analog core regulator or the input to the analog core.** Requires a 1uF capacitor to VSSA. The regulator output is not designed to drive external circuits. **Note that if you use the device with an external core regulator (externally regulated mode), the voltage applied to this pin must not exceed the allowable range of 1.71 V to 1.89 V.** When using the internal core regulator, (internally regulated mode, the default), do not tie any power to this pin. For details see [Power System](#) on page 31.

## VCCD.

**Output of the digital core regulator or the input to the digital core.** The two VCCD pins must be shorted together, with the trace between them as short as possible, and a 1uF capacitor to VSSD. The regulator output is not designed to drive external circuits. **Note that if you use the device with an external core regulator (externally regulated mode), the voltage applied to this pin must not exceed the allowable range of 1.71 V to 1.89 V.** When using the internal core regulator (internally regulated mode, the default), do not tie any power to this pin. For details see [Power System](#) on page 31.

## VDDA

Supply for all analog peripherals and analog core regulator. **VDDA must be the highest voltage present on the device. All other supply pins must be less than or equal to VDDA.**

## VDDD

Supply for all digital peripherals and digital core regulator. VDDD must be less than or equal to VDDA.

## VSSA

Ground for all analog peripherals.

## VSSB

Ground connection for boost pump.

## VSSD

Ground for all digital logic and I/O pins.

## VDDIO0, VDDIO1, VDDIO2, VDDIO3

Supply for I/O pins. See pinouts for specific I/O pin to VDDIO mapping. Each VDDIO must be tied to a valid operating voltage (1.71 V to 5.5 V), and must be less than or equal to VDDA.

## $\overline{\text{XRES}}$ (and configurable $\overline{\text{XRES}}$ )

External reset pin. Active low with internal pull-up. Pin P1[2] may be configured to be a XRES pin; see [“Nonvolatile Latches \(NVLs\)”](#) on page 25.

## 4. CPU

### 4.1 8051 CPU

The CY8C32 devices use a single cycle 8051 CPU, which is fully compatible with the original MCS-51 instruction set. The CY8C32 family uses a pipelined RISC architecture, which executes most instructions in 1 to 2 cycles to provide peak performance of up to 24 MIPS with an average of 2 cycles per instruction. The single cycle 8051 CPU runs ten times faster than a standard 8051 processor.

The 8051 CPU subsystem includes these features:

- Single cycle 8051 CPU
- Up to 64 KB of flash memory, up to 2 KB of EEPROM, and up to 8 KB of SRAM
- 512-byte instruction cache between CPU and flash
- Programmable nested vector interrupt controller
- Direct memory access (DMA) controller
- Peripheral HUB (PHUB)
- External memory interface (EMIF)

### 4.2 Addressing Modes

The following addressing modes are supported by the 8051:

- Direct Addressing: The operand is specified by a direct 8-bit address field. Only the internal RAM and the SFRs can be accessed using this mode.
- Indirect Addressing: The instruction specifies the register which contains the address of the operand. The registers R0 or R1 are used to specify the 8-bit address, while the data pointer (DPTR) register is used to specify the 16-bit address.
- Register Addressing: Certain instructions access one of the registers (R0 to R7) in the specified register bank. These instructions are more efficient because there is no need for an address field.
- Register Specific Instructions: Some instructions are specific to certain registers. For example, some instructions always act on the accumulator. In this case, there is no need to specify the operand.
- Immediate Constants: Some instructions carry the value of the constants directly instead of an address.
- Indexed Addressing: This type of addressing can be used only for a read of the program memory. This mode uses the data pointer as the base and the accumulator value as an offset to read a program memory.
- Bit Addressing: In this mode, the operand is one of 256 bits.

## 4.3.1.2 Logical Instructions

The logical instructions perform Boolean operations such as AND, OR, XOR on bytes, rotate of accumulator contents, and swap of nibbles in an accumulator. The Boolean operations on the bytes are performed on the bit-by-bit basis. [Table 4-2](#) on page 15 shows the list of logical instructions and their description.

**Table 4-2. Logical Instructions**

Mnemonic	Description	Bytes	Cycles
ANL A,Rn	AND register to accumulator	1	1
ANL A,Direct	AND direct byte to accumulator	2	2
ANL A,@Ri	AND indirect RAM to accumulator	1	2
ANL A,#data	AND immediate data to accumulator	2	2
ANL Direct, A	AND accumulator to direct byte	2	3
ANL Direct, #data	AND immediate data to direct byte	3	3
ORL A,Rn	OR register to accumulator	1	1
ORL A,Direct	OR direct byte to accumulator	2	2
ORL A,@Ri	OR indirect RAM to accumulator	1	2
ORL A,#data	OR immediate data to accumulator	2	2
ORL Direct, A	OR accumulator to direct byte	2	3
ORL Direct, #data	OR immediate data to direct byte	3	3
XRL A,Rn	XOR register to accumulator	1	1
XRL A,Direct	XOR direct byte to accumulator	2	2
XRL A,@Ri	XOR indirect RAM to accumulator	1	2
XRL A,#data	XOR immediate data to accumulator	2	2
XRL Direct, A	XOR accumulator to direct byte	2	3
XRL Direct, #data	XOR immediate data to direct byte	3	3
CLR A	Clear accumulator	1	1
CPL A	Complement accumulator	1	1
RL A	Rotate accumulator left	1	1
RLC A	Rotate accumulator left through carry	1	1
RR A	Rotate accumulator right	1	1
RRC A	Rotate accumulator right though carry	1	1
SWAP A	Swap nibbles within accumulator	1	1

## 4.3.1.5 Program Branching Instructions

The 8051 supports a set of conditional and unconditional jump instructions that help to modify the program execution flow. [Table 4-5](#) shows the list of jump instructions.

**Table 4-5. Jump Instructions**

Mnemonic	Description	Bytes	Cycles
ACALL addr11	Absolute subroutine call	2	4
LCALL addr16	Long subroutine call	3	4
RET	Return from subroutine	1	4
RETI	Return from interrupt	1	4
AJMP addr11	Absolute jump	2	3
LJMP addr16	Long jump	3	4
SJMP rel	Short jump (relative address)	2	3
JMP @A + DPTR	Jump indirect relative to DPTR	1	5
JZ rel	Jump if accumulator is zero	2	4
JNZ rel	Jump if accumulator is nonzero	2	4
CJNE A, Direct, rel	Compare direct byte to accumulator and jump if not equal	3	5
CJNE A, #data, rel	Compare immediate data to accumulator and jump if not equal	3	4
CJNE Rn, #data, rel	Compare immediate data to register and jump if not equal	3	4
CJNE @Ri, #data, rel	Compare immediate data to indirect RAM and jump if not equal	3	5
DJNZ Rn, rel	Decrement register and jump if not zero	2	4
DJNZ Direct, rel	Decrement direct byte and jump if not zero	3	5
NOP	No operation	1	1

## 4.4 DMA and PHUB

The PHUB and the DMA controller are responsible for data transfer between the CPU and peripherals, and also data transfers between peripherals. The PHUB and DMA also control device configuration during boot. The PHUB consists of:

- A central hub that includes the DMA controller, arbiter, and router
- Multiple spokes that radiate outward from the hub to most peripherals

There are two PHUB masters: the CPU and the DMA controller. Both masters may initiate transactions on the bus. The DMA channels can handle peripheral communication without CPU intervention. The arbiter in the central hub determines which DMA channel is the highest priority if there are multiple requests.

### 4.4.1 PHUB Features

- CPU and DMA controller are both bus masters to the PHUB
- Eight Multi-layer AHB Bus parallel access paths (spokes) for peripheral access

- Simultaneous CPU and DMA access to peripherals located on different spokes
- Simultaneous DMA source and destination burst transactions on different spokes
- Supports 8, 16, 24, and 32-bit addressing and data

**Table 4-6. PHUB Spokes and Peripherals**

PHUB Spokes	Peripherals
0	SRAM
1	IOs, PICU, EMIF
2	PHUB local configuration, Power manager, Clocks, IC, SWV, EEPROM, Flash programming interface
3	Analog interface and trim, Decimator
4	USB, USB, I <sup>2</sup> C, Timers, Counters, and PWMs
5	Reserved
6	UDBs group 1
7	UDBs group 2

## 4.4.4.5 Scatter Gather DMA

In the case of scatter gather DMA, there are multiple noncontiguous sources or destinations that are required to effectively carry out an overall DMA transaction. For example, a packet may need to be transmitted off of the device and the packet elements, including the header, payload, and trailer, exist in various noncontiguous locations in memory. Scatter gather DMA allows the segments to be concatenated together by using multiple TDs in a chain. The chain gathers the data from the multiple locations. A similar concept applies for the reception of data onto the device. Certain parts of the received data may need to be scattered to various locations in memory for software processing convenience. Each TD in the chain specifies the location for each discrete element in the chain.

## 4.4.4.6 Packet Queuing DMA

Packet queuing DMA is similar to scatter gather DMA but specifically refers to packet protocols. With these protocols, there may be separate configuration, data, and status phases associated with sending or receiving a packet.

For instance, to transmit a packet, a memory mapped configuration register can be written inside a peripheral, specifying the overall length of the ensuing data phase. The CPU can set up this configuration information anywhere in system memory and copy it with a simple TD to the peripheral. After the configuration phase, a data phase TD (or a series of data phase TDs) can begin (potentially using scatter gather). When the data phase TD(s) finish, a status phase TD can be invoked that reads some memory mapped status information from the peripheral and copies it to a location in system memory specified by the CPU for later inspection. Multiple sets of configuration, data, and status phase "subchains" can be strung together to create larger chains that transmit multiple packets in this way. A similar concept exists in the opposite direction to receive the packets.

## 4.4.4.7 Nested DMA

One TD may modify another TD, as the TD configuration space is memory mapped similar to any other peripheral. For example, a first TD loads a second TD's configuration and then calls the second TD. The second TD moves data as required by the application. When complete, the second TD calls the first TD, which again updates the second TD's configuration. This process repeats as often as necessary.

## 4.5 Interrupt Controller

The interrupt controller provides a mechanism for hardware resources to change program execution to a new address, independent of the current task being executed by the main code. The interrupt controller provides enhanced features not found on original 8051 interrupt controllers:

- Thirty two interrupt vectors
- Jumps directly to ISR anywhere in code space with dynamic vector addresses
- Multiple sources for each vector
- Flexible interrupt to vector matching
- Each interrupt vector is independently enabled or disabled
- Each interrupt can be dynamically assigned one of eight priorities
- Eight level nestable interrupts
- Multiple I/O interrupt vectors
- Software can send interrupts
- Software can clear pending interrupts

When an interrupt is pending, the current instruction is completed and the program counter is pushed onto the stack. Code execution then jumps to the program address provided by the vector. After the ISR is completed, a RETI instruction is executed and returns execution to the instruction following the previously interrupted instruction. To do this the RETI instruction pops the program counter from the stack.

If the same priority level is assigned to two or more interrupts, the interrupt with the lower vector number is executed first. Each interrupt vector may choose from three interrupt sources: Fixed Function, DMA, and UDB. The fixed function interrupts are direct connections to the most common interrupt sources and provide the lowest resource cost connection. The DMA interrupt sources provide direct connections to the two DMA interrupt sources provided per DMA channel. The third interrupt source for vectors is from the UDB digital routing array. This allows any digital signal available to the UDB array to be used as an interrupt source. Fixed function interrupts and all interrupt sources may be routed to any interrupt vector using the UDB interrupt source connections.

Figure 4-2 on page 21 represents typical flow of events when an interrupt triggered. Figure 4-3 on page 22 shows the interrupt structure and priority polling.



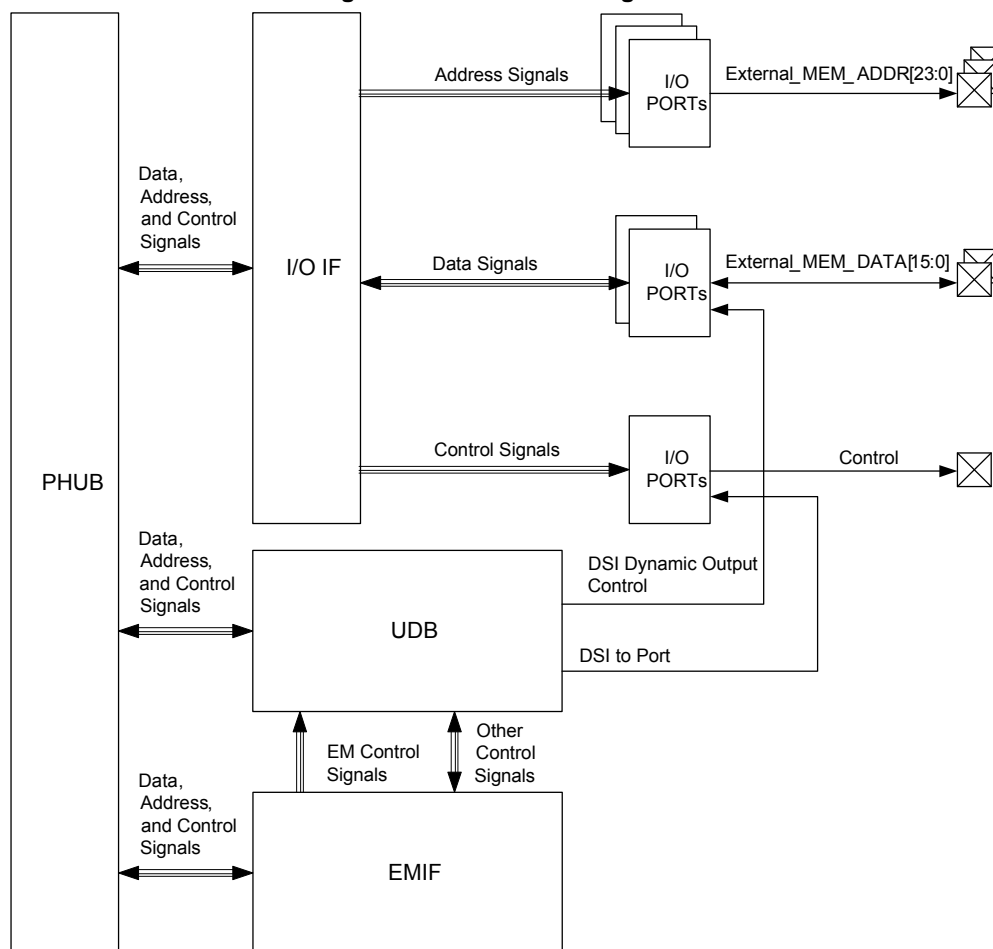
## 5.6 External Memory Interface

CY8C32 provides an external memory interface (EMIF) for connecting to external memory devices. The connection allows read and write accesses to external memories. The EMIF operates in conjunction with UDBs, I/O ports, and other hardware to generate external memory address and control signals. At 33 MHz, each memory access cycle takes four bus clock cycles.

Figure 5-1 is the EMIF block diagram. The EMIF supports synchronous and asynchronous memories. The CY8C32 supports only one type of external memory device at a time.

External memory can be accessed via the 8051 xdata space; up to 24 address bits can be used. See “xdata Space” section on page 28. The memory can be 8 or 16 bits wide.

**Figure 5-1. EMIF Block Diagram**



## 5.7 Memory Map

The CY8C32 memory map is very similar to the MCS-51 memory map.

### 5.7.1 Code Space

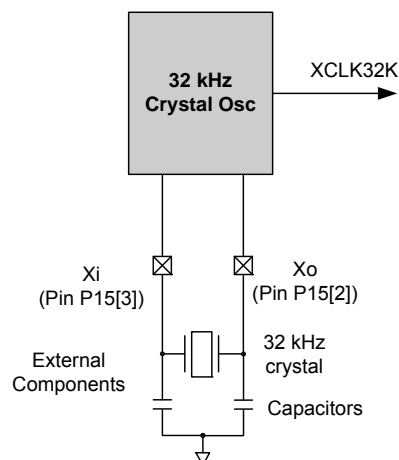
The CY8C32 8051 code space is 64 KB. Only main flash exists in this space. See the “Flash Program Memory” section on page 24.

### 5.7.2 Internal Data Space

The CY8C32 8051 internal data space is 384 bytes, compressed within a 256-byte space. This space consists of 256 bytes of RAM (in addition to the SRAM mentioned in Static RAM on page 24) and a 128-byte space for Special Function Registers (SFRs). See Figure 5-2. The lowest 32 bytes are used for 4 banks of registers R0-R7. The next 16 bytes are bit-addressable.



**Figure 6-3. 32kHzECO Block Diagram**



It is recommended that the external 32.768-kHz watch crystal have a load capacitance (CL) of 6 pF or 12.5 pF. Check the crystal manufacturer's datasheet. The two external capacitors, CL1 and CL2, are typically of the same value, and their total capacitance,  $CL1CL2 / (CL1 + CL2)$ , including pin and trace capacitance, should equal the crystal CL value. For more information, refer to application note [AN54439: PSoC 3 and PSoC 5 External Oscillators](#). See also pin capacitance specifications in the "GPIO" section on page 76.

### 6.1.2.3 Digital System Interconnect

The DSI provides routing for clocks taken from external clock oscillators connected to I/O. The oscillators can also be generated within the device in the digital system and Universal Digital Blocks.

While the primary DSI clock input provides access to all clocking resources, up to eight other DSI clocks (internally or externally generated) may be routed directly to the eight digital clock dividers. This is only possible if there are multiple precision clock sources.

### 6.1.3 Clock Distribution

All seven clock sources are inputs to the central clock distribution system. The distribution system is designed to create multiple high precision clocks. These clocks are customized for the design's requirements and eliminate the common problems found with limited resolution prescalers attached to peripherals. The clock distribution system generates several types of clock trees.

- The master clock is used to select and supply the fastest clock in the system for general clock requirements and clock synchronization of the PSoC device.

- Bus Clock 16-bit divider uses the master clock to generate the bus clock used for data transfers. Bus clock is the source clock for the CPU clock divider.
- Eight fully programmable 16-bit clock dividers generate digital system clocks for general use in the digital system, as configured by the design's requirements. Digital system clocks can generate custom clocks derived from any of the seven clock sources for any purpose. Examples include baud rate generators, accurate PWM periods, and timer clocks, and many others. If more than eight digital clock dividers are required, the Universal Digital Blocks (UDBs) and fixed function Timer/Counter/PWMs can also generate clocks.
- Four 16-bit clock dividers generate clocks for the analog system components that require clocking, such as ADC. The analog clock dividers include skew control to ensure that critical analog events do not occur simultaneously with digital switching events. This is done to reduce analog system noise.

Each clock divider consists of an 8-input multiplexer, a 16-bit clock divider (divide by 2 and higher) that generates ~50 percent duty cycle clocks, master clock resynchronization logic, and deglitch logic. The outputs from each digital clock tree can be routed into the digital system interconnect and then brought back into the clock system as an input, allowing clock chaining of up to 32 bits.

### 6.1.4 USB Clock Domain

The USB clock domain is unique in that it operates largely asynchronously from the main clock network. The USB logic contains a synchronous bus interface to the chip, while running on an asynchronous clock to process USB data. The USB logic requires a 48 MHz frequency. This frequency can be generated from different sources, including DSI clock at 48 MHz or doubled value of 24 MHz from internal oscillator, DSI signal, or crystal oscillator.

## 6.2 Power System

The power system consists of separate analog, digital, and I/O supply pins, labeled VDDA, VDDD, and VDDIOX, respectively. It also includes two internal 1.8 V regulators that provide the digital (VCCD) and analog (VCCA) supplies for the internal core logic. The output pins of the regulators (VCCD and VCCA) and the VDDIO pins must have capacitors connected as shown in [Figure 6-4](#). The two VCCD pins must be shorted together, with as short a trace as possible, and connected to a 1-μF ±10-percent X5R capacitor. The power system also contains a sleep regulator, an I<sup>2</sup>C regulator, and a hibernate regulator.

## 6.4.13 SIO as Comparator

This section applies only to SIO pins. The adjustable input level feature of the SIOs as explained in the [Adjustable Input Level](#) section can be used to construct a comparator. The threshold for the comparator is provided by the SIO's reference generator. The reference generator has the option to set the analog signal routed through the analog global line as threshold for the comparator. Note that a pair of SIO pins share the same threshold.

The digital input path in [Figure 6-10](#) on page 40 illustrates this functionality. In the figure, 'Reference level' is the analog signal routed through the analog global. The hysteresis feature can also be enabled for the input buffer of the SIO, which increases noise immunity for the comparator.

## 6.4.14 Hot Swap

This section applies only to SIO pins. SIO pins support 'hot swap' capability to plug into an application without loading the signals that are connected to the SIO pins even when no power is applied to the PSoC device. This allows the unpowered PSoC to maintain a high impedance load to the external device while also preventing the PSoC from being powered through a SIO pin's protection diode.

Powering the device up or down while connected to an operational I<sup>2</sup>C bus may cause transient states on the SIO pins. The overall I<sup>2</sup>C bus design should take this into account.

## 6.4.15 Over Voltage Tolerance

All I/O pins provide an over voltage tolerance feature at any operating VDD.

- There are no current limitations for the SIO pins as they present a high impedance load to the external circuit where  $V_{DDIO} < V_{IN} \leq 5.5 \text{ V}$ .
- The GPIO pins must be limited to 100  $\mu\text{A}$  using a current limiting resistor. GPIO pins clamp the pin voltage to approximately one diode above the VDDIO supply where  $V_{DDIO} < V_{IN} < V_{DDA}$ .
- In case of a GPIO pin configured for analog input/output, the analog voltage on the pin must not exceed the VDDIO supply voltage to which the GPIO belongs.

A common application for this feature is connection to a bus such as I<sup>2</sup>C where different devices are running from different supply voltages. In the I<sup>2</sup>C case, the PSoC chip is configured into the Open Drain, Drives Low mode for the SIO pin. This allows an external pull-up to pull the I<sup>2</sup>C bus voltage above the PSoC pin supply. For example, the PSoC chip could operate at 1.8 V, and an external device could run from 5 V. Note that the SIO pin's  $V_{IH}$  and  $V_{IL}$  levels are determined by the associated  $V_{DDIO}$  supply pin.

The SIO pin must be in one of the following modes: 0 (high impedance analog), 1 (high impedance digital), or 4 (open drain drives low). See [Figure 6-12](#) for details. Absolute maximum ratings for the device must be observed for all I/O pins.

## 6.4.16 Reset Configuration

While reset is active all I/Os are reset to and held in the High Impedance Analog state. After reset is released, the state can be reprogrammed on a port-by-port basis to pull-down or pull-up. To ensure correct reset operation, the port reset configuration data is stored in special nonvolatile registers. The stored reset data is automatically transferred to the port reset configuration registers at reset release.

## 6.4.17 Low-Power Functionality

In all low-power modes the I/O pins retain their state until the part is awakened and changed or reset. To awaken the part, use a pin interrupt, because the port interrupt logic continues to function in all low-power modes.

## 6.4.18 Special Pin Functionality

Some pins on the device include additional special functionality in addition to their GPIO or SIO functionality. The specific special function pins are listed in [Pinouts](#) on page 6. The special features are:

- Digital
  - 4- to 25- MHz crystal oscillator
  - 32.768-kHz crystal oscillator
  - Wake from sleep on I<sup>2</sup>C address match. Any pin can be used for I<sup>2</sup>C if wake from sleep is not required.
  - JTAG interface pins
  - SWD interface pins
  - SWV interface pins
  - External reset
- Analog
  - High current IDAC output
  - External reference inputs

## 6.4.19 JTAG Boundary Scan

The device supports standard JTAG boundary scan chains on all I/O pins for board level test.

## 7. Digital Subsystem

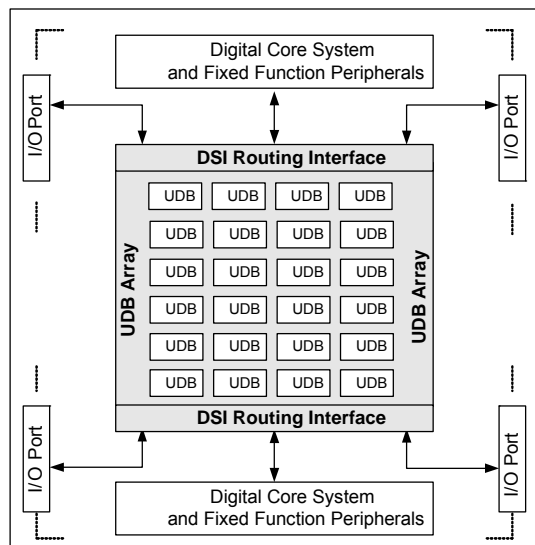
The digital programmable system creates application specific combinations of both standard and advanced digital peripherals and custom logic functions. These peripherals and logic are then interconnected to each other and to any pin on the device, providing a high level of design flexibility and IP security.

The features of the digital programmable system are outlined here to provide an overview of capabilities and architecture. You do not need to interact directly with the programmable digital system at the hardware and register level. PSoC Creator provides a high level schematic capture graphical interface to automatically place and route resources similar to PLDs.

The main components of the digital programmable system are:

- **Universal Digital Blocks (UDB)** – These form the core functionality of the digital programmable system. UDBs are a collection of uncommitted logic (PLD) and structural logic (Datapath) optimized to create all common embedded peripherals and customized functionality that are application or design specific.
- **Universal Digital Block Array** – UDB blocks are arrayed within a matrix of programmable interconnect. The UDB array structure is homogeneous and allows for flexible mapping of digital functions onto the array. The array supports extensive and flexible routing interconnects between UDBs and the Digital System Interconnect.
- **Digital System Interconnect (DSI)** – Digital signals from Universal Digital Blocks (UDBs), fixed function peripherals, I/O pins, interrupts, DMA, and other system core signals are attached to the Digital System Interconnect to implement full featured device connectivity. The DSI allows any digital function to any pin or other feature routability when used with the Universal Digital Block Array.

**Figure 7-1. CY8C32 Digital Programmable Architecture**



### 7.1 Example Peripherals

The flexibility of the CY8C32 family's Universal Digital Blocks (UDBs) and Analog Blocks allow the user to create a wide range of components (peripherals). The most common peripherals were built and characterized by Cypress and are shown in the PSoC Creator component catalog, however, users may also create their own custom components using PSoC Creator. Using PSoC Creator, users may also create their own components for reuse within their organization, for example sensor interfaces, proprietary algorithms, and display interfaces.

The number of components available through PSoC Creator is too numerous to list in the datasheet, and the list is always growing. An example of a component available for use in CY8C32 family, but, not explicitly called out in this datasheet is the UART component.

#### 7.1.1 Example Digital Components

The following is a sample of the digital components available in PSoC Creator for the CY8C32 family. The exact amount of hardware resources (UDBs, routing, RAM, flash) used by a component varies with the features selected in PSoC Creator for the component.

- **Communications**
  - I<sup>2</sup>C
  - UART
  - SPI
- **Functions**
  - EMIF
  - PWMs
  - Timers
  - Counters
- **Logic**
  - NOT
  - OR
  - XOR
  - AND

#### 7.1.2 Example Analog Components

The following is a sample of the analog components available in PSoC Creator for the CY8C32 family. The exact amount of hardware resources (routing, RAM, flash) used by a component varies with the features selected in PSoC Creator for the component.

- **ADC**
  - Delta-sigma
- **DACs**
  - Current
  - Voltage
  - PWM
- **Comparators**

#### 7.1.3 Example System Function Components

The following is a sample of the system function components available in PSoC Creator for the CY8C32 family. The exact amount of hardware resources (UDBs, routing, RAM, flash) used by a component varies with the features selected in PSoC Creator for the component.

- CapSense
- LCD Drive
- LCD Control

Independent of the ALU operation, these functions are available:

- Shift left
- Shift right
- Nibble swap
- Bitwise OR mask

## 7.2.2.3 Conditionals

Each datapath has two compares, with bit masking options. Compare operands include the two accumulators and the two data registers in a variety of configurations. Other conditions include zero detect, all ones detect, and overflow. These conditions are the primary datapath outputs, a selection of which can be driven out to the UDB routing matrix. Conditional computation can use the built in chaining to neighboring UDBs to operate on wider data widths without the need to use routing resources.

## 7.2.2.4 Variable MSB

The most significant bit of an arithmetic and shift function can be programmatically specified. This supports variable width CRC and PRS functions, and in conjunction with ALU output masking, can implement arbitrary width timers, counters and shift blocks.

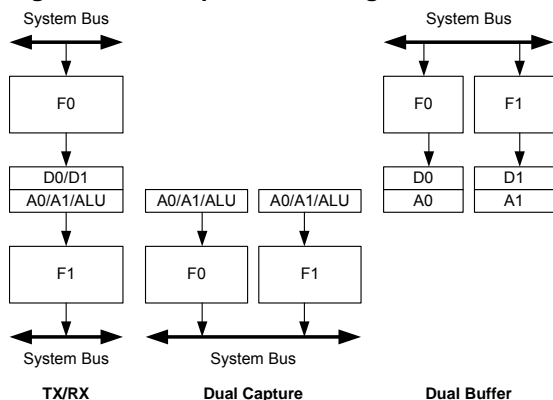
## 7.2.2.5 Built in CRC/PRS

The datapath has built in support for single cycle Cyclic Redundancy Check (CRC) computation and Pseudo Random Sequence (PRS) generation of arbitrary width and arbitrary polynomial. CRC/PRS functions longer than 8 bits may be implemented in conjunction with PLD logic, or built in chaining may be use to extend the function into neighboring UDBs.

## 7.2.2.6 Input/Output FIFOs

Each datapath contains two four-byte deep FIFOs, which can be independently configured as an input buffer (system bus writes to the FIFO, datapath internal reads the FIFO), or an output buffer (datapath internal writes to the FIFO, the system bus reads from the FIFO). The FIFOs generate status that are selectable as datapath outputs and can therefore be driven to the routing, to interact with sequencers, interrupts, or DMA.

**Figure 7-5. Example FIFO Configurations**



## 7.2.2.7 Chaining

The datapath can be configured to chain conditions and signals such as carries and shift data with neighboring datapaths to create higher precision arithmetic, shift, CRC/PRS functions.

## 7.2.2.8 Time Multiplexing

In applications that are over sampled, or do not need high clock rates, the single ALU block in the datapath can be efficiently shared with two sets of registers and condition generators. Carry and shift out data from the ALU are registered and can be selected as inputs in subsequent cycles. This provides support for 16-bit functions in one (8-bit) datapath.

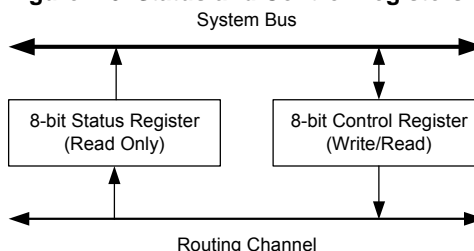
## 7.2.2.9 Datapath I/O

There are six inputs and six outputs that connect the datapath to the routing matrix. Inputs from the routing provide the configuration for the datapath operation to perform in each cycle, and the serial data inputs. Inputs can be routed from other UDB blocks, other device peripherals, device I/O pins, and so on. The outputs to the routing can be selected from the generated conditions, and the serial data outputs. Outputs can be routed to other UDB blocks, device peripherals, interrupt and DMA controller, I/O pins, and so on.

## 7.2.3 Status and Control Module

The primary purpose of this circuitry is to coordinate CPU firmware interaction with internal UDB operation.

**Figure 7-6. Status and Control Registers**



The bits of the control register, which may be written to by the system bus, are used to drive into the routing matrix, and thus provide firmware with the opportunity to control the state of UDB processing. The status register is read-only and it allows internal UDB state to be read out onto the system bus directly from internal routing. This allows firmware to monitor the state of UDB processing. Each bit of these registers has programmable connections to the routing matrix and routing connections are made depending on the requirements of the application.

## 7.2.3.1 Usage Examples

As an example of control input, a bit in the control register can be allocated as a function enable bit. There are multiple ways to enable a function. In one method the control bit output would be routed to the clock control block in one or more UDBs and serve as a clock enable for the selected UDB blocks. A status example is a case where a PLD or datapath block generated a condition, such as a "compare true" condition that is captured and latched by the status register and then read (and cleared) by CPU firmware.

## 9.2 Serial Wire Debug Interface

The SWD interface is the preferred alternative to the JTAG interface. It requires only two pins instead of the four or five needed by JTAG. SWD provides all of the programming and debugging features of JTAG at the same speed. SWD does not provide access to scan chains or device chaining. The SWD clock frequency can be up to 1/3 of the CPU clock frequency.

SWD uses two pins, either two of the JTAG pins (TMS and TCK) or the USBIO D+ and D– pins. The USBIO pins are useful for in system programming of USB solutions that would otherwise require a separate programming connector. One pin is used for the data clock and the other is used for data input and output.

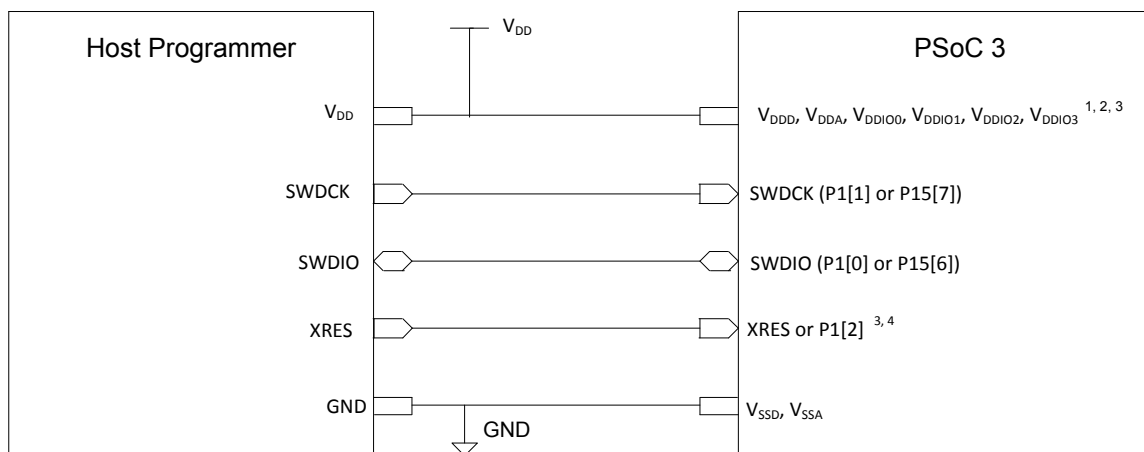
SWD can be enabled on only one of the pin pairs at a time. This only happens if, within 8  $\mu$ s (key window) after reset, that pin pair

(JTAG or USB) receives a predetermined acquire sequence of 1s and 0s. If the NVL latches are set for SWD (see [Section 5.5](#)), this sequence need not be applied to the JTAG pin pair. The acquire sequence must always be applied to the USB pin pair.

SWD is used for debugging or for programming the flash memory.

The SWD interface can be enabled from the JTAG interface or disabled, allowing its pins to be used as GPIO. Unlike JTAG, the SWD interface can always be reacquired on any device during the key window. It can then be used to reenables the JTAG interface, if desired. When using SWD or JTAG pins as standard GPIO, make sure that the GPIO functionality and PCB circuits do not interfere with SWD or JTAG use.

**Figure 9-2. SWD Interface Connections between PSoC 3 and Programmer**



<sup>1</sup> The voltage levels of the Host Programmer and the PSoC 3 voltage domains involved in Programming should be the same. XRES pin (XRES\_N or P1[2]) is powered by VDDIO1. The USB SWD pins are powered by VDD. So for Programming using the USB SWD pins with XRES pin, the VDD, VDDIO1 of PSoC 3 should be at the same voltage level as Host VDD. Rest of PSoC 3 voltage domains (VDDA, VDDIO0, VDDIO2, VDDIO3) need not be at the same voltage level as host Programmer. The Port 1 SWD pins are powered by VDDIO1. So VDDIO1 of PSoC 3 should be at same voltage level as host VDD for Port 1 SWD programming. Rest of PSoC 3 voltage domains (VDD, VDDA, VDDIO0, VDDIO2, VDDIO3) need not be at the same voltage level as host Programmer.

<sup>2</sup> VDDA must be greater than or equal to all other power supplies (VDD, VDDIO's) in PSoC 3.

<sup>3</sup> For Power cycle mode Programming, XRES pin is not required. But the Host programmer must have the capability to toggle power (VDD, VDDA, All VDDIO's) to PSoC 3. This may typically require external interface circuitry to toggle power which will depend on the programming setup. The power supplies can be brought up in any sequence, however, once stable, VDDA must be greater than or equal to all other supplies.

<sup>4</sup> P1[2] will be configured as XRES by default only for 48-pin devices (without dedicated XRES pin). For devices with dedicated XRES pin, P1[2] is GPIO pin by default. So use P1[2] as Reset pin only for 48-pin devices, but use dedicated XRES pin for rest of devices.



## 11.3.3 Inductive Boost Regulator

Unless otherwise specified, operating conditions are:  $V_{BAT} = 0.5\text{ V} - 3.6\text{ V}$ ,  $V_{OUT} = 1.8\text{ V} - 5.0\text{ V}$ ,  $I_{OUT} = 0\text{ mA} - 50\text{ mA}$ ,  $L_{BOOST} = 4.7\text{ }\mu\text{H} - 22\text{ }\mu\text{H}$ ,  $C_{BOOST} = 22\text{ }\mu\text{F} \parallel 3 \times 1.0\text{ }\mu\text{F} \parallel 3 \times 0.1\text{ }\mu\text{F}$ ,  $C_{BAT} = 22\text{ }\mu\text{F}$ ,  $I_F = 1.0\text{ A}$ . Unless otherwise specified, all charts and graphs show typical values.

**Table 11-6. Inductive Boost Regulator DC Specifications**

Parameter	Description	Conditions	Min	Typ	Max	Units
$V_{OUT}$	Boost output voltage <sup>[31]</sup>	$v_{sel} = 1.8\text{ V}$ in register BOOST_CR0	1.71	1.8	1.89	V
		$v_{sel} = 1.9\text{ V}$ in register BOOST_CR0	1.81	1.90	2.00	V
		$v_{sel} = 2.0\text{ V}$ in register BOOST_CR0	1.90	2.00	2.10	V
		$v_{sel} = 2.4\text{ V}$ in register BOOST_CR0	2.16	2.40	2.64	V
		$v_{sel} = 2.7\text{ V}$ in register BOOST_CR0	2.43	2.70	2.97	V
		$v_{sel} = 3.0\text{ V}$ in register BOOST_CR0	2.70	3.00	3.30	V
		$v_{sel} = 3.3\text{ V}$ in register BOOST_CR0	2.97	3.30	3.63	V
		$v_{sel} = 3.6\text{ V}$ in register BOOST_CR0	3.24	3.60	3.96	V
		$v_{sel} = 5.0\text{ V}$ in register BOOST_CR0	4.50	5.00	5.50	V
$V_{BAT}$	Input voltage to boost <sup>[32]</sup>	$I_{OUT} = 0\text{ mA} - 5\text{ mA}$ $v_{sel} = 1.8\text{ V} - 2.0\text{ V}$ , $T_A = 0\text{ }^\circ\text{C} - 70\text{ }^\circ\text{C}$	0.5	—	0.8	V
		$I_{OUT} = 0\text{ mA} - 15\text{ mA}$ $v_{sel} = 1.8\text{ V} - 5.0\text{ V}$ <sup>[33]</sup> , $T_A = -10\text{ }^\circ\text{C} - 85\text{ }^\circ\text{C}$	1.6	—	3.6	V
		$I_{OUT} = 0\text{ mA} - 25\text{ mA}$ $v_{sel} = 1.8\text{ V} - 2.7\text{ V}$ , $T_A = -10\text{ }^\circ\text{C} - 85\text{ }^\circ\text{C}$	0.8	—	1.6	V
		$I_{OUT} = 0\text{ mA} - 50\text{ mA}$ $v_{sel} = 1.8\text{ V} - 3.3\text{ V}$ <sup>[33]</sup> , $T_A = -40\text{ }^\circ\text{C} - 85\text{ }^\circ\text{C}$	1.8	—	2.5	V
			1.3	—	2.5	V
			2.5	—	3.6	V
		$v_{sel} = 2.5\text{ V} - 5.0\text{ V}$ <sup>[33]</sup> , $T_A = -10\text{ }^\circ\text{C} - 85\text{ }^\circ\text{C}$	2.5	—	3.6	V
$I_{OUT}$	Output current	$T_A = 0\text{ }^\circ\text{C} - 70\text{ }^\circ\text{C}$ $V_{BAT} = 0.5\text{ V} - 0.8\text{ V}$	0	—	5	mA
		$T_A = -10\text{ }^\circ\text{C} - 85\text{ }^\circ\text{C}$ $V_{BAT} = 1.6\text{ V} - 3.6\text{ V}$	0	—	15	mA
			0	—	25	mA
			0	—	50	mA
			0	—	50	mA
		$T_A = -40\text{ }^\circ\text{C} - 85\text{ }^\circ\text{C}$ $V_{BAT} = 1.8\text{ V} - 2.5\text{ V}$	0	—	50	mA
$I_{LPK}$	Inductor peak current		—	—	700	mA
$I_Q$	Quiescent current	Boost active mode	—	250	—	$\mu\text{A}$
		Boost sleep mode, $I_{OUT} < 1\text{ }\mu\text{A}$	—	25	—	$\mu\text{A}$
$\text{Reg}_{LOAD}$	Load regulation		—	—	10	%
$\text{Reg}_{LINE}$	Line regulation		—	—	10	%

### Notes

31. Listed  $v_{sel}$  options are characterized. Additional  $v_{sel}$  options are valid and guaranteed by design.

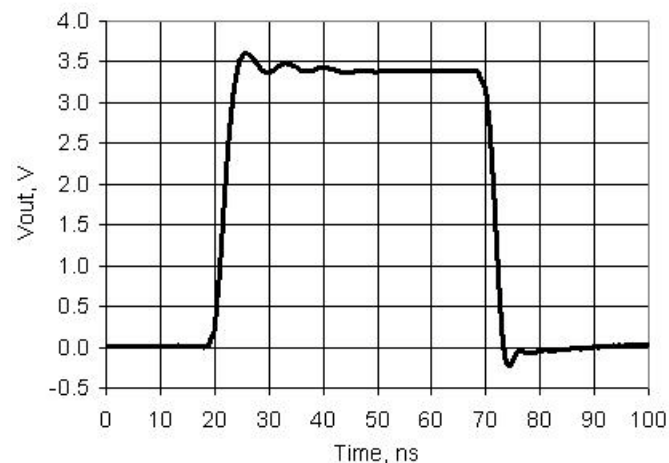
32. The boost will start at all valid  $V_{BAT}$  conditions including down to  $V_{BAT} = 0.5\text{ V}$ .

33. If  $V_{BAT}$  is greater than or equal to  $V_{OUT}$  boost setting, then  $V_{OUT}$  will be less than  $V_{BAT}$  due to resistive losses in the boost circuit.

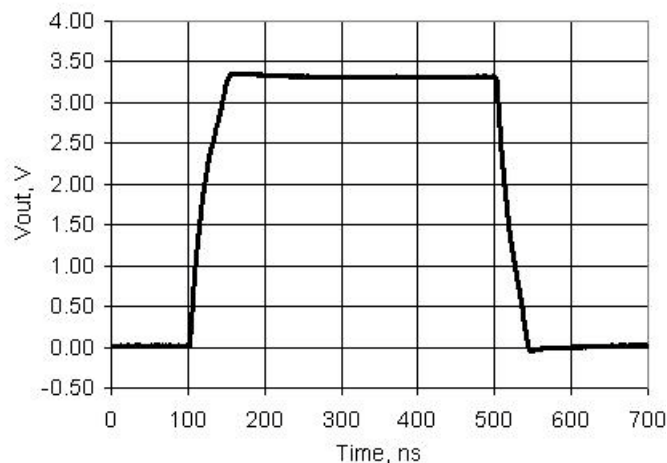
**Table 11-12. SIO AC Specifications** (continued)

Parameter	Description	Conditions	Min	Typ	Max	Units
F <sub>sioout</sub>	SIO output operating frequency					
	2.7 V < V <sub>DDIO</sub> < 5.5 V, Unregulated output (GPIO) mode, fast strong drive mode	90/10% V <sub>DDIO</sub> into 25 pF	–	–	33	MHz
	1.71 V < V <sub>DDIO</sub> < 2.7 V, Unregulated output (GPIO) mode, fast strong drive mode	90/10% V <sub>DDIO</sub> into 25 pF	–	–	16	MHz
	3.3 V < V <sub>DDIO</sub> < 5.5 V, Unregulated output (GPIO) mode, slow strong drive mode	90/10% V <sub>DDIO</sub> into 25 pF	–	–	5	MHz
	1.71 V < V <sub>DDIO</sub> < 3.3 V, Unregulated output (GPIO) mode, slow strong drive mode	90/10% V <sub>DDIO</sub> into 25 pF	–	–	4	MHz
	2.7 V < V <sub>DDIO</sub> < 5.5 V, Regulated output mode, fast strong drive mode	Output continuously switching into 25 pF	–	–	20	MHz
	1.71 V < V <sub>DDIO</sub> < 2.7 V, Regulated output mode, fast strong drive mode	Output continuously switching into 25 pF	–	–	10	MHz
	1.71 V < V <sub>DDIO</sub> < 5.5 V, Regulated output mode, slow strong drive mode	Output continuously switching into 25 pF	–	–	2.5	MHz
F <sub>sioin</sub>	SIO input operating frequency					
	1.71 V ≤ V <sub>DDIO</sub> ≤ 5.5 V	90/10% V <sub>DDIO</sub>	–	–	33	MHz

**Figure 11-20. SIO Output Rise and Fall Times, Fast Strong Mode, V<sub>DDIO</sub> = 3.3 V, 25 pF Load**



**Figure 11-21. SIO Output Rise and Fall Times, Slow Strong Mode, V<sub>DDIO</sub> = 3.3 V, 25 pF Load**





**Table 11-13. SIO Comparator Specifications<sup>[42]</sup>**

Parameter	Description	Conditions	Min	Typ	Max	Units
Vos	Offset voltage	$V_{DDIO} = 2\text{ V}$	–	–	68	mV
		$V_{DDIO} = 2.7\text{ V}$	–	–	72	
		$V_{DDIO} = 5.5\text{ V}$	–	–	82	
TCVos	Offset voltage drift with temp		–	–	250	$\mu\text{V}/^\circ\text{C}$
CMRR	Common mode rejection ratio	$V_{DDIO} = 2\text{ V}$	30	–	–	dB
		$V_{DDIO} = 2.7\text{ V}$	35	–	–	
		$V_{DDIO} = 5.5\text{ V}$	40	–	–	
Tresp	Response time		–	–	30	ns

#### 11.4.3 USBIO

For operation in GPIO mode, the standard range for  $V_{DDD}$  applies, see [Device Level Specifications](#) on page 68.

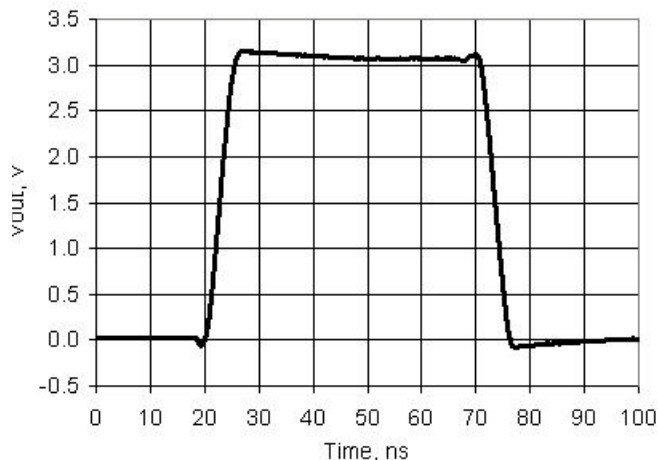
**Table 11-14. USBIO DC Specifications**

Parameter	Description	Conditions	Min	Typ	Max	Units
Rusbi	USB D+ pull-up resistance	With idle bus	0.900	–	1.575	$k\Omega$
Rusba	USB D+ pull-up resistance	While receiving traffic	1.425	–	3.090	$k\Omega$
Vohusb	Static output high	$15\text{ k}\Omega \pm 5\%$ to $V_{SS}$ , internal pull-up enabled	2.8	–	3.6	V
Volusb	Static output low	$15\text{ k}\Omega \pm 5\%$ to $V_{SS}$ , internal pull-up enabled	–	–	0.3	V
Vohgpio	Output voltage high, GPIO mode	$I_{OH} = 4\text{ mA}$ , $V_{DDD} \geq 3\text{ V}$	2.4	–	–	V
Volgpio	Output voltage low, GPIO mode	$I_{OL} = 4\text{ mA}$ , $V_{DDD} \geq 3\text{ V}$	–	–	0.3	V
Vdi	Differential input sensitivity	$ (D+) - (D-) $	–	–	0.2	V
Vcm	Differential input common mode range	–	0.8	–	2.5	V
Vse	Single ended receiver threshold	–	0.8	–	2	V
Rps2	PS/2 pull-up resistance	In PS/2 mode, with PS/2 pull-up enabled	3	–	7	$k\Omega$
Rext	External USB series resistor	In series with each USB pin	21.78 (–1%)	22	22.22 (+1%)	$\Omega$
Zo	USB driver output impedance	Including Rext	28	–	44	$\Omega$
C <sub>IN</sub>	USB transceiver input capacitance	–	–	–	20	pF
I <sub>IL</sub> <sup>[42]</sup>	Input leakage current (absolute value)	25 °C, $V_{DDD} = 3.0\text{ V}$	–	–	2	nA

**Note**

42. Based on device characterization (Not production tested).

$V_{DD} = 3.3\text{ V}$ , 25 pF Load



**Table 11-16. USB Driver AC Specifications**

Parameter	Description	Conditions	Min	Typ	Max	Units
$T_r$	Transition rise time		–	–	20	ns
$T_f$	Transition fall time		–	–	20	ns
TR	Rise/fall time matching	$V_{USB\_5}$ , $V_{USB\_3.3}$ , see <a href="#">USB DC Specifications</a> on page 98	90%	–	111%	
Vcrs	Output signal crossover voltage		1.3	–	2	V

## 11.4.4 XRES

**Table 11-17. XRES DC Specifications**

Parameter	Description	Conditions	Min	Typ	Max	Units
$V_{IH}$	Input voltage high threshold		$0.7 \times V_{DDIO}$	–	–	V
$V_{IL}$	Input voltage low threshold		–	–	$0.3 \times V_{DDIO}$	V
Rpullup	Pull-up resistor		3.5	5.6	8.5	k $\Omega$
$C_{IN}$	Input capacitance <sup>[43]</sup>		–	3	–	pF
$V_H$	Input voltage hysteresis (Schmitt-Trigger) <sup>[43]</sup>		–	100	–	mV
I <sub>diode</sub>	Current through protection diode to $V_{DDIO}$ and $V_{SSIO}$		–	–	100	$\mu$ A

**Table 11-18. XRES AC Specifications**

Parameter	Description	Conditions	Min	Typ	Max	Units
$T_{RESET}$	Reset pulse width		1	–	–	$\mu$ s

### Note

43. Based on device characterization (Not production tested).

### 11.6.6 USB

**Table 11-43. USB DC Specifications**

Parameter	Description	Conditions	Min	Typ	Max	Units
V <sub>USB_5</sub>	Device supply (V <sub>DD</sub> ) for USB operation	USB configured, USB regulator enabled	4.35	–	5.25	V
V <sub>USB_3.3</sub>		USB configured, USB regulator bypassed	3.15	–	3.6	V
V <sub>USB_3</sub>		USB configured, USB regulator bypassed <sup>[54]</sup>	2.85	–	3.6	V
I <sub>USB_Configured</sub>	Device supply current in device active mode, bus clock and IMO = 24 MHz	V <sub>DD</sub> = 5 V, F <sub>CPU</sub> = 1.5 MHz	–	10	–	mA
		V <sub>DD</sub> = 3.3 V, F <sub>CPU</sub> = 1.5 MHz	–	8	–	mA
I <sub>USB_Suspended</sub>	Device supply current in device sleep mode	V <sub>DD</sub> = 5 V, connected to USB host, PICU configured to wake on USB resume signal	–	0.5	–	mA
		V <sub>DD</sub> = 5 V, disconnected from USB host	–	0.3	–	mA
		V <sub>DD</sub> = 3.3 V, connected to USB host, PICU configured to wake on USB resume signal	–	0.5	–	mA
		V <sub>DD</sub> = 3.3 V, disconnected from USB host	–	0.3	–	mA

### 11.6.7 Universal Digital Blocks (UDBs)

PSoC Creator provides a library of pre-built and tested standard digital peripherals (UART, SPI, LIN, PRS, CRC, timer, counter, PWM, AND, OR, and so on) that are mapped to the UDB array. See the component datasheets in PSoC Creator for full AC/DC specifications, APIs, and example code.

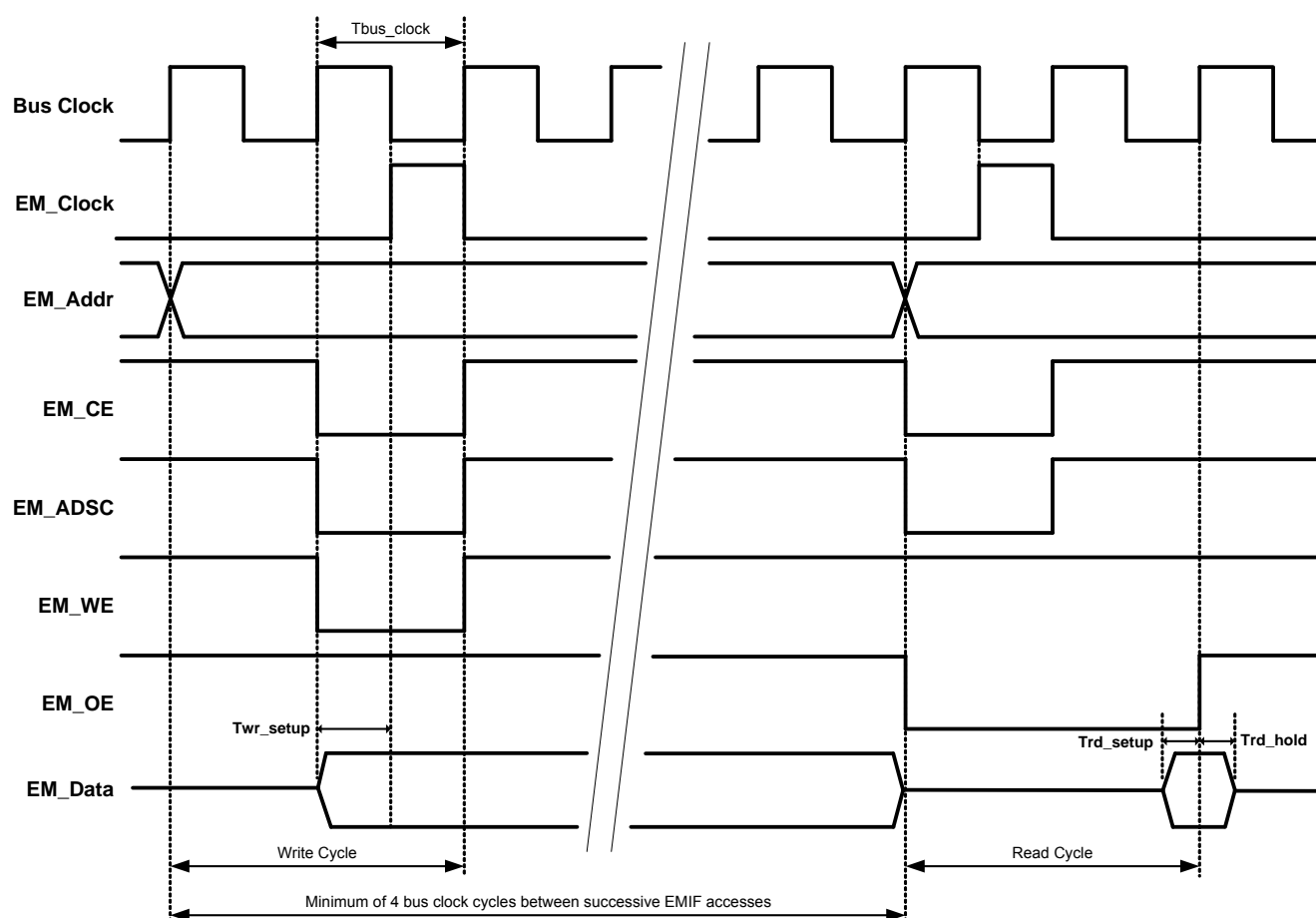
**Table 11-44. UDB AC Specifications**

Parameter	Description	Conditions	Min	Typ	Max	Units
Datapath Performance						
F <sub>MAX_TIMER</sub>	Maximum frequency of 16-bit timer in a UDB pair		–	–	50.01	MHz
F <sub>MAX_ADDER</sub>	Maximum frequency of 16-bit adder in a UDB pair		–	–	50.01	MHz
F <sub>MAX_CRC</sub>	Maximum frequency of 16-bit CRC/PRS in a UDB pair		–	–	50.01	MHz
PLD Performance						
F <sub>MAX_PLD</sub>	Maximum frequency of a two-pass PLD function in a UDB pair		–	–	50.01	MHz
Clock to Output Performance						
t <sub>CLK_OUT</sub>	Propagation delay for clock in to data out, see <a href="#">Figure 11-52</a> on page 99.	25 °C, V <sub>DD</sub> ≥ 2.7 V	–	20	25	ns
t <sub>CLK_OUT</sub>	Propagation delay for clock in to data out, see <a href="#">Figure 11-52</a> on page 99.	Worst-case placement, routing, and pin selection	–	–	55	ns

**Note**

54. Rise/fall time matching (TR) not guaranteed, see [USB Driver AC Specifications](#) on page 83.

**Figure 11-54. Synchronous Write and Read Cycle Timing, No Wait States**



**Table 11-54. Synchronous Write and Read Timing Specifications<sup>[59]</sup>**

Parameter	Description	Conditions	Min	Typ	Max	Units
Fbus_clock	Bus clock frequency <sup>[60]</sup>		–	–	33	MHz
Tbus_clock	Bus clock period <sup>[61]</sup>		30.3	–	–	ns
Twr_Setup	Time from EM_data valid to rising edge of EM_Clock		$T_{bus\_clock} - 10$	–	–	ns
Trd_setup	Time that EM_data must be valid before rising edge of EM_OE		5	–	–	ns
Trd_hold	Time that EM_data must be valid after rising edge of EM_OE		5	–	–	ns

**Notes**

59. Based on device characterization (Not production tested).

60. EMIF signal timings are limited by GPIO frequency limitations. See “GPIO” section on page 76.

61. EMIF output signals are generally synchronized to bus clock, so EMIF signal timings are dependent on bus clock frequency.

## 17. Revision History

Description Title: PSoC® 3: CY8C32 Family Data Sheet Programmable System-on-Chip (PSoC®) Document Number: 001-56955				
Revision	ECN	Submission Date	Orig. of Change	Description of Change
**	2796903	11/04/09	MKEA	New datasheet
*A	2824546	12/09/09	MKEA	Updated I2C section to reflect 1 Mbps. Updated Table 11-6 and 11-7 (Boost AC and DC specs); also added Schottky Diode specs. Changed current for sleep/hibernate mode to include SIO; Added footnote to analog global specs. Updated Figures 1-1, 6-2, 7-14, and 8-1. Updated Table 6-2 and Table 6-3 (Hibernate and Sleep rows) and Power Modes section. Updated GPIO and SIO AC specifications. Updated Gain error in IDAC and VDAC specifications. Updated description of V <sub>DDA</sub> spec in Table 11-1 and removed GPIO Clamp Current parameter. Updated number of UDBs on page 1. Moved FILO from ILO DC to AC table. Added PCB Layout and PCB Schematic diagrams. Updated Fgpiout spec (Table 11-9). Added duty cycle frequency in PLL AC spec table. Added note for Sleep and Hibernate modes and Active Mode specs in Table 11-2. Linked URL in Section 10.3 to PSoC Creator site. Updated Ja and Jc values in Table 13-1. Updated Single Sample Mode and Fast FIR Mode sections. Updated Input Resistance specification in Del-Sig ADC table. Added Tio_init parameter. Updated PGA and UGB AC Specs. Removed SPC ADC. Updated Boost Converter section. Added section 'SIO as Comparator'; updated Hysteresis spec (differential mode) in Table 11-10. Updated V <sub>BAT</sub> condition and deleted Vstart parameter in Table 11-6. Added 'Bytes' column for Tables 4-1 to 4-5.
*B	2873322	02/04/10	MKEA	Changed maximum value of PPOR_TR to '1'. Updated V <sub>BIAS</sub> specification. Updated PCB Schematic. Updated Figure 8-1 and Figure 6-3. Updated Interrupt Vector table, Updated Sales links. Updated JTAG and SWD specifications. Removed Jp-p and Jperiod from ECO AC Spec table. Added note on sleep timer in Table 11-2. Updated ILO AC and DC specifications. Added Resolution parameter in VDAC and IDAC tables. Updated I <sub>OUT</sub> typical and maximum values. Changed Temperature Sensor range to -40 °C to +85 °C. Removed Latchup specification from Table 11-1. Updated DAC details

**Description Title: PSoC® 3: CY8C32 Family Data Sheet Programmable System-on-Chip (PSoC®) (continued)**  
**Document Number: 001-56955**

Revision	ECN	Submission Date	Orig. of Change	Description of Change
*M	3645908	06/14/2012	MKEA	<p>Added paragraph clarifying that to achieve low hibernate current, you must limit the frequency of IO input signals.</p> <p>Revised description of IPOR and clarified PRES term.</p> <p>Changed footnote to state that all GPIO input voltages - not just analog voltages - must be less than Vddio.</p> <p>Updated 100-TQFP package drawing</p> <p>Clarified description of opamp lout spec</p> <p>Changed "compliant with I2C" to "compatible with I2C"</p> <p>Updated 48-QFN package drawing</p> <p>Changed reset status register description text to clarify that not all reset sources are in the register</p> <p>Updated example PCB layout figure</p> <p>Removed text stating that FTW is a wakeup source</p> <p>Changed supply ramp rate spec from 1 V/ns to 0.066 V/μs</p> <p>Added "based on char" footnote to voltage monitors response time spec</p> <p>Changed analog global spec descriptions and values</p> <p>Added spec for ESDhbm for when Vssa and Vssd are separate</p> <p>Added a statement about support for JTAG programmers and file formats</p> <p>Changed comparator specs and conditions</p> <p>Added text describing flash cache, and updated related text</p> <p>Changed text and added figures describing Vddio source and sink</p> <p>Added a statement about support for JTAG programmers and file formats.</p> <p>Changed comparator specs and conditions</p> <p>Added text on adjustability of buzz frequency</p> <p>Updated terminology for "master" and "system" clock</p> <p>Deleted the text "debug operations are possible while the device is reset"</p> <p>Deleted and updated text regarding SIO performance under certain power ramp conditions</p> <p>Removed from boost mention of 22 μH inductors. This included deleting some graph figures.</p> <p>Changed DAC high and low speed/power mode descriptions and conditions</p> <p>Changed IMO startup time spec</p> <p>Added text on XRES and PRES re-arm times</p> <p>Added text about usage in externally regulated mode</p> <p>Updated package diagram spec 001-45616 to *D revision.</p> <p>Changed supply ramp rate spec from 1 V/ns to 0.066 V/μs</p> <p>Changed text describing SIO modes for overvoltage tolerance</p> <p>Added chip Idd specs for active and low-power modes, for multiple voltage, temperature and usage conditions</p> <p>Added chip Idd specs for active and low-power modes, for multiple voltage, temperature and usage conditions</p> <p>Updated del-sig ADC spec tables, to replace three the instances of "16 bit" with "12 bit"</p>
*N	3648803	06/18/2012	WKA/ MKEA	No changes. EROS update.